4.8 kHz, Ultralow Noise, 24-Bit Sigma-Delta ADC with PGA

AD7192

FEATURES

RMS noise: 11 nV @ 4.7 Hz (gain = 128)
15.5 noise-free bits @ 2.4 kHz (gain = 128)
Up to 22 noise-free bits (gain = 1)
Offset drift: 5 nV/°C
Gain drift: 1 ppm/°C
Specified drift over time
2 differential/4 pseudo differential input channels
Automatic channel sequencer
Programmable gain (1 to 128)
Output data rate: 4.7 Hz to 4.8 kHz
Internal or external clock
Simultaneous 50 Hz/60 Hz rejection
4 general-purpose digital outputs
Power supply
AV_{DD}: 3 V to 5.25 V
DV_{DD}: 2.7 V to 5.25 V
Current: 4.35 mA
Temperature range: −40°C to +105°C
Package: 24-lead TSSOP

INTERFACE

3-wire serial
SPI, QSPI™, MICROWIRE™, and DSP compatible
Schmitt trigger on SCLK

APPLICATIONS

Weigh scales
Strain gage transducers
Pressure measurement
Temperature measurement
Chromatography
PLC/DCS analog input modules
Data acquisition
Medical and scientific instrumentation

GENERAL DESCRIPTION

The AD7192 is a low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit sigma-delta (Σ-Δ) analog-to-digital converter (ADC). The on-chip low noise gain stage means that signals of small amplitude can be interfaced directly to the ADC.

The device can be configured to have two differential inputs or four pseudo differential inputs. The on-chip channel sequencer allows several channels to be enabled, and the AD7192 sequentially converts on each enabled channel. This simplifies communication with the part. The on-chip 4.92 MHz clock can be used as the clock source to the ADC or, alternatively, an external clock or crystal can be used. The output data rate from the part can be varied from 4.7 Hz to 4.8 kHz.

The device has two digital filter options. The choice of filter affects the rms noise/noise-free resolution at the programmed output data rate, the settling time, and the 50 Hz/60 Hz rejection. For applications that require all conversions to be settled, the AD7192 includes a zero latency feature.

The part operates with a power supply from 3 V to 5.25 V. It consumes a current of 4.35 mA. It is housed in a 24-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM

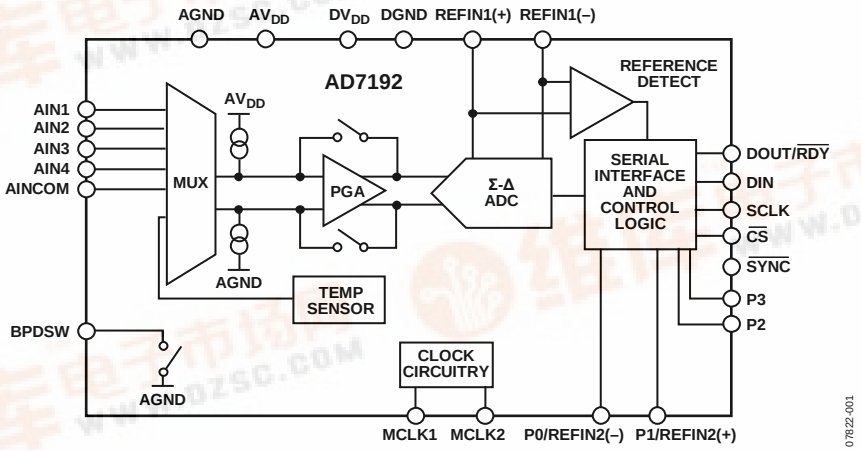

Figure 1.

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5/09—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = 3 V to 5.25 V, DV_{DD} = 2.7 V to 5.25 V, AGND = DGND = 0 V; REFINx(+) = AV_{DD}, REFINx(−) = AGND, MCLK = 4.92 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	AD7192B	Unit	Test Conditions/Comments[1]
ADC			
Output Data Rate	4.7 to 4800	Hz nom	Chop disabled
	1.17 to 1200	Hz nom	Chop enabled, sinc[4] filter
	1.56 to 1600	Hz nom	Chop enabled, sinc[3] filter
No Missing Codes[2]	24	Bits min	FS > 1, sinc[4] filter[3]
	24	Bits min	FS > 4, sinc[3] filter[3]
Resolution			See the RMS Noise and Resolution section
RMS Noise and Output Data Rates			See the RMS Noise and Resolution section
Integral Nonlinearity			
Gain = 1[2]	±10	ppm of FSR max	±2 ppm typical, AV_{DD} = 5 V
	±15	ppm of FSR max	±2 ppm typical, AV_{DD} = 3 V
Gain > 1	±30	ppm of FSR max	±5 ppm typical, AV_{DD} = 5 V
	±30	ppm of FSR max	±12 ppm typical, AV_{DD} = 3 V
Offset Error[4, 5]	±150/gain	µV typ	Chop disabled
	±0.5	µV typ	Chop enabled
Offset Error Drift vs. Temperature	±150/gain	nV/°C typ	Gain = 1 to 16; chop disabled
	±5	nV/°C typ	Gain = 32 to 128; chop disabled
	±5	nV/°C typ	Chop enabled
Offset Error Drift vs. Time	25	nV/1000 hours typ	Gain ≥ 32
Gain Error[4]	±0.001	% typ	AV_{DD} = 5 V, gain = 1, T_A = 25°C (factory calibration conditions)
	−0.39	% typ	Gain = 128, before full-scale calibration (see Table 23)
	±0.003	% typ	Gain > 1, after internal full-scale calibration, AV_{DD} ≥ 4.75 V.
	±0.005	% typ	Gain > 1, after internal full-scale calibration, AV_{DD} < 4.75 V
Gain Drift vs. Temperature	±1	ppm/°C typ	
Gain Drift vs. Time	10	ppm/1000 hours typ	Gain = 1.
Power Supply Rejection	90	dB typ	Gain = 1, V_{IN} = 1 V.
	95	dB min	Gain > 1, V_{IN} = 1 V/gain, 110 dB typ.
Common-Mode Rejection			
@ DC[2]	100	dB min	Gain = 1, V_{IN} = 1 V.
@ DC	110	dB min	Gain > 1, V_{IN} = 1 V/gain.
@ 50 Hz, 60 Hz[2]	120	dB min	10 Hz output data rate, 50 ± 1 Hz, 60 ± 1 Hz.
@ 50 Hz, 60 Hz[2]	120	dB min	50 ± 1 Hz (50 Hz output data rate), 60 ± 1 Hz (60 Hz output data rate).
Normal Mode Rejection[2]			
Sinc[4] Filter			
Internal Clock			
@ 50 Hz, 60 Hz	100	dB min	10 Hz output data rate, 50 ± 1 Hz, 60 ± 1 Hz.
	74	dB min	50 Hz output data rate, REJ60[6] = 1, 50 ± 1 Hz, 60 ± 1 Hz.
@ 50 Hz	96	dB min	50 Hz output data rate, 50 ± 1 Hz.
@ 60 Hz	97	dB min	60 Hz output data rate, 60 ± 1 Hz.

Parameter	AD7192B	Unit	Test Conditions/Comments[1]
External Clock			
@ 50 Hz, 60 Hz	120	dB min	10 Hz output data rate, 50 ± 1 Hz, 60 ± 1 Hz.
	82	dB min	50 Hz output data rate, REJ60[6] = 1, 50 ± 1 Hz, 60 ± 1 Hz.
@ 50 Hz	120	dB min	50 Hz output data rate, 50 ± 1 Hz.
@ 60 Hz	120	dB min	60 Hz output data rate, 60 ± 1 Hz.
Sinc^3 Filter			
Internal Clock			
@ 50 Hz, 60 Hz	75	dB min	10 Hz output data rate, 50 ± 1 Hz, 60 ± 1 Hz.
	60	dB min	50 Hz output data rate, REJ60[6] = 1, 50 ± 1 Hz, 60 ± 1 Hz.
@ 50 Hz	70	dB min	50 Hz output data rate, 50 ± 1 Hz.
@ 60 Hz	70	dB min	60 Hz output data rate, 60 ± 1 Hz.
External Clock			
@ 50 Hz, 60 Hz	100	dB min	10 Hz output data rate, 50 ± 1 Hz, 60 ± 1 Hz.
	67	dB min	50 Hz output data rate, REJ60[6] = 1, 50 ± 1 Hz, 60 ± 1 Hz.
@ 50 Hz	95	dB min	50 Hz output data rate, 50 ± 1 Hz.
@ 60 Hz	95	dB min	60 Hz output data rate, 60 ± 1 Hz.
ANALOG INPUTS			
Differential Input Voltage Ranges	± V_{REF}/gain	V nom	VREF = REFINx(+) − REFINx(−), gain = 1 to 128.
	± (AV_{DD} − 1.25 V)/gain	V min/max	Gain > 1.
Absolute AIN Voltage Limits[2]			
Unbuffered Mode	AGND − 50 mV	V min	
	AV_{DD} + 50 mV	V max	
Buffered Mode	AGND + 250 mV	V min	
	AV_{DD} − 250 mV	V max	
Analog Input Current			
Buffered Mode			
Input Current[2]	±2	nA max	Gain = 1.
	±3	nA max	Gain > 1.
Input Current Drift	±5	pA/°C typ	
Unbuffered Mode			
Input Current	±3.5	µA/V typ	Gain = 1, input current varies with input voltage.
	±1	µA/V typ	Gain > 1.
Input Current Drift	±0.05	nA/V/°C typ	External clock.
	±1.6	nA/V/°C typ	Internal clock.
REFERENCE INPUT			
REFIN Voltage	AV_{DD}	V nom	REFIN = REFINx(+) − REFINx(−).
	1	V min	
	AV_{DD}	V max	The differential input must be limited to ±(AV_{DD} − 1.25 V)/gain when gain > 1.
Absolute REFIN Voltage Limits[2]	GND − 50 mV	V min	
	AV_{DD} + 50 mV	V max	
Average Reference Input Current	4.5	µA/V typ	

Parameter	AD7192B	Unit	Test Conditions/Comments[1]
Average Reference Input Current Drift	±0.03	nA/V/°C typ	External clock.
	±1.3	nA/V/°C typ	Internal clock.
Normal Mode Rejection[2]	Same as for analog inputs		
Common-Mode Rejection	100	dB typ	
Reference Detect Levels	0.3	V min	
	0.6	V max	
TEMPERATURE SENSOR			
Accuracy	±2	°C typ	Applies after user calibration at 25°C.
Sensitivity	2815	Codes/°C typ	Bipolar mode.
BRIDGE POWER-DOWN SWITCH			
R_{ON}	10	Ω max	
Allowable Current[2]	30	mA max	Continuous current.
BURNOUT CURRENTS			
AIN Current	500	nA nom	Analog inputs must be buffered and chop disabled.
DIGITAL OUTPUTS (P0 to P3)			
Output High Voltage, V_{OH}	AV_{DD} − 0.6	V min	AV_{DD} = 3 V, I_{SOURCE} = 100 µA.
Output Low Voltage, V_{OL}	0.4	V max	AV_{DD} = 3 V, I_{SINK} = 100 µA.
Output High Voltage, V_{OH}	4	V min	AV_{DD} = 5 V, I_{SOURCE} = 200 µA.
Output Low Voltage, V_{OL}	0.4	V max	AV_{DD} = 5 V, I_{SINK} = 800 µA.
Floating-State Leakage Current[2]	±100	nA max	
Floating-State Output Capacitance	10	pF typ	
INTERNAL/EXTERNAL CLOCK			
Internal Clock			
Frequency	4.92 ± 4%	MHz min/max	
Duty Cycle	50:50	% typ	
External Clock/Crystal			
Frequency	4.9152	MHz nom	
	2.4576/5.12	MHz min/max	
Input Low Voltage V_{INL}	0.8	V max	DV_{DD} = 5 V.
	0.4	V max	DV_{DD} = 3 V.
Input High Voltage, V_{INH}	2.5	V min	DV_{DD} = 3 V.
	3.5	V min	DV_{DD} = 5 V.
Input Current	±10	µA max	
LOGIC INPUTS			
Input High Voltage, V_{INH}[2]	2	V min	
Input Low Voltage, V_{INL}[2]	0.8	V max	
Hysteresis[2]	0.1/0.25	V min/V max	
Input Currents	±10	µA max	
LOGIC OUTPUT (DOUT/$\overline{RDY}$)			
Output High Voltage, V_{OH}[2]	DV_{DD} − 0.6	V min	DV_{DD} = 3 V, I_{SOURCE} = 100 µA.
Output Low Voltage, V_{OL}[2]	0.4	V max	DV_{DD} = 3 V, I_{SINK} = 100 µA.
Output High Voltage, V_{OH}[2]	4	V min	DV_{DD} = 5 V, I_{SOURCE} = 200 µA.
Output Low Voltage, V_{OL}[2]	0.4	V max	DV_{DD} = 5 V, I_{SINK} = 1.6 mA.
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance	10	pF typ	
Data Output Coding	Offset binary		

Parameter	AD7192B	Unit	Test Conditions/Comments[1]
SYSTEM CALIBRATION[2]			
Full-Scale Calibration Limit	1.05 × FS	V max	
Zero-Scale Calibration Limit	−1.05 × FS	V min	
Input Span	0.8 × FS	V min	
	2.1 × FS	V max	
POWER REQUIREMENTS[7]			
Power Supply Voltage			
AV_{DD} − AGND	3/5.25	V min/max	
DV_{DD} − DGND	2.7/5.25	V min/max	
Power Supply Currents			
AI_{DD} Current	0.6	mA max	0.53 mA typical, gain = 1, buffer off.
	0.85	mA max	0.75 mA typical, gain = 1, buffer on.
	3.2	mA max	2.5 mA typical, gain = 8, buffer off.
	3.6	mA max	3 mA typical, gain = 8, buffer on.
	4.5	mA max	3.5 mA typical, gain = 16 to 128, buffer off.
	5	mA max	4 mA typical, gain = 16 to 128, buffer on.
DI_{DD} Current	0.4	mA max	0.35 mA typical, DV_{DD} = 3 V.
	0.6	mA max	0.5 mA typical, DV_{DD} = 5 V.
	1.5	mA typ	External crystal used.
I_{DD} (Power-Down Mode)	3	μA max	

[1] Temperature range: −40°C to +105°C.
[2] Specification is not production tested but is supported by characterization data at initial product release.
[3] FS is the decimal equivalent of Bit FS9 to Bit FS0 in the mode register.
[4] Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed gain and output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed gain and output data rate.
[5] The analog inputs are configured for differential mode.
[6] REJ60 is a bit in the mode register. When the output data rate is set to 50 Hz, setting REJ60 to 1 places a notch at 60 Hz, allowing simultaneous 50 Hz/60 Hz rejection.
[7] Digital inputs equal to DV_{DD} or DGND.

TIMING CHARACTERISTICS

AV_{DD} = 3 V to 5.25 V, DV_{DD} = 2.7 V to 5.25 V, AGND = DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = DV_{DD}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments[1, 2]
t_3	100	ns min	SCLK high pulse width
t_4	100	ns min	SCLK low pulse width
READ OPERATION			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_5[5, 6]	10	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	80	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high
WRITE OPERATION			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	30	ns min	Data valid to SCLK edge setup time
t_{10}	25	ns min	Data valid to SCLK edge hold time
t_{11}	0	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 3 and Figure 4.
[3] These numbers are measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[4] The SCLK active edge is the falling edge of SCLK.
[5] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[6] $\overline{RDY}$ returns high after a read of the data register. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

CIRCUIT AND TIMING DIAGRAMS

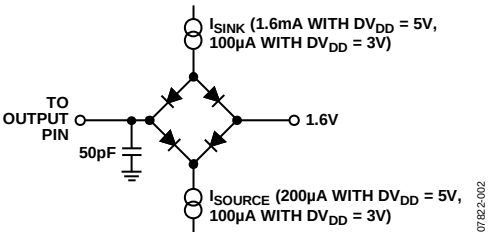

Figure 2. Load Circuit for Timing Characterization

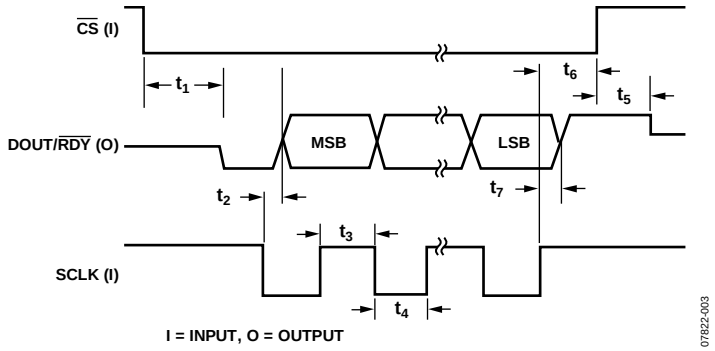

Figure 3. Read Cycle Timing Diagram

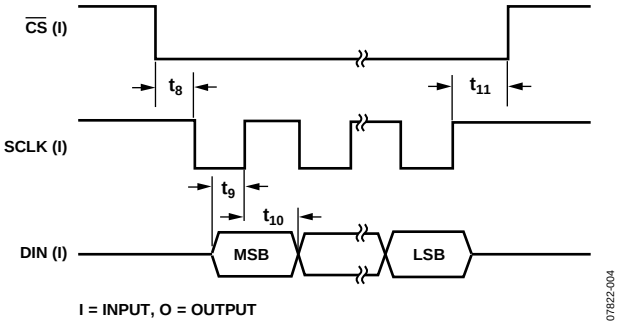

Figure 4. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +6.5 V
DV_{DD} to AGND	−0.3 V to +6.5 V
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
AIN/Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering Reflow	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead TSSOP	128	42	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

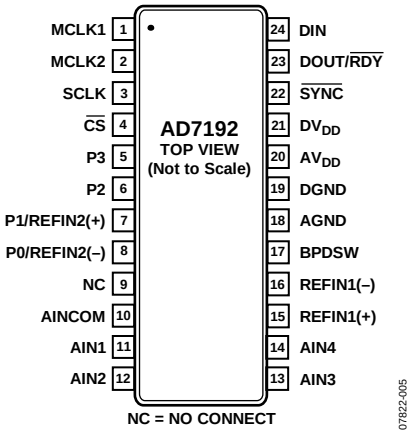

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MCLK1	When the master clock for the device is provided externally by a crystal, the crystal is connected between MCLK1 and MCLK2.
2	MCLK2	Master Clock Signal for the Device. The AD7192 has an internal 4.92 MHz clock. This internal clock can be made available on the MCLK2 pin. The clock for the AD7192 can be provided externally also in the form of a crystal or external clock. A crystal can be tied across the MCLK1 and MCLK2 pins. Alternatively, the MCLK2 pin can be driven with a CMOS-compatible clock and the MCLK1 pin left unconnected.
3	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information transmitted to or from the ADC in smaller batches of data.
4	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device.
5	P3	Digital Output Pin. This pin can function as a general-purpose output bit referenced between AV_{DD} and AGND.
6	P2	Digital Output Pin. This pin can function as a general-purpose output bit referenced between AV_{DD} and AGND.
7	P1/REFIN2(+)	Digital Output Pin/Positive Reference Input. This pin functions as a general-purpose output bit referenced between AV_{DD} and AGND. When the REFSEL bit in the configuration register = 1, this pin functions as REFIN2(+). An external reference can be applied between REFIN2(+) and REFIN2(−). REFIN2(+) can lie anywhere between AV_{DD} and AGND + 1 V. The nominal reference voltage, (REFIN2(+) − REFIN2(−)), is AV_{DD}, but the part functions with a reference from 1 V to AV_{DD}.
8	P0/REFIN2(−)	Digital Output Pin/Negative Reference Input. This pin functions as a general-purpose output bit referenced between AV_{DD} and AGND. When the REFSEL bit in the configuration register = 1, this pin functions as REFIN2(−). This reference input can lie anywhere between AGND and AV_{DD} − 1 V.
9	NC	No Connect. This pin should be tied to AGND.
10	AINCOM	Analog inputs AIN1 to AIN4 are referenced to this input when configured for pseudodifferential operation.
11	AIN1	Analog Input. This pin can be configured as the positive input of a fully differential input pair when used with AIN2 or as a pseudodifferential input when used with AINCOM.
12	AIN2	Analog Input. This pin can be configured as the negative input of a fully differential input pair when used with AIN1 or as a pseudodifferential input when used with AINCOM.

Pin No.	Mnemonic	Description
13	AIN3	Analog Input. This pin can be configured as the positive input of a fully differential input pair when used with AIN4 or as a pseudodifferential input when used with AINCOM.
14	AIN4	Analog Input. This pin can be configured as the negative input of a fully differential input pair when used with AIN3 or as a pseudodifferential input when used with AINCOM.
15	REFIN1(+)	Positive Reference Input. An external reference can be applied between REFIN1(+) and REFIN1(−). REFIN1(+) can lie anywhere between AV_{DD} and AGND + 1 V. The nominal reference voltage, (REFIN1(+) − REFIN1(−)), is AV_{DD}, but the part functions with a reference from 1 V to AV_{DD}.
16	REFIN1(−)	Negative Reference Input. This reference input can lie anywhere between AGND and AV_{DD} − 1 V.
17	BPDSW	Bridge Power-Down Switch to AGND.
18	AGND	Analog Ground Reference Point.
19	DGND	Digital Ground Reference Point.
20	AV_{DD}	Analog Supply Voltage, 3 V to 5.25 V. AV_{DD} is independent of DV_{DD}. Therefore, DV_{DD} can be operated at 3 V with AV_{DD} at 5 V or vice versa.
21	DV_{DD}	Digital Supply Voltage, 2.7 V to 5.25 V. DV_{DD} is independent of AV_{DD}. Therefore, AV_{DD} can be operated at 3 V with DV_{DD} at 5 V or vice versa.
22	$\overline{SYNC}$	Logic input that allows for synchronization of the digital filters and analog modulators when using a number of AD7192 devices. While $\overline{SYNC}$ is low, the nodes of the digital filter, the filter control logic, and the calibration control logic are reset, and the analog modulator is also held in its reset state. $\overline{SYNC}$ does not affect the digital interface but does reset $\overline{RDY}$ to a high state if it is low. $\overline{SYNC}$ has a pull-up resistor internally to DV_{DD}.
23	DOUT/$\overline{RDY}$	Serial Data Output/Data Ready Output. DOUT/$\overline{RDY}$serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{RDY}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{RDY}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{RDY}$ pin. With $\overline{CS}$ low, the data-/control-word information is placed on the DOUT/$\overline{RDY}$ pin on the SCLK falling edge and is valid on the SCLK rising edge.
24	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers in the ADC, with the register selection bits of the communications register identifying the appropriate register.

TYPICAL PERFORMANCE CHARACTERISTICS

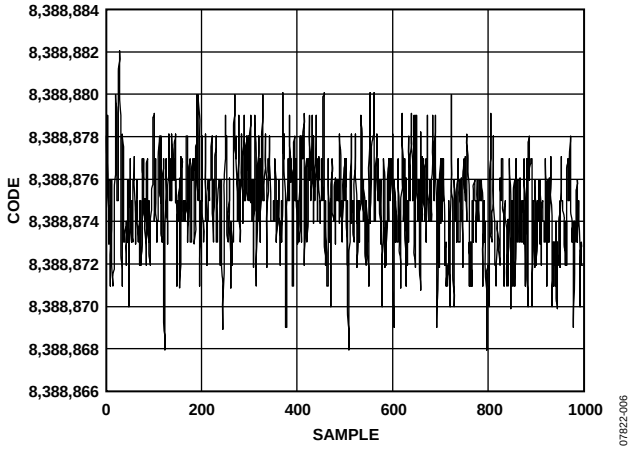

Figure 6. Noise (V_{REF} = AV_{DD} = 5 V, Output Data Rate = 4.7 Hz, Gain = 128, Chop Disabled, Sinc^4 Filter)

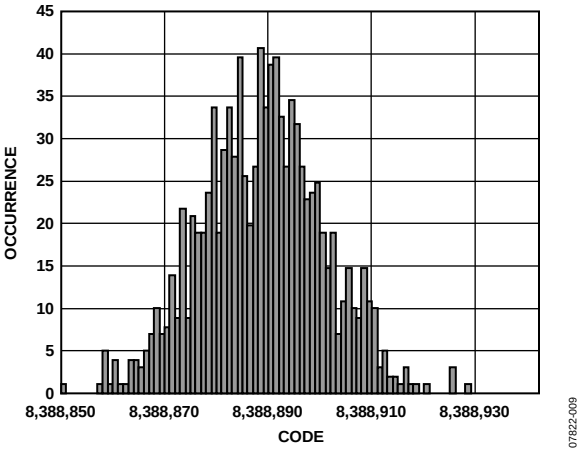

Figure 9. Noise Distribution Histogram (V_{REF} = AV_{DD} = 5 V, Output Data Rate = 2400 Hz, Gain = 1, Chop Disabled, Sinc^4 Filter)

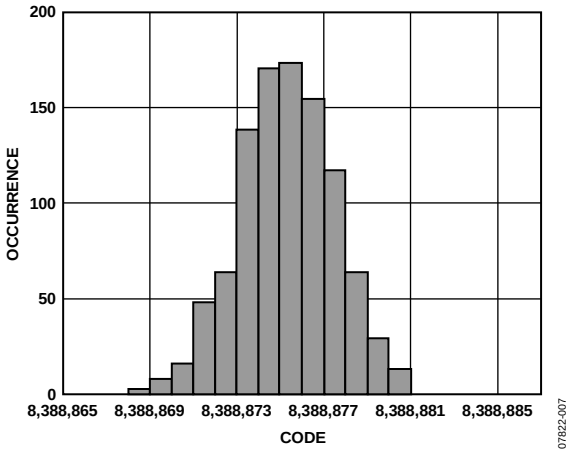

Figure 7. Noise Distribution Histogram (V_{REF} = AV_{DD} = 5 V, Output Data Rate = 4.7 Hz, Gain = 128, Chop Disabled, Sinc^4 Filter)

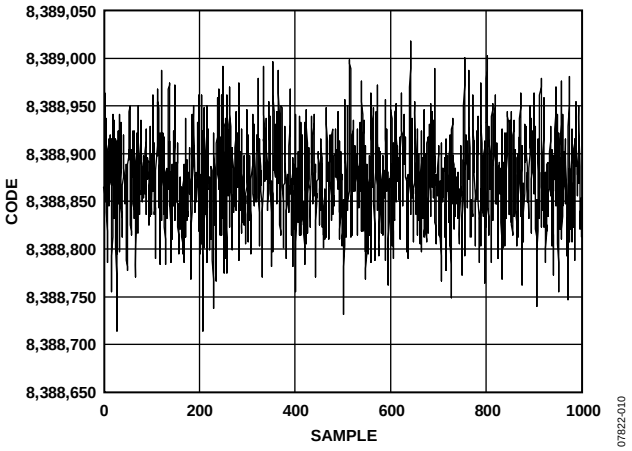

Figure 10. Noise (V_{REF} = AV_{DD} = 5 V, Output Data Rate = 2400 Hz, Gain = 128, Chop Disabled, Sinc^4 Filter)

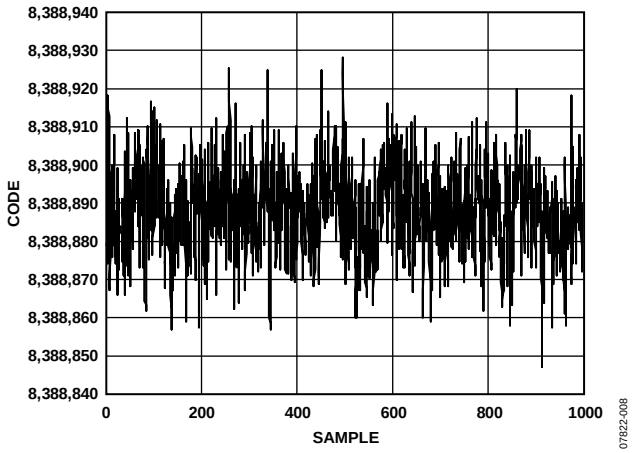

Figure 8. Noise (V_{REF} = AV_{DD} = 5 V, Output Data Rate = 2400 Hz, Gain = 1, Chop Disabled, Sinc^4 Filter)

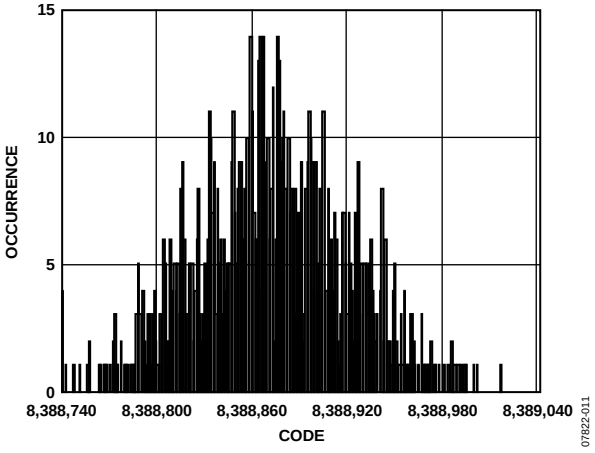

Figure 11. Noise Distribution Histogram (V_{REF} = AV_{DD} = 5 V, Output Data Rate = 2400 Hz, Gain = 128, Chop Disabled, Sinc^4 Filter)

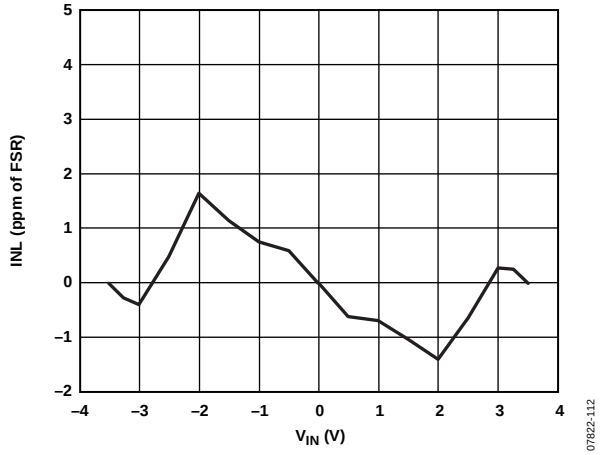

Figure 12. INL (Gain = 1)

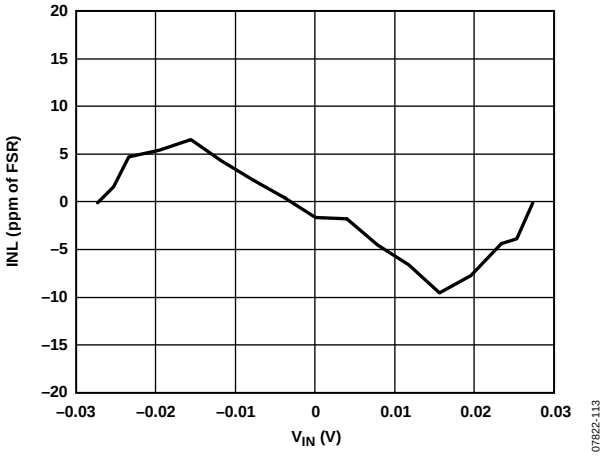

Figure 13. INL (Gain = 128)

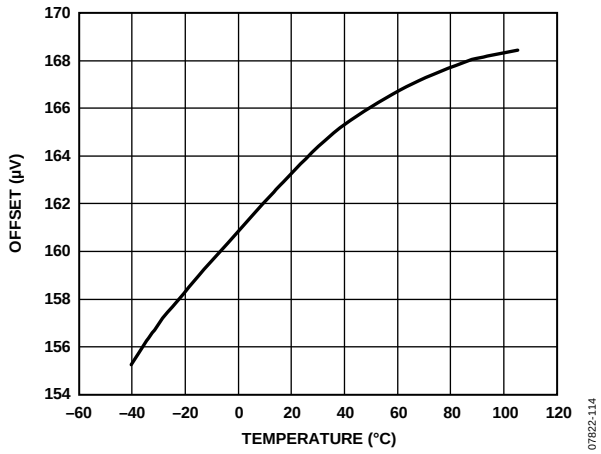

Figure 14. Offset Error (Gain = 1, Chop Disabled)

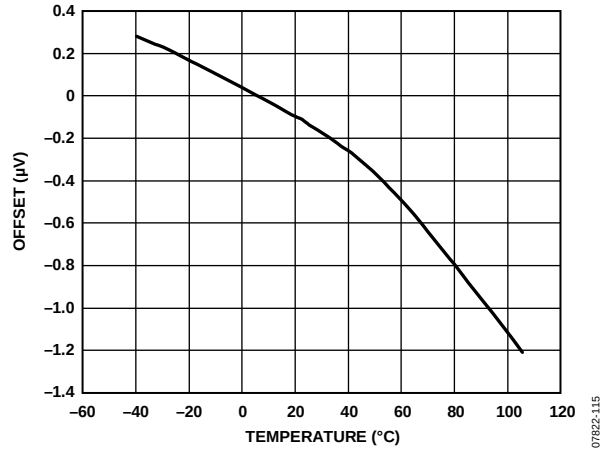

Figure 15. Offset Error (Gain = 128, Chop Disabled)

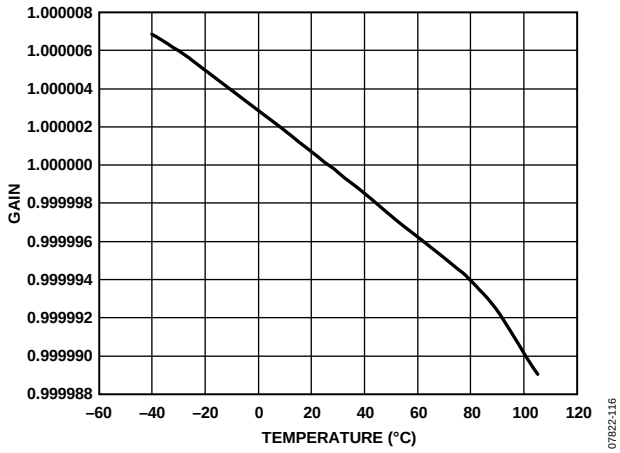

Figure 16. Gain Error (Gain = 1)

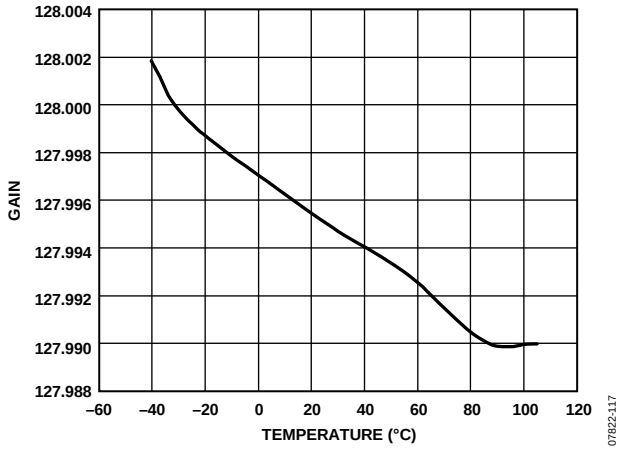

Figure 17. Gain Error (Gain = 128)

RMS NOISE AND RESOLUTION

The AD7192 has a choice of two filter types: sinc[4] and sinc[3]. In addition, the AD7192 can be operated with chop enabled or chop disabled.

The following tables show the rms noise of the AD7192 for some of the output data rates and gain settings with chop disabled and enabled for the sinc[4] and sinc[3] filters. The numbers given are for the bipolar input range with the external 5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. The effective resolution is also shown, and the output peak-to-peak (p-p) resolution, or noise-free resolution, is listed in parentheses. It is important to note that the effective resolution is calculated using the rms noise, whereas the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest ½ LSB.

SINC[4] CHOP DISABLED

Table 6. RMS Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	4.7	852.5	350	50	30	18	13	11
640	7.5	533	425	62	36	21	15	13
480	10	400	490	85	43	23	17	15
96	50	80	2000	260	134	73	46	34
80	60	66.7	2100	273	139	77	48	38
40	120	33.3	2400	315	175	95	64	51
32	150	26.7	2500	335	185	110	71	58
16	300	13.3	3100	420	240	145	95	81
5	960	4.17	4800	690	390	240	170	145
2	2400	1.67	7500	1100	640	390	273	235
1	4800	0.83	16,300	2200	1200	670	427	345

Table 7. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1[1]	Gain of 8[1]	Gain of 16[1]	Gain of 32[1]	Gain of 64[1]	Gain of 128[1]
1023	4.7	852.5	24 (22)	24 (22)	24 (21.5)	24 (21.5)	23.5 (21)	22.5 (20)
640	7.5	533	24 (22)	24 (21.5)	24 (21.5)	23.5 (21)	23 (20.5)	22.5 (20)
480	10	400	24 (21.5)	23.5 (21)	23.5 (21)	23.5 (21)	23 (20.5)	22 (19.5)
96	50	80	22 (19.5)	22 (19.5)	22 (19.5)	22 (19.5)	21.5 (19)	21 (18.5)
80	60	66.7	22 (19.5)	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	20.5 (18)
40	120	33.3	22 (19.5)	21.5 (19)	21.5 (19)	21.5 (19)	21 (18.5)	20.5 (18)
32	150	26.7	21.5 (19)	21.5 (19)	21.5 (19)	21 (18.5)	21 (18.5)	20 (17.5)
16	300	13.3	21.5 (19)	21.5 (19)	21 (18.5)	21 (18.5)	20.5 (18)	19.5 (17)
5	960	4.17	20.5 (18)	20.5 (18)	20.5 (18)	20 (17.5)	19.5 (17)	19 (16.5)
2	2400	1.67	20 (17.5)	20 (17.5)	19.5 (17)	19.5 (17)	19 (16.5)	18 (15.5)
1	4800	0.83	19 (16.5)	19 (16.5)	19 (16.5)	18.5 (16)	18.5 (16)	17.5 (15)

[1] The output peak-to-peak (p-p) resolution is listed in parentheses.

SINC³ CHOP DISABLED

Table 8. RMS Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	4.7	639.4	350	51	30	18	15	12
640	7.5	400	440	62	36	22	18	15
480	10	300	500	87	45	26	19	17
96	50	60	2000	255	134	73	47	36
80	60	50	2100	273	139	77	49	40
40	120	25	2400	315	168	96	66	55
32	150	20	2500	335	185	105	73	62
16	300	10	3100	425	235	136	100	86
5	960	3.13	5300	745	415	250	180	156
2	2400	1.25	55800	7100	3600	1750	910	500
1	4800	0.625	446,000	55,400	28,000	14,000	7000	3500

Table 9. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1[1]	Gain of 8[1]	Gain of 16[1]	Gain of 32[1]	Gain of 64[1]	Gain of 128[1]
1023	4.7	639.4	24 (22)	24 (22)	24 (21.5)	24 (21.5)	23 (20.5)	22.5 (20)
640	7.5	400	24 (21.5)	24 (21.5)	24 (21.5)	23.5 (21)	23 (20.5)	22 (19.5)
480	10	300	24 (21.5)	23.5 (21)	23.5 (21)	23.5 (21)	22.5 (20)	22 (19.5)
96	50	60	22 (19.5)	22 (19.5)	22 (19.5)	22 (19.5)	21.5 (19)	21 (18.5)
80	60	50	22 (19.5)	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	20.5 (18)
40	120	25	22 (19.5)	21.5 (19)	21.5 (19)	21.5 (19)	21 (18.5)	20 (17.5)
32	150	20	21.5 (19)	21.5 (19)	21.5 (19)	21.5 (19)	21 (18.5)	20 (17.5)
16	300	10	21.5 (19)	21.5 (19)	21 (18.5)	21 (18.5)	20.5 (18)	19.5 (17)
5	960	3.13	20.5 (18)	20.5 (18)	20.5 (18)	20 (17.5)	19.5 (17)	18.5 (16)
2	2400	1.25	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)
1	4800	0.625	14 (11.5)	14 (11.5)	14 (11.5)	14 (11.5)	14 (11.5)	14 (11.5)

[1] The output peak-to-peak (p-p) resolution is listed in parentheses.

SINC^4 CHOP ENABLED

Table 10. RMS Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	1.175	1702	248	36	22	13	9	8
640	1.875	1067	301	44	26	15	11	10
480	2.5	800	347	61	31	17	13	11
96	12.5	160	1420	184	95	52	33	25
80	15	133	1490	194	99	55	34	27
40	30	66.7	1700	223	124	68	46	37
32	37.5	53.3	1770	237	131	78	51	42
16	75	26.7	2200	297	170	103	68	58
5	240	8.33	3400	488	276	170	121	103
2	600	3.33	5310	780	453	276	194	167
1	1200	1.67	11,600	1560	849	474	302	244

Table 11. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1[1]	Gain of 8[1]	Gain of 16[1]	Gain of 32[1]	Gain of 64[1]	Gain of 128[1]
1023	1.175	1702	24 (22.5)	24 (22.5)	24 (22)	24 (22)	24 (21.5)	23 (20.5)
640	1.875	1067	24 (22.5)	24 (22)	24 (22)	24 (21.5)	23.5 (21)	23 (20.5)
480	2.5	800	24 (22)	24 (21.5)	24 (21.5)	24 (21.5)	23.5 (21)	22.5 (20)
96	12.5	160	22.5 (20)	22.5 (20)	22.5 (20)	22.5 (20)	22 (19.5)	21.5 (19)
80	15	133	22.5 (20)	22.5 (20)	22.5 (20)	22 (19.5)	22 (19.5)	21 (18.5)
40	30	66.7	22.5 (20)	22 (19.5)	22 (19.5)	22 (19.5)	21.5 (19)	21 (18.5)
32	37.5	53.3	22 (19.5)	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	20.5 (18)
16	75	26.7	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	20 (17.5)
5	240	8.33	21 (18.5)	21 (18.5)	21 (18.5)	20.5 (18)	20 (17.5)	19.5 (17)
2	600	3.33	20.5 (18)	20.5 (18)	20 (17.5)	20 (17.5)	19.5 (17)	18.5 (16)
1	1200	1.67	19.5 (17)	19.5 (17)	19.5 (17)	19 (16.5)	19 (16.5)	18 (15.5)

[1] The output peak-to-peak (p-p) resolution is listed in parentheses.

SINC³ CHOP ENABLED

Table 12. RMS Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	1.56	1282	248	37	22	13	11	9
640	2.5	800	312	44	26	16	13	11
480	3.33	600	354	62	32	19	14	13
96	16.6	120	1415	181	95	52	34	26
80	20	100	1485	194	99	55	35	29
40	40	50	1698	223	119	68	47	39
32	50	40	1768	237	131	75	52	44
16	100	20	2193	301	167	97	71	61
5	320	6.25	3748	527	294	177	128	111
2	800	2.5	39500	5020	2546	1240	644	354
1	1600	1.25	315,400	39,200	19,800	9900	4950	2500

Table 13. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1[1]	Gain of 8[1]	Gain of 16[1]	Gain of 32[1]	Gain of 64[1]	Gain of 128[1]
1023	1.56	1282	24 (22.5)	24 (22.5)	24 (22)	24 (22)	23.5 (21)	23 (20.5)
640	2.5	800	24 (22)	24 (22)	24 (22)	24 (21.5)	23.5 (21)	22.5 (20)
480	3.33	600	24 (22)	24 (21.5)	24 (21.5)	24 (21.5)	23 (20.5)	22.5 (20)
96	16.6	120	22.5 (20)	22.5 (20)	22.5 (20)	22.5 (20)	22 (19.5)	21.5 (19)
80	20	100	22.5 (20)	22.5 (20)	22.5 (20)	22 (19.5)	22 (19.5)	21 (18.5)
40	40	50	22.5 (20)	22 (19.5)	22 (19.5)	22 (19.5)	21.5 (19)	20.5 (18)
32	320	40	22 (19.5)	22 (19.5)	22 (19.5)	22 (19.5)	21.5 (19)	20.5 (18)
16	100	20	22(19.5)	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	20 (17.5)
5	320	6.25	21 (18.5)	20.5 (18)	20.5 (18)	20 (17.5)	19.5 (17)	18.5 (16)
2	800	2.5	17.5 (15)	17.5 (15)	17.5 (15)	17.5 (15)	17.5 (15)	17.5 (15)
1	1600	1.25	14.5 (12)	14.5 (12)	14.5 (12)	14.5 (12)	14.5 (12)	14.5 (12)

[1] The output peak-to-peak (p-p) resolution is listed in parentheses.

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers that are described on the following pages. In the following descriptions, "set" implies a Logic 1 state and "cleared" implies a Logic 0 state, unless otherwise noted.

COMMUNICATIONS REGISTER

(RS2, RS1, RS0 = 0, 0, 0)

The communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation and in which register this operation takes place. For read or write operations, when the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 40 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 14 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, CR denoting that the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$(0)	R/$\overline{\text{W}}$(0)	RS2(0)	RS1(0)	RS0(0)	CREAD(0)	0(0)	0(0)

Table 14. Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write enable bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part does not clock on to subsequent bits in the register. It stays at this bit location until a 0 is written to this bit. After a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits are loaded to the communications register. Idling the DIN pin high between data transfers minimizes the effects of spurious SCLK pulses on the serial interface.
CR6	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register.
CR5 to CR3	RS2 to RS0	Register address bits. These address bits are used to select which registers of the ADC are selected during the serial interface communication (see Table 15).
CR2	CREAD	Continuous read of the data register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read; that is, the contents of the data register are automatically placed on the DOUT pin when the SCLK pulses are applied after the $\overline{\text{RDY}}$ pin goes low to indicate that a conversion is complete. The communications register does not have to be written to for subsequent data reads. To enable continuous read, the Instruction 01011100 must be written to the communications register. To disable continuous read, the Instruction 01011000 must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While continuous read is enabled, the ADC monitors activity on the DIN line so that it can receive the instruction to disable continuous read. Additionally, a reset occurs if 40 consecutive 1s are seen on DIN. Therefore, DIN should be held low until an instruction is to be written to the device.
CR1 to CR0	0	These bits must be programmed to Logic 0 for correct operation.

Table 15. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications register during a write operation	8 bits
0	0	0	Status register during a read operation	8 bits
0	0	1	Mode register	24 bits
0	1	0	Configuration register	24 bits
0	1	1	Data register/data register plus status information	24 bits/32 bits
1	0	0	ID register	8 bits
1	0	1	GPOCON register	8 bits
1	1	0	Offset register	24 bits
1	1	1	Full-scale register	24 bits

STATUS REGISTER

(RS2, RS1, RS0 = 0, 0, 0; Power-On/Reset = 0x80)

The status register is an 8-bit read-only register. To access the ADC status register, the user must write to the communications register, select the next operation to be a read, and load Bit RS2, Bit RS1, and Bit RS0 with 0. Table 16 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, SR denoting that the bits are in the status register. SR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

SR7	**SR6**	**SR5**	**SR4**	**SR3**	**SR2**	**SR1**	**SR0**
$\overline{\text{RDY}}$(1)	ERR(0)	NOREF(0)	PARITY(0)	0(0)	CHD2(0)	CHD1(0)	CHD0(0)

Table 16. Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	$\overline{\text{RDY}}$	Ready bit for the ADC. This bit is cleared when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is set automatically after the ADC data register is read, or a period of time before the data register is updated, with a new conversion result to indicate to the user that the conversion data should not be read. It is also set when the part is placed in power-down mode or idle mode or when $\overline{\text{SYNC}}$ is taken low. The end of a conversion is also indicated by the DOUT/$\overline{\text{RDY}}$ pin. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
SR6	ERR	ADC error bit. This bit is written to at the same time as the $\overline{\text{RDY}}$ bit. This bit is set to indicate that the result written to the ADC data register is clamped to all 0s or all 1s. Error sources include overrange or under-range or the absence of a reference voltage. This bit is cleared when the result written to the data register is within the allowed analog input range again.
SR5	NOREF	No external reference bit. This bit is set to indicate that the selected reference (REFIN1 or REFIN2) is at a voltage that is below a specified threshold. When set, conversion results are clamped to all 1s. This bit is cleared to indicate that a valid reference is applied to the selected reference pins. The NOREF bit is enabled by setting the REFDET bit in the configuration register to 1.
SR4	PARITY	Parity check of the data register. If the ENPAR bit in the mode register is set, the PARITY bit is set if there is an odd number of 1s in the data register. It is cleared if there is an even number of 1s in the data register. The DAT_STA bit in the mode register should be set when the parity check is used. When the DAT_STA bit is set, the contents of the status register are transmitted along with the data for each data register read.
SR3	0	This bit is set to 0.
SR2 to SR0	CHD2 to CHD0	These bits indicate which channel corresponds to the data register contents. They do not indicate which channel is presently being converted but indicate which channel was selected when the conversion contained in the data register was generated.

MODE REGISTER

(RS2, RS1, RS0 = 0, 0, 1; Power-On/Reset = 0x080060)

The mode register is a 24-bit register from which data can be read or to which data can be written. This register is used to select the operating mode, the output data rate, and the clock source. Table 17 outlines the bit designations for the mode register. MR0 through MR23 indicate the bit locations, MR denoting that the bits are in the mode register. MR23 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit. Any write to the mode register resets the modulator and filter and sets the $\overline{\text{RDY}}$ bit.

MR23	**MR22**	**MR21**	**MR20**	**MR19**	**MR18**	**MR17**	**MR16**
MD2(0)	MD1(0)	MD0(0)	DAT_STA(0)	CLK1(1)	CLK0(0)	0	0
MR15	**MR14**	**MR13**	**MR12**	**MR11**	**MR10**	**MR9**	**MR8**
SINC3(0)	0	ENPAR(0)	CLK_DIV(0)	SINGLE(0)	REJ60(0)	FS9(0)	FS8(0)
MR7	**MR6**	**MR5**	**MR4**	**MR3**	**MR2**	**MR1**	**MR0**
FS7(0)	FS6(1)	FS5(1)	FS4(0)	FS3(0)	FS2(0)	FS1(0)	FS0(0)

Table 17. Mode Register Bit Designations

Bit Location	Bit Name	Description
MR23 to MR21	MD2 to MD0	Mode select bits. These bits select the operating mode of the AD7192 (see Table 18).
MR20	DAT_STA	This bit enables the transmission of status register contents after each data register read. When DAT_STA is set, the contents of the status register are transmitted along with each data register read. This function is useful when several channels are selected because the status register identifies the channel to which the data register value corresponds.
MR19, MR18	CLK1, CLK0	These bits are used to select the clock source for the AD7192. Either the on-chip 4.92 MHz clock or an external clock can be used. The ability to use an external clock allows several AD7192 devices to be synchronized. Also, 50 Hz/60 Hz rejection is improved when an accurate external clock drives the AD7192.

CLK1	CLK0	ADC Clock Source
0	0	External crystal. The external crystal is connected from MCLK1 to MCLK2.
0	1	External clock. The external clock is applied to the MCLK2 pin.
1	0	Internal 4.92 MHz clock. Pin MCLK2 is tristated.
1	1	Internal 4.92 MHz clock. The internal clock is available on MCLK2.

MR17, MR16	0	These bits must be programmed with a Logic 0 for correct operation.
MR15	SINC3	Sinc^3 filter select bit. When this bit is cleared, the sinc^4 filter is used (default value). When this bit is set, the sinc^3 filter is used. The benefit of the sinc^3 filter compared to the sinc^4 filter is its lower settling time. For a given output data rate, f_{ADC}, the sinc^3 filter has a settling time of $3/f_{ADC}$ while the sinc^4 filter has a settling time of $4/f_{ADC}$ when chop is disabled. The sinc^4 filter, due to its deeper notches, gives better 50 Hz/60 Hz rejection. At low output data rates, both filters give similar rms noise and similar no missing codes for a given output data rate. At higher output data rates (FS values less than 5), the sinc^4 filter gives better performance than the sinc^3 filter for rms noise and no missing codes.
MR14	0	This bit must be programmed with a Logic 0 for correct operation.
MR13	ENPAR	Enable parity bit. When ENPAR is set, parity checking on the data register is enabled. The DAT_STA bit in the mode register should be set when the parity check is used. When the DAT_STA bit is set, the contents of the status register are transmitted along with the data for each data register read.
MR12	CLK_DIV	Clock Divide by 2. When CLK_DIV is set, the master clock is divided by 2. For normal conversions, this bit should be set to 0. When performing internal full-scale calibrations, this bit must be set when AV_{DD} is less than 4.75 V. The calibration accuracy is optimized when chop is enabled and a low output data rate is used while performing the calibration. When AV_{DD} is greater than or equal to 4.75 V, it is not compulsory to set the CLK_DIV bit when performing internal full-scale calibrations.
MR11	SINGLE	Single cycle conversion enable bit. When this bit is set, the AD7192 settles in one conversion cycle so that it functions as a zero-latency ADC. This bit has no effect when multiple analog input channels are enabled or when the single conversion mode is selected.
MR10	REJ60	This bit enables a notch at 60 Hz when the first notch of the sinc filter is at 50 Hz. When REJ60 is set, a filter notch is placed at 60 Hz when the sinc filter first notch is at 50 Hz. This allows simultaneous 50 Hz/60 Hz rejection.
MR9 to MR0	FS9 to FS0	Filter output data rate select bits. The 10 bits of data programmed into these bits determine the filter cut-off frequency, the position of the first notch of the filter, and the output data rate for the part. In association with the gain selection, they also determine the output noise (and, therefore, the effective resolution) of the device (see Table 6 through Table 13). When chop is disabled and continuous conversion mode is selected, *Output Data Rate* = (*MCLK*/1024)/*FS* where *FS* is the decimal equivalent of the code in Bit FS0 to Bit FS9 and is in the range 1 to 1023, and *MCLK* is the master clock frequency. With a nominal MCLK of 4.92 MHz, this results in an output data rate from 4.69 Hz to 4.8 kHz. With chop disabled, the first notch frequency is equal to the output data rate when converting on a single channel. When chop is enabled, *Output Data Rate* = (*MCLK*/1024)/(*N x FS*) where *FS* is the decimal equivalent of the code in Bit FS0 to Bit FS9 and is in the range 1 to 1023, and *MCLK* is the master clock frequency. With a nominal MCLK of 4.92 MHz, this results in a conversion rate from 4.69/N Hz to 4.8/N kHz, where N is the order of the sinc filter. The sinc filter's first notch frequency is equal to N × output data rate. The chopping introduces notches at odd integer multiples of (output data rate/2).

Table 18. Operating Modes

MD2	MD1	MD0	Mode
0	0	0	Continuous conversion mode (default). In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. The DOUT/RDY pin and the RDY bit in the status register go low when a conversion is complete. The user can read these conversions by setting the CREAD bit in the communications register to 1, which enables continuous read. When continuous read is enabled, the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output each conversion by writing to the communications register. After power-on, a reset, or a reconfiguration of the ADC, the complete settling time of the filter is required to generate the first valid conversion. Subsequent conversions are available at the selected output data rate, which is dependent on filter choice.
0	0	1	Single conversion mode. When single conversion mode is selected, the ADC powers up and performs a single conversion on the selected channel. The internal clock requires up to 1 ms to power up and settle. The ADC then performs the conversion, which requires the complete settling time of the filter. The conversion result is placed in the data register. RDY goes low, and the ADC returns to power-down mode. The conversion remains in the data register until another conversion is performed. RDY remains active (low) until the data is read or another conversion is performed.
0	1	0	Idle mode. In idle mode, the ADC filter and modulator are held in a reset state even though the modulator clocks are still provided.
0	1	1	Power-down mode. In power-down mode, all AD7192 circuitry, except the bridge power-down switch, is powered down. The bridge power-down switch remains active because the user may need to power up the sensor prior to powering up the AD7192 for settling reasons. The external crystal, if selected, remains active.
1	0	0	Internal zero-scale calibration. An internal short is automatically connected to the input. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.
1	0	1	Internal full-scale calibration. A full-scale input voltage is automatically connected to the input for this calibration. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error. When AV_{DD} is less than 4.75 V, the CLK_DIV bit must be set when performing the internal full-scale calibration.
1	1	0	System zero-scale calibration. The user should connect the system zero-scale input to the channel input pins as selected by the CH7 to CH0 bits in the configuration register. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. A system zero-scale calibration is required each time the gain of a channel is changed.
1	1	1	System full-scale calibration. The user should connect the system full-scale input to the channel input pins as selected by the CH7 to CH0 bits in the configuration register. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed.

CONFIGURATION REGISTER

(RS2, RS1, RS0 = 0, 1, 0; Power-On/Reset = 0x000117)

The configuration register is a 24-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for unipolar or bipolar mode, to enable or disable the buffer, to enable or disable the burnout currents, to select the gain, and to select the analog input channel.

Table 19 outlines the bit designations for the filter register. CON0 through CON23 indicate the bit locations. CON denotes that the bits are in the configuration register. CON23 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

CON23	**CON22**	**CON21**	**CON20**	**CON19**	**CON18**	**CON17**	**CON16**
CHOP(0)	0(0)	0(0)	REFSEL(0)	0(0)	0(0)	0(0)	(0)
CON15	**CON14**	**CON13**	**CON12**	**CON11**	**CON10**	**CON9**	**CON8**
CH7(0)	CH6(0)	CH5(0)	CH4(0)	CH3(0)	CH2(0)	CH1(0)	CH0(1)
CON7	**CON6**	**CON5**	**CON4**	**CON3**	**CON2**	**CON1**	**CON0**
BURN(0)	REFDET(0)	0(0)	BUF(1)	U/$\overline{B}$ (0)	G2(1)	G1(1)	G0(1)

Table 19. Configuration Register Bit Designations

Bit Location	Bit Name	Description				
CON23	CHOP	Chop enable bit. When the CHOP bit is cleared, chop is disabled. When the CHOP bit is set, chop is enabled. When chop is enabled, the offset and offset drift of the ADC are continuously removed. However, this increases the conversion time and settling time of the ADC. For example, when FS = 96 decimal and the sinc^4 filter is selected, the conversion time with chop enabled equals 80 ms and the settling time equals 160 ms. With chop disabled, higher conversion rates are allowed. For an FS word of 96 decimal and the sinc^4 filter selected, the conversion time is 20 ms and the settling time is 80 ms. However, at low gains, periodic calibrations may be required to remove the offset and offset drift.				
CON22, CON21	0	These bits must be programmed with a Logic 0 for correct operation.				
CON20	REFSEL	Reference select bits. The reference source for the ADC is selected using these bits.				
		REFSEL	**Reference Voltage**			
		0	External reference applied between REFIN1(+) and REFIN1(−).			
		1	External reference applied between the P1/REFIN2(+) and P0/REFIN2(−) pins.			
CON19 to CON16	0	These bits must be programmed with a Logic 0 for correct operation.				
CON15 to CON8	CH7 to CH0	Channel select bits. These bits are used to select which channels are enabled on the AD7192 (see Table 20). Several channels can be selected, and the AD7192 automatically sequences them. The conversion on each channel requires the complete settling time. When performing calibrations or when accessing the calibration registers, only one channel can be selected.				
CON7	BURN	When this bit is set to 1, the 500 nA current sources in the signal path are enabled. When BURN = 0, the burnout currents are disabled. The burnout currents can be enabled only when the buffer is active and when chop is disabled.				
CON6	REFDET	Enables the reference detect function. When set, the NOREF bit in the status register indicates when the external reference being used by the ADC is open circuit or less than 0.6 V maximum. The reference detect circuitry operates only when the ADC is active.				
CON5	0	This bit must be programmed with a Logic 0 for correct operation.				
CON4	BUF	Enables the buffer on the analog inputs. If cleared, the analog inputs are unbuffered, lowering the power consumption of the device. If this bit is set, the analog inputs are buffered, allowing the user to place source impedances on the front end without contributing gain errors to the system. With the buffer disabled, the voltage on the analog input pins can be from 50 mV below AGND to 50 mV above AV_{DD}. When the buffer is enabled, it requires some headroom; therefore, the voltage on any input pin must be limited to 250 mV within the power supply rails.				
CON3	U/$\overline{B}$	Polarity select bit. When this bit is set, unipolar operation is selected. When this bit is cleared, bipolar operation is selected.				
CON2 to CON0	G2 to G0	Gain select bits. These bits are written by the user to select the ADC input range as follows:				
		G2	**G1**	**G0**	**Gain**	**ADC Input Range (5 V Reference)**
		0	0	0	1	±5 V
		0	0	1	Reserved	
		0	1	0	Reserved	
		0	1	1	8	±625 mV
		1	0	0	16	±312.5 mV
		1	0	1	32	±156.2 mV
		1	1	0	64	±78.125 mV
		1	1	1	128	±39.06 mV

Table 20. Channel Selection

Channel Enable Bits in the Configuration Register								Channel Enabled		Status Register Bits CHD[2:0]	Calibration Register Pair
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	Positive Input AIN(+)	Negative Input AIN(−)		
							1	AIN1	AIN2	000	0
						1		AIN3	AIN4	001	1
					1			Temperature sensor		010	None
				1				AIN2	AIN2	011	0
			1					AIN1	AINCOM	100	0
		1						AIN2	AINCOM	101	1
	1							AIN3	AINCOM	110	2
1								AIN4	AINCOM	111	3

DATA REGISTER

(RS2, RS1, RS0 = 0, 1, 1; Power-On/Reset = 0x000000)

The conversion result from the ADC is stored in this data register. This is a read-only, 24-bit register. On completion of a read operation from this register, the $\overline{RDY}$ pin/bit is set. When the DAT_STA bit in the mode register is set to 1, the contents of the status register are appended to each 24-bit conversion. This is advisable when several analog input channels are enabled because the three LSBs of the status register (CHD2 to CHD0) identify the channel from which the conversion originated.

ID REGISTER

(RS2, RS1, RS0 = 1, 0, 0; Power-On/Reset = 0xX0)

The identification number for the AD7192 is stored in the ID register. This is a read-only register.

GPOCON REGISTER

(RS2, RS1, RS0 = 1, 0, 1; Power-On/Reset = 0x00)

The GPOCON register is an 8-bit register from which data can be read or to which data can be written. This register is used to enable the general-purpose digital outputs.

Table 21 outlines the bit designations for the GPOCON register. GP0 through GP7 indicate the bit locations. GP denotes that the bits are in the GPOCON register. GP7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
0(0)	BPDSW(0)	GP32EN(0)	GP10EN(0)	P3DAT(0)	P2DAT(0)	P1DAT(0)	P0DAT(0)

Table 21. Register Bit Designations

Bit Location	Bit Name	Description
GP7	0	This bit must be programmed with a Logic 0 for correct operation.
GP6	BPDSW	Bridge power-down switch control bit. This bit is set by the user to close the bridge power-down switch BPDSW to AGND. The switch can sink up to 30 mA. The bit is cleared by the user to open the bridge power–down switch. When the ADC is placed in power-down mode, the bridge power-down switch remains active.
GP5	GP32EN	Digital Output P3 and Digital Output P2 enable. When GP32EN is set, the P3 and P2 digital outputs are active. When GP32EN is cleared, the P3 and P2 pins are tristated, and the P3DAT and P2DAT bits are ignored.
GP4	GP10EN	Digital Output P1 and Digital Output P0 enable. When GP10EN is set, the P1 and P0 digital outputs are active. When GP10EN is cleared, the P1 and P0 outputs are tristated, and the P1DAT and P0DAT bits are ignored. The P1 and P0 pins can be used as a reference input to REFIN2 when the REFSEL bit in the configuration register is set to 1.
GP3	P3DAT	Digital Output P3. When GP32EN is set, the P3DAT bit sets the value of the P3 general-purpose output pin. When P3DAT is high, the P3 output pin is high. When P3DAT is low, the P3 output pin is low. When the GPOCON register is read, the P3DAT bit reflects the status of the P3 pin if GP32EN is set.
GP2	P2DAT	Digital Output P2. When GP32EN is set, the P2DAT bit sets the value of the P2 general-purpose output pin. When P2DAT is high, the P2 output pin is high. When P2DAT is low, the P2 output pin is low. When the GPOCON register is read, the P2DAT bit reflects the status of the P2 pin if GP32EN is set.
GP1	P1DAT	Digital Output P1. When GP10EN is set, the P1DAT bit sets the value of the P1 general-purpose output pin. When P1DAT is high, the P1 output pin is high. When P1DAT is low, the P1 output pin is low. When the GPOCON register is read, the P1DAT bit reflects the status of the P1 pin if GP10EN is set.
GP0	P0DAT	Digital Output P0. When GP10EN is set, the P0DAT bit sets the value of the P0 general-purpose output pin. When P0DAT is high, the P0 output pin is high. When P0DAT is low, the P0 output pin is low. When the GPOCON register is read, the P0DAT bit reflects the status of the P0 pin if GP10EN is set.

OFFSET REGISTER

(RS2, RS1, RS0 = 1, 1, 0; Power-On/Reset = 0x800000)

The offset register holds the offset calibration coefficient for the ADC. The power-on reset value of the offset register is 0x800000. The AD7192 has four offset registers; therefore, each channel has a dedicated offset register (see Table 20). Each of these registers is a 24-bit read/write register. This register is used in conjunction with its associated full-scale register to form a register pair. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. The AD7192 must be placed in power-down mode or idle mode when writing to the offset register.

FULL-SCALE REGISTER

(RS2, RS1, RS0 = 1, 1, 1; Power-On/Reset = 0x5XXXX0)

The full-scale register is a 24-bit register that holds the full-scale calibration coefficient for the ADC. The AD7192 has four full-scale registers; therefore, each channel has a dedicated full-scale register (see Table 20). The full-scale registers are read/write registers. However, when writing to the full-scale registers, the ADC must be placed in power-down mode or idle mode. These registers are configured at power-on with factory-calibrated full-scale calibration coefficients, the calibration being performed at gain = 1. Therefore, every device has different default coefficients. The default value is automatically overwritten if an internal or system full-scale calibration is initiated by the user or if the full-scale register is written to.

ADC CIRCUIT INFORMATION

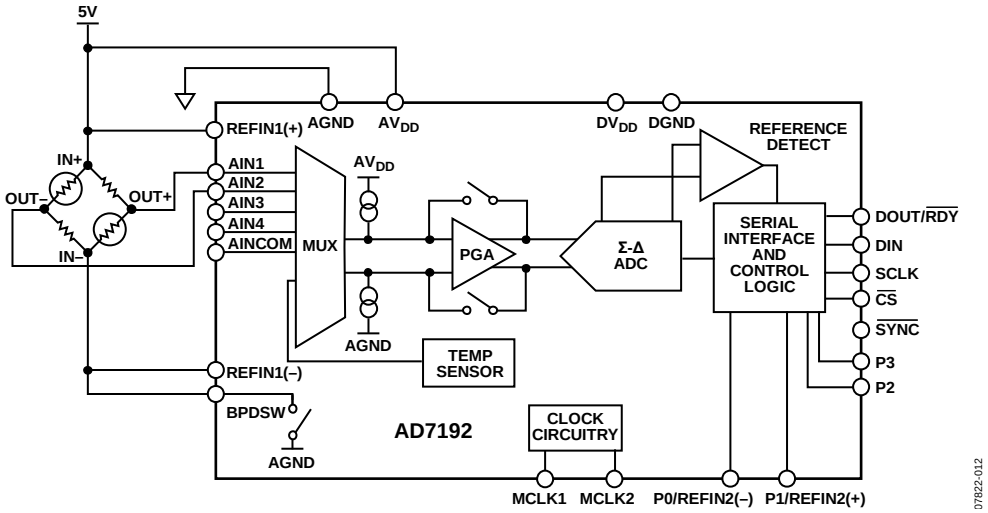

Figure 18. Basic Connection Diagram

OVERVIEW

The AD7192 is an ultralow noise ADC that incorporates a Σ-Δ modulator, a buffer, PGA, and on-chip digital filtering intended for the measurement of wide dynamic range signals such as those in pressure transducers, weigh scales, and strain gage applications.

The part can be configured to have two differential inputs or four pseudo differential inputs that can be buffered or unbuffered. Figure 18 shows the basic connections required to operate the part.

FILTER, OUTPUT DATA RATE, AND SETTLING TIME

A Σ-Δ ADC consists of a modulator followed by a digital filter. The AD7192 has two filter options: a sinc^3 filter and a sinc^4 filter. The filter is selected using the SINC3 bit in the mode register. When the SINC3 bit is set to 0 (default value), the sinc^4 filter is selected. The sinc^3 filter is selected when the SINC3 bit is set to 1.

At low output data rates (<1 kHz), the noise-free resolution is comparable for the two filter types. However, at the higher update rates, the sinc^4 filter gives better noise-free resolution.

The sinc^4 filter also leads to better 50 Hz and 60 Hz rejection. While the notch positions are not affected by the order of the filter, the higher order filter has wider notches, which leads to better rejection in the band (±1 Hz) around the notches. It also gives better stop-band attenuation. The benefit of the sinc^3 filter is its lower settling time for the same output data rate.

Chop Disabled

The output data rate (the rate at which conversions are available on a single channel when the ADC is continuously converting) is equal to

$$f_{ADC} = f_{CLK}/(1024 \times FS[9:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} = master clock (4.92 MHz nominal).
FS[9:0] is the decimal equivalent of Bit FS9 to Bit FS0 in the mode register.

The output data rate can be programmed from 4.7 Hz to 4800 Hz; that is, FS[9:0] can have a value from 1 to 1023.

The previous equation is valid for both the sinc^3 and sinc^4 filters. The settling time for the sinc^4 filter is equal to

$$t_{SETTLE} = 4/f_{ADC}$$

and the settling time for the sinc^3 filter is equal to

$$t_{SETTLE} = 3/f_{ADC}$$

Figure 19 and Figure 20 show the frequency response of the sinc^4 filter and sinc^3 filter, respectively, for an output data rate of 50 Hz.

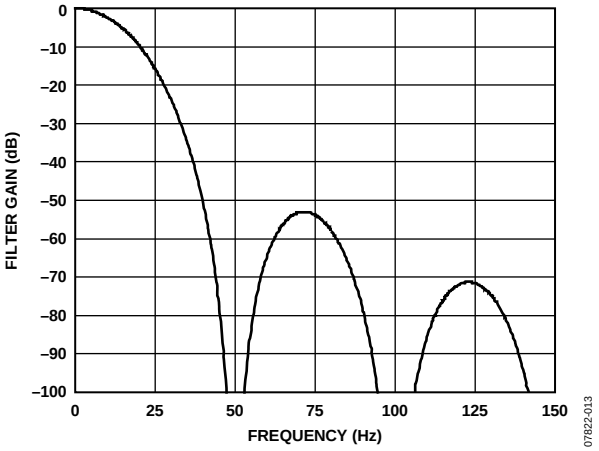

Figure 19. Sinc^4 Filter Response (50 Hz Output Data Rate)

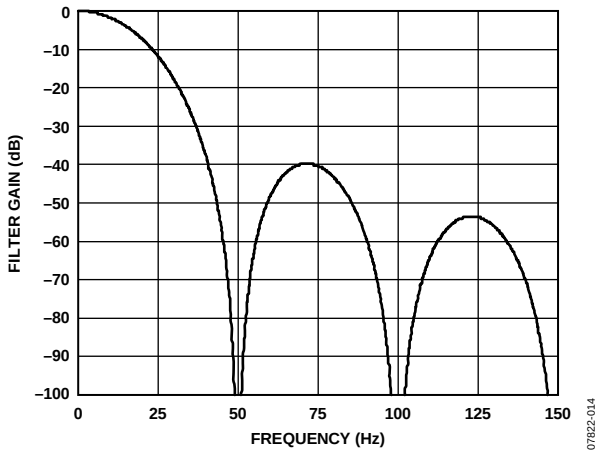

Figure 20. Sinc³ Filter Response (50 Hz Output Data Rate)

The sinc⁴ filter provides 50 Hz (±1 Hz) rejection in excess of 120 dB, assuming a stable master clock, and the sinc³ filter gives a rejection of 100 dB. The stop-band attenuation is, typically, 53 dB for the sinc⁴ filter but equal to 40 dB for the sinc³ filter.

The 3 dB frequency for the sinc⁴ filter is equal to

$$f_{3dB} = 0.23 \times f_{ADC}$$

and for the sinc³ filter, the 3 dB frequency is equal to

$$f_{3dB} = 0.272 \times f_{ADC}$$

Chop Enabled

With chop enabled, the ADC offset and offset drift are minimized. When chop is enabled, the analog input pins are continuously swapped. Therefore, with the analog input pins connected in one direction, the settling time of the sinc filter is allowed to elapse until a valid conversion is available. The analog input pins are then inverted, and another valid conversion is obtained. Subsequent conversions are then averaged so that the offset is minimized. This continuous swapping of the analog input pins and the averaging of subsequent conversions means that the offset drift is also minimized.

Chopping affects the output data rate and settling time of the ADC. For sinc⁴, the output data rate is equal to

$$f_{ADC} = f_{CLK}/(4 \times 1024 \times FS[9:0])$$

For sinc³, the output data rate is equal to

$$f_{ADC} = f_{CLK}/(3 \times 1024 \times FS[9:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} = master clock (4.92 MHz nominal).
$FS[9:0]$ is the decimal equivalent of Bit FS9 to Bit FS0 in the mode register.

The value of FS[9:0] can be varied from 1 to 1023. This results in an output data rate of 1.173 Hz to 1200 Hz for the sinc⁴ filter and 1.56 Hz to 1600 Hz for the sinc³ filter. The settling time for sinc³ or sinc⁴ is equal to

$$t_{SETTLE} = 2/f_{ADC}$$

Therefore, with chop enabled, the settling time is reduced for a given output data rate compared to the chop disabled mode. However, for a given FS[9:0] value, the output data rate is less with chop enabled when compared with the chop disabled mode. For either the sinc³ or sinc⁴ filter, the cutoff frequency f_{3dB} is equal to

$$f_{3dB} = 0.24 \times f_{ADC}$$

Figure 21 and Figure 22 show the filter response for the sinc⁴ filter and sinc³ filter, respectively, when chop is enabled. As shown in the plots, the stop-band attenuation is less when compared with the chop disabled modes.

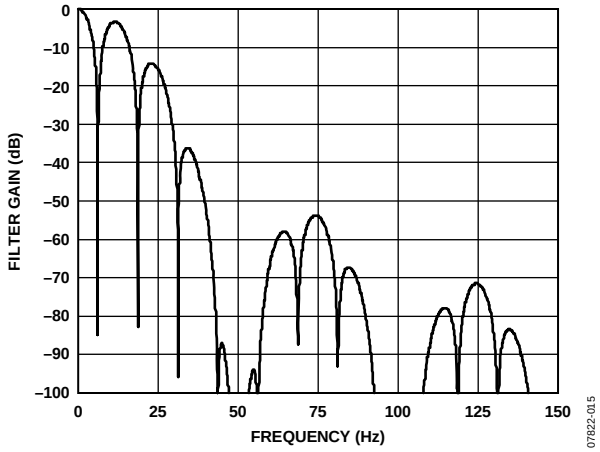

Figure 21. Sinc⁴ Filter Response (Output Data Rate =12.5 Hz, Chop Enabled)

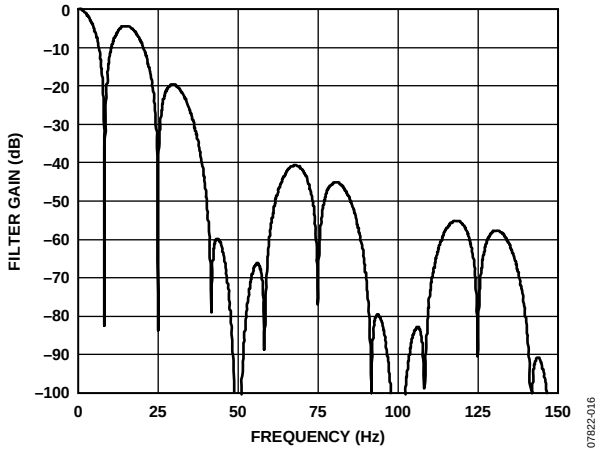

Figure 22. Sinc³ Filter Response (Output Data Rate = 16.6 Hz, Chop Enabled)

50 Hz/60 Hz Rejection

Normal mode rejection is one of the main functions of the digital filter. With chop disabled, 50 Hz rejection is obtained when the output data rate is set to 50 Hz, and 60 Hz rejection is achieved when the output data rate is set to 60 Hz. Simultaneous 50 Hz and 60 Hz rejection is obtained when the output data rate is set to 10 Hz. Simultaneous 50 Hz/60 Hz rejection can also be achieved using the REJ60 bit in the mode register. When the output data rate is programmed to 50 Hz and the REJ60 bit is set to 1, notches are placed at both 50 Hz and 60 Hz. Figure 23 and Figure 24 show the frequency response of the sinc^4 filter and sinc^3 filter, respectively, when the output data rate is programmed to 50 Hz and REJ60 is set to 1.

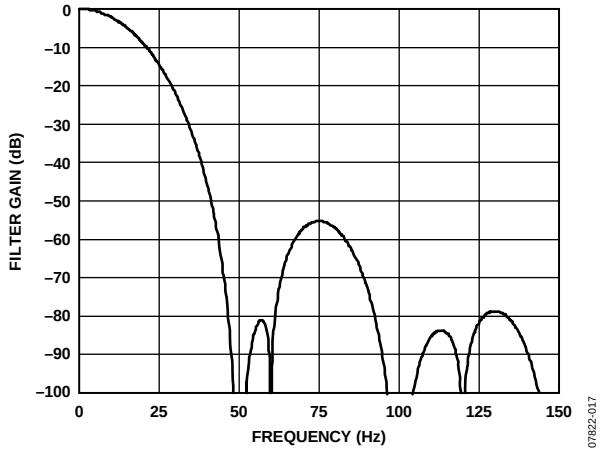

Figure 23. Sinc^4 Filter Response (50 Hz Output Data Rate, REJ60=1)

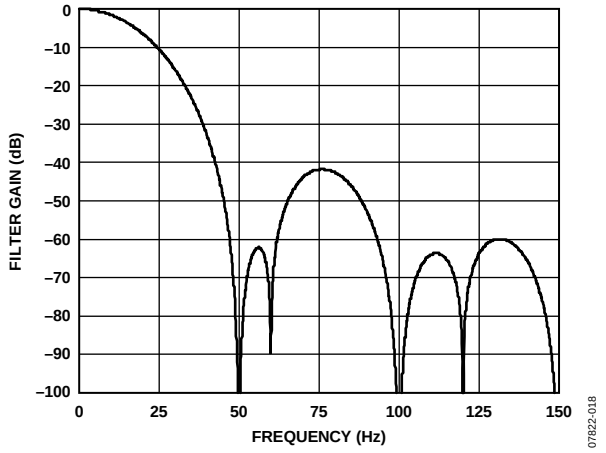

Figure 24. Sinc^3 Filter Response (50 Hz Output Data Rate, REJ60=1)

Again, the sinc^4 filter provides better 50 Hz/60 Hz rejection than the sinc^3 filter. Also, better stop-band attenuation is achieved with the sinc^4 filter.

When chop is enabled, lower output data rates must be used to achieve 50 Hz and 60 Hz rejection. With REJ60 set to 1, an output data rate of 12.5 Hz gives simultaneous 50 Hz/60 Hz rejection when the sinc^4 filter is selected, whereas an output data rate of 16.7 Hz gives simultaneous 50 Hz/60 Hz rejection when the sinc^3 filter is used. Figure 25 and Figure 26 show the filter response for both output data rates when REJ60 is set to 1.

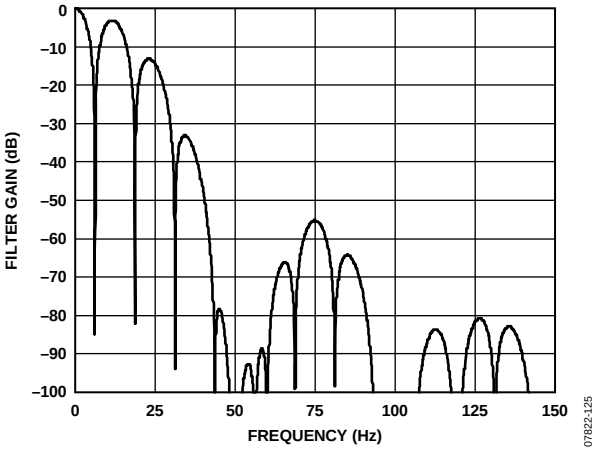

Figure 25. Sinc^4 Filter Response (12.5 Hz Output Data Rate, Chop Enabled, REJ60 = 1)

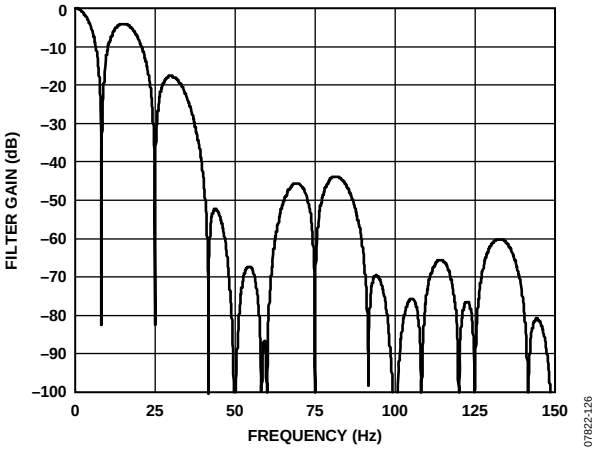

Figure 26. Sinc^3 Filter Response (16.7 Hz Output Data Rate, Chop Enabled, REJ60 = 1)

Zero Latency

Zero latency is enabled by setting the SINGLE bit in the mode register to 1. With zero latency, the complete settling time is allowed for each conversion. Therefore,

$$f_{ADC} = 1/t_{SETTLE}$$

Zero latency means that the output data rate is constant irrespective of the number of analog input channels enabled; the user does not need to consider the effects of channel changes on the output data rate. The disadvantages of zero latency are the increased noise for a given output data rate compared with the nonzero latency mode. For example, when zero latency is not enabled, the AD7192 has a noise-free resolution of 18.5 bits when the output data rate is 50 Hz and the gain is set to 128. When zero latency is enabled, the ADC has a resolution of 17.5 bits peak-to-peak when the output data rate is 50 Hz. The filter response also changes. Figure 19 shows the filter response for the sinc^4 filter when the output data rate is 50 Hz (zero latency disabled). Figure 27 shows the filter response when zero latency is enabled and the output data rate

is 50 Hz (sinc^4 filter); 50 Hz rejection is no longer achieved. The ADC must operate with an output data rate of 12.5 Hz to obtain 50 Hz rejection when zero latency is enabled. To obtain simultaneous 50 Hz/60 Hz rejection, the REJ60 bit in the mode register can be set when the output data rate is equal to 12.5 Hz. The stop-band attenuation is considerably reduced also (3 dB compared with 53 dB in the nonzero latency mode).

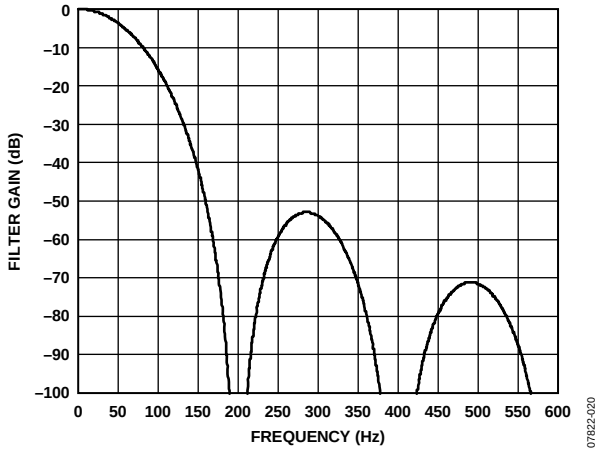

Figure 27. Sinc^4 Filter Response (50 Hz Output Data Rate, Zero Latency)

Channel Sequencer

The AD7192 includes a channel sequencer, which simplifies communications with the device in multichannel applications. The sequencer also optimizes the channel throughput of the device because the sequencer switches channels at the optimum rate rather than waiting for instructions via the SPI interface.

Bit CH0 to Bit CH7 in the configuration register are used to enable the required channels. In continuous conversion mode, the ADC selects each of the enabled channels in sequence and performs a conversion on the channel. The $\overline{\text{RDY}}$ pin goes low when a valid conversion is available on each channel. When several channels are enabled, the contents of the status register should be attached to the 24-bit word so that the user can identify the channel that corresponds to each conversion. To attach the status register value to the conversion, Bit DAT_STA in the mode register should be set to 1.

When several channels are enabled, the ADC must allow the complete settling time to generate a valid conversion each time that the channel is changed. The AD7192 takes care of this: when a channel is selected, the modulator and filter are reset and the $\overline{\text{RDY}}$ pin is taken high. The AD7192 then allows the complete settling time to generate the first conversion. $\overline{\text{RDY}}$ goes low only when a valid conversion is available. The AD7192 then selects the next enabled channel and converts on that channel. The user can then read the data register while the ADC is performing the conversion on the next channel.

The time required to read a valid conversion from all enabled channels is equal to

$$t_{SETTLE} \times number\ of\ enabled\ channels$$

For example, if the sinc^4 filter is selected, chop is disabled, and zero latency is disabled, the settling time for each channel is equal to

$$t_{SETTLE} = 4/f_{ADC}$$

where f_{ADC} is the output data rate when continuously converting on a single channel. The time required to sample N channels is

$$4/(f_{ADC} \times N)$$

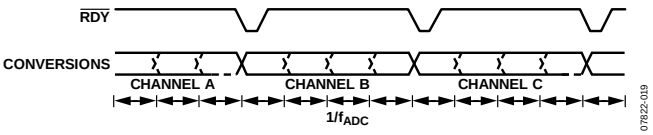

Figure 28. Channel Sequencer

DIGITAL INTERFACE

As indicated in the On-Chip Registers section, the programmable functions of the AD7192 are controlled using a set of on-chip registers. Data is written to these registers via the serial interface of the part. Read access to the on-chip registers is also provided by this interface. All communication with the part must start with a write to the communications register. After power-on or reset, the device expects a write to its communications register. The data written to this register determines whether the next operation is a read operation or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part begins with a write operation to the communications register, followed by a write to the selected register. A read operation from any other register (except when continuous read mode is selected) starts with a write to the communications register, followed by a read operation from the selected register.

The serial interface of the AD7192 consists of four signals: $\overline{\text{CS}}$, DIN, SCLK, and DOUT/$\overline{\text{RDY}}$. The DIN line is used to transfer data into the on-chip registers, and DOUT/$\overline{\text{RDY}}$ is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or DOUT/$\overline{\text{RDY}}$) occur with respect to the SCLK signal.

The DOUT/$\overline{\text{RDY}}$ pin functions as a data ready signal also, the line going low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the data register to indicate when not to read from the device, to ensure that a data read is not attempted while the register is being updated. $\overline{\text{CS}}$ is used to select a device. It can be used to decode the AD7192 in systems where several components are connected to the serial bus.

Figure 3 and Figure 4 show timing diagrams for interfacing to the AD7192, with $\overline{\text{CS}}$ being used to decode the part. Figure 3 shows the timing for a read operation from the output shift register of the AD7192, and Figure 4 shows the timing for a write operation to the input shift register. It is possible to read the same word from the data register several times even though the DOUT/$\overline{\text{RDY}}$

line returns high after the first read operation. However, care must be taken to ensure that the read operations are completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD7192. The end of the conversion can be monitored using the $\overline{RDY}$ bit or pin. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idle high between data transfers.

The AD7192 can be operated with $\overline{CS}$ used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$ because $\overline{CS}$ normally occurs after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

The serial interface can be reset by writing a series of 1s to the DIN input. If a Logic 1 is written to the AD7192 DIN line for at least 40 serial clock cycles, the serial interface is reset. This ensures that the interface can be reset to a known state if the interface gets lost due to a software error or some glitch in the system. Reset returns the interface to the state in which it expects a write to the communications register. This operation resets the contents of all registers to their power-on values. Following a reset, the user should allow a period of 500 µs before addressing the serial interface.

The AD7192 can be configured to continuously convert or to perform a single conversion (see Figure 29 through Figure 31).

Single Conversion Mode

In single conversion mode, the AD7192 is placed in power-down mode after conversions. When a single conversion is initiated by setting MD2, MD1, and MD0 to 0, 0, 1, respectively, in the mode register, the AD7192 powers up, performs a single conversion, and then returns to power-down mode. The on-chip oscillator requires 1 ms, approximately, to power up.

DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. If $\overline{CS}$ is low, DOUT/$\overline{RDY}$ remains high until another conversion is initiated and completed. The data register can be read several times, if required, even when DOUT/$\overline{RDY}$ has gone high.

If several channels are enabled, the ADC sequences through the enabled channels and performs a conversion on each channel. When a conversion is started, DOUT/$\overline{RDY}$ goes high and remains high until a valid conversion is available. As soon as the conversion is available, DOUT/$\overline{RDY}$ goes low. The ADC then selects the next channel and begins a conversion. The user can read the present conversion while the next conversion is being performed. As soon as the next conversion is complete, the data register is updated; therefore, the user has a limited period in which to read the conversion. When the ADC has performed a single conversion on each of the selected channels, it returns to power-down mode.

If the DAT_STA bit in the mode register is set to 1, the contents of the status register are output along with the conversion each time that the data read is performed. The four LSBs of the status register indicate the channel to which the conversion corresponds.

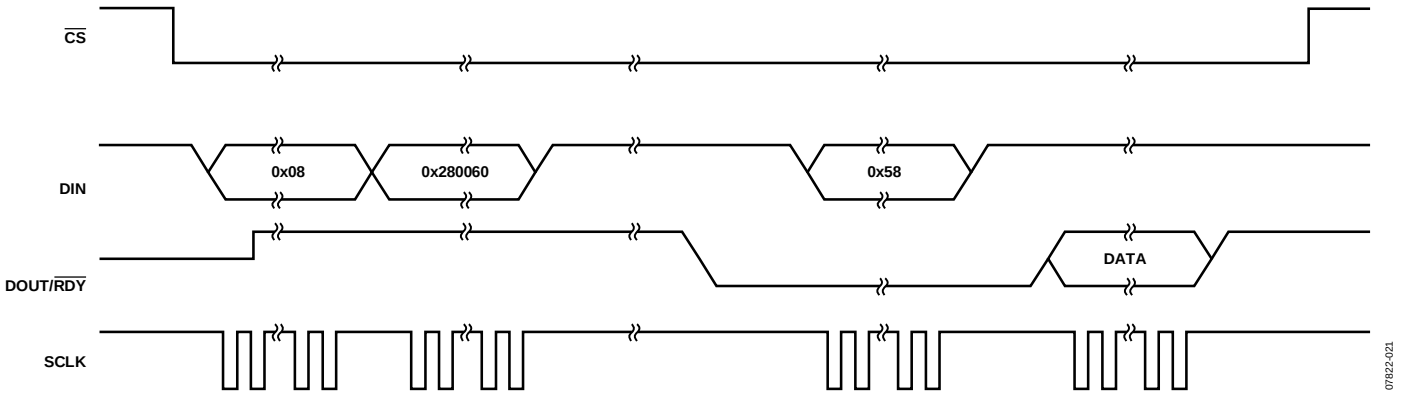

Figure 29. Single Conversion

Continuous Conversion Mode

Continuous conversion is the default power-up mode. The AD7192 converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is completed. To read a conversion, the user writes to the communications register, indicating that the next operation is a read of the data register. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion or else the new conversion word is lost.

When several channels are enabled, the ADC continuously loops through the enabled channels, performing one conversion on each channel per loop. The data register is updated as soon as each conversion is available. The DOUT/$\overline{RDY}$ pin pulses low each time a conversion is available. The user can then read the conversion while the ADC converts on the next enabled channel.

If the DAT_STA bit in the mode register is set to 1, the contents of the status register are output along with the conversion each time that the data read is performed. The status register indicates the channel to which the conversion corresponds.

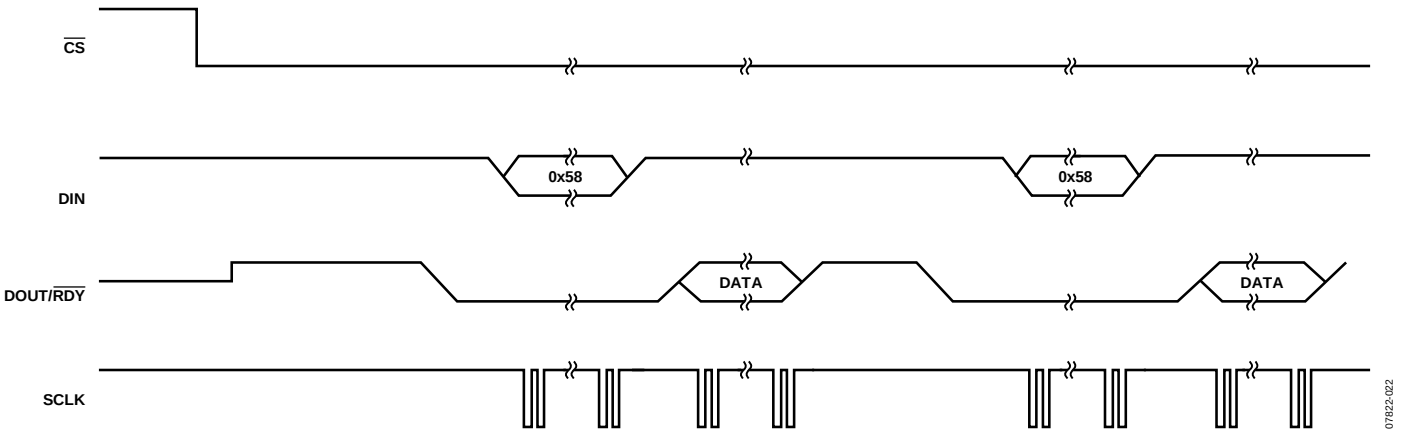

Figure 30. Continuous Conversion

Continuous Read

Rather than write to the communications register each time a conversion is complete to access the data, the AD7192 can be configured so that the conversions are placed on the DOUT/$\overline{RDY}$ line automatically. By writing 01011100 to the communications register, the user need only apply the appropriate number of SCLK cycles to the ADC, and the conversion word is automatically placed on the DOUT/$\overline{RDY}$ line when a conversion is complete. The ADC should be configured for continuous conversion mode.

When DOUT/$\overline{RDY}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC; the data conversion is then placed on the DOUT/$\overline{RDY}$ line. When the conversion is read, DOUT/$\overline{RDY}$ returns high until the next conversion is available. In this mode, the data can be read only once. Also, the user must ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion, or if insufficient serial clocks are applied to the AD7192 to read the word, the serial output register is reset when the next conversion is complete, and the new conversion is placed in the output serial register.

To exit the continuous read mode, the Instruction 01011000 must be written to the communications register while the $\overline{RDY}$ pin is low. While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset occurs if 40 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.

When several channels are enabled, the ADC continuously steps through the enabled channels and performs one conversion on each channel each time that it is selected. DOUT/$\overline{RDY}$ pulses low when a conversion is available. When the user applies sufficient SCLK pulses, the data is automatically placed on the DOUT/$\overline{RDY}$ pin. If the DAT_STA bit in the mode register is set to 1, the contents of the status register are output along with the conversion. The status register indicates the channel to which the conversion corresponds.

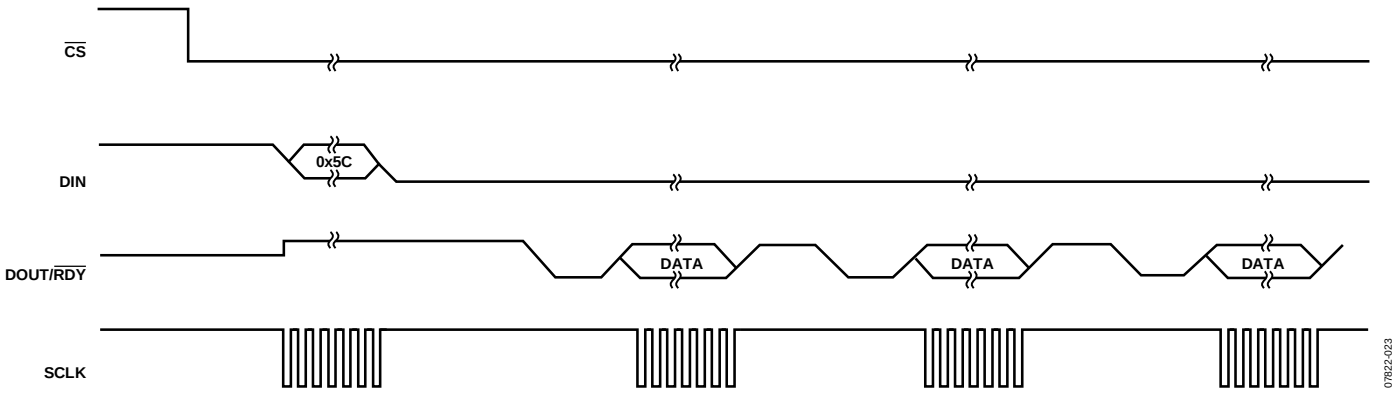

Figure 31. Continuous Read

CIRCUIT DESCRIPTION

ANALOG INPUT CHANNEL

The AD7192 has two differential/four pseudodifferential analog input channels, which can be buffered or unbuffered. In buffered mode (the BUF bit in the configuration register is set to 1), the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive-type sensors such as strain gages or resistance temperature detectors (RTDs).

When BUF = 0, the part is operated in unbuffered mode. This results in a higher analog input current. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause gain errors, depending on the output impedance of the source that is driving the ADC input. Table 22 shows the allowable external resistance/capacitance values for unbuffered mode at a gain of 1 such that no gain error at the 20-bit level is introduced.

Table 22. External R-C Combination for No 20-Bit Gain Error

C (pF)	R (Ω)
50	1.4 k
100	850
500	300
1000	230
5000	30

The absolute input voltage range in buffered mode is restricted to a range between AGND + 250 mV and AV_{DD} − 250 mV. Care must be taken in setting up the common-mode voltage so that these limits are not exceeded. Otherwise, there is degradation in linearity and noise performance.

The absolute input voltage in unbuffered mode includes the range between AGND − 50 mV and AV_{DD} + 50 mV. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to AGND.

PROGRAMMABLE GAIN ARRAY (PGA)

When the gain stage is enabled, the output from the buffer is applied to the input of the PGA. The presence of the PGA means that signals of small amplitude can be gained within the AD7192 while still maintaining excellent noise performance. For example, when the gain is set to 128, the rms noise is 11 nV, typically, when the output data rate is 4.7 Hz, which is equivalent to 22.5 bits of effective resolution or 20 bits of noise-free resolution.

The AD7192 can be programmed to have a gain of 1, 8, 16, 32, 64, and 128 using Bit G2 to Bit G0 in the configuration register. Therefore, with an external 2.5 V reference, the unipolar ranges are from 0 mV to 19.53 mV to 0 V to 2.5 V and the bipolar ranges are from ±19.53 mV to ±2.5 V.

The analog input range must be limited to ±(AV_{DD} − 1.25 V)/gain because the PGA requires some headroom. Therefore, if AV_{DD} = 5 V, the maximum analog input that can be applied to the AD7192 is 0 to 3.75 V/gain in unipolar mode or ±3.75 V/gain in bipolar mode.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the AD7192 can accept either unipolar or bipolar input voltage ranges. A bipolar input range does not imply that the part can tolerate negative voltages with respect to system AGND. In pseudo-differential mode, signals are referenced to AINCOM, while in differential mode, signals are referenced to the negative input of the differential pair. For example, if AINCOM is 2.5 V and the AD7192 AIN1 analog input is configured for unipolar mode with a gain of 2, the input voltage range on the AIN1 pin is 2.5 V to 3.75 V when a 2.5 V reference is used.

If AINCOM is 2.5 V and the AD7192 AIN1 analog input is configured for bipolar mode with a gain of 2, the analog input range on AIN1 is 1.25 V to 3.75 V The bipolar/unipolar option is chosen by programming the U/$\overline{B}$ bit in the configuration register.

DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00...00, a midscale voltage resulting in a code of 100...000, and a full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = (2^N \times AIN \times Gain)/V_{REF}$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000...000, a zero differential input voltage resulting in a code of 100...000, and a positive full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN \times Gain/V_{REF}) + 1]$$

where *AIN* is the analog input voltage, *Gain* is the PGA setting (1 to 128), and $N = 24$.

CLOCK

The AD7192 includes an internal 4.92 MHz clock on-chip. This internal clock has a tolerance of ±4%. Either the internal clock or an external crystal/clock can be used as the clock source to the AD7192. The clock source is selected using the CLK1 and CLK0 bits in the mode register. When an external crystal is used, it must be connected across the MCLK1 and MCLK2 pins. The crystal manufacturer recommends the load capacitances required for the crystal. The MCLK1 and MCLK2 pins of the AD7192 have a capacitance of 15 pF, typically. If an external

clock source is used, the clock source must be connected to the MCLK2 pin, and the MCLK1 pin can be left floating.

The internal clock can also be made available at the MCLK2 pin. This is useful when several ADCs are used in an application and the devices must be synchronized. The internal clock from one device can be used as the clock source for all ADCs in the system. Using a common clock, the devices can be synchronized by applying a common reset to all devices, or the $\overline{\text{SYNC}}$ pin can be pulsed.

BURNOUT CURRENTS

The AD7192 contains two 500 nA constant current generators, one sourcing current from AV_{DD} to AIN(+) and one sinking current from AIN(−) to AGND, where AIN(+) is the positive analog input terminal and AIN(−) is the negative analog input terminal in differential mode and AINCOM in pseudodifferential mode. The currents are switched to the selected analog input pair. Both currents are either on or off, depending on the burnout current enable (BURN) bit in the configuration register.

These currents can be used to verify that an external transducer is still operational before attempting to take measurements on that channel. After the burnout currents are turned on, they flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. It takes some time for the burnout currents to detect an open circuit condition because the currents must charge any external capacitors.

There are several reasons that a fault condition is detected. The front-end sensor may be open circuit. It could also mean that the front-end sensor is overloaded or the reference may be absent and the NOREF bit in the status register is set, thus clamping the data to all 1s.

The user must check these three cases before making a judgment. If the voltage measured is 0 V, it may indicate that the transducer has short circuited. The current sources work over the normal absolute input voltage range specifications when the analog inputs are buffered and chop is disabled.

REFERENCE

The ADC has a fully differential input capability for the reference channel. In addition, the user has the option of selecting one of two external reference options (REFIN1(x) or REFIN2(x)). The reference source for the AD7192 is selected using the REFSEL bit in the configuration register. The REFIN2(x) pins are dual purpose: they can function as two general-purpose output pins or as reference pins. When the REFSEL bit is set to 1, these pins automatically function as reference pins.

The common-mode range for these differential inputs is from AGND to AV_{DD}. The reference input is unbuffered; therefore, excessive R-C source impedances introduce gain errors. The reference voltage REFIN (REFINx(+) − REFINx(−)) is AV_{DD} nominal, but the AD7192 is functional with reference voltages from 1 V to AV_{DD}. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source is removed because the application is ratiometric. If the AD7192 is used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7192 include the ADR421 and ADR431, which are low noise references. These references have low output impedances and are, therefore, tolerant to having decoupling capacitors on REFINx(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. External decoupling on the REFINx pins is not recommended in this type of circuit configuration.

REFERENCE DETECT

The AD7192 includes on-chip circuitry to detect whether the part has a valid reference for conversions or calibrations. This feature is enabled when the REFDET bit in the configuration register is set to 1. If the voltage between the selected REFINx(+) and REFINx(−) pins is between 0.3 V and 0.6 V, the AD7192 detects that it no longer has a valid reference. In this case, the NOREF bit of the status register is set to 1. If the AD7192 is performing normal conversions and the NOREF bit becomes active, the conversion result is all 1s.

Therefore, it is not necessary to continuously monitor the status of the NOREF bit when performing conversions. It is only necessary to verify its status if the conversion result read from the ADC data register is all 1s. If the AD7192 is performing either an offset or full-scale calibration and the NOREF bit becomes active, the updating of the respective calibration registers is inhibited to avoid loading incorrect coefficients to these registers, and the ERR bit in the status register is set. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, the status of the ERR bit should be checked at the end of the calibration cycle.

RESET

The circuitry and serial interface of the AD7192 can be reset by writing consecutive 1s to the device; 40 consecutive 1s are required to perform the reset. This resets the logic, the digital filter, and the analog modulator, whereas all on-chip registers are reset to their default values. A reset is automatically performed on power-up. When a reset is initiated, the user must allow a period of 500 µs before accessing any of the on-chip registers. A reset is useful if the serial interface loses synchronization due to noise on the SCLK line.

SYSTEM SYNCHRONIZATION

The $\overline{\text{SYNC}}$ input allows the user to reset the modulator and the digital filter without affecting any of the setup conditions on the part. This allows the user to start gathering samples of the analog input from a known point in time, that is, the rising edge of $\overline{\text{SYNC}}$. $\overline{\text{SYNC}}$ needs to be taken low for at least four master clock cycles to implement the synchronization function.

If multiple AD7192 devices are operated from a common master clock, they can be synchronized so that their data registers are updated simultaneously. A falling edge on the $\overline{\text{SYNC}}$ pin resets the digital filter and the analog modulator and places the AD7192 into a consistent, known state. While the $\overline{\text{SYNC}}$ pin is low, the AD7192 is maintained in this state. On the $\overline{\text{SYNC}}$ rising edge, the modulator and filter are taken out of this reset state and, on the next clock edge, the part starts to gather input samples again. In a system using multiple AD7192 devices, a common signal to their $\overline{\text{SYNC}}$ pins synchronizes their operation. This is normally done after each AD7192 has performed its own calibration or has calibration coefficients loaded into its calibration registers. The conversions from the AD7192s are then synchronized.

The part is taken out of reset on the master clock falling edge following the $\overline{\text{SYNC}}$ low to high transition. Therefore, when multiple devices are being synchronized, the $\overline{\text{SYNC}}$ pin should be taken high on the master clock rising edge to ensure that all devices begin sampling on the master clock falling edge. If the $\overline{\text{SYNC}}$ pin is not taken high in sufficient time, it is possible to have a difference of one master clock cycle between the devices; that is, the instant at which conversions are available differs from part to part by a maximum of one master clock cycle.

The $\overline{\text{SYNC}}$ pin can also be used as a start conversion command. In this mode, the rising edge of $\overline{\text{SYNC}}$ starts conversion, and the falling edge of $\overline{\text{RDY}}$ indicates when the conversion is complete. The settling time of the filter has to be allowed for each data register update. For example, if the ADC is configured to use the sinc^4 filter, zero latency is disabled, and chop is disabled, the settling time equals $4/f_{ADC}$ where f_{ADC} is the output data rate when continuously converting on a single channel.

TEMPERATURE SENSOR

Embedded in the AD7192 is a temperature sensor. This is selected using the CH2 bit in the configuration register. When the CH2 bit is set to 1, the temperature sensor is enabled. When the temperature sensor is selected and bipolar mode is selected, the device should return a code of 0x800000 when the temperature is 0 K. A one-point calibration is needed to get the optimum performance from the sensor. Therefore, a conversion at 25°C should be recorded and the sensitivity calculated. The sensitivity is 2815 codes/°C, approximately. The equation for the temperature sensor is

$$Temp\ (\text{K}) = (Conversion - 0\text{x}800000)/2815\ \text{K}$$

$$Temp\ (^\circ\text{C}) = Temp\ (\text{K}) - 273$$

Following the one-point calibration, the internal temperature sensor has an accuracy of ±2 °C, typically.

BRIDGE POWER-DOWN SWITCH

In bridge applications such as strain gages and load cells, the bridge itself consumes the majority of the current in the system. For example, a 350 Ω load cell requires 15 mA of current when excited with a 5 V supply. To minimize the current consumption of the system, the bridge can be disconnected (when it is not being used) using the bridge power-down switch. Figure 18 shows how the bridge power-down switch is used. The switch can withstand 30 mA of continuous current, and it has an on resistance of 11 Ω maximum.

LOGIC OUTPUTS

The AD7192 has four general-purpose digital outputs, P0, P1, P2, and P3. These are enabled using the GP32EN and GP10EN bits in the GPOCON register. The pins can be pulled high or low using the P0DAT to P3DAT bits in the GPOCON register; that is, the value at the pin is determined by the setting of the P0DAT to P3DAT bits. The logic levels for these pins are determined by AV_{DD} rather than by DV_{DD}. When the GPOCON register is read, Bit P0DAT to Bit P3DAT reflect the actual value at the pins. This is useful for short-circuit detection.

These pins can be used to drive external circuitry, for example, an external multiplexer. If an external multiplexer is used to increase the channel count, the multiplexer logic pins can be controlled via the AD7192 general-purpose output pins. The general-purpose output pins can be used to select the active multiplexer pin. Because the operation of the multiplexer is independent of the AD7192, the AD7192 modulator and filter should be reset using the $\overline{\text{SYNC}}$ pin or by a write to the mode or configuration register each time that the multiplexer channel is changed.

ENABLE PARITY

The AD7192 also has a parity check function on chip that detects 1-bit errors in the serial communications between the ADC and the microprocessor. When the ENPAR bit in the mode register is set to 1, parity is enabled. The contents of the status register must be transmitted along with each 24-bit conversion when the parity function is enabled. To append the contents of the status register to each conversion read, the DAT_STA bit in the mode register should be set to 1. For each conversion read, the parity bit in the status register is programmed so that the overall number of 1s transmitted in the 24-bit data-word is even. Therefore, for example, if the 24-bit conversion contains eleven 1s (binary format), the parity bit is set to 1 so that the total number of 1s in the serial transmission is even. If the microprocessor receives an odd number of 1s, it knows that the data received has been corrupted.

The parity function detects only 1-bit errors. For example, two bits of corrupt data can result in the microprocessor receiving an even number of 1s. Therefore, an error condition is not detected.

CALIBRATION

The AD7192 provides four calibration modes that can be programmed via the mode bits in the mode register. These modes are internal zero-scale calibration, internal full-scale calibration, system zero-scale calibration, and system full-scale calibration. A calibration can be performed at any time by setting the MD2 to MD0 bits in the mode register appropriately. A calibration should be performed when the gain is changed. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register. The offset calibration coefficient is subtracted from the result prior to multiplication by the full-scale coefficient.

To start a calibration, write the relevant value to the MD2 to MD0 bits. The DOUT/$\overline{\text{RDY}}$ pin and the $\overline{\text{RDY}}$ bit in the status register go high when the calibration is initiated. When the calibration is complete, the contents of the corresponding calibration registers are updated, the $\overline{\text{RDY}}$ bit in the status register is reset, the DOUT/$\overline{\text{RDY}}$ pin returns low (if $\overline{\text{CS}}$ is low), and the AD7192 reverts to idle mode.

During an internal zero-scale or full-scale calibration, the respective zero input and full-scale input are automatically connected internally to the ADC input pins. A system calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the ADC pins before initiating the calibration mode. In this way, errors external to the ADC are removed.

From an operational point of view, treat a calibration like another ADC conversion. A zero-scale calibration, if required, must always be performed before a full-scale calibration. Set the system software to monitor the $\overline{\text{RDY}}$ bit in the status register or the DOUT/$\overline{\text{RDY}}$ pin to determine the end of calibration via a polling sequence or an interrupt-driven routine.

With chop disabled, both an internal zero-scale calibration and a system zero-scale calibration require a time equal to the settling time, t_{SETTLE} ($4/f_{ADC}$ for the sinc^4 filter and $3/f_{ADC}$ for the sinc^3 filter).

With chop enabled, an internal zero-scale calibration is not needed because the ADC itself minimizes the offset continuously. However, if an internal zero-scale calibration is performed, the settling time, t_{SETTLE} ($2/f_{ADC}$), is required to perform the calibration. Similarly, a system zero-scale calibration requires a time of t_{SETTLE} to complete.

To perform an internal full-scale calibration, a full-scale input voltage is automatically connected to the selected analog input for this calibration. For a gain of 1, the time required for an internal full-scale calibration is equal to t_{SETTLE}. For higher gains, the internal full-scale calibration requires a time of $2 \times t_{SETTLE}$. A full-scale calibration is recommended each time the gain of a channel is changed to minimize the full-scale error.

A system full-scale calibration requires a time of t_{SETTLE}. With chop disabled, the zero-scale calibration (internal or system zero-scale) should be performed before the system full-scale calibration is initiated.

An internal zero-scale calibration, system zero-scale calibration, and system full-scale calibration can be performed at any output data rate. An internal full-scale calibration can be performed at any output data rate for which the filter word, FS[9:0], is divisible by 16, FS[9:0] being the decimal equivalent of the 10-bit word written to Bit FS9 to Bit FS0 in the mode register. Therefore, internal full-scale calibrations can be performed at output data rates such as 10 Hz or 50 Hz when chop is disabled. Using these lower output data rates results in better calibration accuracy.

The offset error is, typically, 150 μV/gain. If the gain is changed, it is advisable to perform a calibration. A zero-scale calibration (an internal zero-scale calibration or a system zero-scale calibration) reduces the offset error to the order of the noise.

The gain error of the AD7192 is factory calibrated at a gain of 1 with a 5 V power supply at ambient temperature. Following this calibration, the gain error is 0.001%, typically, at 5 V. Table 23 shows the typical uncalibrated gain error for the different gain settings.

Table 23. Typical Precalibration Gain Error vs. Gain

Gain	Precalibration Gain Error (%)
8	−0.11
16	−0.20
32	−0.23
64	−0.29
128	−0.39

An internal full-scale calibration reduces the gain error to 0.001%, typically, when the gain is equal to 1. For higher gains, the gain error post internal full-scale calibration is 0.003%, typically when AV_{DD} is equal to 5 V. When AV_{DD} is less than

4.75 V, the gain error post internal full-scale calibration is 0.005%, typically.

When AV_{DD} is less than 4.75 V, the CLK_DIV bit must be set when performing internal full-scale calibrations. The accuracy of the internal full-scale calibration is further increased if chop is enabled and a low output data rate is used while performing the calibration.

A system full-scale calibration reduces the gain error to the order of the noise irrespective of the analog power supply voltage.

The AD7192 gives the user access to the on-chip calibration registers, allowing the microprocessor to read the calibration coefficients of the device and also to write its own calibration coefficients from prestored values in the EEPROM. A read of the registers can be performed at any time. However, the ADC must be placed in power-down or idle mode when writing to the registers. The values in the calibration registers are 24 bits wide. The span and offset of the part can also be manipulated using the registers.

GROUNDING AND LAYOUT

Because the analog inputs and reference inputs are differential, most of the voltages in the analog modulator are common-mode voltages. The high common-mode rejection of the part removes common-mode noise on these inputs. The analog and digital supplies to the AD7192 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency.

Connect an R-C filter to each analog input pin to provide rejection at the modulator sampling frequency. A 100 Ω resistor in series with each analog input, a 0.1 µF capacitor between the analog input pins, and a 0.01 µF capacitor from each analog input to AGND are advised.

The digital filter also removes noise from the analog and reference inputs provided that these noise sources do not saturate the analog modulator. As a result, the AD7192 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7192 is so high and the noise levels from the converter so low, care must be taken with regard to grounding and layout.

The printed circuit board (PCB) that houses the ADC must be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes because it gives the best shielding.

Although the AD7192 has separate pins for analog and digital ground, the AGND and DGND pins are tied together internally via the substrate. Therefore, the user must not tie these two pins to separate ground planes unless the ground planes are connected together near the AD7192.

In systems in which the AGND and DGND are connected somewhere else in the system (that is, the power supply of the system), they should not be connected again at the AD7192 because a ground loop results. In these situations, it is recommended that the ground pins of the AD7192 be tied to the AGND plane.

In any layout, the user must keep in mind the flow of currents in the system, ensuring that the paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND.

Avoid running digital lines under the device, because this couples noise onto the die, and allow the analog ground plane to run under the AD7192 to prevent noise coupling. The power supply lines to the AD7192 must use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Shield fast switching signals like clocks with digital ground to prevent radiating noise to other sections of the board, and never run clock signals near the analog inputs. Avoid crossover of digital and analog signals. Run traces on opposite sides of the board at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, whereas signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. Decouple all analog supplies with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to AGND. To achieve the best results from these decoupling components, place them as close as possible to the device, ideally right up against the device. Decouple all logic chips with 0.1 µF ceramic capacitors to DGND. In systems in which a common supply voltage is used to drive both the AV_{DD} and DV_{DD} of the AD7192, it is recommended that the system AV_{DD} supply be used. For this supply, place the recommended analog supply decoupling capacitors between the AV_{DD} pin of the AD7192 and AGND and the recommended digital supply decoupling capacitor between the DV_{DD} pin of the AD7192 and DGND.

APPLICATIONS INFORMATION

The AD7192 provides a low-cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, the part is more immune to noisy environments, making it ideal for use in sensor measurement and industrial and process control applications.

WEIGH SCALES

Figure 32 shows the AD7192 being used in a weigh scale application. The load cell is arranged in a bridge network and gives a differential output voltage between its OUT+ and OUT– terminals. Assuming a 5 V excitation voltage, the full-scale output range from the transducer is 10 mV when the sensitivity is 2 mV/V. The excitation voltage for the bridge can be used to directly provide the reference for the ADC because the reference input range includes the supply voltage.

A second advantage of using the AD7192 in transducer-based applications is that the bridge power-down switch can be fully utilized to minimize the power consumption of the system. The bridge power-down switch is connected in series with the cold side of the bridge. In normal operation, the switch is closed and measurements can be taken. In applications in which current consumption is being minimized, the AD7192 can be placed in standby mode, thus significantly reducing the power consumed in the application. In addition, the bridge power-down switch can be opened while in standby mode, thus avoiding unnecessary power consumption by the front-end transducer. When the part is taken out of standby mode and the bridge power-down switch is closed, the user should ensure that the front end circuitry is fully settled before attempting a read from the AD7192.

For simplicity, external filters are not included in Figure 32. However, an R-C antialias filter must be included on each analog input. This is required because the on-chip digital filter does not provide any rejection around the modulator sampling frequency or multiples of this frequency. Suitable values are a 100 Ω resistor in series with each analog input, a 0.1 µF capacitor between the analog input pins, and a 0.01 µF capacitor from each analog input pin to AGND.

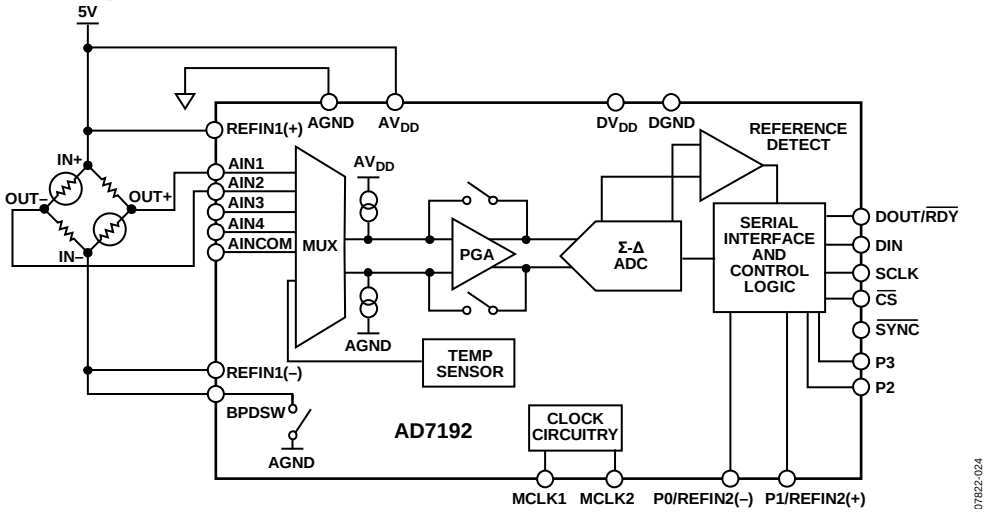

Figure 32. Typical Application (Weigh Scale)

OUTLINE DIMENSIONS

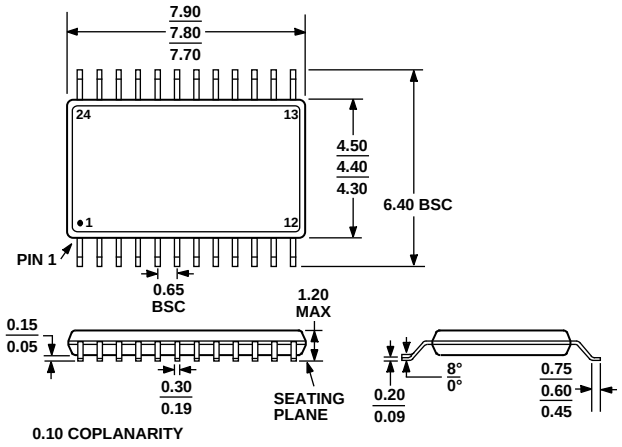

Figure 33. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7192BRUZ[1]	–40°C to +105°C	24-Lead TSSOP	RU-24
AD7192BRUZ-REEL[1]	–40°C to +105°C	24-Lead TSSOP	RU-24

[1] Z = RoHS Compliant Part.

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