查询"LC896431"供应商



CMOS IC

LC896431

MD Decoder IC

Overview

The LC896431 implements playback signal processing that conforms to the MiniDisc format standards. This device was designed to form a chip set in conjunction with a SANYO RF amplifier IC.

Features

- Fabricated in a CMOS process for low power
- An application system can be created easily by combining this IC with a SANYO RF amplifier IC.
- Provides digital servo functions and a VCEC for high-speed access.
- Allows the creation of optimal systems by integrating 8× oversampling digital filters, a 1-bit D/A converter, and a low-pass filter on the same chip.

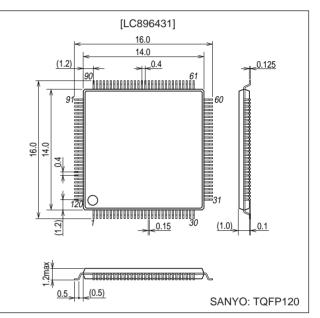
Functions

- Full complement of automatic adjustment functions
- Intensity, defect, and shock detection
- Both CLV and CAV control
- VCEC circuit
- Automatic adjustment functions
- High-performance ATRAC3 decoder
- EFM data demodulation
- Error detection and correction (C1: E12, C2: E24)
- Error correction RAM
- Intelligent commands
- Anti-shock control
- ADIP demodulation and decoding
- Digital servo
- EFM ACIRC decoding
- High-performance 1-bit D/A converter
- · Built-in second-order low-pass filter for audio output
- · Power saving function for the stopped and paused states

Package Dimensions

unit: mm

3257-TQFP120



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Specifications

Maximum Ratings at $V_{SS} = 0 V$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD1} max		2.7	V
Supply voltage	V _{DD2} max		2.7	V
Input and output voltage	V _I , V _O		0 to V _{DD2}	V
Operating temperature *1	Topr		-10 to +70	°C
Storage temperature	Tstg		-55 to +125	°C
Input and output current *2	I _I , I _O		±20	mA

Notes: 1. Does not guarantee continuous operation.

2. Maximum output current that flows constantly (except OUTL, OUTR, SLC0, PD0 pins)

Allowable Operating Ranges at $Ta = -10^{\circ}C$ to $+70^{\circ}C$, $V_{SS} = 0$ V

In case of external I/O power supply, $V_{DD2} = 2.3 \text{ V}$

Doror	Parameter		Symbol Conditions	Ratings			Unit
Fala				min	typ	max	Unit
	External I/O	V _{DD2}		2.2	2.3	2.4	
	Internal	V _{DD}		1.5	1.6	1.8	
Supply voltage		AV _{DD}		2.2	_	2.6	V
	Analog system	AV _{DD1}		2.2	_	2.6	
		VCV _{DD}		2.2	—	2.6	

In case of external I/O power supply, $V_{DD2} = 2.5 \text{ V}$

Parameter		Symbol	Symbol Conditions -	Ratings			Unit
Fala	Falameter			min	typ	max	Unit
	External I/O	V _{DD2}		2.2	2.5	2.55	
	Internal	V _{DD}		1.55	1.6	1.80	
Supply voltage		AV _{DD}		2.2	—	2.6	V
	Analog system	AV _{DD1}		2.2	—	2.6	
		VCV _{DD}		2.2	_	2.6	

Notes: 1. Supply all power supplies at less than the maximum gradient of 0.4 V/ms, and implement a delay of 10 ms or longer for current to go from 0 V to 2.4 V.

2. Supply all power supplies simultaneously so that there are no delay differences among them.

3. Supply 0 to the RESETB pin only upon power application, and following power application, supply 1 and use with this value.

Electrical Characteristics DC characteristics Input/output level: at Ta = -10 to 70° C, $V_{SS} = 0$ V, $V_{DD1} = 1.5$ to 1.8 V, $V_{DD2} = 2.2$ to 2.55 V

Parameter	Symbol	Symbol Conditions	Ratings			Unit
Falameter	Symbol	Conditions	min	typ	max	Unit
		Except *1 to *3	$V_{DD2} imes 0.75$	_	—	
Input high-level voltage	VIH	*1	$V_{DD2} imes 0.80$	_	_	V
		*2	V _{DD2} /2 + 0.10	_	V _{DD2}	
	VIL	Except *1 to *3	—	_	$V_{DD2}\!\times\!0.25$	4 1
Input low-level voltage		*1	—	_	$V_{DD2}\!\times\!0.20$	
		*2	V _{SS}	_	V _{DD2} /2 - 0.10	
Output high-level voltage	V _{OH}	I _{OH2} = -1 mA, Except *4	$V_{DD2} imes 0.80$	_	_	V
Output low-level voltage	V _{OL}	I _{OL} = 1 mA, Except *4	—	_	$V_{DD2}\!\times\!0.15$	V
Output leakage current	I _{OZ}	*5	-10.0	_	10.0	μΑ
Pull-up resistance	R _{UP}		46	100	270	kΩ

Notes: *1: CL, CE, RESETB, ADIPWO, HFL

*2: EFMIN

*3: PEAK, BOTTOM, ABCD, TE, FE, VC

*4: OUTL, OUTR

*5: During high-impedance output. Current also flows through pull-up resistance for MD3 to 0.

• XIN, XOUT, SLC0, and PD0 are not included in DC characteristics.

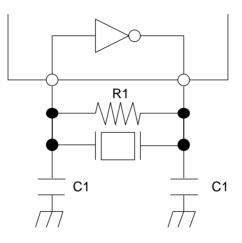
• The FR, ISET, SLCIST bias resistance pins are not included in DC characteristics.

Analog characteristics Input/output level: at Ta = -10 to +70 $^{\circ}C,$ V_{SS} = 0 V, V_{DD1} = 2.2 to 2.6 V

Parameter	Symbol	vmbol Conditions	Ratings			Unit
Faranieter	Symbol	min	typ	max		
Analog input voltage	VI	PEAK, BOTTOM, ABCD, TE, FE, VC	$AV_{DD1} imes 0.2$	_	$AV_{DD1} imes 0.8$	V
Input load capacitance		PEAK, BOTTOM, ABCD, TE, FE, VC	—	_	7.5	pF

Oscillation amplifier

Note: Xtal is limited to the basic mode.



Pin Functions

 $I/O \rightarrow I$: Input pin, O: Output pin, B: Bidirectional pin

Note: Do not leave V_{DD} and V_{SS} open, connect all to power supply, ground.

1 V _{DC} — Pewer supply pin 2 SHOCK 0 SHOCKENNG output pin 3 SLC0 0 HF signal aliae level adjustment amplifier 4 SLCBT 1 Bias resistance pin of alize level adjustment amplifier 5 EFMIN 1 HF signal sile level adjustment amplifier 6 RESETB 1 System reset 7 HFL 1 Track detection signal input pin 8 TEST2 1 Test input pin 9 PDO O VCEC ground pin 11 F.R 1 Bias resistance pin for conciliation frequency of VCEC 13 VCV ₀₀ — VCEC prover supply pin 14 Alvgait — Digita lever in any signal input pin 15 PEAK 1 PEAK signal input pin 16 BOTTOM 1 Main beam light instrantly signal input pin 17 ABCD 1 Main beam light instrantly signal input pin 18 TE 1 Tracking arero signal lep	Pin No.	Pin Name	I/O	Function
3 SLCD 0 HF signal slob level output pin 4 SLCIST 1 Bas resistance pin of slob evel adjustment amplifier 5 EFMIN 1 HF signal input pin 6 RESETB 1 System reset 7 HFL 1 Track detection signal input pin 8 TESTZ 1 Test input pin 9 PDO OCEC current charge pump output pin 10 VCVss — VCEC growing pin 11 FR 1 Bas resistance pin for cacillation frequency of VCEC 12 ISET 1 Bas resistance pin for cacillation frequency of VCEC 13 VCVsp — VCEC power supply pin 14 AVssit — Digital serva grows input pin 15 PEAK 1 PEAK signal input pin 16 TE 1 Tracking arrow signal input pin 17 ABCD 1 Main beam light intensity signal input pin 18 TE 1 Tracking arrows grow grow grow grow grow grow grow grow	1	V _{DD2}	_	Power supply pin
4 SLCST 1 Bias resistance pin of size level adjustment amplifier 5 EFMIN 1 HF signal input pin 6 RESETB System reset 7 HFL 1 Track detection signal input pin 8 TEST2 1 Total input pin 9 PDO O VCEC current charge pump output pin 10 VCVsg — VCEC current charge pump output pin 11 FR 1 Bias resistance pin for coalitation frequency of VCEC 12 VSET 1 Bias resistance pin for coalitation frequency of VCEC 13 VCVsp — VCEC power supply pin 14 AVsst — Digital servo ground pin 15 BOTTOM 1 BOTTOM signal input pin 16 REC 1 Main beam light interativ signal input pin 17 ABCD 1 Main beam light input pin 18 TE 1 Tracking dial acturpt pin 20 VC 1 Motopin paterin	2	SHOCK	0	SHOCK/RFNG output pin
S EFMIN I HF signal input pin 6 RESETB I System reset 7 HFL I Track detection signal input pin 8 TEST2 I Test input pin 9 PDO OCEC current charge pump output pin 10 VCVgs VCEC ground pin 11 FR I Bias resistance pin for casolitation frequency of VCEC 12 ISET I Bias resistance pin for casolitation frequency of VCEC 13 VCVgp Digital serve ground pin 14 AVsss Digital serve ground pin 15 PEAK I PEAK signal input pin 16 BOTTOM I BOTTOM signal input pin 17 AABCD I Midpoint potential input pin 18 TE I Tracking error signal input pin 20 VC I Midpoint potential input pin 21 AVgpoin Digital serve power suppiy pin 22	3	SLCO	0	HF signal slice level output pin
6 RESETS 1 System reset 7 HFL 1 Track detection signal input pin 8 TEST2 1 Test Imput pin 9 PDO O VCEC current charge pump output pin 10 VCVsg.	4	SLCIST	I	Bias resistance pin of slice level adjustment amplifier
7 HFL I Track detection signal input pin 8 TEST2 I Test input pin 9 PDO O VCEC current charge pump output pin 10 VCVsg — VCEC ground pin 11 FR I Bias resistance pin for ourrent charge pump of VCEC 12 ISET I Bias resistance pin for ourrent charge pump of VCEC 13 VCVpp — VCEC power supply pin 14 AVss1 — Digital serve ground pin 15 PEAK I PEAK signal input pin 16 BOTTOM III BOTTOM signal input pin 17 ABCD I Main beam light intensity signal input pin 18 TE I Tracking arror signal input pin 20 VC I Midpoint potential input pin 21 AVpon — Disk mode switch output 23 DSW0 B* Disk mode switch output pin 24 SSC B* ABCC orifset control signal output pin <	5	EFMIN	I	HF signal input pin
8 TEST2 1 Test input pin 9 POO O VCEC current charge pump output pin 10 VCVsg – VCEC ground pin 11 FR I Bias resistance pin for concillaton frequency of VCEC 12 ISET I Bias resistance pin for concillaton frequency of VCEC 13 VCVbg – VCEC power supply pin 14 AVsg1 – Digital serve ground pin 15 PEAK I PEAK Signal input pin 16 BOTTOM I BOTTOM fagnal input pin 17 ABCD I Mancheam light intensity signal input pin 19 FE I Focus error signal input pin 20 VC I Mincheam light intensity signal input pin 21 AVpo1 – Digital serve power supply pin 22 DSW1 B* Disk mode switch output 23 DBWO B* ABCO cortest signal output pin 24 SGC B* Troeking balaeo control signal output pin	6	RESETB	I	System reset
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10 VCV ₃₅ — VCEC ground pin 11 FR I Bias resistance pin for callation frequency of VCEC 12 IISET I Bias resistance pin for callation frequency of VCEC 13 VCV ₃₀ — VCEC power supply pin 14 AV ₃₅₁ — Digital serve ground pin 15 PEAK I PEAK signal input pin 16 BOTTOM BOTTOM signal input pin 17 AACD I Main beam fight intervis signal input pin 18 TE I Tracking error signal input pin 19 FE I Focus error signal input pin 20 VC I Midpoint potential input pin 21 AV ₀₀₁ — Digital servo power supply pin 22 DSW0 B* Disk mode switch output 23 DSW0 B* Disk mode switch output pin 24 SGC B* ACC cortrol signal output pin 25 AOFFSET B* Focus datarco cortrol signal output pin	8	TEST2		
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32 FBAL B* Focus balance control output pin 33 SPPWMF B* Spindle PWM output pin 34 SPPWMR B* Spindle PWM output pin 35 MD7 B DRAM data input/output pin 36 MD6 B DRAM data input/output pin 37 MD5 B DRAM data input/output pin 38 MD4 B DRAM data input/output pin 39 V _{DD2} Power supply pin 40 MD3 B DRAM data input/output pin 41 MD2 B DRAM data input/output pin 42 MD1 B DRAM data input/output pin 43 MD0 B DRAM data input/output pin 44 PCK O VCEC system clock signal output pin 45 V _{DD2} Power supply pin 46 V _{SS} - Ground pin 47 DEFECT B* Defect signal input/output pin 48 MD15 B				
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39VDD2—Power supply pin40MD3BDRAM data input/output pin41MD2BDRAM data input/output pin42MD1BDRAM data input/output pin43MD0BDRAM data input/output pin44PCKOVCEC system clock signal output pin45VDD2—Power supply pin46VSS—Ground pin47DEFECTB*Defect signal input/output pin48MD15BDRAM data input/output pin49MD14BDRAM data input/output pin50MD13BDRAM data input/output pin51MD12BDRAM data input/output pin52VSS—Ground pin	37	MD5	В	DRAM data input/output pin
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42 MD1 B DRAM data input/output pin 43 MD0 B DRAM data input/output pin 44 PCK O VCEC system clock signal output pin 45 V _{DD2} Power supply pin 46 V _{SS} Ground pin 47 DEFECT B* Defect signal input/output pin 48 MD15 B DRAM data input/output pin 49 MD14 B DRAM data input/output pin 50 MD13 B DRAM data input/output pin 51 MD12 B DRAM data input/output pin 52 V _{SS} Ground pin	40	MD3	В	DRAM data input/output pin
43MD0BDRAM data input/output pin44PCKOVCEC system clock signal output pin45V _{DD2} Power supply pin46V _{SS} Ground pin47DEFECTB*Defect signal input/output pin48MD15BDRAM data input/output pin49MD14BDRAM data input/output pin50MD13BDRAM data input/output pin51MD12BDRAM data input/output pin52V _{SS} Ground pin	41	MD2		DRAM data input/output pin
44 PCK O VCEC system clock signal output pin 45 V _{DD2} — Power supply pin 46 V _{SS} — Ground pin 47 DEFECT B* Defect signal input/output pin 48 MD15 B DRAM data input/output pin 49 MD14 B DRAM data input/output pin 50 MD13 B DRAM data input/output pin 51 MD12 B DRAM data input/output pin 52 V _{SS} — Ground pin	42	MD1	В	DRAM data input/output pin
45 V _{DD2} — Power supply pin 46 V _{SS} — Ground pin 47 DEFECT B* Defect signal input/output pin 48 MD15 B DRAM data input/output pin 49 MD14 B DRAM data input/output pin 50 MD13 B DRAM data input/output pin 51 MD12 B DRAM data input/output pin 52 V _{SS} — Ground pin	43	MD0	В	DRAM data input/output pin
46 V _{SS} Ground pin 47 DEFECT B* Defect signal input/output pin 48 MD15 B DRAM data input/output pin 49 MD14 B DRAM data input/output pin 50 MD13 B DRAM data input/output pin 51 MD12 B DRAM data input/output pin 52 V _{SS} Ground pin	44	PCK	0	VCEC system clock signal output pin
47 DEFECT B* Defect signal input/output pin 48 MD15 B DRAM data input/output pin 49 MD14 B DRAM data input/output pin 50 MD13 B DRAM data input/output pin 51 MD12 B DRAM data input/output pin 52 V _{SS} — Ground pin	45	V _{DD2}		Power supply pin
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49 MD14 B DRAM data input/output pin 50 MD13 B DRAM data input/output pin 51 MD12 B DRAM data input/output pin 52 V _{SS} — Ground pin	47	DEFECT	B*	Defect signal input/output pin
50 MD13 B DRAM data input/output pin 51 MD12 B DRAM data input/output pin 52 V _{SS} — Ground pin	48	MD15	В	DRAM data input/output pin
51 MD12 B DRAM data input/output pin 52 V _{SS} — Ground pin	49	MD14	В	DRAM data input/output pin
52 V _{SS} — Ground pin	50	MD13	В	DRAM data input/output pin
	51	MD12	В	DRAM data input/output pin
53 MD11 B DRAM data input/output ain	52	V _{SS}	—	Ground pin
	53	MD11	В	DRAM data input/output pin

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Pin No.	Pin Name	I/O	Function
54	MD10	В	DRAM data input/output pin
55	MD9	В	DRAM data input/output pin
56	MD8	В	DRAM data input/output pin
57	SLPWMF	B*	Sled PWM output pin
58	SLPWMR	B*	Sled PWM output pin
59	SLD0	B*	Sled control signal output pin
60	V _{SS}		Ground pin
61	V _{DD2}	_	Power supply pin
62	SLD1	В	Sled control signal input/output pin
63	V _{DD}		Internal power supply pin
64	SLD2	I	Sled control signal input pin
65	SLD3	I	Sled control signal input pin
66	FOPWMF	B*	Focus PWM output pin
67	FOPWMR	B*	Focus PWM output pin
68	TRPWMF	B*	Tracking PWM output pin
69	TRPWMR	B*	Tracking PWM output pin
70	FG		Speed pulse input pin
71	VP	B*	CLV servo lock judgment output pin
72	FOK	B*	Focus OK signal output pin
73	FAST	B*	FAST signal output pin
73	CL		CPU interface data transfer clock input pin
74	CE		CPU interface chip enable signal input pin
75	DI		
			CPU interface data input pin
77	DO	0	CPU interface data output pin
78	WRQB	0	CPU interface interrupt signal output pin
79	INTB	0	CPU interface interrupt signal output pin
80	FSEQ	B*	Frame synchronization detection signal output pin
81	F16M	B*	16.9344 MHz output pin
82	ENH	B*	De-emphasis specification output pin
83	LRCO	B*	LR clock output pin
84	DDATA	B*	Speech signal data output pin
85	BCO	B*	Bit clock output pin
86	DDOUT (DEFECT)	B*	Digital audio output pin
87	V _{DD2}	_	Power supply pin
88	XIN	I	16.9344 MHz oscillation input pin
89	XOUT	0	16.9344 MHz oscillation output pin
90	V _{SS}		Ground pin
91	V _{DD}	_	Internal power supply pin
92	AV _{SS}	—	1-bit DAC ground pin
93	OUTR	0	1-bit DAC right channel output pin
94	OUTL	0	1-bit DAC left channel output pin
95	AV _{DD}		1-bit DAC power supply pin
96	MCASB	B*	DRAM CAS signal output pin
97	MOEB	B*	DRAM OE signal output pin
98	MAD9	B*	DRAM address output pin
99	MAD8	B*	DRAM address output pin
100	MAD7	B*	DRAM address output pin
101	TEST1	I	Test input pin
102	MAD6	B*	DRAM address output pin
103	MAD5	B*	DRAM address output pin
104	MAD4	B*	DRAM address output pin
105	TEST3	I	Test input pin
106	V _{SS}	_	Ground pin
107	V _{DD2}	_	Power supply pin
108	SMON3	B*	Monitor signal output pin
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Pin No.	Pin Name	I/O	Function
110	MAD3	B*	DRAM address output pin
111	MAD2	B*	DRAM address output pin
112	MAD1	B*	DRAM address output pin
113	MAD0	B*	DRAM address output pin
114	SMON1	B*	Monitor signal output pin
115	SMON0	B*	Monitor signal output pin
116	MRASB	B*	DRAM RAS signal output pin
117	MWEB	B*	DRAM WE signal output pin
118	ADIPWO	I	Wobble signal input pin
119	V _{DD}	—	Internal power supply pin
120	V _{SS}	_	Ground pin

Note: * Output/input only during testing. Normally output.

TEST1 to TEST3: Always use fixed to High.

MD3 to MD0: Pull-up I/O with resistor

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