1.6-Gbps to 2.5-Gbps Class V Transceiver

FEATURES

- 1.6- to 2.5-Gbps (Gigabits Per Second) Serializer/Deserializer
- Hot-Plug Protection
- High-Performance 68-Pin Ceramic Quad Flat Pack Package (HFG)
- Low-Power Operation
- Programmable Preemphasis Levels on Serial Output
- Interfaces to Backplane, Copper Cables, or Optical Converters
- On-Chip 8-Bit/10-Bit Encoding/Decoding, Comma Detect
- On-Chip PLL Provides Clock Synthesis From Low-Speed Reference
- Low Power: <500 mW
- 3-V Tolerance on Parallel Data Input Signals
- 16-Bit Parallel TTL-Compatible Data Interface
- Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link
- Military Temperature Range (–55°C to 125°C T_{case})
- Loss of Signal (LOS) Detection
- Integrated 50-Ω Termination Resistors on RX

DESCRIPTION

The TLK2711 is a member of the WizardLink transceiver family of multigigabit transceivers, intended for use in ultra-high-speed bidirectional point-to-point data transmission systems. The TLK2711 supports an effective serial interface speed of 1.6 Gbps to 2.5 Gbps, providing up to 2 Gbps of data bandwidth.

The primary application of the TLK2711 is to provide high-speed I/O data channels for point-to-point baseband data transmission over controlled impedance media of approximately 50 Ω. The transmission media can be printed circuit board, copper cables, or fiber-optic cable. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector terminals, and transmit/receive terminals. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel, which can be a coaxial copper cable, a controlled impedance backplane, or an optical link. It is then reconstructed into its original parallel format. It offers significant power and cost savings over parallel solutions, as well as scalability for higher data rates in the future.

The TLK2711 performs parallel-to-serial and serial-to-parallel data conversion. The clock extraction functions as a physical layer (PHY) interface device. The serial transceiver interface operates at a maximum speed of 2.5 Gbps. The transmitter latches 16-bit parallel data at a rate based on the supplied reference clock (TXCLK). The 16-bit parallel data is internally encoded into 20 bits using an 8-bit/10-bit (8b/10b) encoding format. The resulting 20-bit word is then transmitted differentially at 20 times the reference clock (TXCLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the recovered clock (RXCLK). It then decodes the 20-bit wide data using the 8-bit/10-bit decoding format resulting in 16 bits of parallel data at the receive data terminals (RXD0–RXD15). The outcome is an effective data payload of 1.28 Gbps to 2 Gbps (16 bits data × the frequency).

The TLK2711 is available in a 68-pin ceramic nonconductive tie-bar package (HFG).

NOTE:

The errata noted in the commercial TLK2711 device titled "Errata to the TLK2711, 1.6-to-2.7 GBPS Transceiver Data Sheet– PLL False Lock Problem" does not apply to the TLK2711-SP device. The TLK2711-SP is functionally equivalent to the TLK2711A commercial device.

The TLK2711 provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer, providing the protocol device with a functional self-check of the physical interface.

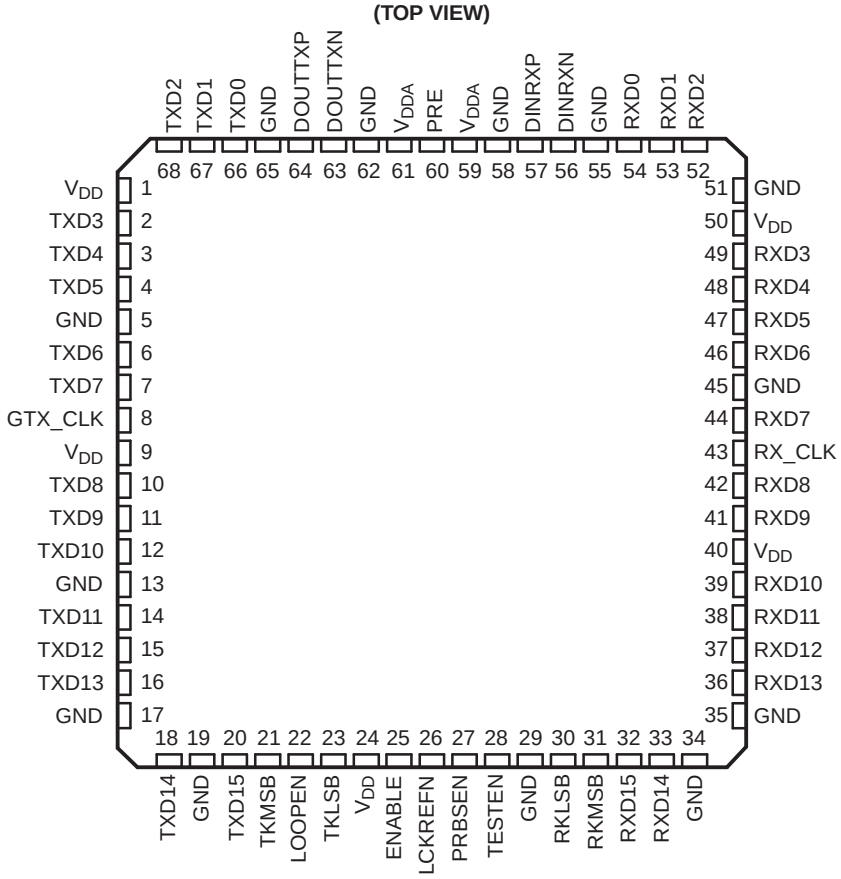
The TLK2711 has a loss of signal (LOS) detection circuit for conditions where the incoming signal no longer has a sufficient voltage amplitude to keep the clock recovery circuit in lock.

The TLK2711 allows users to implement redundant ports by connecting receive data bus terminals from two TLK2711 devices together. Asserting the LCKREFN to a low state causes the receive data bus terminals (RXD0–RXD15, RXCLK, RKLSB, and RKMSB) to go to a high-impedance state. This places the device in a transmit-only mode, since the receiver is not tracking the data.

The TLK2711 I/Os are 3-V compatible. The TLK2711 is characterized for operation from –55°C to 125°C T_{case}.

The TLK2711 is designed to be hot-plug capable. An on-chip power-on reset circuit holds the RXCLK low, and goes to high impedance on the parallel-side output signal terminals, as well as TXP and TXN during power up.

HFG PACKAGE
(TOP VIEW)



ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	TLK2711 - HFG	5962-0522101VXC	5962-0522101VXC TLK2711HFG

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

BLOCK DIAGRAM

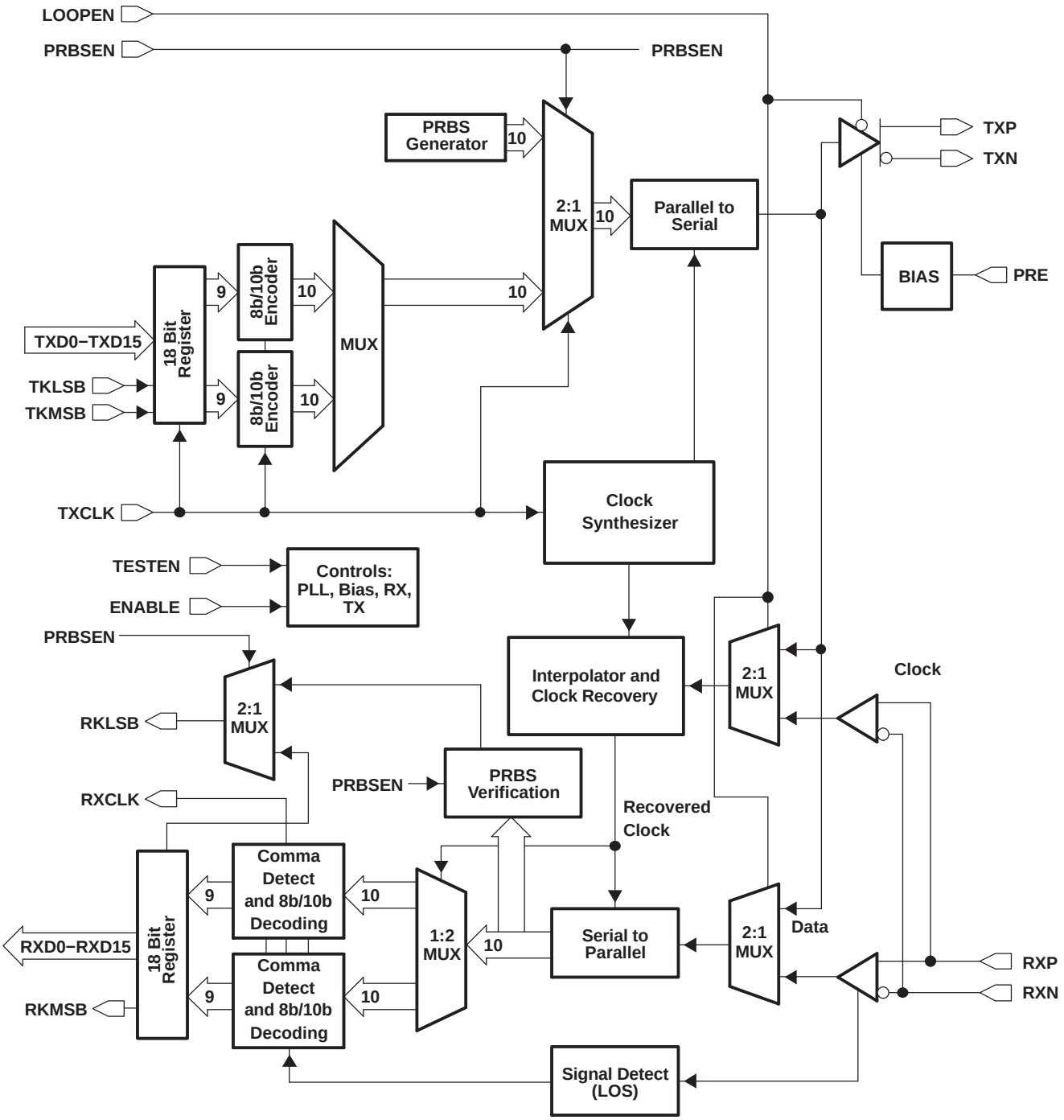


Figure 1. TLK2711 Block Diagram

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
DOUTTXN DOUTTXP	63 64	O	Serial transmit outputs. TXP and TXN are differential serial outputs that interface to copper or an optical I/F module. These terminals transmit NRZ data at a rate of 20 times the TXCLK value. TXP and TXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low. During power-on reset, these terminals are high impedance.
ENABLE	25	I(1)	Device enable. When this terminal is held low, the device is placed in power-down mode. Only the signal detect circuit on the serial receive pair is active. When asserted high while the device is in power-down mode, the transceiver goes into power-on reset before beginning normal operation.
GND	5, 13, 17, 19, 29, 34, 35, 45, 51, 55, 58, 62, 65		Analog and digital logic ground. Provides a ground for the logic circuits, digital I/O buffers, and the high-speed analog circuits.
LCKREFN	26	I(1)	Lock to reference. When LCKREFN is low, the receiver clock is frequency locked to TXCLK. This places the device in a transmit-only mode since the receiver is not tracking the data. When LCKREFN is asserted low, the receive data bus terminals (RXD0–RXD15, RXCLK, RKLSB, and RKMSB) are in a high-impedance state. When LCKREFN is deasserted high, the receiver is locked to the received data stream.
LOOPEN	22	I(2)	Loop enable. When LOOPEN is active high, the internal loopback path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The TXP and TXN outputs are held in a high-impedance state during the loopback test. LOOPEN is held low during standard operational state, with external serial outputs and inputs active.
PRE	60	I(2)	Preemphasis control. Selects the amount of preemphasis to be added to the high-speed serial output drivers. Left low or unconnected, 5% preemphasis is added. Pulled high, 20% preemphasis is added.
PRBSEN	27	I(2)	PRBS test enable. When asserted high, results of pseudo-random bit stream (PRBS) tests can be monitored on the RKLSB terminal. A high on RKLSB indicates that valid PRBS is being received.
RKLSB	30	O	K-code indicator/PRBS test results. When RKLSB is asserted high, an 8-bit/10-bit K code was received and is indicated by data bits RXD0–RXD7. When RKLSB is asserted low, an 8-bit/10-bit D code is received and is presented on data bits RXD0–RXD7. When PRBSEN is asserted high, this pin is used to indicate status of the PRBS test results (high = pass).
RKMSB	31	O	K-code indicator. When RKMSB is asserted high an 8-bit/10-bit K code was received and is indicated by data bits RXD8–RXD15. When RKMSB is asserted low an 8-bit/10-bit D code was received and is presented on data bits RXD8–RXD15. If the differential signal on RXN and RXP drops below 200 mV, RXD0–RXD15, RKLSB, and RKMSB are all asserted high.
RXCLK RX_CLK	43	O	Recovered clock. Output clock that is synchronized to RXD0–RXD9, RKLSB, and RKMSB. RXCLK is the recovered serial data rate clock divided by 20. RXCLK is held low during power-on reset.
RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7 RXD8 RXD9 RXD10 RXD11 RXD12 RXD13 RXD14 RXD15	54 53 52 49 48 47 46 44 42 41 39 38 37 36 33 32	O	Receive data bus. These outputs carry 16-bit parallel data output from the transceiver to the protocol device, synchronized to RXCLK. The data is valid on the rising edge of RXCLK as shown in Figure 5. These terminals are in high-impedance state during power-on reset.
DINRXN DINRXP	56 57	I	Serial receive inputs. RXP and RXN together are the differential serial input interface from a copper or an optical I/F module.
TESTEN	28	I(2)	Test mode enable. This terminal should be left unconnected or tied low.

(1) Internal 10-kΩ pullup
(2) Internal 10-kΩ pulldown

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
TKLSB	23	I(3)	K-code generator (LSB). When TKLSB is high, an 8-bit/10-bit K code is transmitted as controlled by data bits TXD0–TXD7. When TKLSB is low, an 8-bit/10-bit D code is transmitted as controlled by data bits TXD0–TXD7.
TKMSB	21	I(3)	K-code generator (MSB). When TKMSB is high, an 8-bit/10-bit K code is transmitted as controlled by data bits TXD8–TXD15. When TKMSB is low, an 8-bit/10-bit D code is transmitted as controlled by data bits TXD8–TXD15.
TXCLK GTX_CLK	8	I	Reference clock. TXCLK is a continuous external input clock that synchronizes the transmitter interface signals TKMSB, TKLSB, and TXD0–TXD15. The frequency range of TXCLK is 80 MHz to 135 MHz. The transmitter uses the rising edge of this clock to register the 16-bit input data TXD0–TXD15 for serialization.
TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7 TXD8 TXD9 TXD10 TXD11 TXD12 TXD13 TXD14 TXD15	66 67 68 2 3 4 6 7 10 11 12 14 15 16 18 20	I	Transmit data bus. These inputs carry the 16-bit parallel data output from a protocol device to the transceiver for encoding, serialization, and transmission. This 16-bit parallel data is clocked into the transceiver on the rising edge of TXCLK as shown in Figure 2.
VDD	1, 9, 24, 40, 50		Digital logic power. Provides power for all digital circuitry and digital I/O buffers.
VDDA	59, 61		Analog power. VDDA provides a supply reference for the high-speed analog circuits, receiver, and transmitter.

(3) Internal 10-kΩ pullup

DETAILED DESCRIPTION

Transmit Interface

The transmitter interface registers valid incoming 16-bit-wide data (TXD0–TXD15) on the rising edge of the TXCLK. The data is then 8-bit/10-bit encoded, serialized, and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (TXCLK) by a factor of 10 times, creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register, which transmits data on both the rising and falling edges of the bit clock, providing a serial data rate that is 20 times the reference clock. Data is transmitted least significant bit (LSB) (TXD0) first.

Transmit Data Bus

The transmit data bus interface accepts 16-bit single-ended TTL parallel data at the TXD0–TXD15 terminals. Data and K-code control is valid on the rising edge of the TXCLK. The TXCLK is used as the word clock. The data, K-code, and clock signals must be properly aligned as shown in Figure 2. Detailed timing information can be found in the electrical characteristics table.

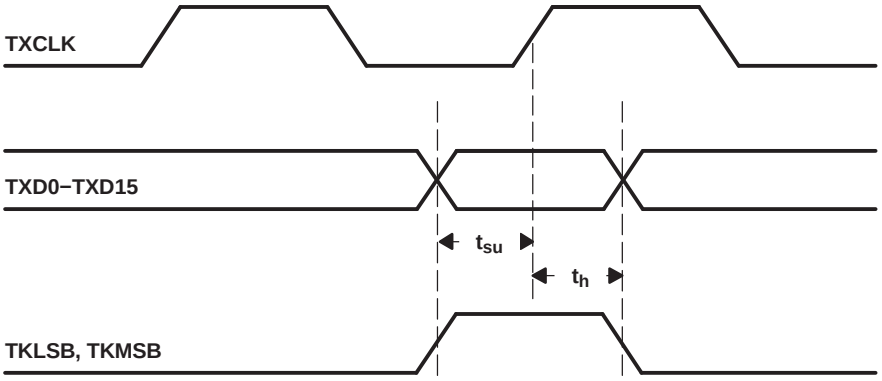


Figure 2. Transmit Timing Waveform

Data Transmission Latency

The data transmission latency of the TLK2711 is defined as the delay from the initial 16-bit word load to the serial transmission of bit 0. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum transmit latency $t_{d(Tx\ latency)}$ is 34 bit times; the maximum is 38 bit times. Figure 3 shows the timing relationship between the transmit data bus, the TXCLK, and the serial transmit terminals.

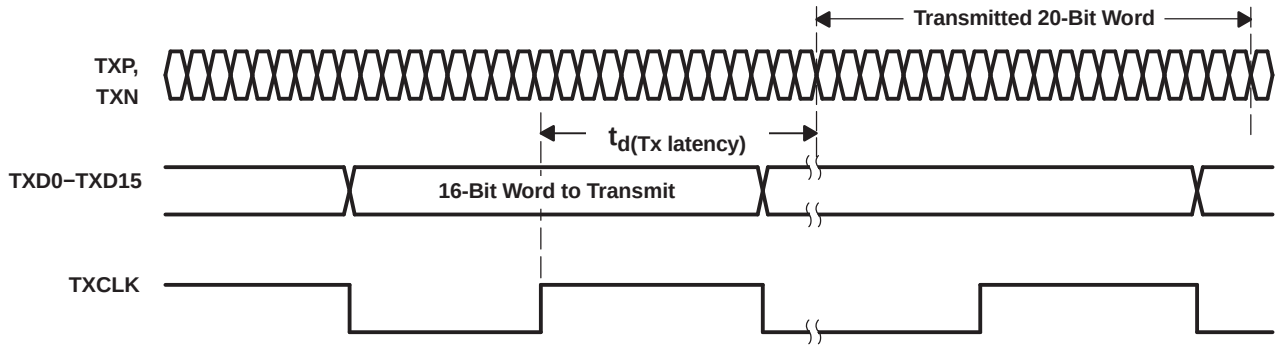


Figure 3. Transmitter Latency

8-Bit/10-Bit Encoder

All true serial interfaces require a method of encoding to ensure minimum transition density, so that the receiving phase-locked loop (PLL) has a minimal number of transitions to stay locked on. The encoding scheme maintains the signal dc balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking. The TLK2711 uses the 8-bit/10-bit encoding algorithm that is used by fibre channel and gigabit ethernet. This is transparent to the user, as the TLK2711 internally encodes and decodes the data such that the user reads and writes actual 16-bit data.

The 8-bit/10-bit encoder converts 8-bit-wide data to a 10-bit-wide encoded data character to improve its transmission characteristics. Since the TLK2711 is a 16-bit-wide interface, the data is split into two 8-bit-wide bytes for encoding. Each byte is fed into a separate encoder. The encoding is dependent upon two additional input signals, TKMSB and TKLSB.

Table 1. Transmit Data Controls

TKLSB	TKMSB	16 BIT PARALLEL INPUT	
0	0	Valid data on TXD0–TXD7,	Valid data TXD8–TXD15
0	1	Valid data on TXD0–TXD7,	K code on TXD8–TXD15
1	0	K code on TXD0–TXD7,	Valid data on TXD8–TXD15
1	1	K code on TXD0–TXD7,	K code on TXD8–TXD15

Pseudo-Random Bit Stream (PRBS) Generator

The TLK2711 has a built-in 2^7–1 PRBS function. When the PRBSEN terminal is forced high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data from the normal input source is ignored during the PRBS mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a bit error rate tester (BERT), the receiver of another TLK2711, or looped back to the receive input. Since the PRBS is not really random but a predetermined sequence of ones and zeroes, the data can be captured and checked for errors by a BERT.

Parallel to Serial

The parallel-to-serial shift register takes in the 20-bit-wide data word multiplexed from the two parallel 8-bit/10-bit encoders and converts it to a serial stream. The shift register is clocked on both the rising and falling edge of the internally generated bit clock, which is 10 times the TXCLK input frequency. The LSB (TXD0) is transmitted first.

High-Speed Data Output

The high-speed data output driver consists of a voltage mode logic (VML) differential pair optimized for a 50-Ω impedance environment. The magnitude of the differential pair signal swing is compatible with pseudo emitter coupled logic (PECL) levels when ac coupled. The line can be directly coupled or ac coupled. See Figure 13 and Figure 14 for termination details. The outputs also provide preemphasis to compensate for ac loss when driving a cable or PCB backplane trace over a long distance (see Figure 4). The level of preemphasis is controlled by PRE (see Table 2).

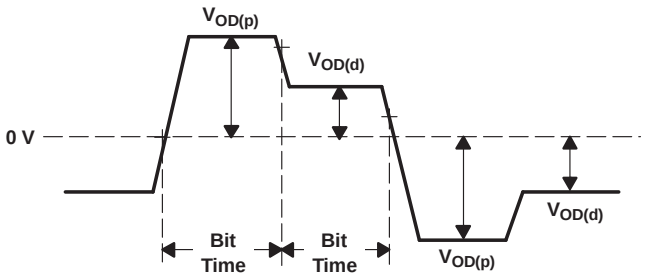


Figure 4. Output Voltage Under Preemphasis (VTXP–VTXN)

Table 2. Programmable Preemphasis

PRE	PREEMPHASIS LEVEL (%) $V_{OD(P)}$, $V_{OD(D)}$ (1)
0	5%
1	20%

(1) $V_{OD(p)}$: Voltage swing when there is a transition in the data stream.
$V_{OD(d)}$: Voltage swing when there is no transition in the data stream.

Receive Interface

The receiver interface of the TLK2711 accepts 8-bit/10-bit encoded differential serial data. The interpolator and clock recovery circuit locks to the data stream and extracts the bit-rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to two separate 10-bit word boundaries, 8-bit/10-bit decoded, and output on a 16-bit-wide parallel bus synchronized to the extracted receive clock. The data is received LSB (RXD0) first.

Receive Data Bus

The receive bus interface drives 16-bit-wide single-ended TTL parallel data at the RXD0–RXD15 terminals. Data is valid on the rising edge of the RXCLK. The RXCLK is used as the recovered word clock. The data, RKLSB, RKMSB, and clock signals are aligned as shown in Figure 5. Detailed timing information can be found in the switching characteristics table.

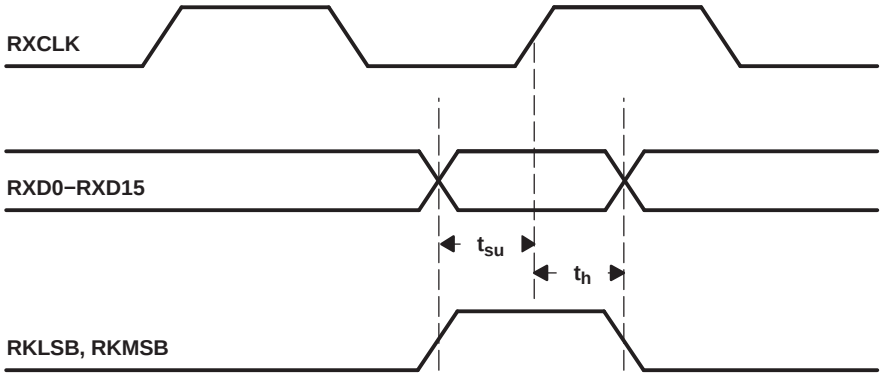


Figure 5. Receive Timing Waveform

Data Reception Latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum receive latency $t_{d(Rx\ latency)}$ is 76 bit times; the maximum is 107 bit times. Figure 6 shows the timing relationship between the serial receive terminals, the recovered word clock (RXCLK), and the receive data bus.

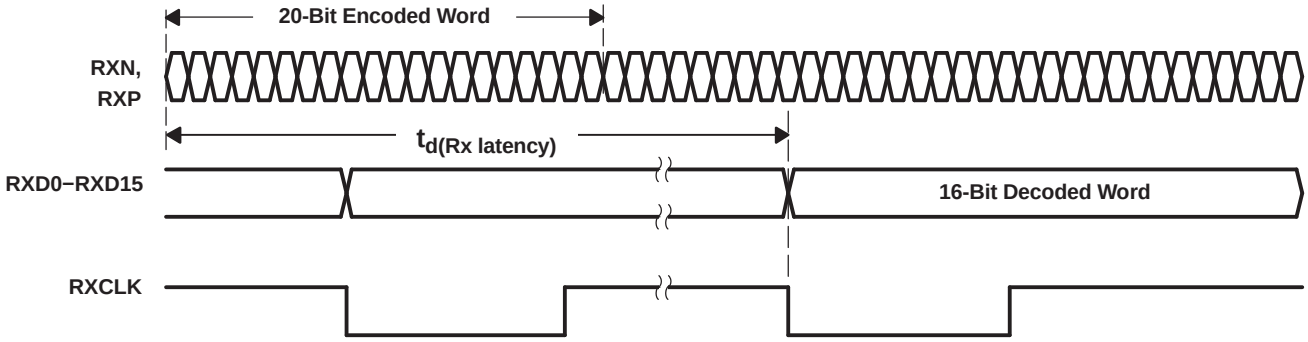


Figure 6. Receiver Latency

Serial to Parallel

Serial data is received on the RXP and RXN terminals. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within 200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. The 10-bit-wide parallel data is then multiplexed and fed into two separate 8-bit/10-bit decoders, where the data is then synchronized to the incoming data stream word boundary by detection of the comma 8-bit/10-bit synchronization pattern.

Comma Detect and 8-Bit/10-Bit Decoding

The TLK2711 has two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10-bit encoded data (half of the 20-bit received word) back into eight bits. The comma-detect circuit is designed to provide for byte synchronization to an 8-bit/10-bit transmission code. When parallel data is clocked into a parallel-to-serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to recognize the byte boundary. Typically, this is accomplished through the use of a synchronization pattern. This is typically a unique pattern of ones and zeros that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. The 8-bit/10-bit encoding contains a character called the comma (b0011111 or b1100000), which is used by the comma-detect circuit on the TLK2711 to align the received serial data back to its original byte boundary. The decoder detects the comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding; the comma is mapped into the LSB. The decoder then converts the data back into 8-bit data. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (RXCLK) and output valid on the rising edge of the RXCLK.

NOTE:

The TLK2711 only achieves byte alignment on the 0011111 comma.

Decoding provides two additional status signals, RKLSB and RKMSB. When RKLSB is asserted, an 8-bit/10-bit K code is received and the specific K code is presented on the data bits RXD0–RXD7; otherwise, an 8-bit/10-bit D code is received. When RKMSB is asserted, an 8-bit/10-bit K code is received and the specific K-code is presented on data bits RXD8–RXD15; otherwise, an 8-bit/10-bit D code is received (see Table 3). The valid K codes the TLK2711; decodes are provided in Table 4. An error detected on either byte, including K codes not in Table 4, causes that byte only to indicate a K0.0 code on the RKxSB and associated data pins, where K0.0 is known to be an invalid 8-bit/10-bit code. A loss of input signal causes a K31.7 code to be presented on both bytes, where K31.7 is also known to be an invalid 8-bit/10-bit code.

Table 3. Receive Status Signals

RKLSB	RKMSB	DECODED 20-BIT OUTPUT	
0	0	Valid data on RXD0–RXD7,	Valid data RXD8–RXD15
0	1	Valid data on RXD0–RXD7,	K code on RXD8–RXD15
1	0	K code on RXD0–RXD7,	Valid data on RXD8–RXD15
1	1	K code on RXD0–RXD7,	K code on RXD8–RXD15

Table 4. Valid K Characters

K CHARACTER	RECEIVE DATA BUS RXD0–RXD7 OR RXD8–RXD15
K28.0	000 11100
K28.1(1)	001 11100
K28.2	010 11100
K28.3	011 11100
K28.4	100 11100
K28.5(1)	101 11100
K28.6	110 11100
K28.7(1)	111 11100
K23.7	111 10111
K27.7	111 11011
K29.7	111 11101
K30.7	111 11110

(1) Should only be present on RXD0–RXD7 when in running disparity <0

Power-Down Mode

The TLK2711 goes into power-down mode when the ENABLE pin is pulled low. In the power-down mode, the serial transmit pins (TXN), the receive data bus pins (RXD0–RXD15), and RKLSB goes into a high-impedance state. In the power-down condition, the signal detection circuit draws less than 15 mW. When the TLK2711 is in the power-down mode, the clock signal on the TXCLK terminal must be provided if LOS functionality is needed.

Loss of Signal (LOS) Detection

The TLK2711 has a LOS detection circuit for conditions where the incoming signal no longer has a sufficient voltage level to keep the clock recovery circuit in lock. The signal detection circuit is intended to be an indication of gross signal error conditions, such as a detached cable or no signal being transmitted, and not an indication of signal coding health. The TLK2711 reports this condition by asserting RKLSB, RKMSB, and RXD0–RXD15 terminals to a high state. As long as the differential signal is above 200 mV in differential magnitude, the LOS circuit does not signal an error condition.

PRBS Verification

The TLK2711 also has a built-in BERT function in the receiver side that is enabled by the PRBSEN. It can check for errors and report the errors by forcing the RKLSB terminal low.

Reference Clock Input

The reference clock (TXCLK) is an external input clock that synchronizes the transmitter interface. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. The internal serialization bit clock is frequency locked to the reference clock and used to clock out the serial transmit data on both its rising and falling edges, providing a serial data rate that is 20 times the reference clock.

Operating Frequency Range

The TLK2711 operates at a serial data rate from 1.6 Gbps to 2.5 Gbps. To achieve these serial rates, TXCLK must be within 80 MHz to 125 MHz. The TXCLK must be within ±100 PPM of the desired parallel data rate clock.

Testability

The TLK2711 has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable terminal allows for all circuitry to be disabled so that a quiescent current test can be performed. The PRBS function allows for built-in self-test (BIST).

Loopback Testing

The transceiver can provide a self-test function by enabling (LOOPEN) the internal loopback path. Enabling this terminal causes serial-transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. The external differential output is held in a high-impedance state during the loopback testing.

Built-In Self-Test (BIST)

The TLK2711 has a BIST function. By combining PRBS with loopback, an effective self-test of all the circuitry running at full speed can be realized. The successful completion of the BIST is reported on the RKLSB terminal.

Power-On Reset

Upon application of minimum valid power, the TLK2711 generates a power-on reset. During the power-on reset the RXD0–RXD15, RKLSB, and RKMSB signal terminals go to a high-impedance state. The RXCLK is held low. The length of the power-on reset cycle is dependent upon the TXCLK frequency, but is less than 1 ms.

ABSOLUTE MAXIMUM RATINGS

over operating temperature range (unless otherwise noted)(1)

			UNIT
V_{DD}	Supply voltage range(2)		–0.3 V to 3 V
	Voltage range	TXD0–TXD15, ENABLE, TXCLK, TKMSB, TKLSB, LOOPEN, PRBSEN, LCKREFN, PRE	–0.3 V to 4 V
		All other terminals	–0.3 V to V_{DD} , V_{DDA} + 0.3 V
P_D	Package power dissipation		See Dissipation Rating Table
T_{stg}	Storage temperature range		–65°C to 150°C
	Electrostatic discharge	HBM	2 kV
T_c	Characterized case operating temperature range	HFG	–55°C to 125°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are stated with respect to network ground.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	Frequency range 1.6 Gbps to 2 Gbps	2.375	2.5	2.625	V
		Frequency range 1.6 Gbps to 2.5 Gbps	2.5	2.6	2.7	
I_{CC}	Supply current	Frequency = 1.6 Gbps, PRBS pattern		110		mA
		Frequency = 2.5 Gbps, PRBS pattern		160		
P_D	Power dissipation	Frequency = 1.6 Gbps, PRBS pattern		275		mW
		Frequency = 2.5 Gbps, PRBS pattern		400		
		Frequency = 2.5 Gbps, PRBS pattern			550	
	Shutdown current	Enable = 0, V_{DDA}, V_{DD} terminals, V_{DD} = MAX		3		mA
	PLL startup lock time	V_{DD}, V_{DDC} = 2.375 V		0.1	0.4	ms
	Data acquisition time			1024		Bits
T_c	Operating case temperature		–55		125	°C

REFERENCE CLOCK (TXCLK) TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	Receiver data rate/20	–100		100	ppm
Frequency tolerance		–100		100	ppm
Duty cycle		40%	50%	60%	
Jitter	Peak to peak			40	ps

TTL INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted),
TTL signals: TXD0–TXD15, TXCLK, LOOPEN, LCKREFN, ENABLE, PRBS_EN, TKLSB, TKMSB, PRE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	See Figure 7	1.7			V
V_{IL}	Low-level input voltage	See Figure 7			0.8	V
I_{IH}	Input high current	V_{DD} = MAX, V_{IN} = 2 V			40	µA
I_{IL}	Input low current	V_{DD} = MAX, V_{IN} = 0.4 V	–40			µA
C_I	Receiver input capacitance			6		pF
t_r	Rise time, TXCLK, TKMSB, TKLSB, TXD0–TXD15	0.7 V to 1.9 V, C = 5 pF, See Figure 7		1		ns
t_f	Fall time, TXCLK, TKMSB, TKLSB, TXD0–TXD15	1.9 V to 0.7 V, C = 5 pF, See Figure 7		1		ns
t_{su}	TXD0–TXD15, TKMSB, TKLSB setup to ↑ TXCLK	See Figure 7 (1)	1.5			ns
t_h	TXD, TKMSB, TKLSB hold to ↑ TXCLKS	See Figure 7 (1)	0.4			ns

(1) Nonproduction tested parameters

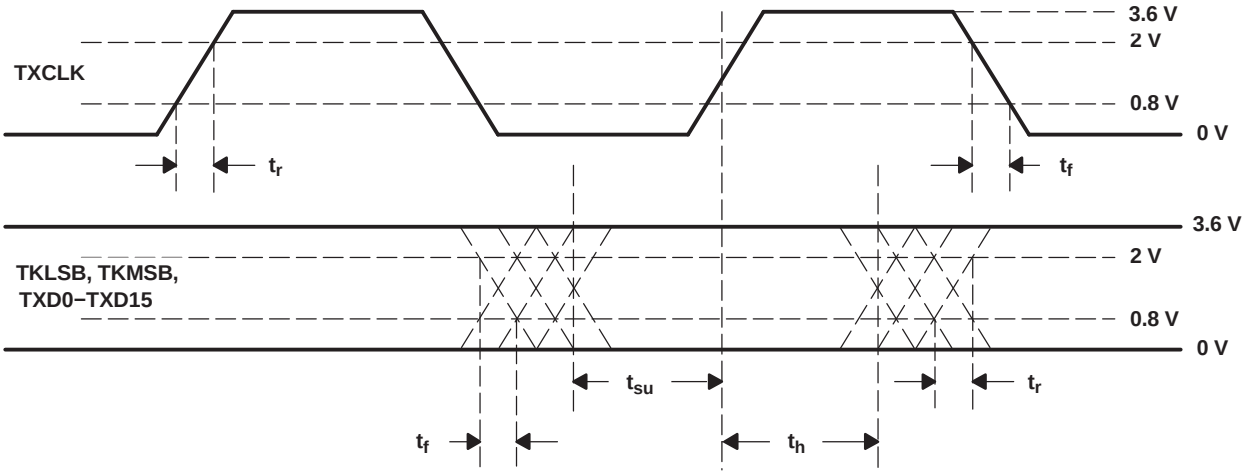


Figure 7. TTL Data Input Valid Levels for AC Measurements

TTL OUTPUT SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA, V_{DD} = MIN	2.1	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA, V_{DD} = MIN		0.25	0.5	V
$t_{r(slew)}$	Slew rate (rising), magnitude of RXCLK, RKLSB, RKMSB, RXD0–RXD15	0.8 V to 2 V, C = 5 pF, See Figure 8	0.5			V/ns
$t_{f(slew)}$	Slew rate (falling), magnitude of RXCLK, RKLSB, RKMSB, RXD0–RXD15	0.8 V to 2 V, C = 5 pF, See Figure 8	0.5			V/ns
t_{su}	RXD0–RXD15, RKMSB, RKLSB setup to ↑ RXCLK	50% voltage swing, TXCLK = 80 MHz, See Figure 8 (1)	3			ns
		50% voltage swing, TXCLK = 125 MHz, See Figure 8 (1)	2.5			
t_h	RXD0–RXD15, RKMSB, RKLSB hold to ↑ RXCLK	50% voltage swing, TXCLK = 80 MHz, See Figure 8 (1)	3			ns
		50% voltage swing, TXCLK = 125 MHz, See Figure 8 (1)	2			

(1) Nonproduction tested parameters

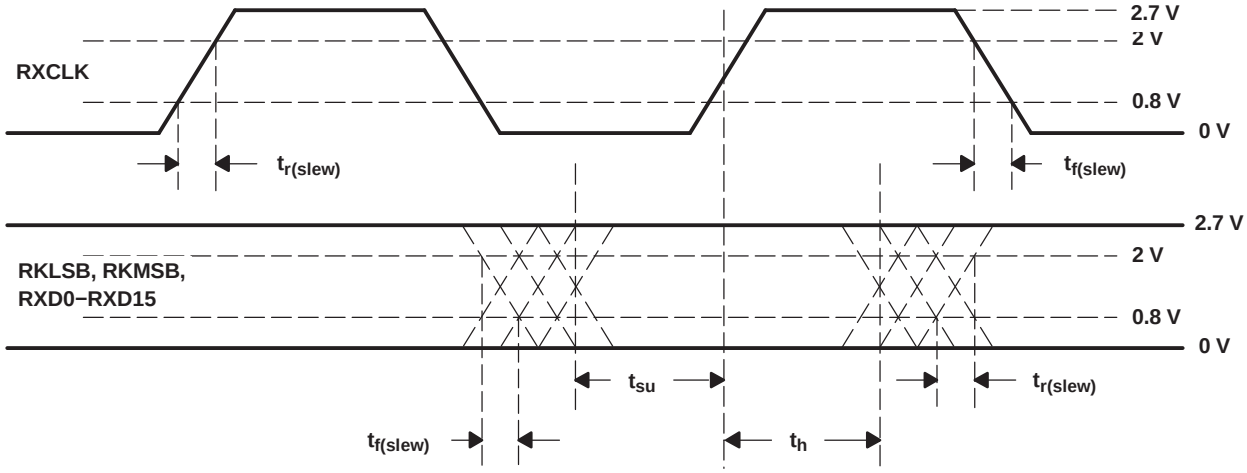


Figure 8. TTL Data Output Valid Levels for AC Measurements

TRANSMITTER/RECEIVER CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(p)}$	Preemphasis VOD, direct, $V_{OD(p)}$ = |VTXP – VTXN|	Rt = 50 Ω, PREM = high, dc-coupled, See Figure 9	655	800	1100	mV
		Rt = 50 Ω, PREM = low, dc coupled, See Figure 9	590	740	1050	
$V_{OD(pp\_p)}$	Differential, peak-to-peak output voltage with preemphasis	Rt = 50 Ω, PREM = high, dc coupled, See Figure 9	1310	1600	2200	mV_{p-p}
		Rt = 50 Ω, PREM = low, dc coupled, See Figure 9	1180	1480	2100	
$V_{OD(d)}$	Deemphais output voltage, |VTXP – VTXN|	Rt = 50 Ω, dc coupled, See Figure 9	540	650	950	mV
$V_{OD(pp\_d)}$	Differential, peak-to-peak output voltage with deemphasis	Rt = 50 Ω, dc coupled, See Figure 9	1080	1300	1900	mV_{p-p}
$V_{(cmt)}$	Transmit common mode voltage range, (VTXP + VTXN)/2	Rt = 50 Ω, See Figure 9	1000	1250	1450	mV
V_{ID}	Receiver input voltage differential, |VRXP – VRXN|	(1)	220		1600	mV
$V_{(cmr)}$	Receiver common mode voltage range, (VRXP + VRXN)/2	(1)	1000	1250	2250	mV
I_{lkg}	Receiver input leakage current		–10		10	µA
C_I	Receiver input capacitance			4		pF
	Serial data total jitter (peak to peak)	Differential output jitter at 2.5 Gbps, Random + deterministic, PRBS pattern		0.28		UI(2)
		Differential output jitter at 1.6 Gbps, Random + deterministic, PRBS pattern		0.32		
t_t, t_f	Differential output signal rise, fall time (20% to 80%)	RL = 50 Ω, CL = 5 pF, See Figure 9		150		ps
	Jitter tolerance eye closure	Differential input jitter, random + deterministic, PRBS pattern at zero crossing(1)	0.4			UI
$t_{d(Tx\ latency)}$	Tx latency	See Figure 3	34		38	Bits
$t_{d(Rx\ latency)}$	Rx latency	See Figure 6	76		107	Bits

(1) Nonproduction tested parameters
(2) UI is the time interval of one serialized bit.

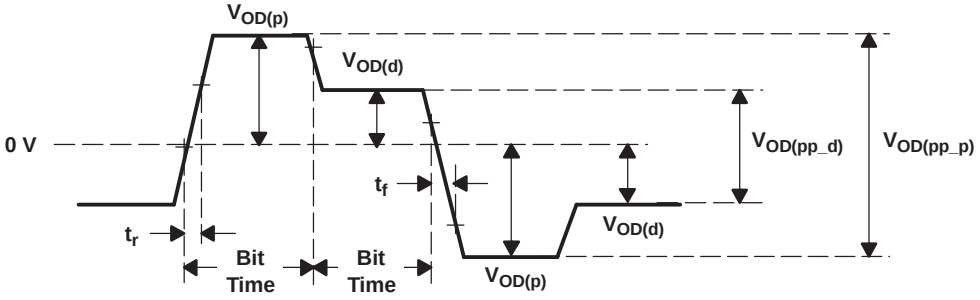


Figure 9. Differential and Common-Mode Output Voltage

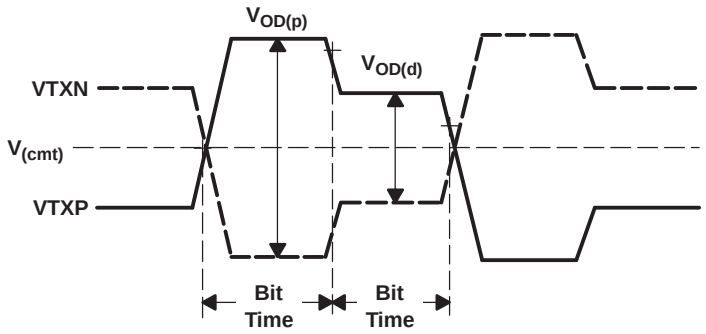


Figure 10. Common-Mode Output Voltage Definitions

THERMAL INFORMATION

Thermal Characteristics

PARAMETER		TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, per JESD 51-5 methodology	31.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	MIL-STD-883 Test Method 1012	2.96	°C/W

Thermal notes: This CQFP package has built in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. In order to efficiently remove heat and provide a low-impedance ground path, a thermal land is required on the surface of the PCB directly underneath the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, the PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. TI typically recommends an 11,9-mm x 11.9-mm board-mount thermal pad with a 4,2-mm x 4,2-mm solder mask defined pad attach opening. This allows maximum area for thermal dissipation, while allowing leads pad to solder pad clearance. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically ground potential.

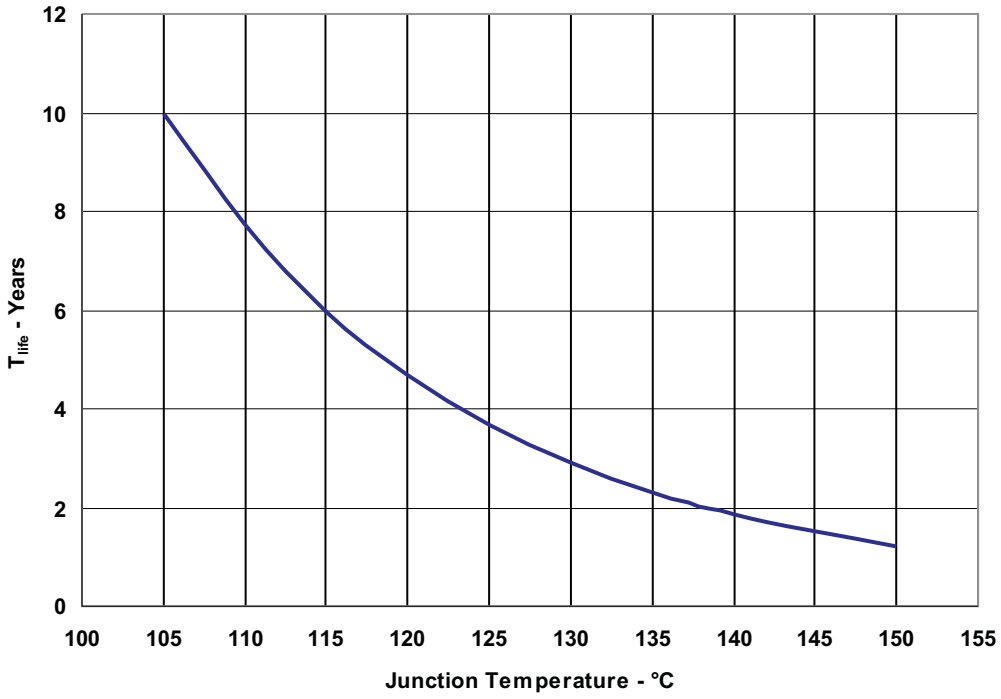
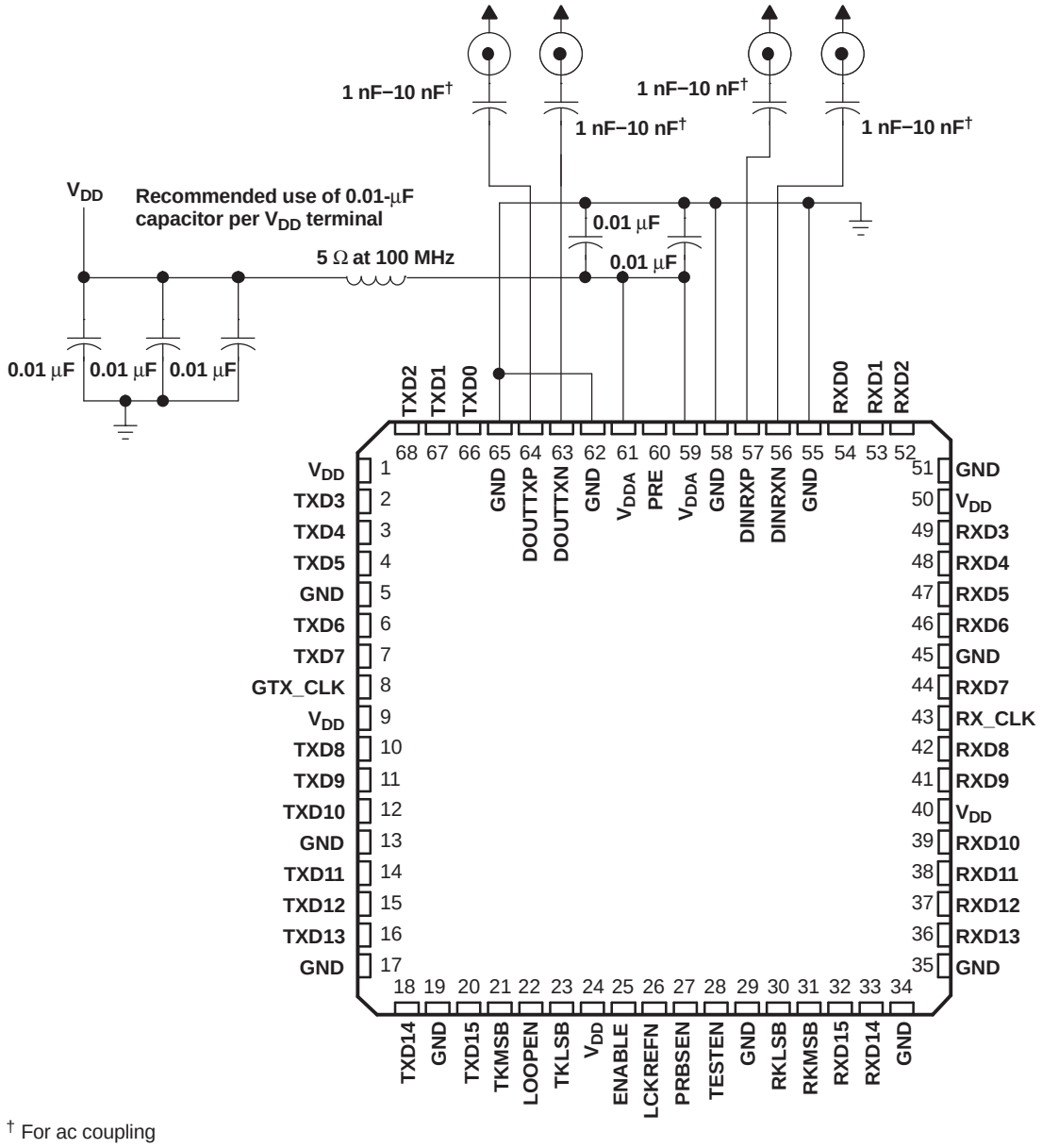


Figure 11. T_{life} vs Junction Temperature

APPLICATION INFORMATION



† For ac coupling

Figure 12. External Component Interconnection

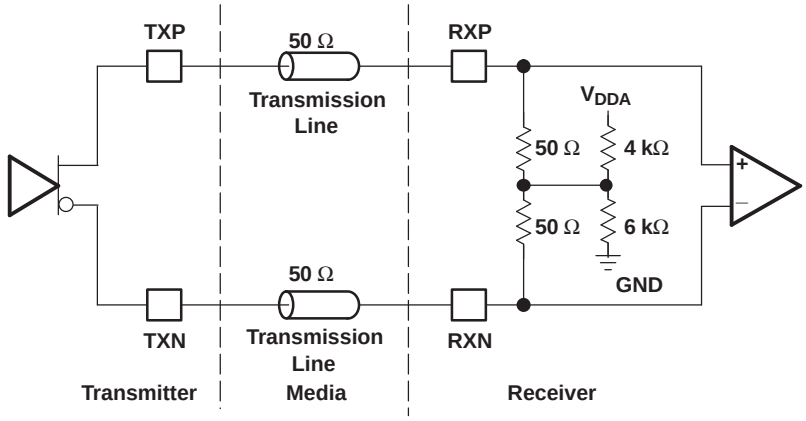


Figure 13. High-Speed I/O Directly-Coupled Mode

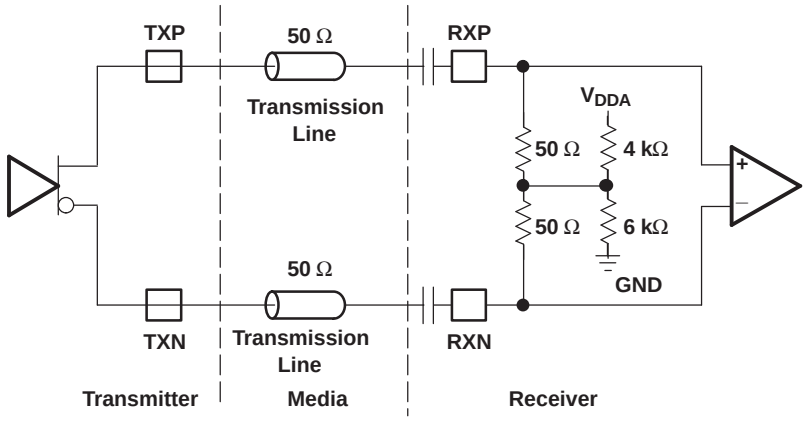


Figure 14. High-Speed I/O AC-Coupled Mode

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
5962-0522101VXC	ACTIVE	CFP	HFG	68	1	TBD	Call TI	N / A for Pkg

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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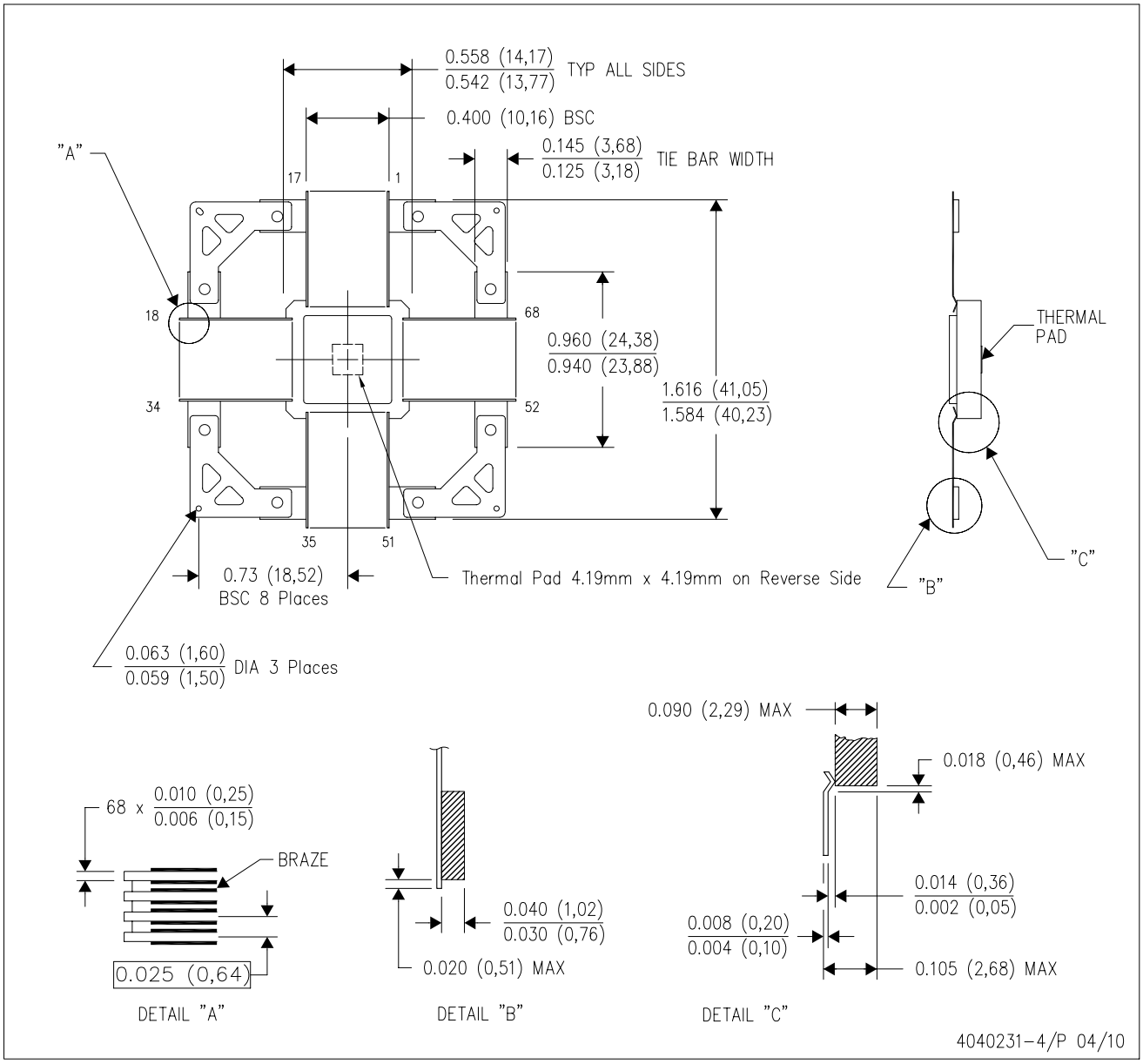
OTHER QUALIFIED VERSIONS OF TLK2711-SP :

- Catalog: TLK2711

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

HFG (S–CQFP–F68) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Thermal dissipation enhancement provided by vias to external bottom pad.
H. Lid and Thermal pad are connected to GND leads.

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