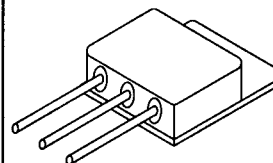
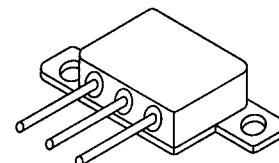




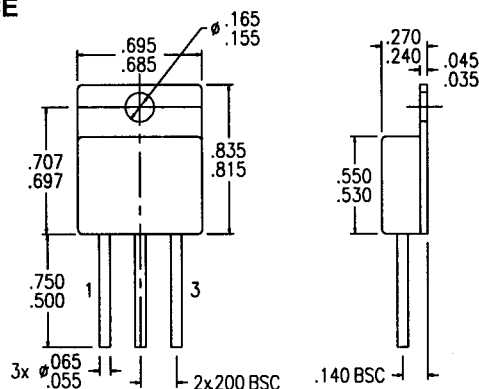
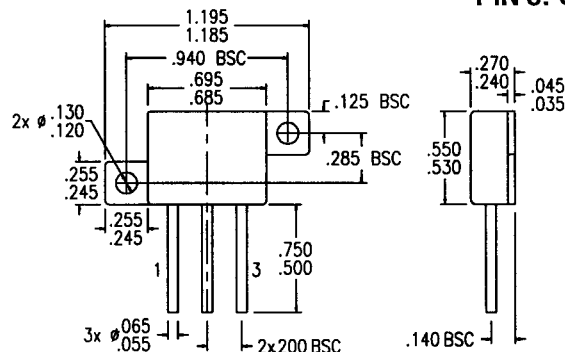
PRELIMINARY

SOLID STATE DEVICES, INC14849 Firestone Boulevard · La Mirada, CA 90638
Phone: (714) 670-SSDI (7734) · Fax: (714) 522-7424**Designer's Data Sheet****FEATURES:**

- Rugged construction with polysilicon gate
- Low RDS(on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input and transfer capacitance for easy paralleling
- Ceramic Seals for improved hermeticity
- Hermetically sealed package
- TX, TXV and Space Level screening available
- Replaces: IXTH75N10 Types

SFF75N10N
SFF75N10P**75 AMP**
100 VOLTS
0.025 Ω
N-CHANNEL
POWER MOSFET**TO-258****TO-259****MAXIMUM RATINGS**

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V _{DS}	100	Volts
Gate to Source Voltage	V _{GS}	±20	Volts
Continuous Drain Current	I _D	75	Amps
Operating and Storage Temperature	T _{op} & T _{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case	R _{θJC}	0.83	°C/W
Total Device Dissipation @ TC=25°C Total Device Dissipation @ TC=55°C	P _D	150 114	Watts
Repetitive Avalanche Energy	E _{AR}	30	mJ

PACKAGE OUTLINE: TO-258 (N)**PIN OUT:****PIN 1: DRAIN****PIN 2: SOURCE****PIN 3: GATE****PACKAGE OUTLINE: TO-259 (P)****PIN OUT:****PIN 1: DRAIN****PIN 2: SOURCE****PIN 3: GATE**

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: F00157 C**MED**

SFF75N10N

SFF75N10P

查询"SFF75N10N"供应商

PRELIMINARY



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ELECTRICAL CHARACTERISTICS @ $T_J=25^\circ\text{C}$ (Unless Otherwise Specified)

RATING	SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage ($V_{GS}=0\text{ V}$, $I_D=250\mu\text{A}$)	BV_{DSS}	100	---	---	V
Drain to Source on State Resistance ($V_{GS}=10\text{ V}$) $I_D=37.5\text{ A}$ $I_D=75\text{ A}$	$R_{DS(on)}$	---	---	0.025 0.030	Ω
On State Drain Current ($V_{DS} > I_D(on) \times R_{DS(on)}$ Max, $V_{GS}=10\text{ V}$)	$I_D(on)$	75	---	---	A
Gate Threshold Voltage ($V_{DS} \geq V_{GS}$, $I_D=4\text{ mA}$)	$V_{GS(th)}$	2.0	---	4.0	V
Forward Transconductance ($V_{DS} > I_D(on) \times R_{DS(on)}$ Max, $I_{DS}=50\%$ rated I_D)	g_{fs}	25	30	---	S(V)
Zero Gate Voltage Drain Current ($V_{DS}=\text{max rated voltage}$, $V_{GS}=0\text{ V}$) ($V_{DS}=80\%$ rated V_{DS} , $V_{GS}=0\text{ V}$, $T_A=125^\circ\text{C}$)	I_{DSS}	---	---	250 1000	μA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V_{GS} I_{GSS}	---	---	+200 -200	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	$V_{GS}=10\text{ Volts}$ 50% rated V_{DS} 50% Rated I_D Q_g Q_{gs} Q_{gd}	---	160 16 50	260 70 160	nC
Turn on Delay Time Rise Time Turn Off Delay Time Fall Time	$V_{DD}=50\%$ rated V_{DS} 50% rated I_D $R_G=6.2\Omega$ $V_{GS}=10\text{ V}$ $t_{d(on)}$ t_r $t_{d(off)}$ t_f	---	30 35 100 40	40 100 120 80	nsec
Diode Forward Voltage ($I_S=\text{rated } I_D$, $V_{GS}=0\text{ V}$, $T_J=25^\circ\text{C}$)	V_{SD}	---	1.3	1.75	V
Diode Reverse Recovery Time Reverse Recovery Charge	$T_J=25^\circ\text{C}$ $I_F=10\text{ A}$ $di/dt=100\text{ A}/\mu\text{sec}$ t_{rr} Q_{RR}	---	120 ---	200 ---	nsec μC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{GS}=0\text{ Volts}$ $V_{DS}=25\text{ Volts}$ $f=1\text{ MHz}$ C_{iss} C_{oss} C_{rss}	---	4500 1600 800	---	pF

SAFE OPERATING AREA (S.O.A.)
 $T_C = 25^\circ\text{C}$, D.C. CONDITION

