REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14									

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 19 MAY 1989

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS UV ERASABLE PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88548
A	67268	

SHEET 1 OF 14

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1283

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88548	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(see 6.4)	900 gate EPLD	60 ns

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x 0.620" x 0.225"), dual-in-line package 1/

1.3 Absolute maximum ratings.

Supply voltage range, (V_{CC})	-2.0 V dc to 7.0 V dc
Programming supply voltage range (V_{PP})	-2.0 V dc to +13.5 V dc
DC input voltage (V_I) 2/	-0.5 V dc to V_{CC} +0.3 V dc
Power dissipation (P_D)	750 mW
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+200°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.3 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.0 V dc to V_{CC} +0.3 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input rise time (T_R)	500 ns maximum
Input fall time (T_F)	500 ns maximum
Clock pins, rise time	100 ns maximum
Clock pins, fall time	100 ns maximum

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ Minimum dc input voltage is -0.3 V dc. During transitions the inputs may undershoot to -2.0 V dc for periods less than 20 ns under no load conditions.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range. Additionally the low power standby power mode is disabled. AC testing load conditions are shown on figure 3.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc (unless otherwise specified)	Device type	Group A subgroups	Limits Min	Limits Max	Unit
High level input voltage	V_{IH}		01	1, 2, 3	2.0	V_{CC} +0.3 2/	V
Low level input voltage	V_{IL}		01	1, 2, 3	-0.3 2/	0.8	V
Low level output voltage	V_{OL}	I_{OL} = 4.0 mA	01	1, 2, 3		0.45	V
High level TTL output voltage	V_{OH}	I_{OH} = -4.0 mA	01	1, 2, 3	2.4		V
High level CMOS output voltage	V_{OH}	I_{OH} = -2.0 mA	01	1, 2, 3	3.84		V
Input leakage current	I_I	$V_I = V_{CC}$ or GND	01	1, 2, 3	-10	10	µA
3-state output off current	I_{OZ}	$V_O = V_{CC}$ or GND	01	1, 2, 3	-10	10	µA
V_{CC} supply current 3/	I_{CC}	V_{IN} = 0V or V_{CC} f = 1.0 MHz	01	1, 2, 3		100	mA
Input capacitance	C_{IN}	V_{IN} = 0 V dc; f = 1.0 MHz measured from pin to V_{SS} see 4.3.1c	01	4		20	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V dc; f = 1.0 MHz measured from pin to V_{SS} see 4.3.1c	01	4		20	pF
Clock pin capacitance	C_{CLK}	V_{IN} = 0 V dc; f = 1.0 MHz measured from pin to V_{SS} see 4.3.1c	01	4		20	pF
Clk/V_{PP} capacitance	C_{VPP}	V_{OUT} = 0 V dc; f = 1.0 MHz measured from pin to V_{SS} see 4.3.1c	01	4		80	pF
Functional tests		See 4.3.1d	01	7, 8			
Input to non-registered output 4/	t_{PD}	C_L = 50 pF see figures 3 and 4	01	9, 10, 11		60	ns
Input to output enable 4/	t_{PZX}		01	9, 10, 11		60	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, 4.5 V dc $\le V_{CC} \le$ 5.5 V dc (unless otherwise specified)	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Input to output disable 4/ 5/	t_{PXZ}	C_L = 5 pF, see figures 3 and 4, output change = 500 mV	01	9, 10, 11		60	ns
Asynchronous output clear time 4/	t_{CLR}	C_L = 50 pF see figures 3 and 4 (as applicable)	01	9, 10, 11		70	ns
Input setup time 4/	t_{SU}		01	9, 10, 11	50		ns
Input hold time hold time 4/	t_H		01	9, 10, 11	0		ns
Clock high time 2/	t_{CH}		01	9, 10, 11	25		ns
Clock low time 2/	t_{CL}		01	9, 10, 11	25		ns
Clock to output delay	t_{CO1}		01	9, 10, 11		30	ns
Minimum clock period (register output feedback to register input, internal path 3/	t_{CNT}		01	9, 10, 11		70	ns
Maximum frequency ($1/t_{SU}$) 4/ 6/ 7/	f_{MAX}		01	9, 10, 11	20		MHz
Minimum clock period ($t_{SU} + t_{CO1}$)	t_{P2}		01	9, 10, 11		80	ns
Internal maximum frequency ($1/t_{CNT}$) 3/ 8/	f_{CNT}		01	9, 10, 11	14.3		MHz
Asynchronous input setup time 2/ 4/	t_{ASU}		01	9, 10, 11	15		ns
Asynchronous input hold time 2/ 4/	t_{AH}		01	9, 10, 11	15		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, 4.5 V dc $\le V_{CC} \le$ 5.5 V dc (unless otherwise specified)	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Asynchronous clock high time 2/	t_{ACH}	C_L = 50 pF see figures 3 and 4 (as applicable)	01	9, 10, 11	25		ns
Asynchronous clock low time 2/	t_{ACL}		01	9, 10, 11	25		ns
Asynchronous clock 4/ to output delay	t_{ACO1}		01	9, 10, 11		65	ns
Asynchronous minimum clock period 3/ 9/ (register output feedback to register input, internal path	t_{ACNT}		01	9, 10, 11		70	ns
Asynchronous internal maximum frequency 10/ ($1/t_{ACNT}$)	f_{ACNT}		01	9, 10, 11	14.3		MHz

1/ Screening and characterization of ac delay parameters is typically conducted while operating at less than maximum frequency.

2/ May not be tested, but shall be guaranteed to the limits specified in table I.

3/ Tested using data pattern specified by device manufacturer, correlated to 24 bit counter and no output loading.

4/ All array-dependent delays are specified for an XOR pattern. This pattern involves two product terms and two pure inputs with all other product terms in the macrocell held low by one EPROM pulldown. Other patterns may result in longer delays than those specified. Delays involving only one product term such as t_{PXZ} are specified for an "XOR-like" pattern which involves one pure input switching at a time, and the single product term.

5/ Not tested directly, but guaranteed by testing of t_{PD}.

6/ f_{MAX} represents the highest frequency for pipelined data.

7/ Not tested directly, but derived from t_{SU}.

8/ Not tested directly, but derived from t_{CNT}.

9/ Not tested directly, but guaranteed by testing of t_{CNT}.

10/ Not tested directly, but derived from t_{ACNT}.

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3.5 Processing EPLDS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPLDS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPLDS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.5.3 Verification of erasure of programmability of EPLDS. When specified, devices shall be verified as either programmed to the specific pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. All devices shall be tested using the test patterns specified in the footnotes of table I.

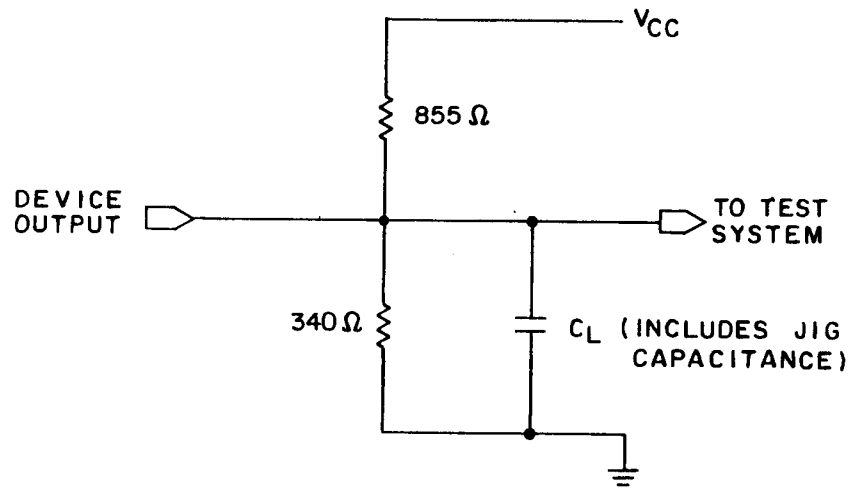
d. A data retention stress test shall be included as part of the screening procedure (may be performed prior to the internal visual inspection of method 5004 of MIL-STD-883 at the discretion of the manufacturer) and shall consist of the following steps:

Device type	01
Case outline	Q
Terminal number	Terminal symbol
1	CLK1
2	INPUT
3	INPUT
4	INPUT
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	INPUT
18	INPUT
19	INPUT
20	GND
21	CLK2
22	INPUT
23	INPUT
24	INPUT
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	INPUT
38	INPUT
39	INPUT
40	V_{CC}

FIGURE 1. Terminal connections.

Mode	CLK2/V_{PP}	CLK1/PGM	I/O	Input
Normal Operation	V_{IL} or V_{IH} (clock)	V_{IL} or V_{IH} (clock)	defined by application	V_{IL} or V_{IH} (data input)
Program	V_{PP} (programming supply)	V_{ILP} (program pulse)	V_{IHP} or V_{ILP} (data input)	V_{IHP} or V_{ILP} (address)
Verify	Don't care	V_{HH} (verify control)	data out V_{OH} or V_{OL}	V_{ILP} or V_{IHP} (address)

FIGURE 2. Truth table (unprogrammed).

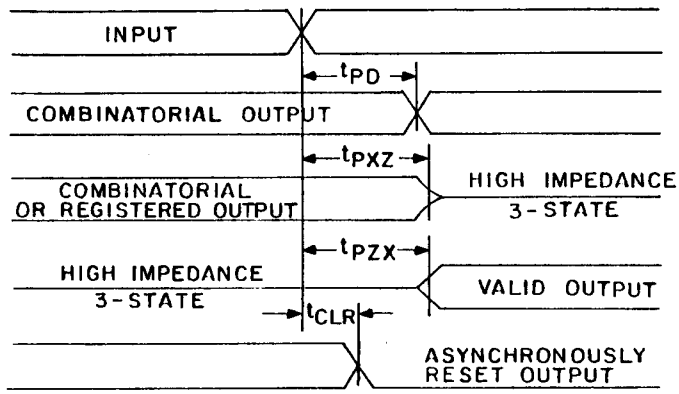


DEVICE INPUT RISE AND FALL TIMES ≤ 6ns

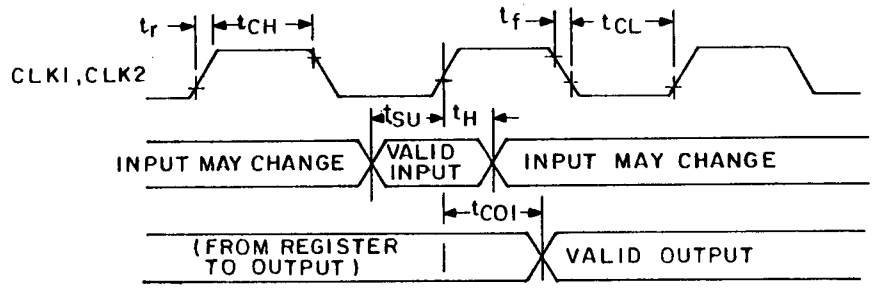
FIGURE 3. Test load circuit.

NOTE
t_r and t_f = 6 ns maximum.
t_{CL} and t_{CH} are specified at 0.3 V and 2.7 V respectively all other timings are at 1.5 V, input levels are at 0 V and 3 V.

COMBINATORIAL MODE



SYNCHRONOUS CLOCK MODE



ASYNCHRONOUS CLOCK MODE

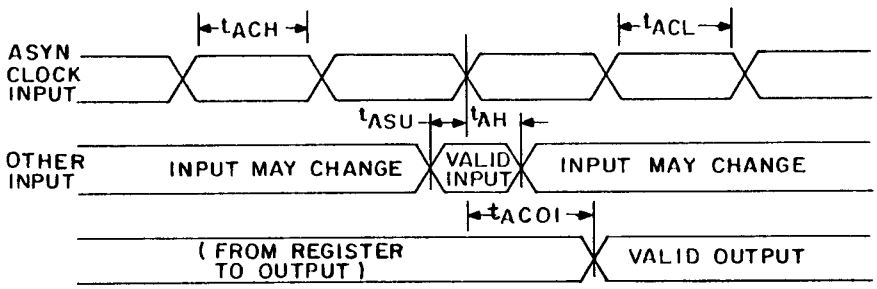


FIGURE 4. Switching waveforms.

Margin test method

(1) Each device shall be verified to be erased and subjected to a full functional test. Each device shall then have greater than 99 percent of all user bit locations (except the security bit) programmed and verified.

(2) Each device shall then be subjected to an unbiased retention bake at 140°C for 72 hours minimum (or equivalent time and temperature implied by an activation energy of 0.4 eV).

(3) After the retention bake, each device shall again be verified. Each device shall then be electrically tested with guardbanding. A margin voltage of V_{CC} = 5.8 V dc (minimum) shall be used, and each programmed bit shall be verified to maintain the proper logic state. All remaining bits not programmed before retention bake shall be programmed and verified to be programmed except the security bit.

(4) Any device containing a bit which does not verify as programmed, or erased, as applicable, or which does not maintain the proper logic state during margin testing, shall be rejected and shall not be delivered to this drawing.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, C_{CLK} and C_{VPP} measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. As a minimum, subgroups 7 and 8 shall consist of verifying the EPLD pattern as specified in footnotes of table I.

e. All devices selected for testing shall be programmed as specified in the footnotes of table I. After completion of all testing, the devices shall be erased and verified to be erased.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein, using test pattern specifed in table I footnotes.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7,8, 9,10,11
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7,8
Group A test requirements (method 5005)	1,2,3,4**,7, 8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8,10

* PDA applies to subgroup 1.
** See 4.3.1c.

4.4 Erasing procedures. The recommended erasure procedure is exposing to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of fifteen (15) Ws/cm. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 W/cm power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm (1 week at 12,000 W/cm). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

4.6 Electrostatic discharge sensitivity (ESDS). Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015 and MIL-M-38510 for initial testing and after any design or process changes which may affect input or output protection circuitry. The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 2,000 volts or greater shall be considered as conforming to the requirements of this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8854801QX	67183 34649	EP900DM883B MD5C090

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 5000 W. Chandler Boulevard Chandler, AZ 85226
67183	Altera Corporation 3525 Monroe Street Santa Clara, CA 95051