



## 12-Bit, Parallel Input, Multiplying Digital-to-Analog Converter

### FEATURES

- 2.5 V to 5.5 V Supply Operation
- Fast Parallel Interface: 17ns Write Cycle
- Update Rate of 20.4 MSPS
- 10 MHz Multiplying Bandwidth
- $\pm 10$  V Reference Input
- Low Glitch Energy: 5 nV-s
- Extended Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- 20-Lead QFN and 20-Lead TSSOP Packages
- 12-Bit Monotonic
- $\pm 1$  LSB INL
- 4-Quadrant Multiplication
- Power-On Reset with Brownout Detection
- Readback Function
- Industry-Standard Pin Configuration

### APPLICATIONS

- Portable Battery-Powered Instruments
- Waveform Generators
- Analog Processing
- Programmable Amplifiers and Attenuators
- Digitally-Controlled Calibration
- Programmable Filters and Oscillators
- Composite Video
- Ultrasound

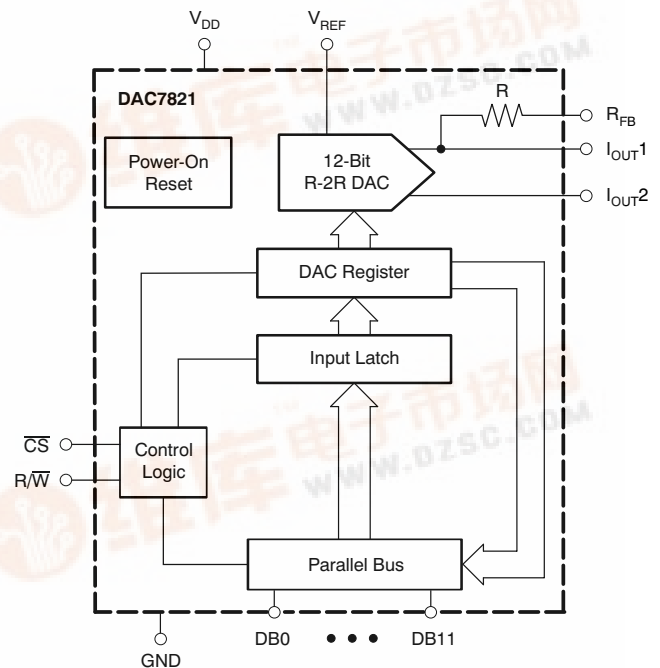
### DESCRIPTION

The DAC7821 is a CMOS 12-bit current output digital-to-analog converter (DAC). This device operates from a single 2.5 V to 5.5 V power supply, making it suitable to battery-powered and many other applications.

This DAC operates with a fast parallel interface. Data readback allows the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with zeroes and the DAC outputs are at zero scale.

The DAC7821 offers excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidth of 10 MHz. The applied external reference input voltage ( $V_{\text{REF}}$ ) determines the full-scale output current. An integrated feedback resistor ( $R_{\text{FB}}$ ) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier.

The DAC7821 is available in a 20-lead TSSOP package as well as a small 20-lead QFN package (available Q2 2006).



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC7821	20-TSSOP	PW	-40°C to +125°C	DAC7821	DAC7821IPW	70, Tube
					DAC7821IPWR	2000, Tape and Reel
DAC7821	20-QFN <sup>(2)</sup>	RGP	-40°C to +125°C	DAC7821	DAC7821IRGPT	250, Tape and Reel
					DAC7821IRGPR	3000, Tape and Reel

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or refer to our web site at [www.ti.com](http://www.ti.com).

(2) Available 2Q 2006.

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	DAC7821	UNIT
$V_{DD}$ to GND	-0.3 to +7.0	V
Digital input voltage to GND	-0.3 to $V_{DD} + 0.3$	V
$V_{OUT}$ to GND	-0.3 to $V_{DD} + 0.3$	V
Operating temperature range	-40 to +125	°C
Storage temperature range	-65 to +150	°C
Junction temperature ( $T_J$ max)	+150	°C
ESD Rating, HBM	3000	V
ESD Rating, CDM	1000	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

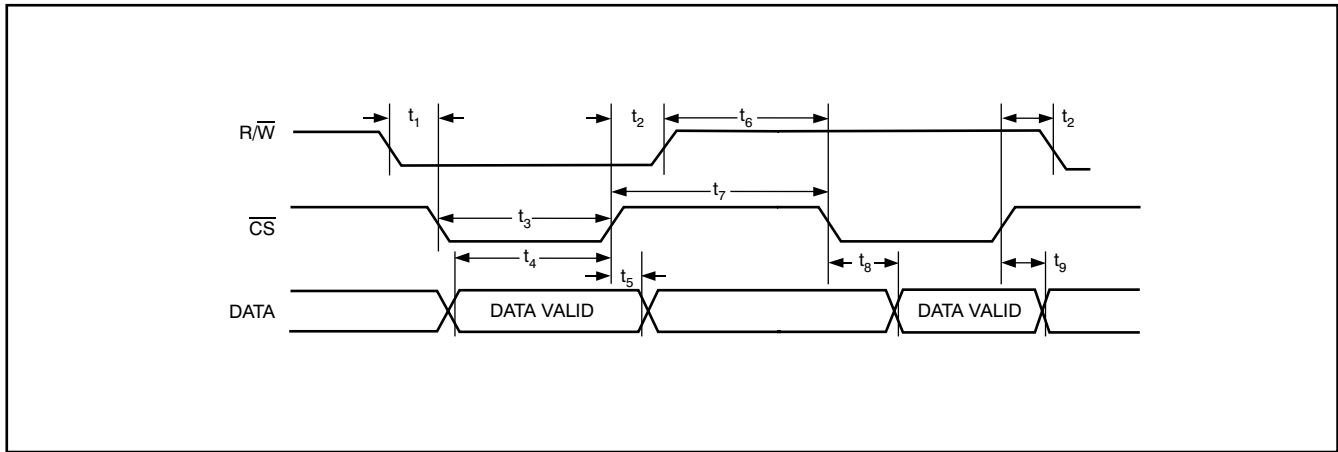
**ELECTRICAL CHARACTERISTICS**

$V_{DD} = +2.5\text{ V to }+5.5\text{ V}$ ;  $I_{OUT1} = \text{Virtual GND}$ ;  $I_{OUT2} = 0\text{V}$ ;  $V_{REF} = +10\text{ V}$ ;  $T_A = \text{full operating temperature}$ . All specifications  $-40^\circ\text{C to }+125^\circ\text{C}$ , unless otherwise noted.

PARAMETER	CONDITIONS	DAC7821			UNITS
		MIN	TYP	MAX	
<b>STATIC PERFORMANCE</b>					
Resolution		12			Bits
Relative accuracy				$\pm 1$	LSB
Differential nonlinearity				$\pm 1$	LSB
Output leakage current	Data = 000h, $T_A = +25^\circ\text{C}$			$\pm 10$	nA
Output leakage current	Data = 000h, $T_A = T_{MAX}$			$\pm 20$	nA
Full-scale gain error	All ones loaded to DAC register		$\pm 5$	$\pm 10$	mV
Full-scale tempco			$\pm 5$		ppm/ $^\circ\text{C}$
Output capacitance	Code dependent		30		pF
<b>REFERENCE INPUT</b>					
$V_{REF}$ range		-15		15	V
Input resistance		8	10	12	k $\Omega$
$R_{FB}$ resistance		8	10	12	k $\Omega$
<b>LOGIC INPUTS AND OUTPUT<sup>(1)</sup></b>					
Input low voltage	$V_{IL}$ $V_{DD} = +2.7\text{V}$			0.6	V
	$V_{IL}$ $V_{DD} = +5\text{V}$			0.8	V
Input high voltage	$V_{IH}$ $V_{DD} = +2.7\text{V}$	2.1			V
	$V_{IH}$ $V_{DD} = +5\text{V}$	2.4			V
Input leakage current	$I_{IL}$			10	$\mu\text{A}$
Input capacitance	$C_{IL}$			10	pF
<b>POWER REQUIREMENTS</b>					
$V_{DD}$		2.7		5.5	V
$I_{DD}$ (normal operation)	Logic inputs = 0 V			5	$\mu\text{A}$
$V_{DD} = +4.5\text{ V to }+5.5\text{ V}$	$V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$		0.8	5	$\mu\text{A}$
$V_{DD} = +2.5\text{ V to }+3.6\text{ V}$	$V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$		0.4	2.5	$\mu\text{A}$
<b>AC CHARACTERISTICS</b>					
Output voltage settling time				0.2	$\mu\text{s}$
Reference multiplying BW	$V_{REF} = 7 V_{PP}$ , Data = FFFh		10		MHz
DAC glitch impulse	$V_{REF} = 0\text{ V to }10\text{ V}$ , Data = 7FFh to 800h to 7FFh		5		nV-s
Feedthrough error $V_{OUT}/V_{REF}$	Data = 000h, $V_{REF} = 100\text{kHz}$		-70		dB
Digital feedthrough			2		nV-s
Total harmonic distortion			-105		dB
Output spot noise voltage			18		$\text{nV}/\sqrt{\text{Hz}}$

(1) Specified by design and characterization; not production tested.

TIMING INFORMATION



**TIMING REQUIREMENTS: 2.5 V to 4.5 V**

At  $t_r = t_f = 1$  ns (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ ;  $V_{DD} = +2.5$  V to  $+4.5$  V,  $V_{REF} = +10$  V,  $I_{OUT2} = 0$  V. All specifications  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise noted.

PARAMETER <sup>(1)</sup>	TEST CONDITIONS	DAC7821			UNIT
		MIN	TYP	MAX	
$t_1$	R/W to CS setup time	0			ns
$t_2$	R/W to CS hold time	0			ns
$t_3$	CS low time (write cycle)	10			ns
$t_4$	Data setup time	6			ns
$t_5$	Data hold time	0			ns
$t_6$	R/W high to CS low	5			ns
$t_7$	CS min high time	9			ns
$t_8$	Data access time		20	40	ns
$t_9$	Bus relinquish time		5	10	ns

(1) Ensured by design; not production tested.

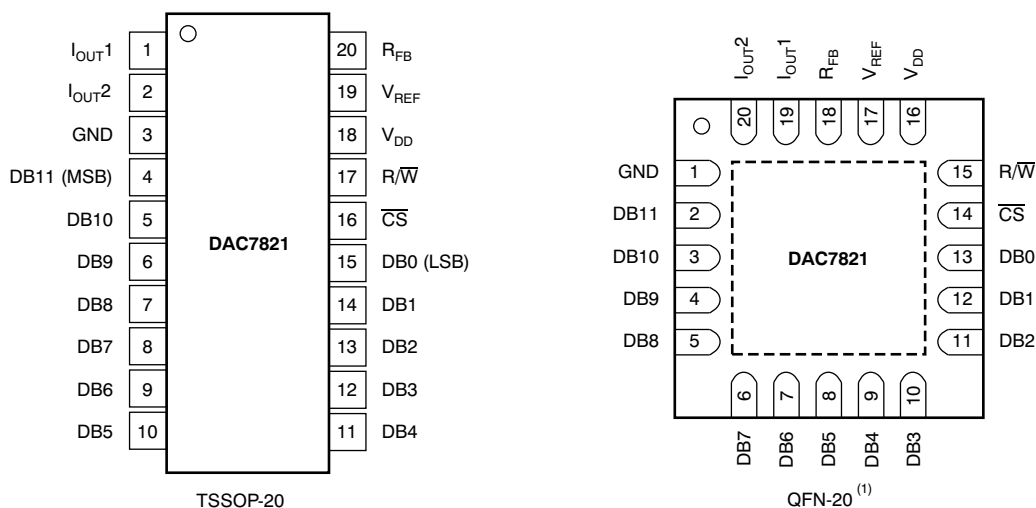
**TIMING REQUIREMENTS: 4.5 V to 5.5 V**

At  $t_r = t_f = 1$  ns (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ ;  $V_{DD} = +4.5$  V to  $+5.5$  V,  $V_{REF} = +10$  V,  $I_{OUT2} = 0$  V. All specifications  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise noted.

PARAMETER <sup>(1)</sup>	TEST CONDITIONS	DAC7821			UNIT
		MIN	TYP	MAX	
$t_1$	R/W to CS setup time	0			ns
$t_2$	R/W to CS hold time	0			ns
$t_3$	CS low time (write cycle)	10			ns
$t_4$	Data setup time	6			ns
$t_5$	Data hold time	0			ns
$t_6$	R/W high to CS low	5			ns
$t_7$	CS min high time	7			ns
$t_8$	Data access time		10	20	ns
$t_9$	Bus relinquish time		5	10	ns

(1) Ensured by design; not production tested.

## DEVICE INFORMATION



(1) QFN-20 package available 2Q 2006.

## TERMINAL FUNCTIONS

TERMINAL		NAME	DESCRIPTION
TSSOP NO.	QFN NO.		
1	19	I <sub>OUT1</sub>	DAC current output.
2	20	I <sub>OUT2</sub>	DAC analog ground. This pin is normally tied to the analog ground of the system.
3	1	GND	Ground pin.
4–15	2–13	DB11 – DB0	Parallel data bits 11 to 0.
16	14	$\overline{CS}$	Chip select input. Active low. Used in conjunction with R/ $\overline{W}$ to load parallel data to the input latch or read data from the DAC register. Rising edge of $\overline{CS}$ loads data.
17	15	R/ $\overline{W}$	Read/Write. When low, use in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to read back contents of DAC register.
18	16	V <sub>DD</sub>	Positive power supply input. These parts can be operated from a supply of 2.5 V to 5.5 V.
19	17	V <sub>REF</sub>	DAC reference voltage input.
20	18	R <sub>FB</sub>	DAC feedback resistor pin. Establish voltage output for the DAC by connecting to external amplifier output.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

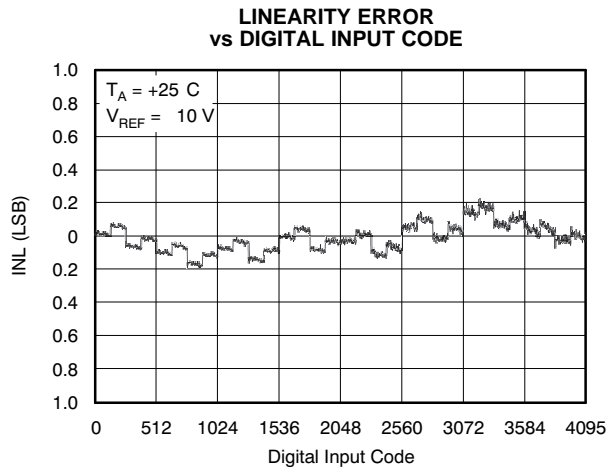


Figure 1.

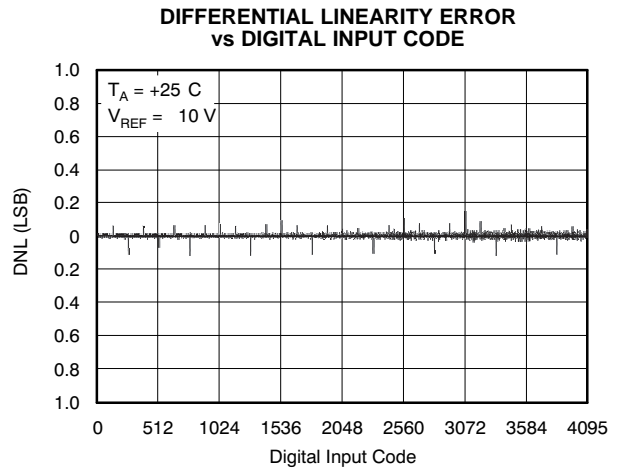


Figure 2.

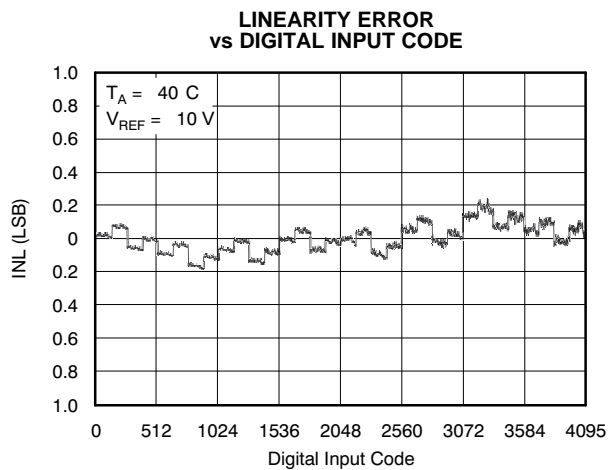


Figure 3.

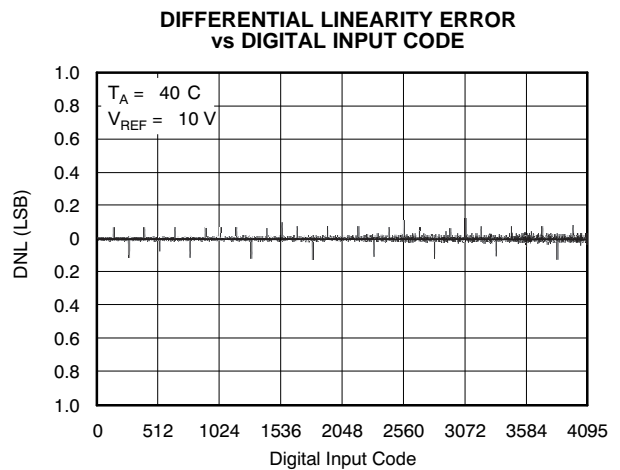


Figure 4.

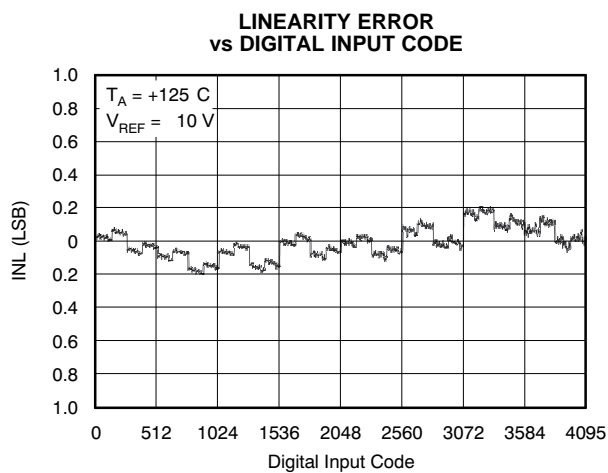


Figure 5.

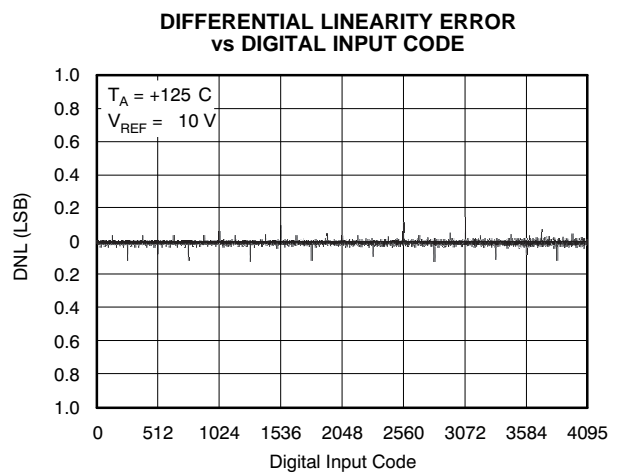


Figure 6.

TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$  (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

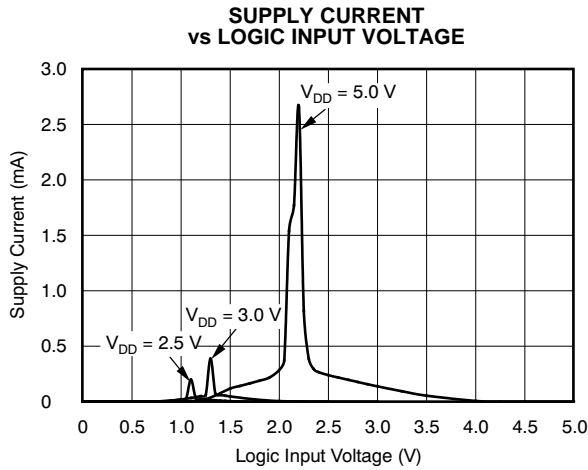


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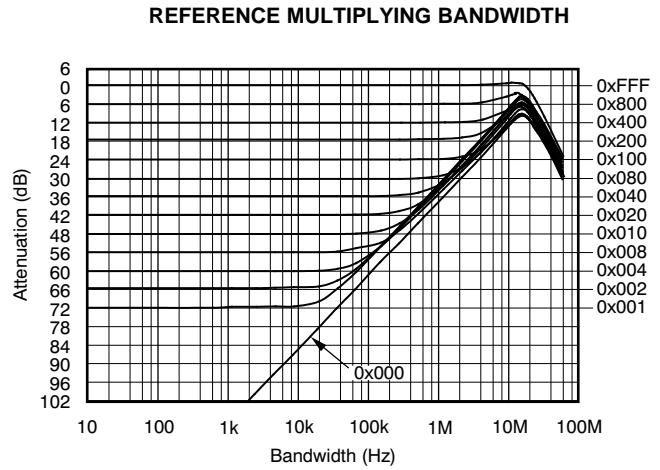


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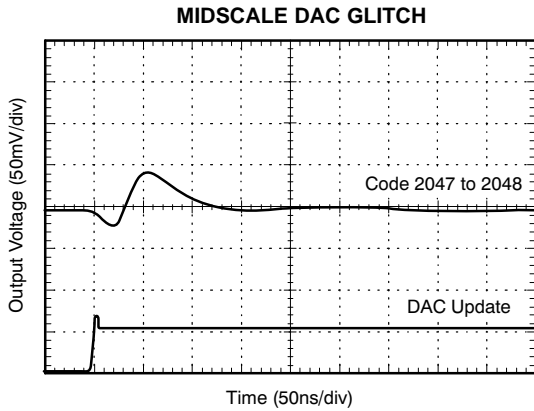


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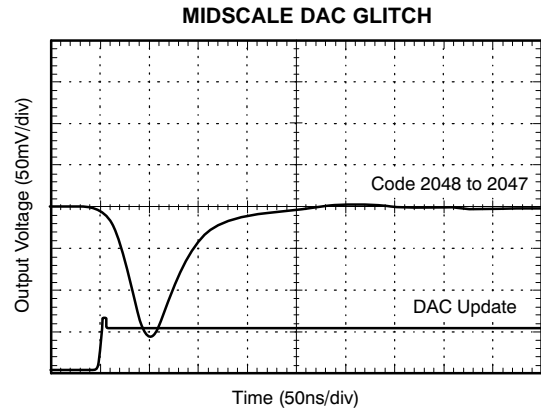


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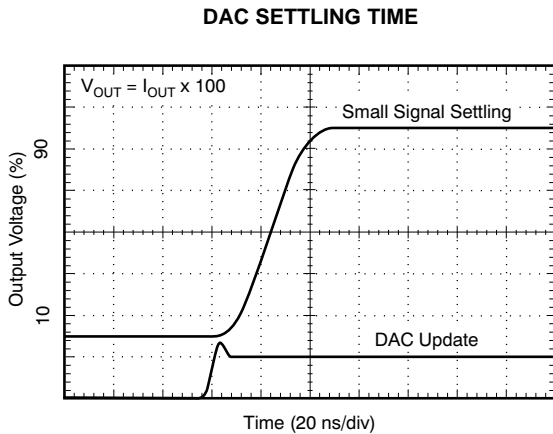


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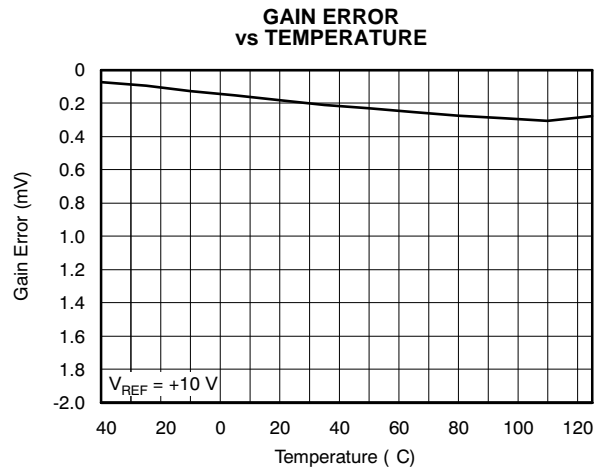
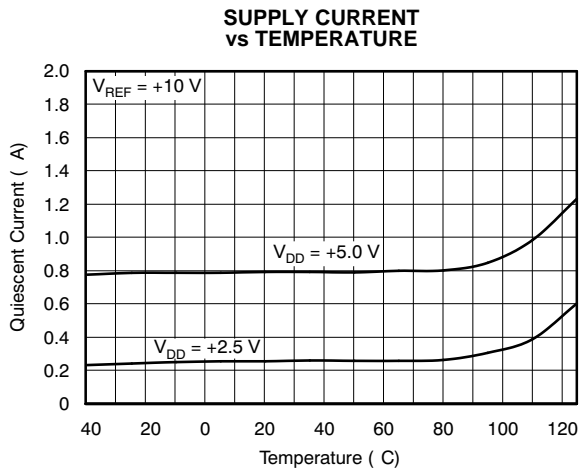


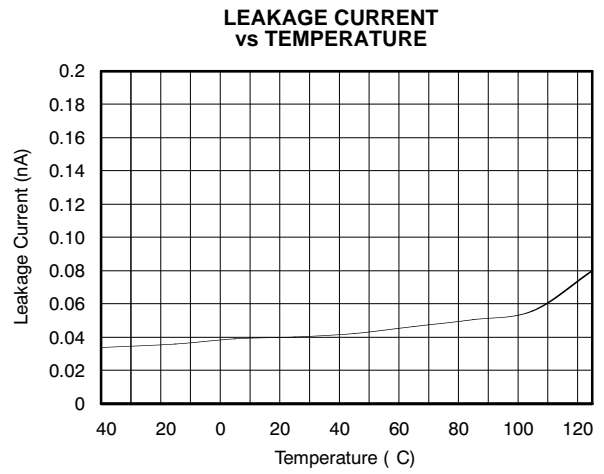
Figure 12.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.



**Figure 13.**

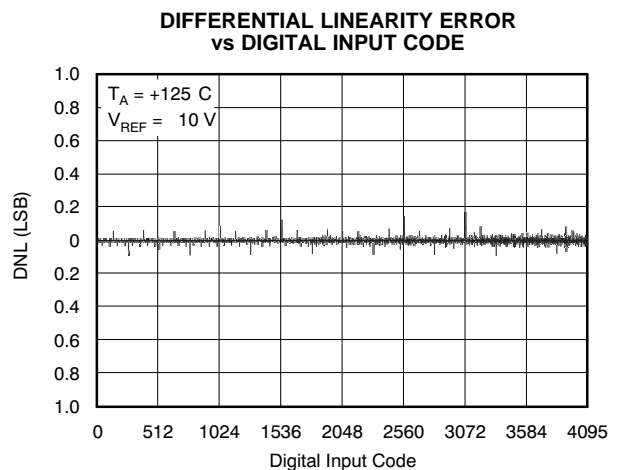
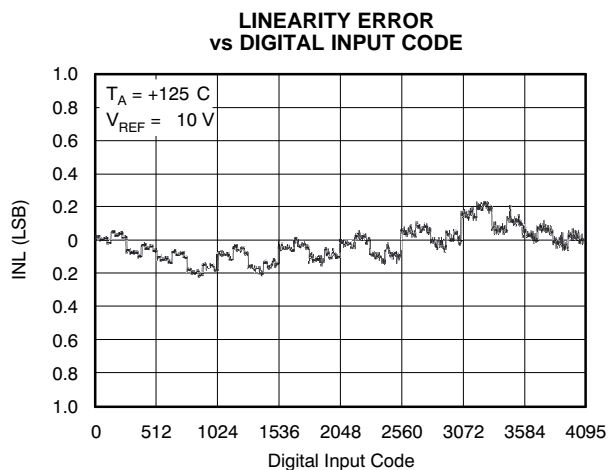
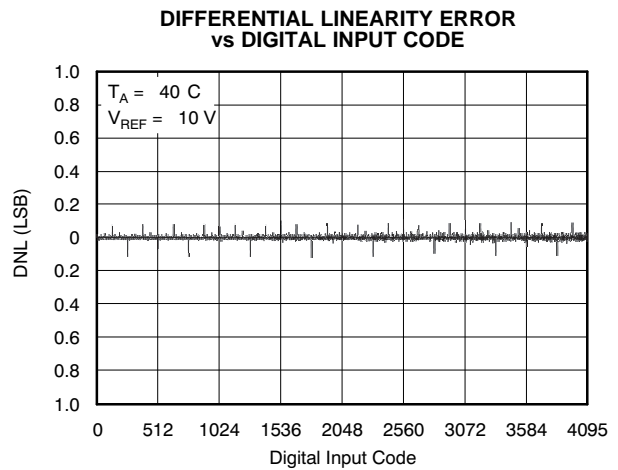
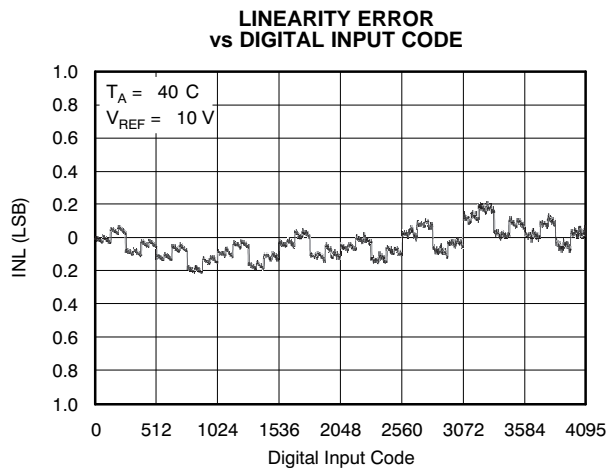
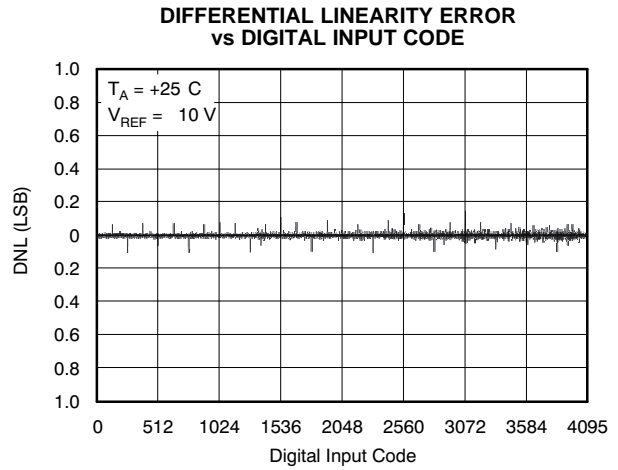
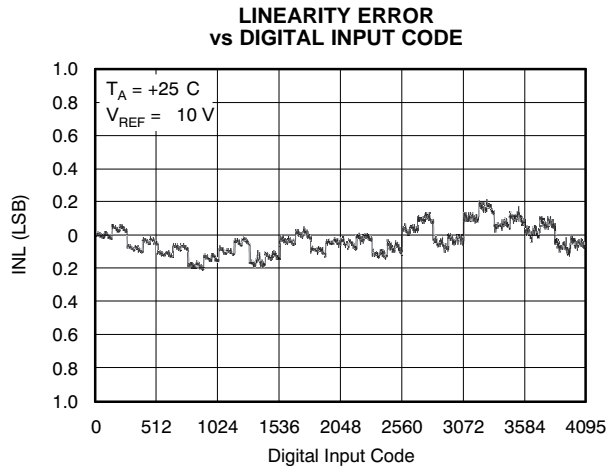


**Figure 14.**



**TYPICAL CHARACTERISTICS:  $V_{DD} = +2.5 V$**

At  $T_A = +25^\circ C$ , unless otherwise noted.



TYPICAL CHARACTERISTICS:  $V_{DD} = +2.5\text{ V}$  (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

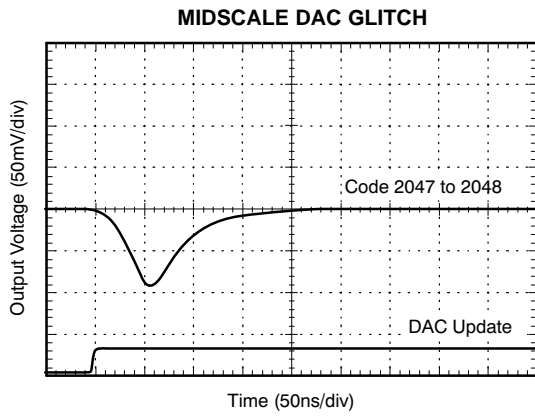


Figure 21.

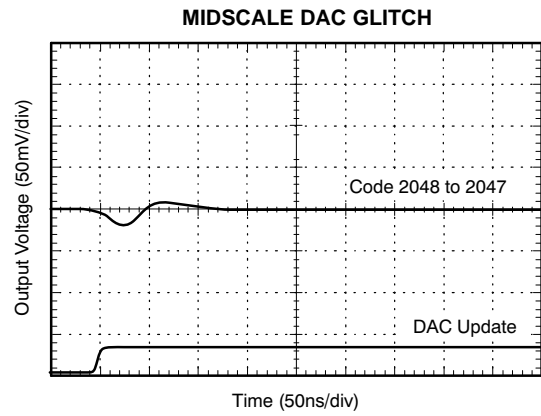


Figure 22.

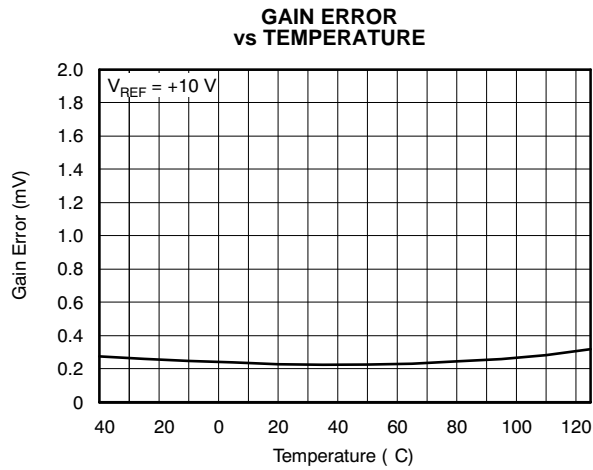


Figure 23.

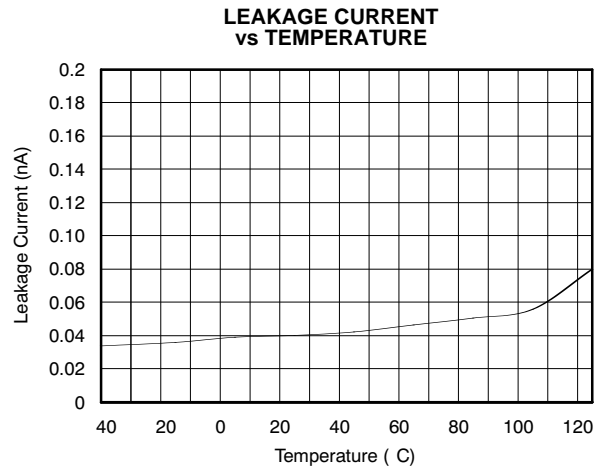


Figure 24.

## THEORY OF OPERATION

The DAC7821 is a single channel current output, 12-bit digital-to-analog converter (DAC). The architecture, illustrated in Figure 25, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to I<sub>OUT1</sub> or the I<sub>OUT2</sub> terminal. The I<sub>OUT1</sub> terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input V<sub>REF</sub> that determines the DAC full-scale current. The R-2R ladder presents a code-independent load impedance to the external reference of 10 kΩ ±20%. The external reference voltage can vary over a range of -15 V to +15 V, thus providing bipolar I<sub>OUT</sub> current operation. By using an external I/V converter and the DAC7821 R<sub>FB</sub> resistor, output voltage ranges of -V<sub>REF</sub> to V<sub>REF</sub> can be generated.

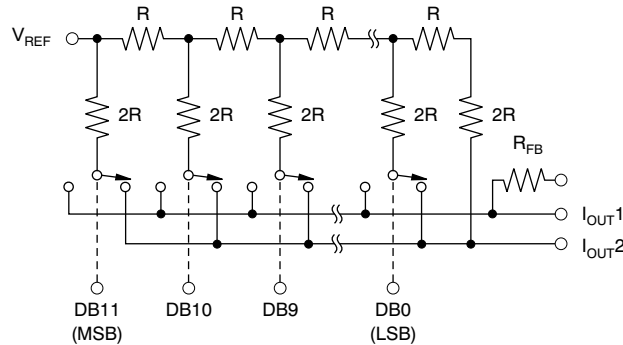


Figure 25. Equivalent R-2R DAC Circuit

When using an external I/V converter and the DAC7821 R<sub>FB</sub> resistor, the DAC output voltage is given by Equation 1:

$$V_{OUT} = + V_{REF} \times \frac{CODE}{4096} \quad (1)$$

Each DAC code determines the 2R leg switch position to either GND or I<sub>OUT1</sub>. Because the DAC output impedance as seen looking into the I<sub>OUT1</sub> terminal changes versus code, the external I/V converter noise gain will also change. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I<sub>OUT1</sub> terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC7821 as a result of offset modulation versus DAC code.

For best linearity performance of the DAC7821, an op amp with a low input offset voltage (OPA277) is recommended (see Figure 26). This circuit allows V<sub>REF</sub> swinging from -10 V to +10 V.

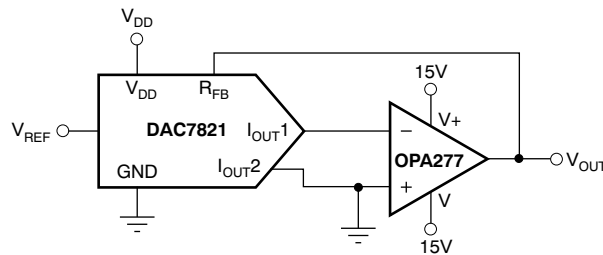
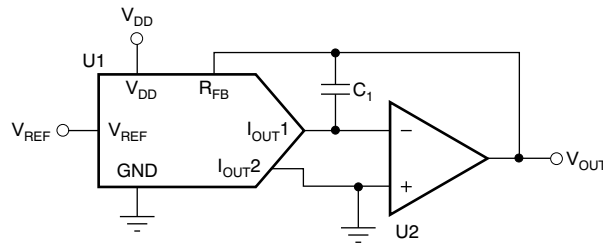


Figure 26. Voltage Output Configuration

## APPLICATION INFORMATION

### Stability Circuit

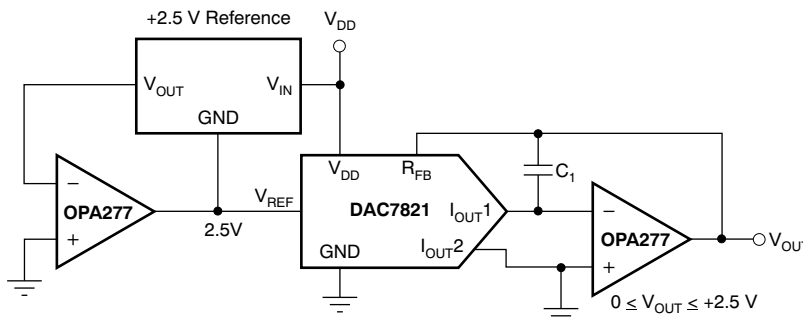
For a current-to-voltage design (see [Figure 27](#)), the DAC7821 current output ( $I_{OUT}$ ) and the connection with the inverting node of the op amp should be as short as possible and according to correct printed circuit board (PCB) layout design. For each code change, there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor  $C_1$  (1 pF to 5 pF typ) can be added to the design, as shown in [Figure 27](#).



**Figure 27. Gain Peaking Prevention Circuit with Compensation Capacitor**

### Positive Voltage Output Circuit

As [Figure 28](#) illustrates, in order to generate a positive voltage output, a negative reference is input to the DAC7821. This design is suggested instead of using an inverting amp to invert the output as a result of resistor tolerance errors. For a negative reference,  $V_{OUT}$  and GND of the reference are level-shifted to a virtual ground and a  $-2.5$  V input to the DAC7821 with an op amp.



**Figure 28. Positive Voltage Output Circuit**

### Bipolar Output Section

The DAC7821, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output  $I_{OUT}$  is the inverse of the input reference voltage at  $V_{REF}$ .

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in [Figure 29](#), external op amp U4 is added as a summing amp and has a gain of 2X that widens the output span to 5 V. A 4-quadrant multiplying circuit is implemented by using a 2.5 V offset of the reference voltage to bias U4. According to the circuit transfer equation given in [Equation 2](#), input data (D) from code 0 to full-scale produces output voltages of  $V_{OUT} = -2.5$  V to  $V_{OUT} = +2.5$  V.

$$\left( V_{OUT} = \left( \frac{D}{0.5 \times 2^N} + 1 \right) \times V_{REF} \right) \quad (2)$$

### APPLICATION INFORMATION (continued)

External resistance mismatching is the significant error in [Figure 29](#).

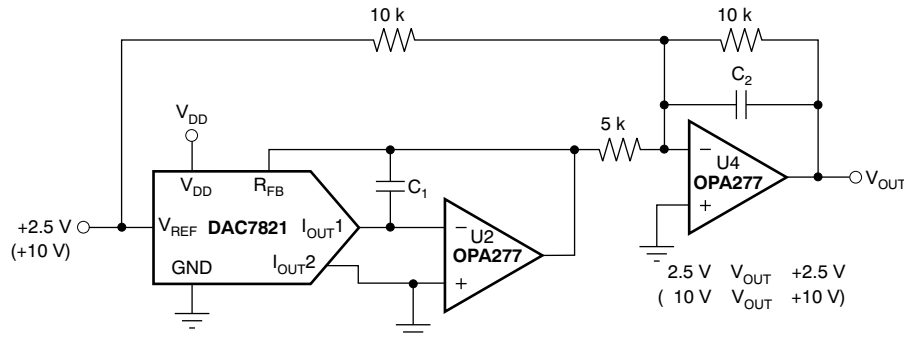


Figure 29. Bipolar Output Circuit

### Programmable Current Source Circuit

A DAC7821 can be integrated into the circuit in [Figure 30](#) to implement an improved Howland current pump for precise voltage-to-current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by [Equation 3](#):

$$I_L = \frac{(R_2 + R_3)' R_1}{R_3} \times V_{REF} \times D \quad (3)$$

The value of  $R_3$  in the previous equation can be reduced to increase the output current drive of  $U_3$ .  $U_3$  can drive  $\pm 20$  mA in both directions with voltage compliance limited up to 15 V by the  $U_3$  voltage supply. Elimination of the circuit compensation capacitor  $C_1$  in the circuit is not suggested as a result of the change in the output impedance  $Z_o$ , according to [Equation 4](#):

$$Z_o = \frac{R_1' R_3 (R_1 \times R_2)}{R_1 (R_2' \times R_3') + R_1' (R_2 \times R_3)} \quad (4)$$

As shown in [Equation 4](#), with matched resistors,  $Z_o$  is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used,  $Z_o$  is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating  $C_1$  into the circuit, possible oscillation problems are eliminated. The value of  $C_1$  can be determined for critical applications; for most applications, however, a value of several pF is suggested.

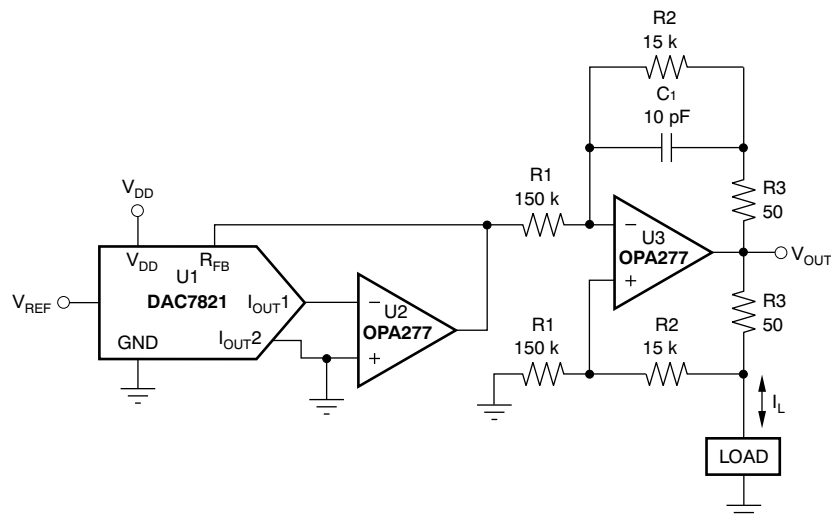


Figure 30. Programmable Bidirectional Current Source Circuit

## APPLICATION INFORMATION (continued)

### Parallel Interface

Data is loaded to the DAC7821 as a 12-bit parallel word. The bi-directional bus is controlled with  $\overline{CS}$  and  $R/\overline{W}$ , allowing data to be written to or read from the DAC register. To write to the device,  $\overline{CS}$  and  $R/\overline{W}$  are brought low, and data available on the data lines fills the input register. The rising edge of  $\overline{CS}$  latches the data and transfers the latched data-word to the DAC register. The DAC latches are not transparent; therefore, a write sequence must consist of a falling and rising edge on  $\overline{CS}$  in order to ensure that data is loaded to the DAC register and its analog equivalent is reflected on the DAC output.

To read data stored in the device,  $R/\overline{W}$  is held high and  $\overline{CS}$  is brought low. Data is loaded from the DAC register back to the input register and out onto the data line, where it can be read back to the controller.

### Cross-Reference

The DAC7821 has an industry-standard pinout. [Table 1](#) provides the cross-reference information.

**Table 1. Cross-Reference**

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC7821	±1	±1	–40°C to +125°C	20-Lead TSSOP	TSSOP-20	AD5445
DAC7821	±1	±1	–40°C to +125°C	20-Lead QFN <sup>(1)</sup>	QFN-20	AD5445

(1) Available 2Q 2006.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
DAC7821IPW	ACTIVE	TSSOP	PW	20	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7821IPWG4	ACTIVE	TSSOP	PW	20	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7821IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7821IPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7821IRGPR	PREVIEW	QFN	RGP	20	3000	TBD	Call TI	Call TI
DAC7821IRGPT	PREVIEW	QFN	RGP	20	250	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

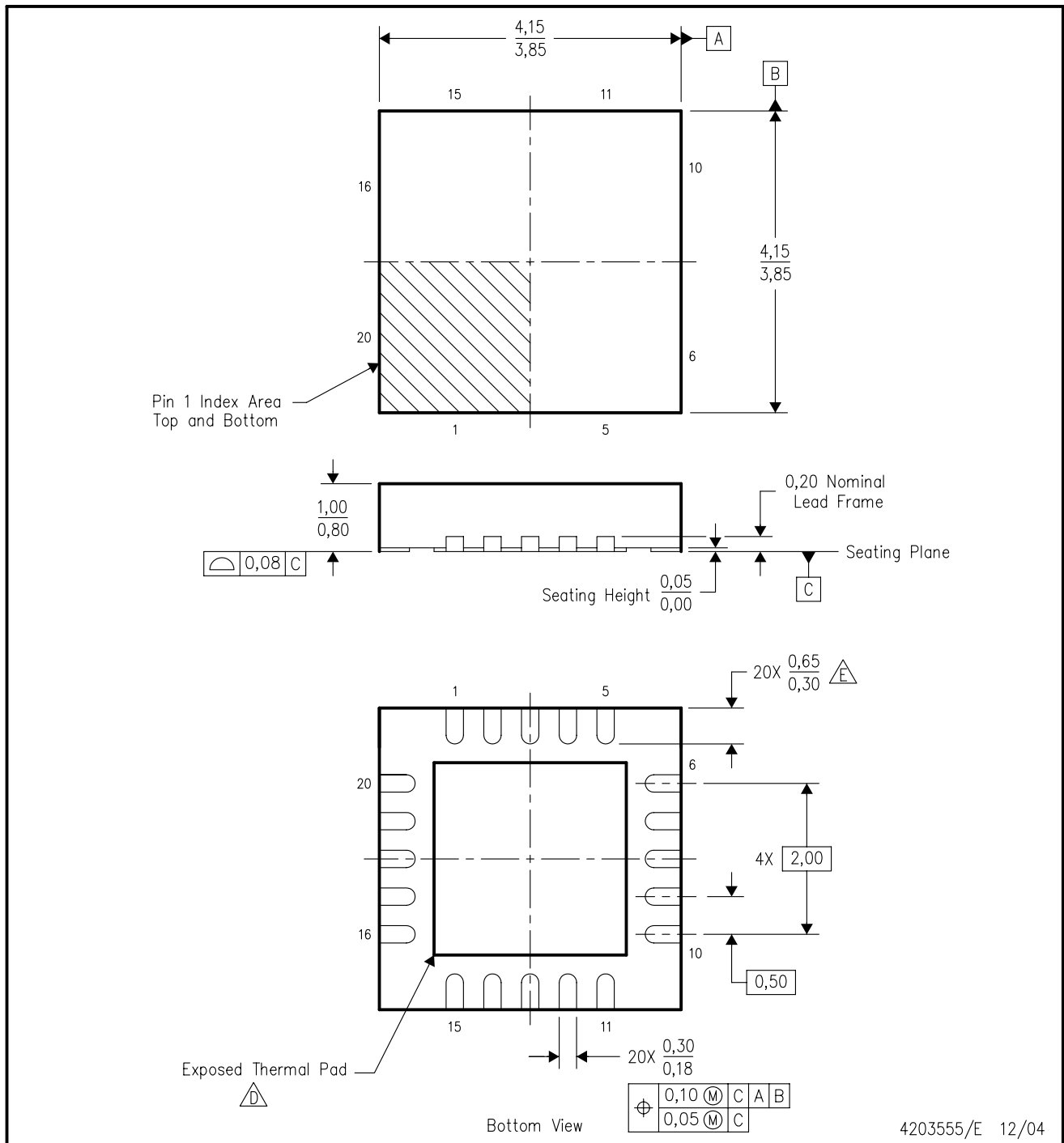
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[查询"DAC7821IPWG4"供应商](#)

RGP (S-PQFP-N20)

PLASTIC QUAD FLATPACK



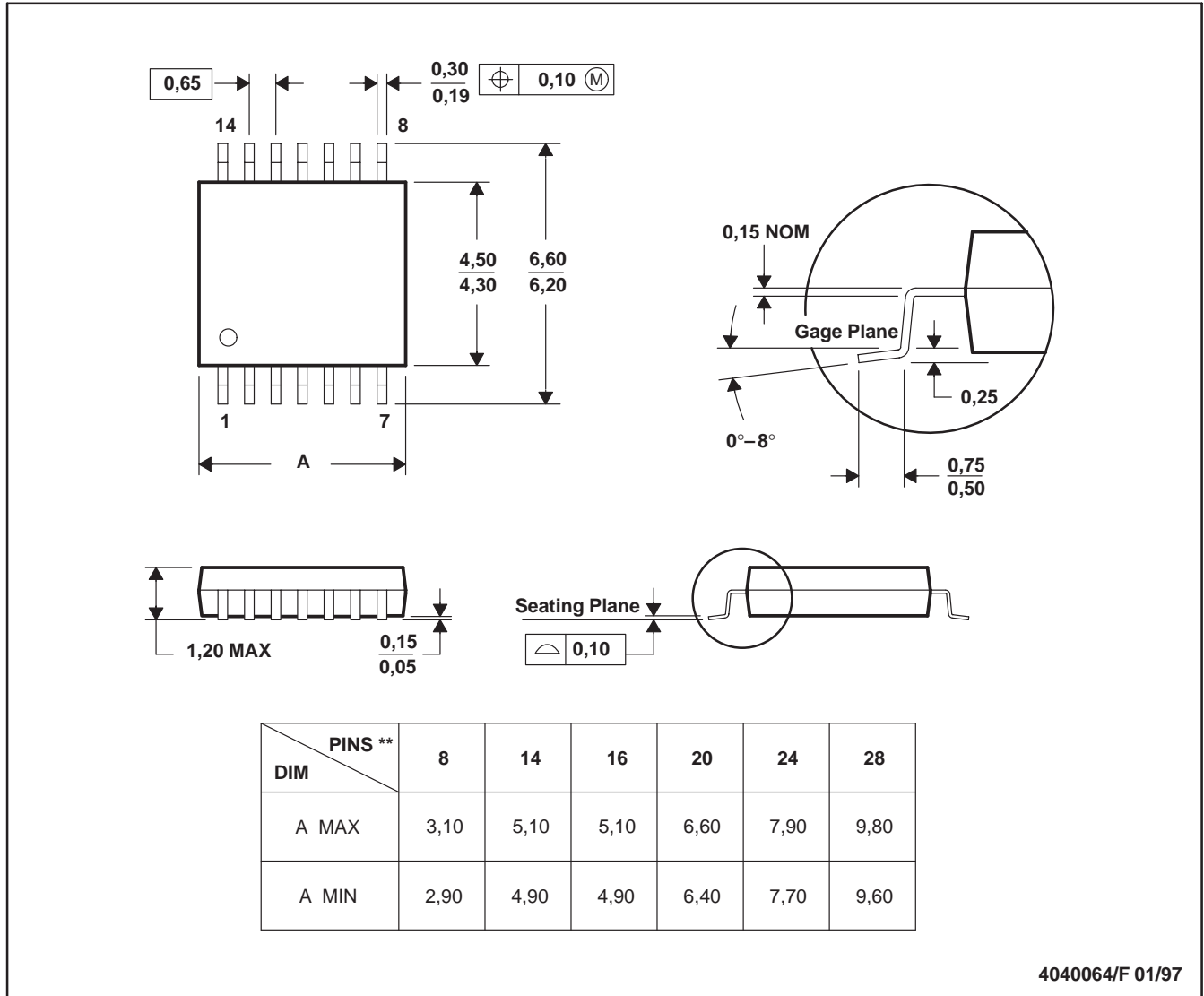
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - $\triangle D$  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - $\triangle E$  Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.



PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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