

# CY54FCT827T, CY74FCT827T 10-BIT BUFFERS WITH 3-STATE OUTPUTS

SCCS034A – SEPTEMBER 1994 – REVISED OCTOBER 2001

查询"CY74FCT827CTSOCT"供应商

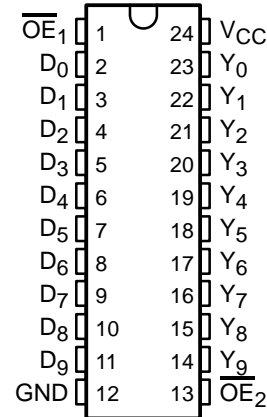
- Function, Pinout, and Drive Compatible With FCT, F, and AM29827 Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- 3-State Outputs
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT827T
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT827T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current

## description

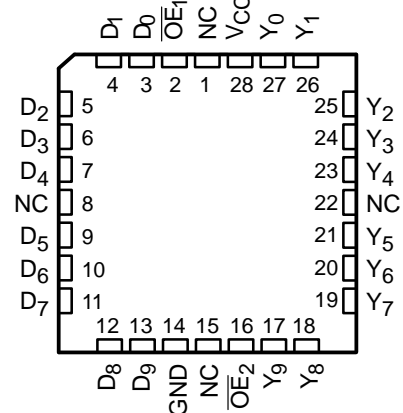
The 'FCT827T devices are 10-bit bus drivers that provide high-performance bus-interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NANDed output enables for maximum control flexibility. The 'FCT827T devices are designed for high-capacitance-load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All outputs are designed for low-capacitance bus loading in the high-impedance state.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

CY74FCT827T . . . Q OR SO PACKAGE  
(TOP VIEW)



CY74FCT827T . . . L PACKAGE  
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# CY54FCT827T, CY74FCT827T

## 10-BIT BUFFERS

### WITH 3-STATE OUTPUTS

SCCS 44116 REVISED OCTOBER 2001  
 零件 CY54FCT827CTSOCT 供規

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	QSOP – Q	Tape and reel	4.4	CY74FCT827CTQCT	FCT827C	
	SOIC – SO	Tube	4.4	CY74FCT827CTSOC	FCT827C	
		Tape and reel	4.4	CY74FCT827CTSOCT		
	-40°C to 85°C	QSOP – Q	Tape and reel	8	CY74FCT827ATQCT	FCT827A
		SOIC – SO	Tube	8	CY74FCT827ATSOC	FCT827A
			Tape and reel	8	CY74FCT827ATSOCT	
-55°C to 125°C	LCC – L	Tube	9	CY54FCT827ATLMB		

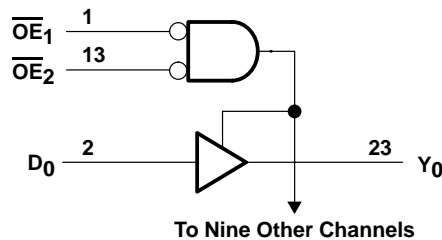
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### FUNCTION TABLE

INPUTS			OUTPUT Y	FUNCTION
$\overline{OE}_1$	$\overline{OE}_2$	D		
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	3-state
X	H	X	Z	

H = High logic level, L = Low logic level, X = Don't care, Z = High-impedance state

#### Logic diagram (positive logic)



Pin numbers shown are for the Q and SO packages.

#### absolute maximum rating over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range to ground potential	-0.5 V to 7 V
DC input voltage range	-0.5 V to 7 V
DC output voltage range	-0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package	61°C/W
SO package	46°C/W
Ambient temperature range with power applied, T <sub>A</sub>	-65°C to 135°C
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.



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**recommended operating conditions (see Note 2)**

		CY54FCT827T			CY74FCT827T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			V
I <sub>OH</sub>	High-level output current				-12			mA
I <sub>OL</sub>	Low-level output current				32			mA
T <sub>A</sub>	Operating free-air temperature	-55			125			°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		CY54FCT827T			CY74FCT827T			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>IN</sub> = -18 mA	-0.7			-1.2			V
	V <sub>CC</sub> = 4.75 V,	I <sub>IN</sub> = -18 mA				-0.7			
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -12 mA	2.4	3.3					V
	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -32 mA				2			
		I <sub>OH</sub> = -15 mA				2.4			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 32 mA	0.3			0.55			V
	V <sub>CC</sub> = 4.75 V,	I <sub>OL</sub> = 64 mA				0.3			
V <sub>hys</sub>	All inputs		0.2			0.2			V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>IN</sub> = V <sub>CC</sub>	5						μA
	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = V <sub>CC</sub>				5			
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>IN</sub> = 2.7 V				±1			μA
	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = 2.7 V				±1			
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>IN</sub> = 0.5 V				±1			μA
	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = 0.5 V				±1			
I <sub>ozH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>OUT</sub> = 2.7 V	10						μA
	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 2.7 V				10			
I <sub>ozL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>OUT</sub> = 0.5 V	-10						μA
	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 0.5 V				-10			
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V,	V <sub>OUT</sub> = 0 V	-60	-120	-225				mA
	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 0 V				-60	-120	-225	
I <sub>off</sub>	V <sub>CC</sub> = 0 V,	V <sub>OUT</sub> = 4.5 V	±1			±1			μA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.1			0.2			mA
	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.1			
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open		0.5			2			mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open					0.5			

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND



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SCCS 441167 (REV. 10/97) (REV. 10/97)  
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS		CY54FCT827T		CY74FCT827T		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
I <sub>CCD</sub> †	V <sub>CC</sub> = 5.5 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2 = \text{GND}$ , V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V		0.06	0.12			mA/MHz	
	V <sub>CC</sub> = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2 = \text{GND}$ , V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.06	0.12		
I <sub>C</sub> #	V <sub>CC</sub> = 5.5 V, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2 = \text{GND}$	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.7	1.4		mA	
			V <sub>IN</sub> = 3.4 V or GND	1	2.4			
		10 bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	1.6	3.2			
			V <sub>IN</sub> = 3.4 V or GND	4.1	13.2			
	V <sub>CC</sub> = 5.25 V, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2 = \text{GND}$	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V			0.7		1.4
			V <sub>IN</sub> = 3.4 V or GND			1		2.4
10 bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				1.6	3.2		
	V <sub>IN</sub> = 3.4 V or GND				4.1	13.2		
C <sub>i</sub>			5	10	5	10	pF	
C <sub>o</sub>			9	12	9	12	pF	

† This parameter is derived for use in total power-supply calculations.

$$\# I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$$

Where:

I<sub>C</sub> = Total supply current

I<sub>CC</sub> = Power-supply current with CMOS input levels

ΔI<sub>CC</sub> = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)

D<sub>H</sub> = Duty cycle for TTL inputs high

N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.



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**switching characteristics over operating free-air temperature range (see Figure 1)**

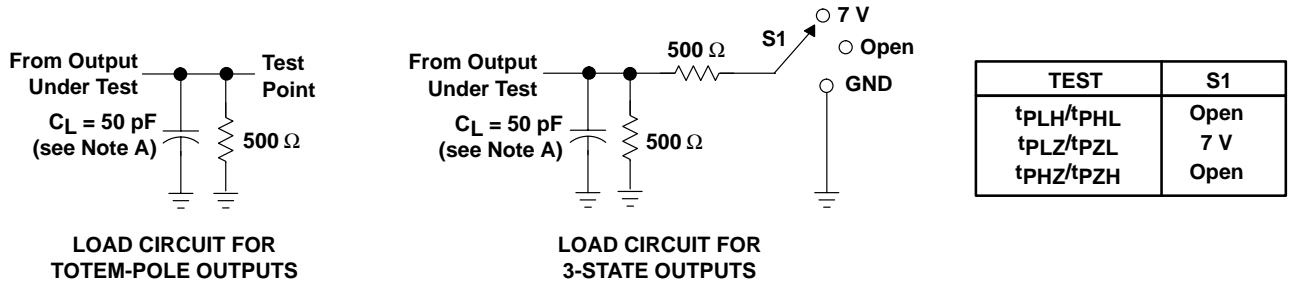
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY54FCT827AT		CY74FCT827AT		CY74FCT827CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	9	1.5	8	1.5	4.4	ns
t <sub>PHL</sub>				1.5	9	1.5	8	1.5	4.4	
t <sub>PLH</sub>	D	Y	C <sub>L</sub> = 300 pF, R <sub>L</sub> = 500 Ω	1.5	17	1.5	15	1.5	10	ns
t <sub>PHL</sub>				1.5	17	1.5	15	1.5	10	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	13	1.5	12	1.5	7	ns
t <sub>PZL</sub>				1.5	13	1.5	12	1.5	7	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 300 pF, R <sub>L</sub> = 500 Ω	1.5	25	1.5	23	1.5	14	ns
t <sub>PZL</sub>				1.5	25	1.5	23	1.5	14	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 500 Ω	1.5	9	1.5	9	1.5	5.7	ns
t <sub>PHL</sub>				1.5	9	1.5	9	1.5	5.7	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	10	1.5	10	1.5	6	ns
t <sub>PHL</sub>				1.5	10	1.5	10	1.5	6	



# CY54FCT827T, CY74FCT827T 10-BIT BUFFERS WITH 3-STATE OUTPUTS

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資料 CY54FCT827C/SCT 供電

## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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Texas Instruments  
Post Office Box 655303  
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