

April 1988 Revised September 2000

74F11

Triple 3-Input AND Gate

General Description

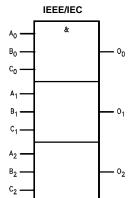
This device contains three independent gates, each of which performs the logic AND function.

Ordering Code:

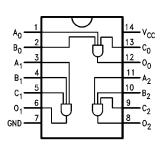
Order Number	Package Number	Package Description					
74F11SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow					
74F11SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide					
74F11PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide					

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}	
A_n, B_n, C_n	Inputs	1.0/1.0	20 μA/-0.6 mA	
O_n	Outputs	50/33.3	-1 mA/20 mA	

Absolute Maximum Ratings(Note 1)

-65°C to +150°C Storage Temperature -55°C to +125°C Ambient Temperature under Bias

Junction Temperature under Bias -55°C to +150°C V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V Input Voltage (Note 2) -0.5V to +7.0VInput Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output 3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature 0°C to +70°C Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device -0.5 V to V_{CC} may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

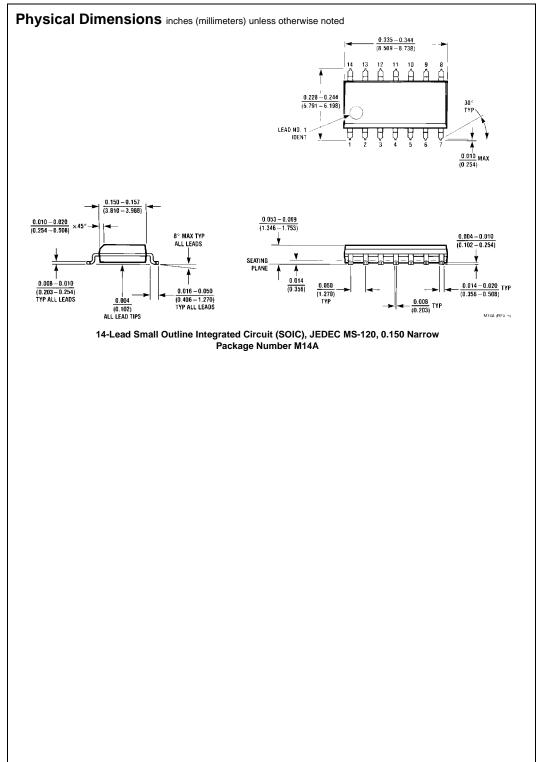
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

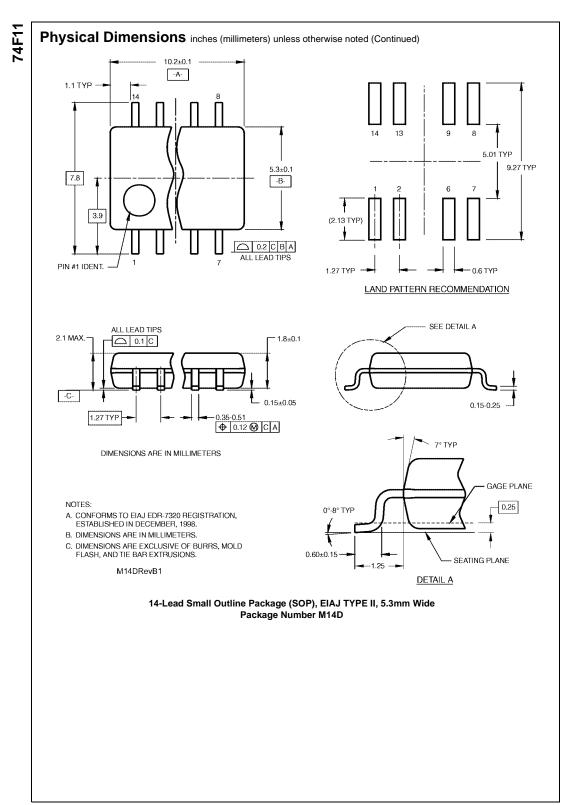
DC Electrical Characteristics

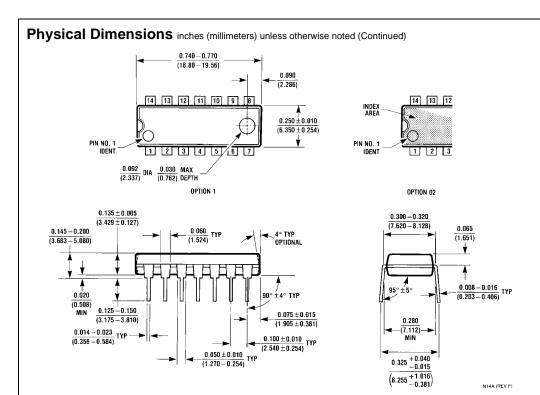
Symbol	Parameter Input HIGH Voltage		Min	Тур	Max	Units	V _{CC}	Conditions	
V _{IH}			2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH 10	0% V _{CC}	2.5			V	Min	I _{OH} = -1 mA	
	Voltage	5% V _{CC}	2.7					$I_{OH} = -1 \text{ mA}$	
V _{OL}	· ·	0% V _{CC}			0.5	V	Min	I _{OL} = 20 mA	
	Voltage					-		10L 20 1171	
I _{IH}	Input HIGH				5.0	μА	Max	V _{IN} = 2.7V	
	Current					μ		TIN	
I _{BVI}	Input HIGH Current	t HIGH Current			7.0	μА	Max	V _{IN} = 7.0V	
	Breakdown Test				7.0	μΛ	IVIGA	1 IN 7.0 V	
I _{CEX}	Output HIGH				50	μА	Max	V _{OUT} = V _{CC}	
	Leakage Current				30	μΛ	IVIAX	v001 − vCC	
V _{ID}	Input Leakage Test		4.75			V	0.0	I _{ID} = 1.9 μA	
								All other pins grounded	
I _{OD}	Output Leakage Circuit Current			3.75	3.75	μА	0.0	V _{IOD} = 150 mV	
					3.73			All other pins grounded	
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V	
Ios	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V	
I _{CCH}	Power Supply Current			4.1	6.2	mA	Max	V _O = HIGH	
I _{CCL}	Power Supply Current			6.5	9.7	mA	Max	$V_O = LOW$	

AC Electrical Characteristics

	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			T _A −55°C	to +125°C	$T_A = 0$ °C to +70°C			
Symbol					$V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		V _{CC} = +5.0V C _L = 50 pF		Units	
		Min	Тур	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay	3.0	4.2	5.6	2.5	7.5	3.0	6.6	ns	
t _{PHL}	A_n , B_n , C_n to O_n	2.5	4.1	5.5	2.0	7.5	2.5	6.5	115	







14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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