14-Bit, 2500 MSPS, RF Digital-to-Analog Converter

AD9739

FEATURES

- Dynamic performance
  - DOCSIS 3.0 performance
    - 8 QAM carriers @ 400 MHz IF: −71 dBc
    - 16 QAM carriers @ 400 MHz IF: −68 dBc
    - 32 QAM carriers @ 400 MHz IF: −65 dBc
    - 72 QAM carriers @ 600 MHz IF: −61 dBc
  - Single-carrier WCDMA ACLR performance @ 2457.6 MSPS
    - f_{OUT} = 350 MHz (normal mode)
      - 1st adjacent channel: −80 dBc
      - 5th adjacent channel: −80.5 dBc
    - f_{OUT} = 2100 MHz (mix mode)
      - 1st adjacent channel: −69 dBc
      - 5th adjacent channel: −75 dBc
  - Single-tone NSD performance @ 2.4 GSPS
    - −166 dBm/Hz @ 100 MHz IF
    - −162 dBm/Hz @ 1 GHz IF
- RF synthesis support
  - FS mix, RZ modes
- Dual-port LVDS data interface with on-chip 100 Ω terminations
- Low power: 1.1 W @ 2.5 GSPS

APPLICATIONS

- Broadband communications systems
  - CMTS/VOD
- Cellular infrastructure
- Point-to-point wireless
- Instrumentation, automatic test equipment
- Radar, avionics

GENERAL DESCRIPTION

The AD9739 is a high performance, high frequency 14-bit DAC that provides sample rates up to 2500 MSPS, permitting multicarrier generation up to the Nyquist frequency in baseband mode and second and third Nyquist zones in mix mode. It includes a serial peripheral interface (SPI) for configuration and readback of status registers. A dual-port LVDS interface is used to enable the high sample rate with existing FGPA/ASIC technology. The output current can be programmed over a range of 8.66 mA to 31.66 mA. The AD9739 is manufactured on a 0.18 µm CMOS process and operates from 1.8 V and 3.3 V supplies. It is supplied in a 160-ball chip scale ball grid array for reduced package parasitics.

FUNCTIONAL BLOCK DIAGRAM

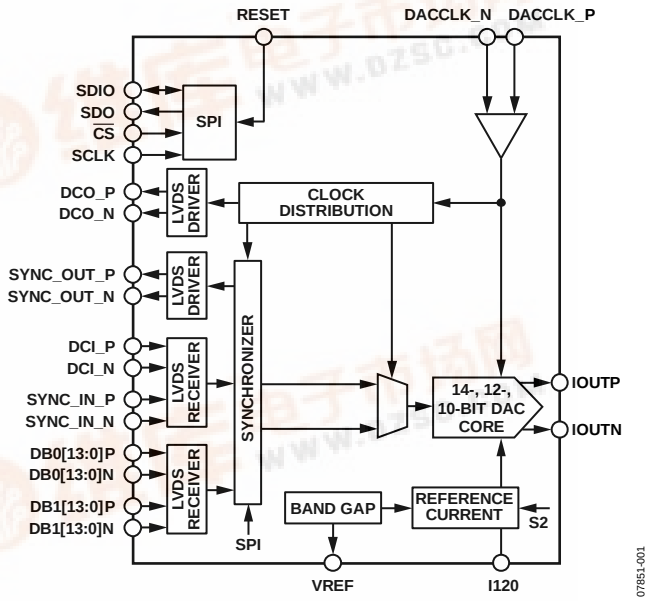

Figure 1.

PRODUCT HIGHLIGHTS

1. Low noise and intermodulation distortion (IMD) performance enable high quality synthesis of wideband signals up to 1 GHz.
2. A dual-port interface with double data rate (DDR) LVDS data receivers supports the maximum conversion rate of 2500 MSPS.
3. Manufactured on a CMOS process, the AD9739 uses a proprietary switching technique that enhances dynamic performance.
4. The current output(s) of the AD9739 are easily configured for single-ended or differential circuit topologies.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

1/09—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{FS} = 20 mA.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		14		Bits
ACCURACY				
Integral Nonlinearity (INL)		±1.3		LSB
Differential Nonlinearity (DNL)		±0.8		LSB
ANALOG OUTPUTS				
Gain Error (with Internal Reference)		5.5		%
Full-Scale Output Current	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	V
Output Resistance		10		MΩ
Output Capacitance		1		pF
TEMPERATURE DRIFT				
Gain		60		ppm/°C
Reference Voltage		20		ppm/°C
REFERENCE				
Internal Reference Voltage		1.2		V
Output Resistance[1]		5		kΩ
ANALOG SUPPLY VOLTAGES				
VDDA	3.1	3.3	3.5	V
VDDC	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES				
VDD33	3.10	3.3	3.5	V
VDD	1.70	1.8	1.90	V
SUPPLY CURRENTS AND POWER DISSIPATION 2.0 GSPS				
I_{VDDA}		37	38	mA
I_{VDDC}		159	166	mA
I_{VDD33}		34	37	mA
I_{VDD}		233	238	mA
Power Dissipation		0.940	0.975	W
Sleep Mode				
I_{VDDA}		2.5	2.75	mA
Power-Down Mode[2]				
I_{VDDA}		0.02	0.135	mA
I_{VDDC}		3.8		mA
I_{VDD33}		0.5	1.3	mA
I_{VDD}		0.1	2.75	mA
SUPPLY CURRENTS AND POWER DISSIPATION 2.5 GSPS				
I_{VDDA}		37		mA
I_{VDDC}		223		mA
I_{VDD33}		34		mA
I_{VDD}		290		mA
Power Dissipation		1.16		W

[1] Use an external amplifier to drive any external load.
[2] All power-down bits set (Register 0x01, Bit 0, Bit 1, Bit 4, Bit 5; Register 0x02, Bit 3).

DIGITAL SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{FS} = 20 mA. LVDS drivers and receivers are compliant to the IEEE-1596 reduced range link, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
LVDS DATA INPUTS				
(DB0[13:0]P, DB0[13:0]N, DB1[13:0]P, DB1[13:0]N) DB+ = V_{IA}, DB−= V_{IB}				
Input Voltage Range, V_{IA} or V_{IB}	825		1575	mV
Input Differential Threshold, V_{IDTH}	−100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$		20		mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
LVDS Input Rate	1250			MSPS
LVDS Minimum Data Valid Period (t_{MDE})			344	ps
Input Capacitance		1.2		pF
LVDS CLOCK INPUT				
(DCI_P, DCI_N) DCI_P = V_{IA}, DCI_N = V_{IB}				
Input Voltage Range, V_{IA} or V_{IB}	825		1575	mV
Input Differential Threshold, V_{IDTH}	−100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$		20		mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
Maximum Clock Rate	625			MHz
LVDS CLOCK OUTPUT				
(DCO_P, DCO_N) DCO_P = V_{OA}, DCO_N = V_{OB} 100 Ω Termination				
Output Voltage High, V_{OA} or V_{OB}			1375	mV
Output Voltage Low, V_{OA} or V_{OB}	1025			mV
Output Differential Voltage, $\|V_{OD}\|$	150	200	250	mV
Output Offset Voltage, V_{OS}	1150		1250	mV
Output Impedance, Single-Ended, R_O	40	100	140	Ω
R_O Mismatch Between A and B, ΔRO			10	%
Change in $\|V_{OD}\|$ Between 0 and 1, $\|\Delta V_{OD}\|$			25	mV
Change in V_{OS} Between 0 and 1, ΔV_{OS}			25	mV
Output Current, Driver Shorted to Ground, I_{SA}, I_{SB}			20	mA
Output Current, Drivers Shorted Together, I_{SAB}			4	mA
Power-Off Output Leakage, $\|I_{XA}\|$, $\|I_{XB}\|$			10	mA
Maximum Clock Rate	625			MHz
DAC CLOCK INPUT (DACCLK_P, DACCLK_N)				
Differential Peak-to-Peak Voltage		1.8		V
Common-Mode Voltage		900		mV
Maximum Clock Rate				
VDD = 1.8 V ± 5%	800		2400	MSPS
VDD = 1.89 V ± 5%	800		2500	MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (f_{SCLK}, $1/t_{SCLK}$)			20	MHz
Minimum Pulse Width High, t_{PWH}	20			ns
Minimum Pulse Width Low, t_{PWL}	20			ns
Minimum SDIO and $\overline{CS}$ to SCLK Setup, t_{DS}		10		ns
Minimum SCLK to SDIO Hold, t_{DH}		5		ns
Maximum SCLK to Valid SDIO and SDO, t_{DV}		20		ns
Minimum SCLK to Invalid SDIO and SDO, t_{DNV}		5		ns

Parameter	Min	Typ	Max	Unit
INPUTS (SDI, SDIO, SCLK, $\overline{CS}$)				
Voltage in High, V_{IH}	2.0	3.3		V
Voltage in Low, V_{IL}		0	0.8	V
Current in High, I_{IH}	−10		+10	µA
Current in Low, I_{IL}	−10		+10	µA
SDIO Output				
Voltage Out High, V_{OH}	2.4		3.6	V
Voltage Out Low, V_{OL}	0		0.4	V
Current Out High, I_{OH}		4		mA
Current Out Low, I_{OL}		4		mA

AC SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{FS} = 20 mA.

Table 3.

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum Update Rate	800		2500	MSPS
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 1200 MSPS				
f_{OUT} = 100 MHz		72		dBc
f_{OUT} = 350 MHz		69		dBc
f_{OUT} = 550 MHz		60		dBc
f_{DAC} = 2000 MSPS				
f_{OUT} = 70 MHz		76		dBc
f_{OUT} = 100 MHz		70.5		dBc
f_{OUT} = 350 MHz		61.5		dBc
f_{OUT} = 550 MHz		61.5		dBc
f_{OUT} = 850 MHz		59		dBc
f_{DAC} = 2400 MSPS				
f_{OUT} = 100 MHz		69.5		dBc
f_{OUT} = 350 MHz		58.5		dBc
f_{OUT} = 550 MHz		54		dBc
f_{OUT} = 950 MHz		60		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 1200 MSPS, $f_{OUT2} = f_{OUT1}$ + 1.25 MHz				
f_{OUT} = 100 MHz		92		dBc
f_{OUT} = 350 MHz		90		dBc
f_{OUT} = 550 MHz		81		dBc
f_{DAC} = 2000 MSPS, $f_{OUT2} = f_{OUT1}$ + 1.25 MHz				
f_{OUT} = 100 MHz		93		dBc
f_{OUT} = 350 MHz		74		dBc
f_{OUT} = 550 MHz		71		dBc
f_{OUT} = 850 MHz		67.5		dBc
f_{DAC} = 2400 MSPS				
f_{OUT} = 100 MHz		94		dBc
f_{OUT} = 350 MHz		78		dBc
f_{OUT} = 550 MHz		72		dBc
f_{OUT} = 950 MHz		68		dBc

Parameter	Min	Typ	Max	Unit
NOISE SPECTRAL DENSITY (NSD)				
Single Tone, f_{DAC} = 2400 MSPS				
f_{OUT} = 100 MHz		−166		dBm/Hz
f_{OUT} = 350MHz		−161		dBm/Hz
f_{OUT} = 550 MHz		−160		dBm/Hz
f_{OUT} = 850 MHz		−160		dBm/Hz
Eight-Tone, f_{DAC} = 2400 MSPS, 500 kHz Tone Spacing				
f_{OUT} = 100 MHz		−168		dBm/Hz
f_{OUT} = 350 MHz		−166		dBm/Hz
f_{OUT} = 550 MHz		−166		dBm/Hz
f_{OUT} = 850 MHz		−165		dBm/Hz
WCDMA Adjacent Channel Leakage Ratio (ACLR), Single Carrier				
f_{DAC} = 2457.6 MSPS, f_{OUT} = 150 MHz		80.5		dBc
f_{DAC} = 2457.6 MSPS f_{OUT} = 350 MHz		80		dBc
f_{DAC}= 2457.6 MSPS, f_{OUT} = 550 MHz		79		dBc
f_{DAC}= 2457.6 MSPS, f_{OUT} = 950 MHz		78		dBc
WCDMA Second ACLR, Single Carrier				
f_{DAC} = 2457.6 MSPS, f_{OUT} = 150 MHz		84		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 350 MHz		80		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 550 MHz		80		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 950 MHz		79		dBc
WCDMA ACLR, Single Carrier (Mix Mode Second Nyquist Zone)				
f_{DAC} = 2457.6 MSPS, f_{OUT} = 1300 MHz		73.5		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 1700 MHz		73.5		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2100 MHz		69		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2400 MHz		68		dBc
WCDMA Second ACLR, Single Carrier (Mix Mode Second Nyquist Zone)				
f_{DAC} = 2457.6 MSPS, f_{OUT} = 1300 MHz		74.5		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 1700 MHz		74		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2100 MHz		72		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2400 MHz		71		dBc
WCDMA ACLR, Single Carrier (Mix Mode Third Nyquist Zone)				
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2500 MHz		68		dBc
f_{DAC} = 2457. MSPS, f_{OUT} = 2800 MHz		66		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 3200 MHz		66		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 3600 MHz		64		dBc
WCDMA ACLR, Single Carrier (Mix Mode Third Nyquist Zone)				
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2500 MHz		70		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2800 MHz		67		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 3200 MHz		67		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 3600 MHz		64.5		dBc

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect To	Rating
VDDA	VSSA	−0.3 V to +3.6 V
VDD33	VSS	−0.3 V to +3.6 V
VDD	VSS	−0.3 V to +1.98 V
VDDC	VSSC	−0.3 V to +1.98 V
VSSA	VSS	−0.3 V to +0.3 V
VSSA	VSSC	−0.3 V to +0.3 V
VSS	VSSC	−0.3 V to +0.3 V
DACCLK_P, DACCLK_N	VSSC	−0.3 V to CVDD18 + 0.18 V
DCI, DCO	VSS	−0.3 V to DVDD33 + 0.3 V
LVDS Data Inputs	VSS	−0.3 V to DVDD33 + 0.3 V
IOUTP, IOUTN	VSSA	−1.0 V to AVDD33 + 0.3 V
I120, VREF, IPTAT	VSSA	−0.3 V to AVDD33 + 0.3 V
IRQ, $\overline{CS}$, SCLK, SDO, SDIO, RESET	VSS	−0.3 V to DVDD33 + 0.3 V
Junction Temperature		150°C
Storage Temperature		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
160-Ball CSP_BGA	31.2	7.0	°C/W[1]

[1] With no airflow movement.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

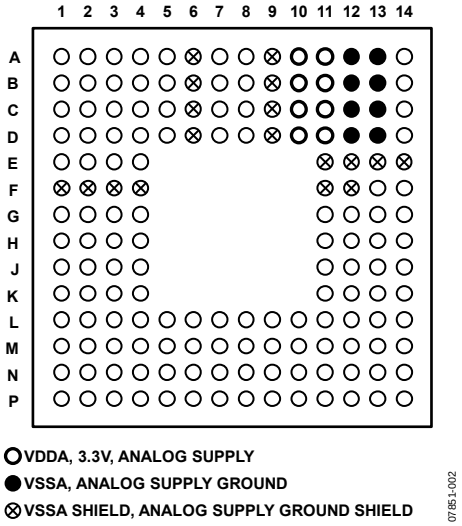


Figure 2. Analog Supply Pins (Top View)

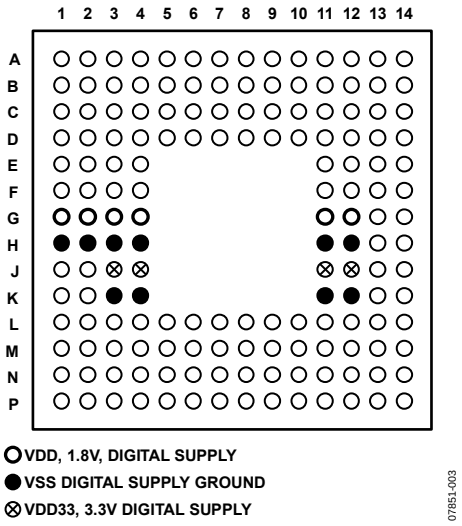


Figure 3. Digital Supply Pins (Top View)

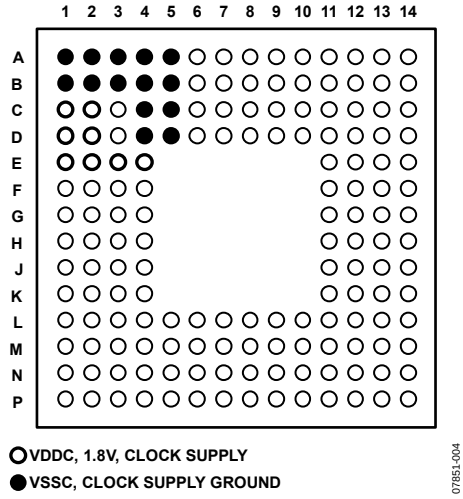


Figure 4. Digital LVDS Clock Supply Pins (Top View)

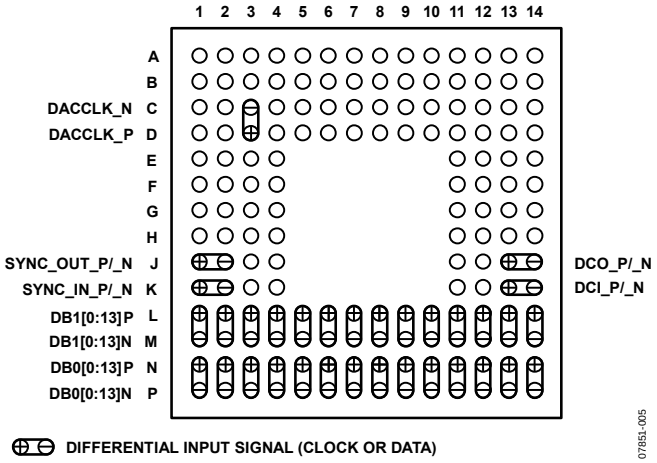


Figure 5. Digital LVDS Input, Clock I/O (Top View)

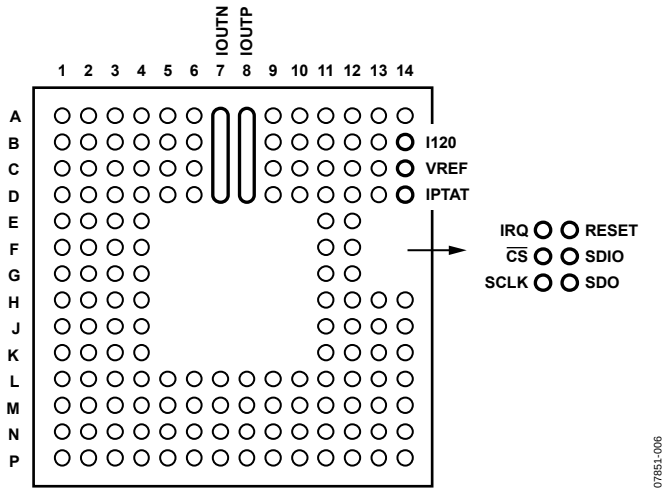


Figure 6. Analog I/O and SPI Control Pins (Top View)

Table 6. AD9739 Pin Function Descriptions

Pin No.	Mnemonic	Description
C1, C2, D1, D2, E1, E2, E3, E4	VDDC	1.8 V Clock Supply.
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C4, C5, D4, D5	VSSC	Clock Supply Ground.
A10, A11, B10, B11, C10, C11, D10, D11	VDDA	3.3 V Analog Supply.
A12, A13, B12, B13, C12, C13, D12, D13,	VSSA	Analog Supply Ground.
A6, A9, B6, B9, C6, C9, D6, D9, F1, F2, F3, F4, E11, E12, E13, E14, F11, F12	VSSA Shield	Analog Supply Ground Shield. Tie to VSSA at the DAC.
A14	NC	No Connect
A7, B7, C7, D7	IOUTN	DAC Negative Output. 10 mA to 30 mA full-scale output current.
A8, B8, C8, D8	IOUTP	DAC Positive Output. 10 mA to 30 mA full-scale output current.
B14	I120	Nominal 1.2 V Reference. Tie to analog ground via a 10 kΩ resistor to generate a 120 µA reference current.
C14	VREF	Band Gap Voltage Reference I/O. Tie to analog ground via a 1 nF capacitor; output impedance is approximately 5 kΩ.
D14	IPTAT	Factory Test Pin. Output current, proportional to absolute temperature, is approximately 10 µA at 25°C with a slope of approximately 20 nA/°C.
C3, D3	DACCLK_N/DACCLK_P	Negative/Positive DAC Clock Input (DACCLK).
F13	IRQ	IRQ. Active low open-drain interrupt request output; pull up to DVDD33 with a 10 kΩ resistor.
F14	RESET	RESET. 1 resets the AD9739.
G13	$\overline{CS}$	See the Serial Peripheral Interface section for the pin description.
G14	SDIO	See the Serial Peripheral Interface section for the pin description.
H13	SCLK	See the Serial Peripheral Interface section for the pin description.
H14	SDO	See the Serial Peripheral Interface section for the pin description.
J3, J4, J11, J12	VDD33	3.3 V Digital Supply.
G1, G2, G3, G4, G11, G12	VDD	1.8 V Digital Supply.
H1, H2, H3, H4, H11, H12, K3, K4, K11, K12	VSS	Digital Supply Ground.
J1, J2	SYNC_OUT_P/SYNC_OUT_N	Positive/Negative SYNC Output (SYNC_OUT).[1]
K1, K2	SYNC_IN_P/SYNC_IN_N	Positive/Negative SYNC Input (SYNC_IN).[1]
J13, J14	DCO_P/DCO_N	Positive/Negative Data Output Clock (DCO).[1]
K13, K14	DCI_P/DCI_N	Positive/Negative Data Input Clock (DCI).[1]

Pin No.	Mnemonic	Description
L1, M1	DB1[0]P/DB1[0]N	Port 1 Positive/Negative Data Input Bit 0.[1]
L2, M2	DB1[1]P/DB1[1]N	Port 1 Positive/Negative Data Input Bit 1.[1]
L3, M3	DB1[2]P/DB1[2]N	Port 1 Positive/Negative Data Input Bit 2.[1]
L4, M4	DB1[3]P/DB1[3]N	Port 1 Positive/Negative Data Input Bit 3.[1]
L5, M5	DB1[4]P/DB1[4]N	Port 1 Positive/Negative Data Input Bit 4.[1]
L6, M6	DB1[5]P/DB1[5]N	Port 1 Positive/Negative Data Input Bit 5.[1]
L7, M7	DB1[6]P/DB1[6]N	Port 1 Positive/Negative Data Input Bit 6.[1]
L8, M8	DB1[7]P/DB1[7]N	Port 1 Positive/Negative Data Input Bit 7.[1]
L9, M9	DB1[8]P/DB1[8]N	Port 1 Positive/Negative Data Input Bit 8.[1]
L10, M10	DB1[9]P/DB1[9]N	Port 1 Positive/Negative Data Input Bit 9.[1]
L11, M11	DB1[10]P/DB1[10]N	Port 1 Positive/Negative Data Input Bit 10.[1]
L12, M12	DB1[11]P/DB1[11]N	Port 1 Positive/Negative Data Input Bit 11.[1]
L13, M13	DB1[12]P/DB1[12]N	Port 1 Positive/Negative Data Input Bit 12.[1]
L14, M14	DB1[13]P/DB1[13]N	Port 1 Positive/Negative Data Input Bit 13.[1]
N1, P1	DB0[0]P/DB0[0]N	Port 0 Positive/Negative Data Input Bit 0.[1]
N2, P2	DB0[1]P/DB0[1]N	Port 0 Positive/Negative Data Input Bit 1.[1]
N3, P3	DB0[2]P/DB0[2]N	Port 0 Positive/Negative Data Input Bit 2.[1]
N4, P4	DB0[3]P/DB0[3]N	Port 0 Positive/Negative Data Input Bit 3.[1]
N5, P5	DB0[4]P/DB0[4]N	Port 0 Positive/Negative Data Input Bit 4.[1]
N6, P6	DB0[5]P/DB0[5]N	Port 0 Positive/Negative Data Input Bit 5.[1]
N7, P7	DB0[6]P/DB0[6]N	Port 0 Positive/Negative Data Input Bit 6.[1]
N8, P8	DB0[7]P/DB0[7]N	Port 0 Positive/Negative Data Input Bit 7.[1]
N9, P9	DB0[8]P/DB0[8]N	Port 0 Positive/Negative Data Input Bit 8.[1]
N10, P10	DB0[9]P/DB0[9]N	Port 0 Positive/Negative Data Input Bit 9.[1]
N11, P11	DB0[10]P/DB0[10]N	Port 0 Positive/Negative Data Input Bit 10.[1]
N12, P12	DB0[11]P/DB0[11]N	Port 0 Positive/Negative Data Input Bit 11.[1]
N13, P13	DB0[12]P/DB0[12]N	Port 0 Positive/Negative Data Input Bit 12.[1]
N14, P14	DB0[13]P/DB0[13]N	Port 0 Positive/Negative Data Input Bit 13.[1]

[1] Conforms to IEEE-1596 reduced range link.

TYPICAL PERFORMANCE CHARACTERISTICS

STATIC LINEARITY

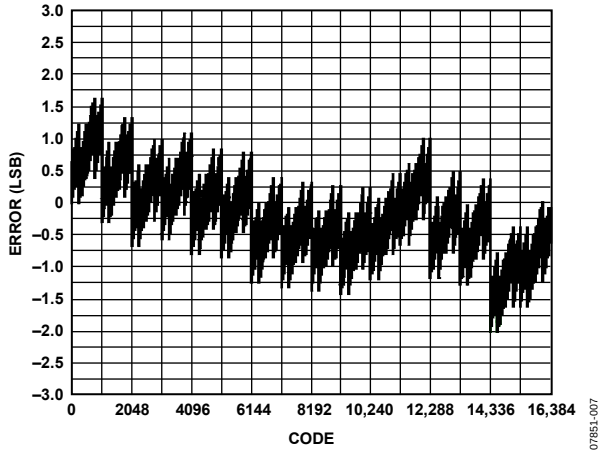


Figure 7. Typical INL, 20 mA @ 25°C

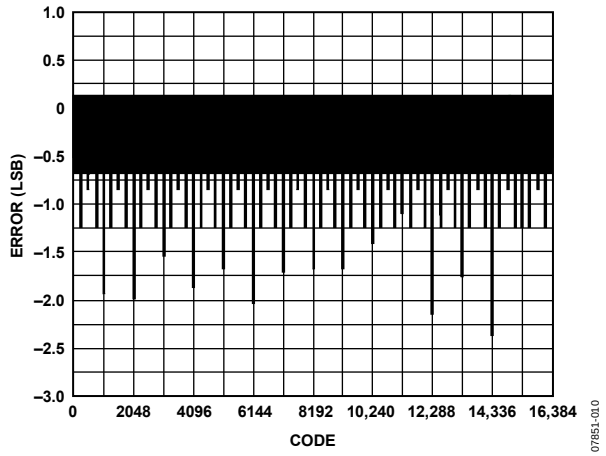


Figure 8. Typical DNL, 20 mA @ 25°C

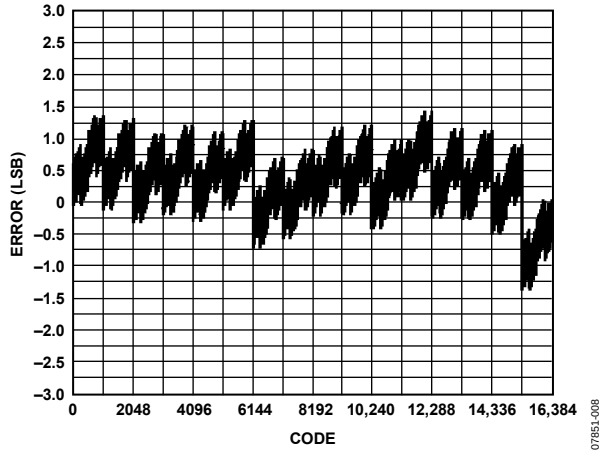


Figure 9. Typical INL, 20 mA @ −40°C

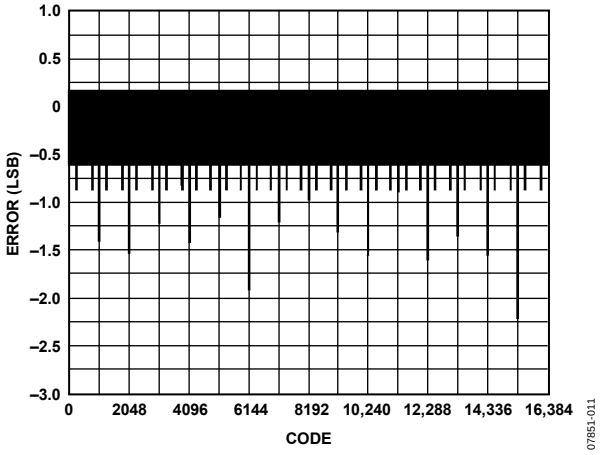


Figure 10. Typical DNL, 20 mA @ −40°C

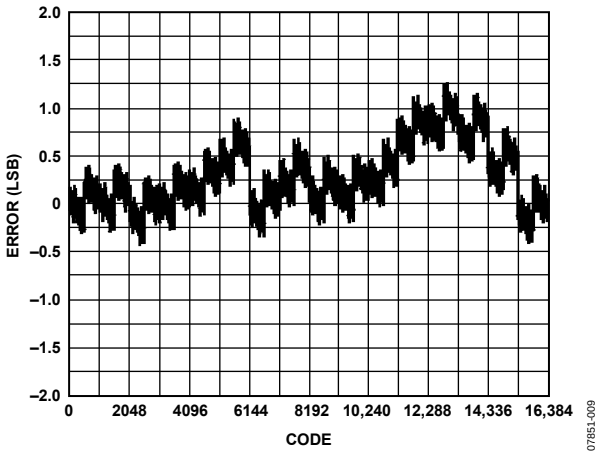


Figure 11. Typical INL, 20 mA @ 85°C

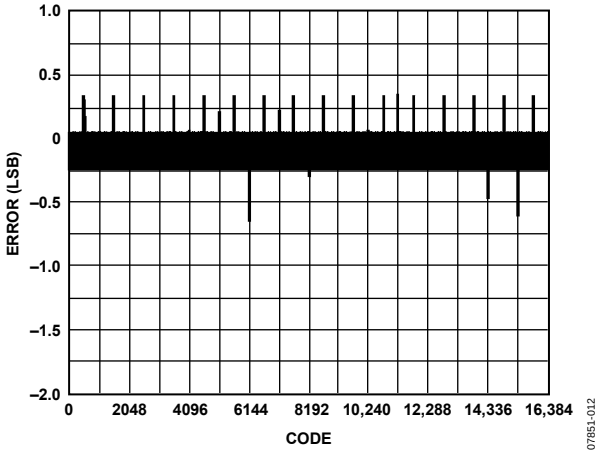


Figure 12. Typical DNL, 20 mA @ 85°C

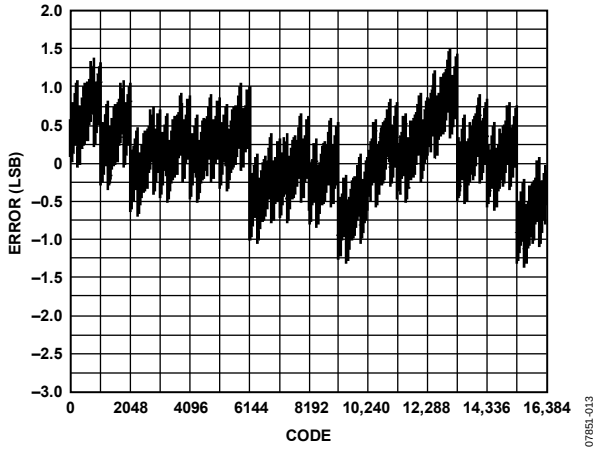


Figure 13. Typical INL, 10 mA @ 25°C

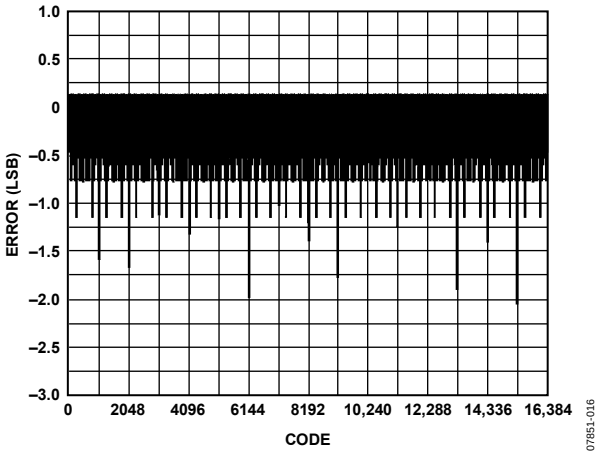


Figure 14. Typical DNL, 10 mA @ 25°C

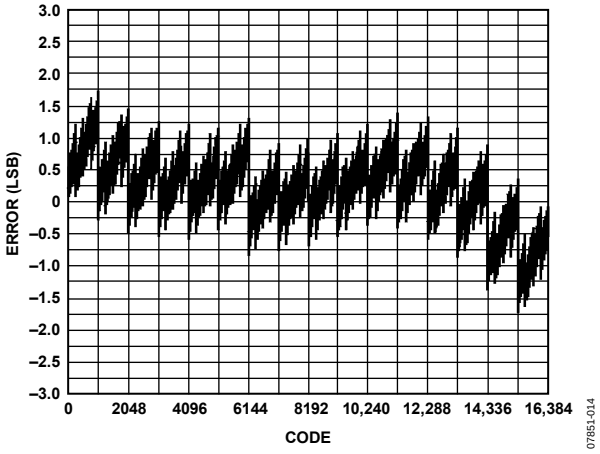


Figure 15. Typical INL, 30 mA @ 25°C

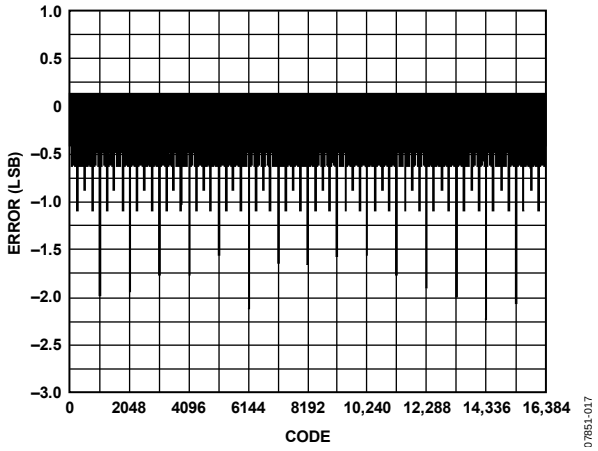


Figure 16. Typical DNL, 30 mA @ 25°C

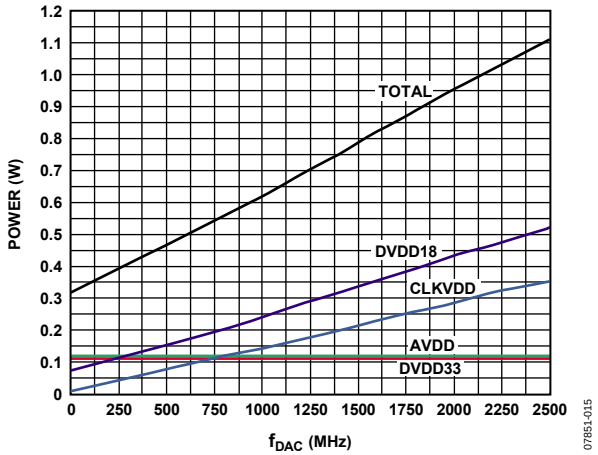


Figure 17. Power Consumption vs. f_{DAC} @ 25°C

DYNAMIC PERFORMANCE NORMAL MODE, 20 MA FULL SCALE (UNLESS OTHERWISE NOTED)

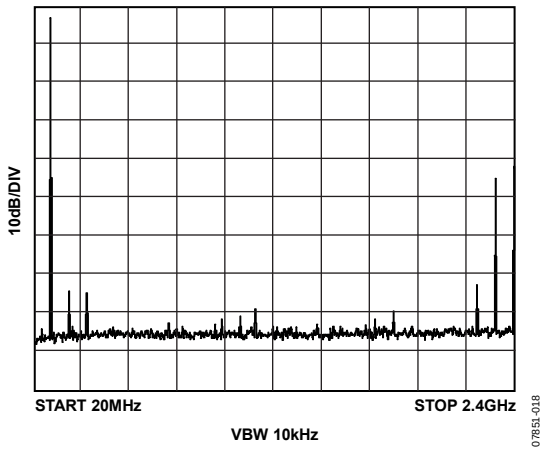


Figure 18. Single Tone Spectrum @ f_{OUT} = 91 MHz, f_{DAC} = 2.4 GSPS

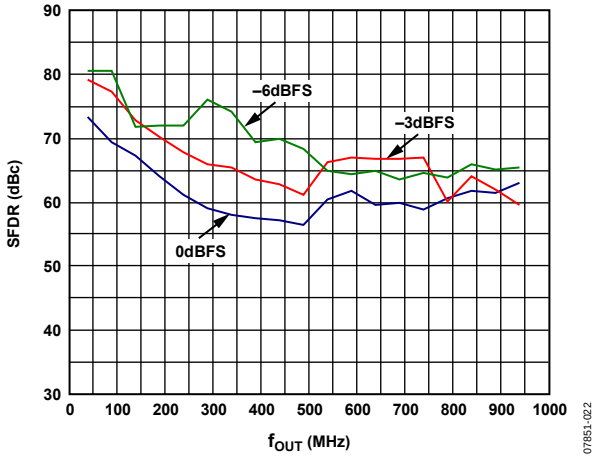


Figure 21. SFDR vs. f_{OUT} over DIGFS @ 2.0 GSPS

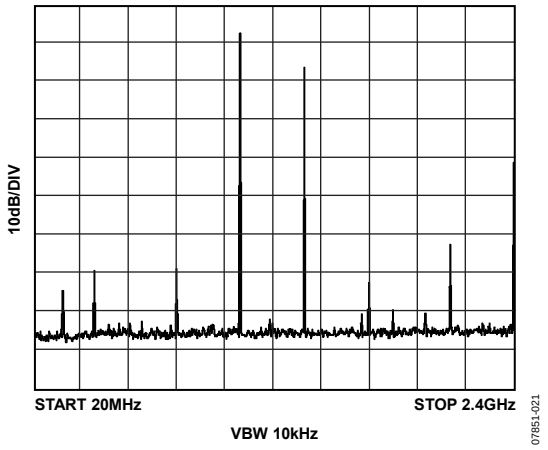


Figure 19. Single Tone Spectrum @ f_{OUT} = 1091 MHz, f_{DAC} = 2.4 GSPS

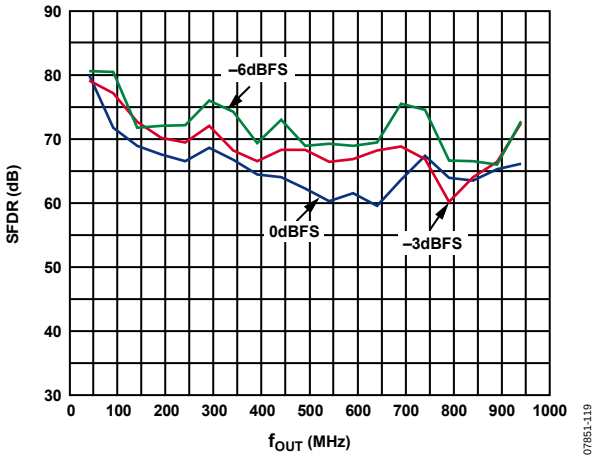


Figure 22. SFDR for Second Harmonic over f_{OUT} WRT DIGFS @ 2.0 GSPS

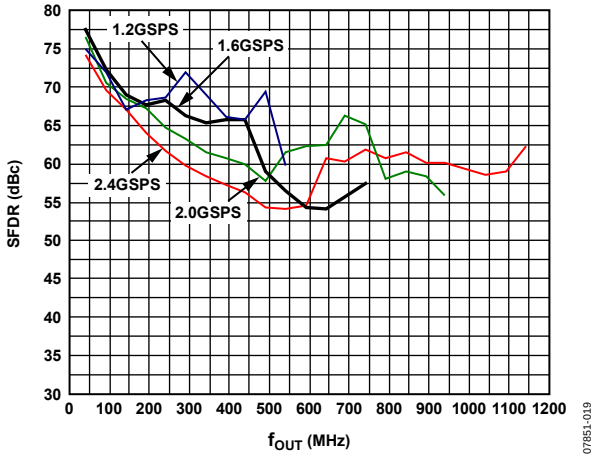


Figure 20. SFDR vs. f_{OUT} over f_{DAC}

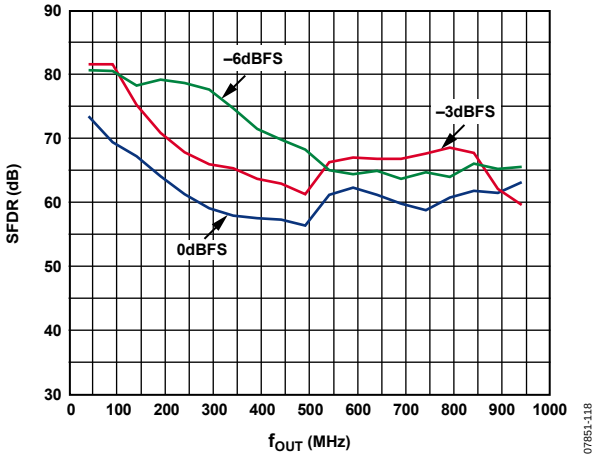


Figure 23. SFDR for Third Harmonic over f_{OUT} WRT DIGFS @ 2.0 GSPS

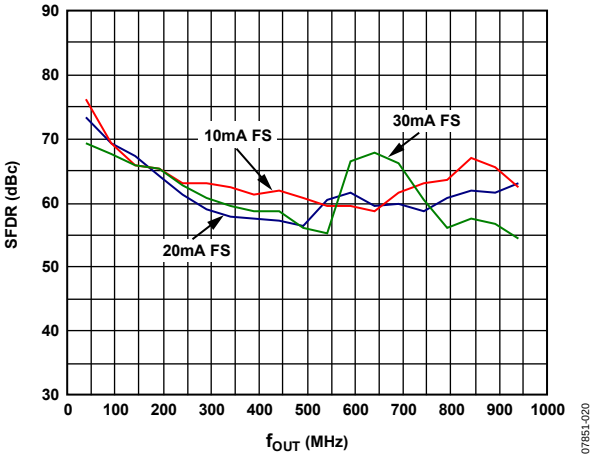


Figure 24. SFDR vs. f_{OUT} over ANAFS @ 2.0 GSPS

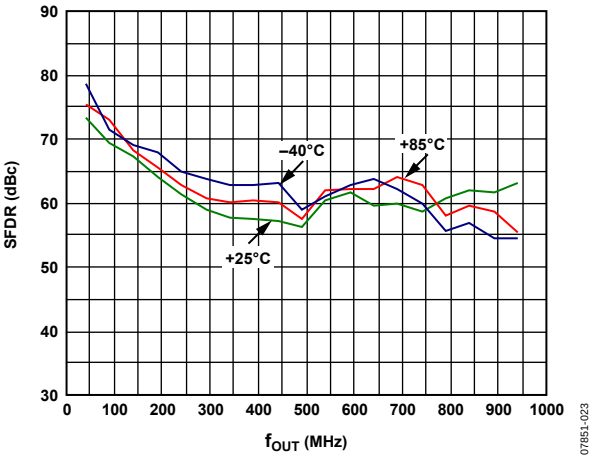


Figure 25. SFDR vs. f_{OUT} over Temperature @ 2.0 GSPS

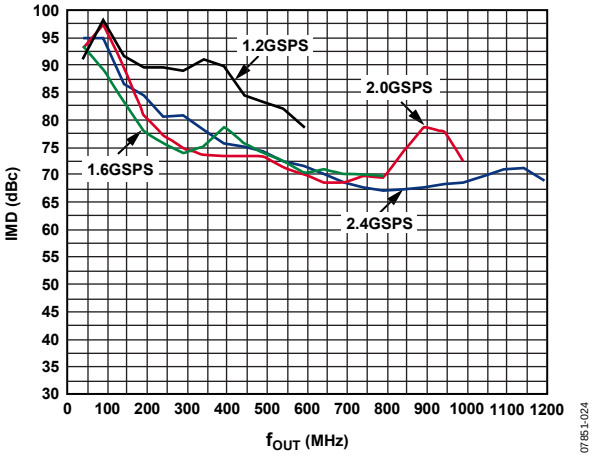


Figure 26. IMD vs. f_{OUT} over f_{DAC}

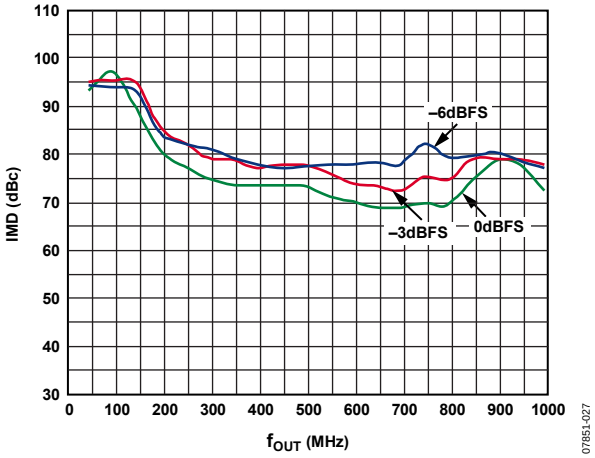


Figure 27. IMD vs. f_{OUT} over DIGFS @ 2.0 GSPS

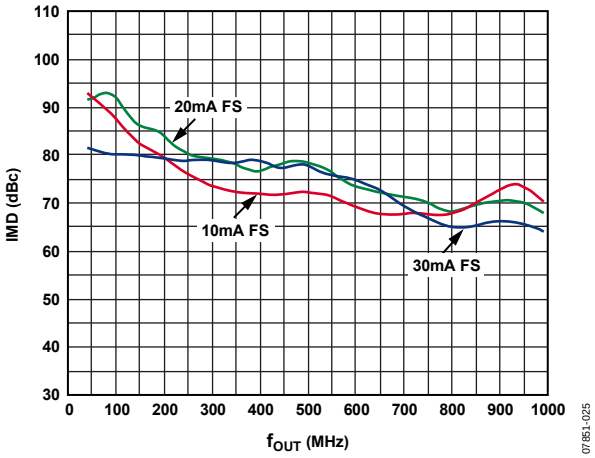


Figure 28. IMD vs. f_{OUT} over ANAFS @ 2.0 GSPS

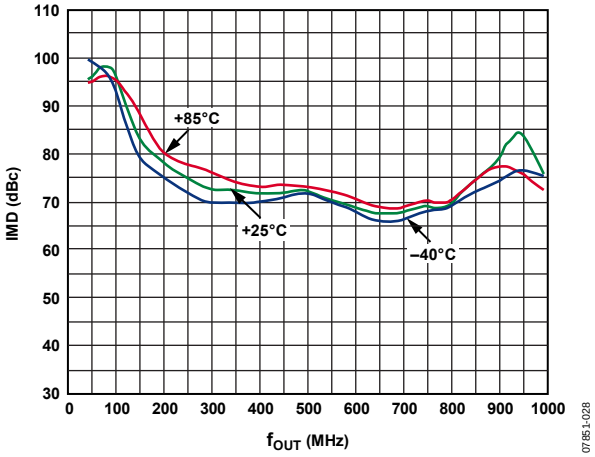


Figure 29. IMD vs. f_{OUT} over Temperature @ 2.0 GSPS

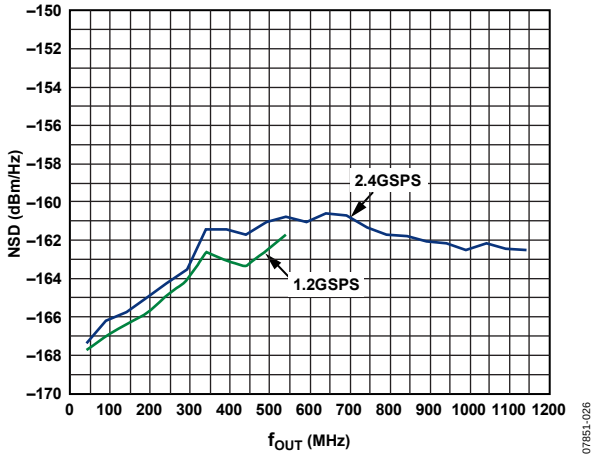


Figure 30. Single-Tone NSD vs. f_{OUT} over f_{DAC}

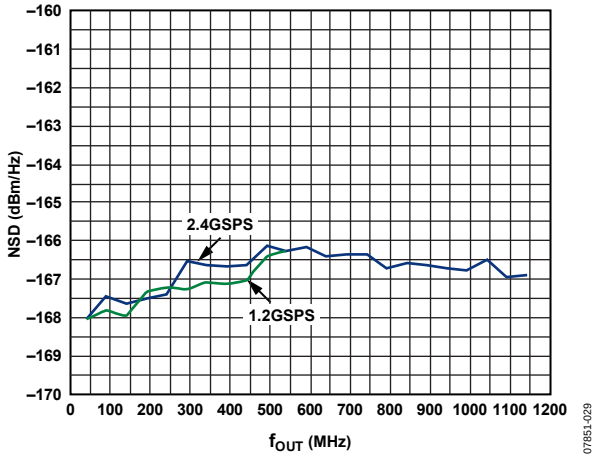


Figure 31. Eight-Tone NSD vs. f_{OUT} over f_{DAC}

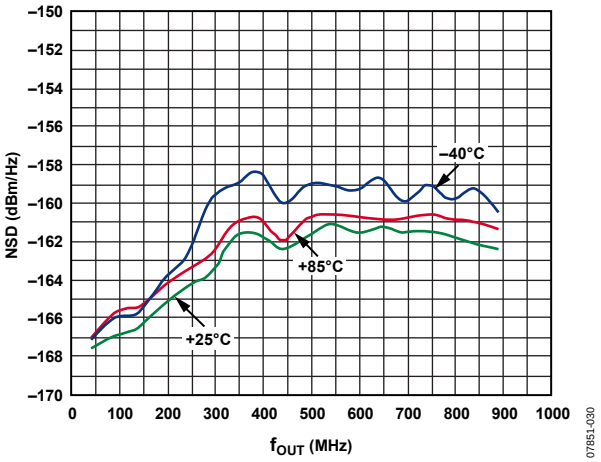


Figure 32. Single-Tone NSD vs. f_{OUT} over Temperature @ 2.0 GSPS

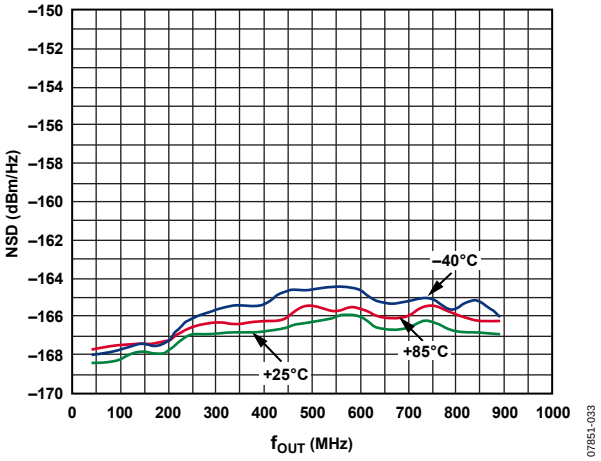


Figure 33. Eight-Tone NSD vs. f_{OUT} over Temperature @ 2.0 GSPS

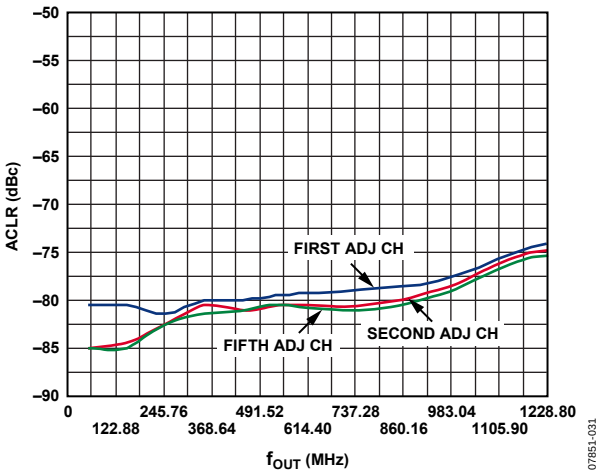


Figure 34. Single-Carrier WCDMA ACLR vs. f_{OUT} @ 2457.6 MSPS

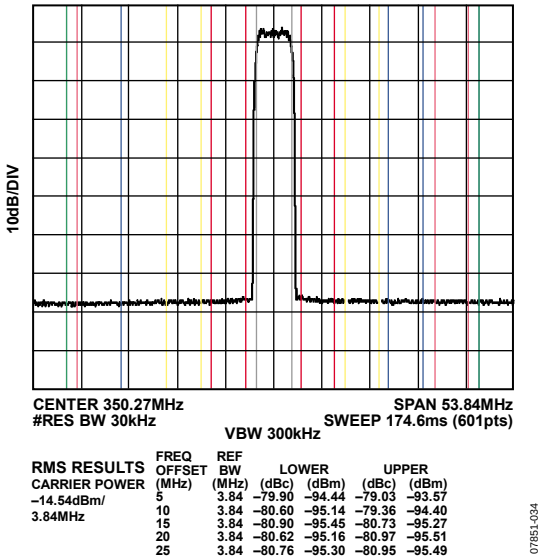


Figure 35. Typical Single-Carrier WCDMA ACLR Performance @ 350 MHz f_{DAC} = 2457.6 MSPS

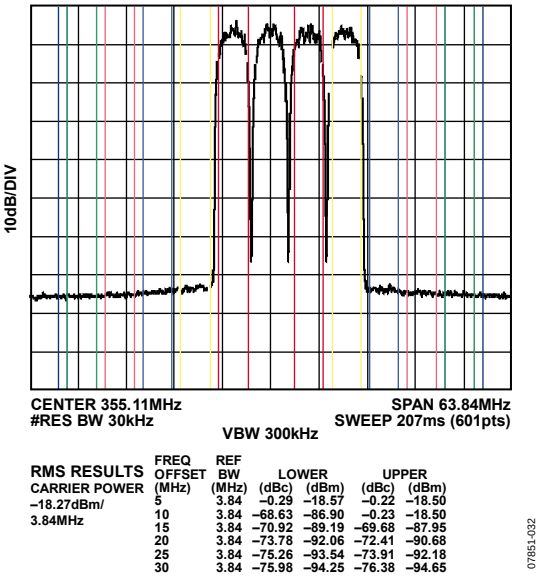


Figure 36. Typical Four-Carrier WCDMA ACLR Performance @ 350 MHz, f_{DAC} = 2457.6 MSPS

DYNAMIC PERFORMANCE MIX MODE, 20 mA FULL SCALE

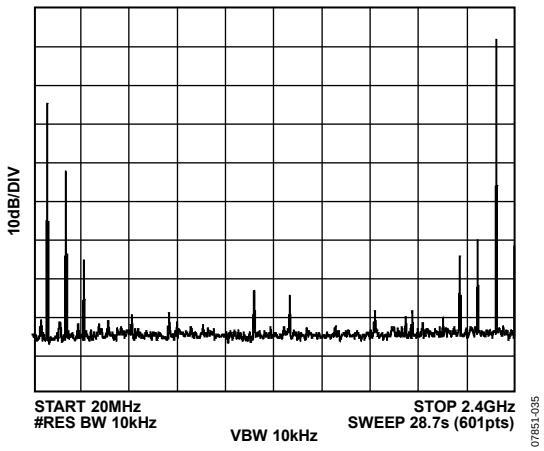


Figure 37. Single-Tone Spectrum in Mix Mode @ f_{OUT} = 2.31 GHz, f_{DAC} = 2.4 GSPS

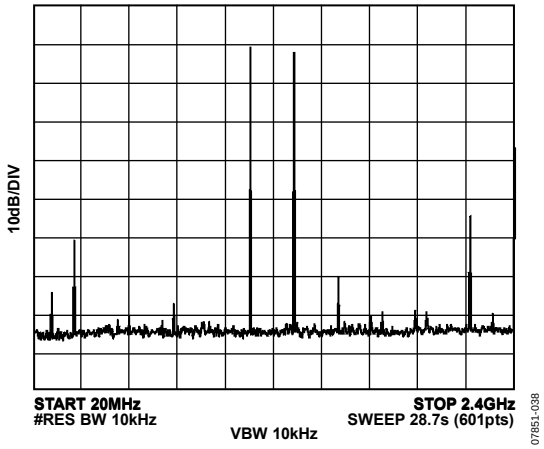


Figure 38. Single-Tone Spectrum in Mix Mode @ f_{OUT} = 1.31 GHz, f_{DAC} = 2.4 GSPS

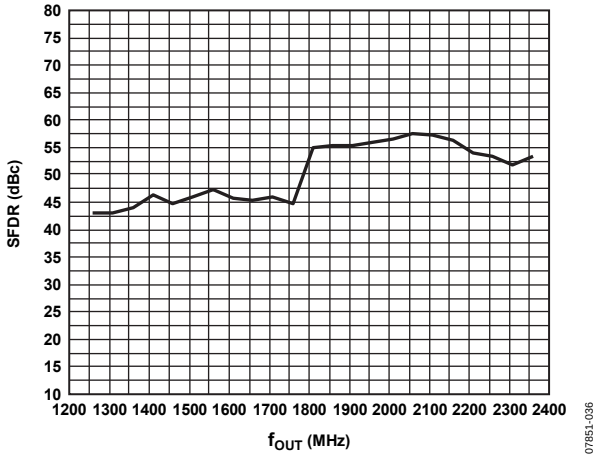


Figure 39. SFDR in Mix Mode vs. f_{OUT} @ 2.4 GSPS

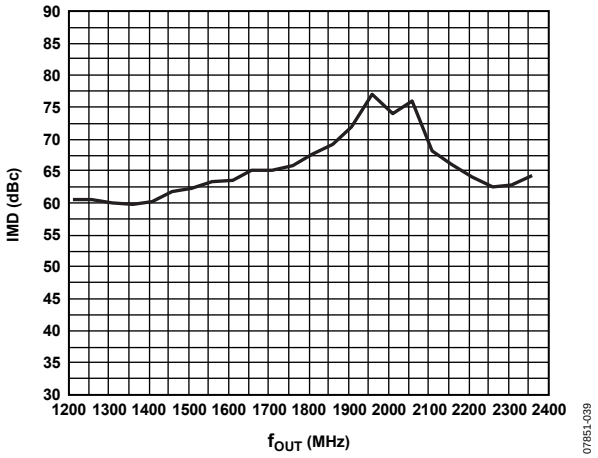


Figure 40. IMD in Mix Mode vs. f_{OUT} @ 2.4 GSPS

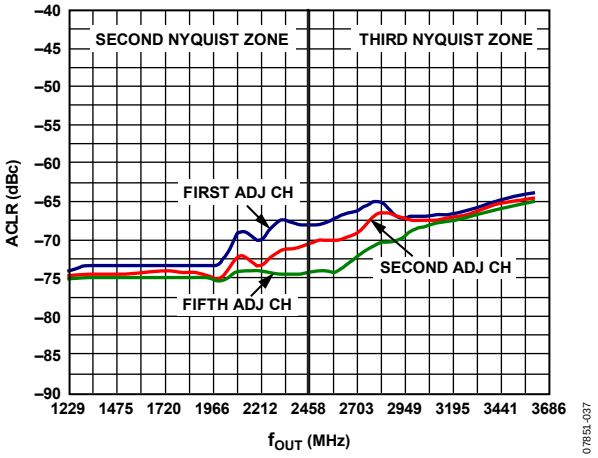


Figure 41. Single-Carrier WCDMA ACLR vs. f_{OUT} @ 2457.6 MSPS

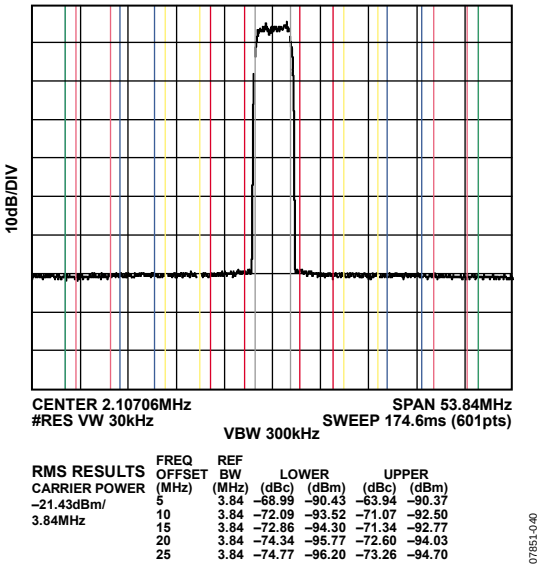
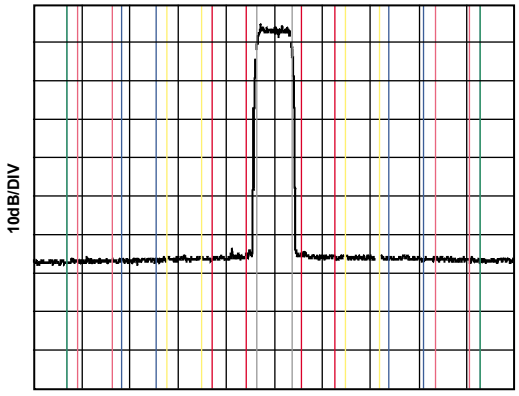


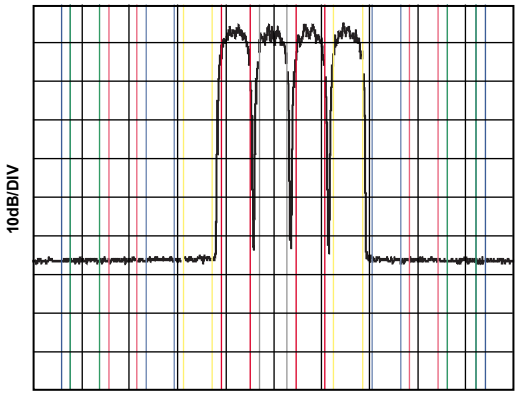
Figure 42. Typical Single-Carrier WCDMA ACLR Performance @ 2.1 GHz, f_{DAC} = 2457.6 MSPS (Second Nyquist Zone)



RMS RESULTS CARRIER POWER	FREQ OFFSET (MHz)	REF BW (MHz)	LOWER (dBc)	LOWER (dBm)	UPPER (dBc)	UPPER (dBm)
–24.4dBm/ 3.84MHz	5	3.84	–64.90	–89.30	–63.82	–88.22
	10	3.84	–66.27	–90.67	–65.70	–90.10
	15	3.84	–68.44	–92.84	–66.55	–90.95
	20	3.84	–70.20	–94.60	–68.95	–93.35
	25	3.84	–70.85	–95.25	–70.45	–94.85

07851-041

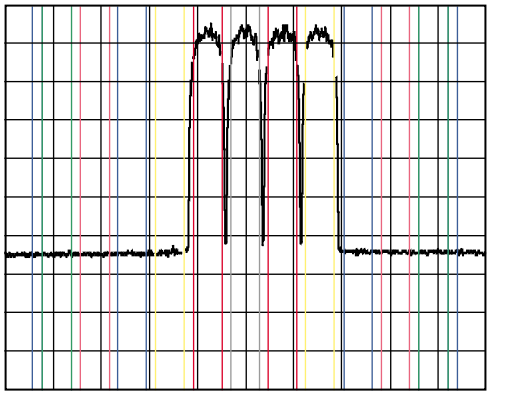
Figure 43. Typical Single-Carrier WCDMA ACLR Performance @ 2.8 GHz, f_{DAC} = 2457.6 MSPS (Third Nyquist Zone)



RMS RESULTS CARRIER POWER	FREQ OFFSET (MHz)	REF BW (MHz)	LOWER (dBc)	LOWER (dBm)	UPPER (dBc)	UPPER (dBm)
–25.53dBm/ 3.84MHz	5	3.84	0.22	–25.31	0.24	–25.29
	10	3.84	–66.68	–92.21	0.14	–25.38
	15	3.84	–68.01	–93.53	–66.82	–92.35
	20	3.84	–68.61	–94.14	–67.83	–93.36
	25	3.84	–68.87	–94.40	–67.64	–93.17
	30	3.84	–69.21	–94.74	–68.50	–94.03

07851-043

Figure 44. Typical Four-Carrier WCDMA ACLR Performance @ 2.1 GHz, f_{DAC} = 2457.6 MSPS (Second Nyquist Zone)



RMS RESULTS CARRIER POWER	FREQ OFFSET (MHz)	REF BW (MHz)	LOWER (dBc)	LOWER (dBm)	UPPER (dBc)	UPPER (dBm)
–27.98dBm/ 3.84MHz	5	3.84	–0.42	–28.40	–0.10	–28.07
	10	3.84	–64.32	–92.30	–0.08	–28.06
	15	3.84	–66.03	–94.01	–65.37	–93.34
	20	3.84	–66.27	–94.24	–66.06	–94.03
	25	3.84	–66.82	–94.79	–63.36	–93.34
	30	3.84	–67.16	–95.13	–66.54	–94.51

07851-042

Figure 45. Typical Four-Carrier WCDMA ACLR Performance @ 2.8 GHz f_{DAC} = 2457.6 MSPS (Third Nyquist Zone)

DOCSIS PERFORMANCE

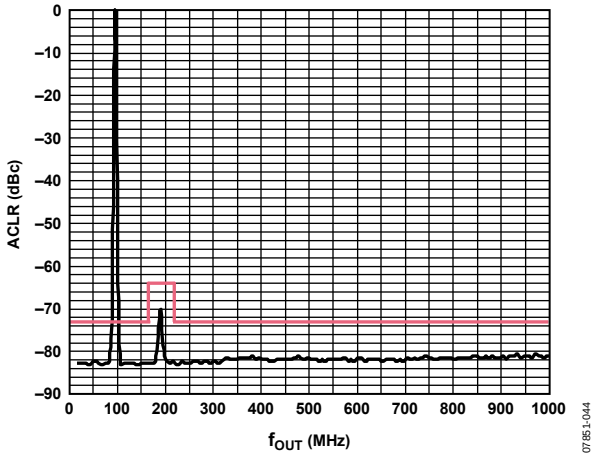


Figure 46. Single-Carrier DOCSIS ACLR Spectral Plot @ 91 MHz (DOCSIS SPEC (Red Line) Is 73 dBc ; Harmonic Exception Is 63 dBc)

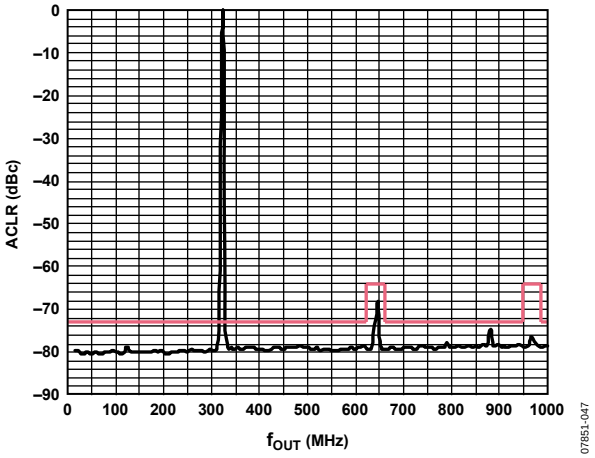


Figure 49. Single-Carrier DOCSIS ACLR Spectral Plot @ 325 MHz (DOCSIS SPEC (Red Line) Is 73 dBc ; Harmonic Exception Is 63 dBc)

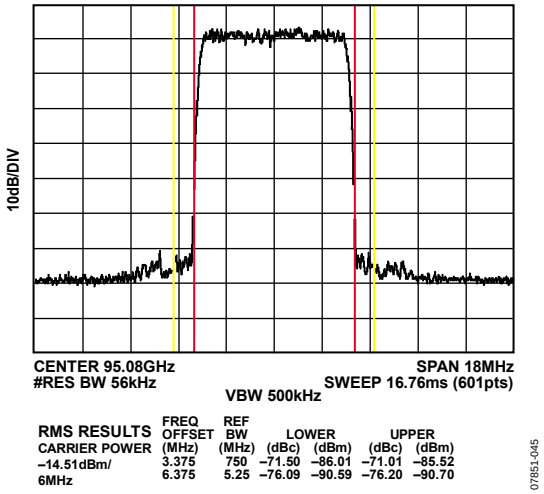


Figure 47. Single-Carrier DOCSIS Close-in ACLR Plot @ 91 MHz (Two Closest Channels)

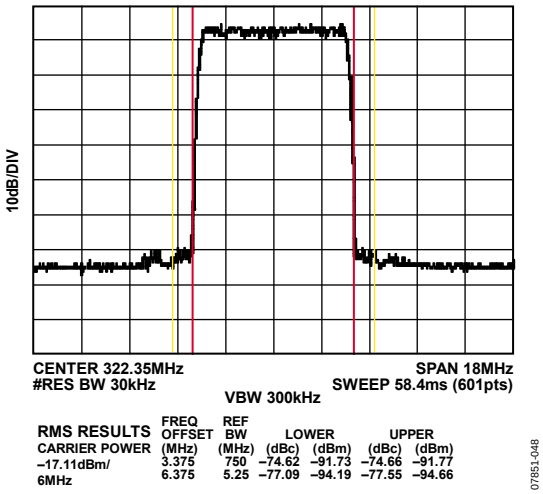


Figure 50. Single-Carrier DOCSIS Close-in ACLR Plot @ 325 MHz (Two Closest Channels)

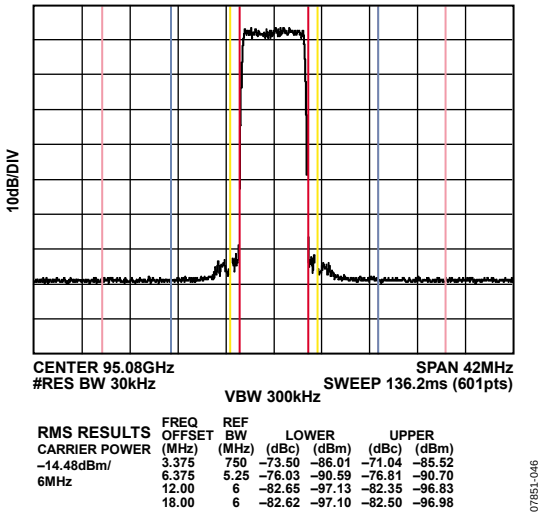


Figure 48. Single-Carrier DOCSIS Close-in ACLR Plot @ 91 MHz

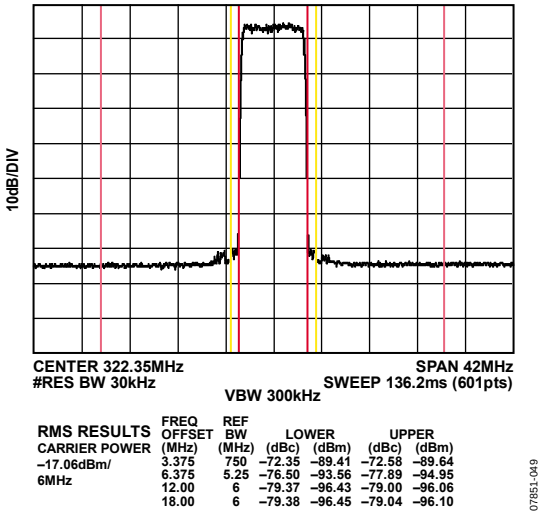


Figure 51. Single-Carrier DOCSIS Close-in ACLR Plot @ 325 MHz

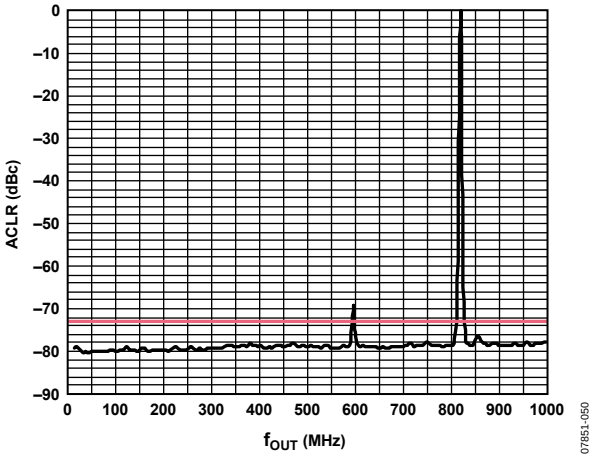


Figure 52. Single-Carrier DOCSIS ACLR Spectral Plot @ 825 MHz (DOCSIS SPEC (Red Line) Is 73 dBc ; Harmonic Exception Is 63 dBc)

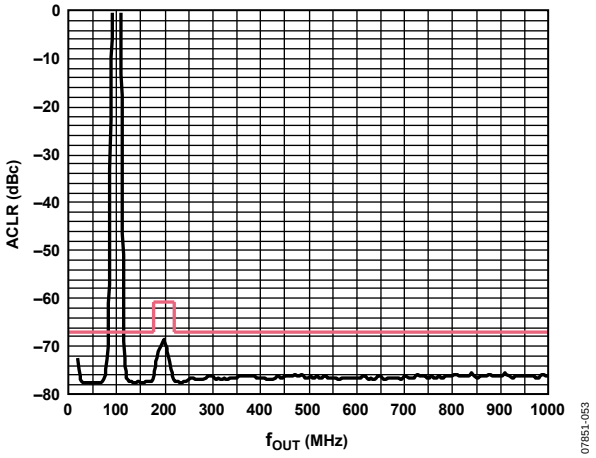


Figure 55. Four-Carrier DOCSIS ACLR Spectral Plot @ 91 MHz (DOCSIS SPEC (Red Line) Is 67 dBc; Harmonic Exception Is 61 dBc)

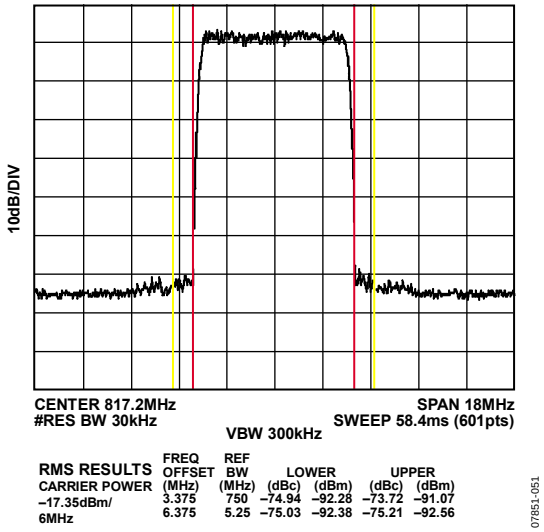


Figure 53. Single-Carrier DOCSIS Close-in ACLR Plot @ 825 MHz (Two Closest Channels)

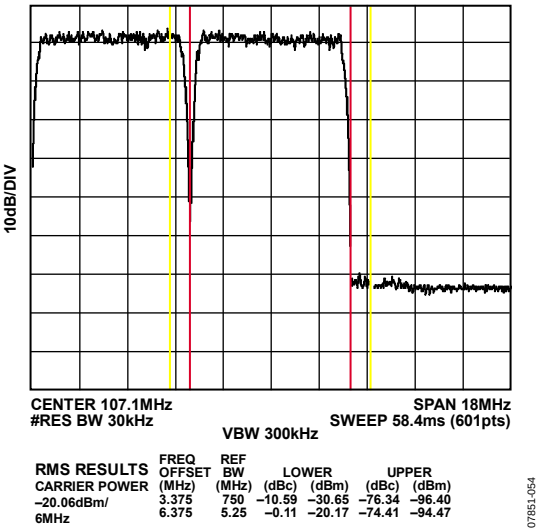


Figure 56. Four-Carrier DOCSIS Close-in ACLR Plot @ 91 MHz (Two Closest Channels)

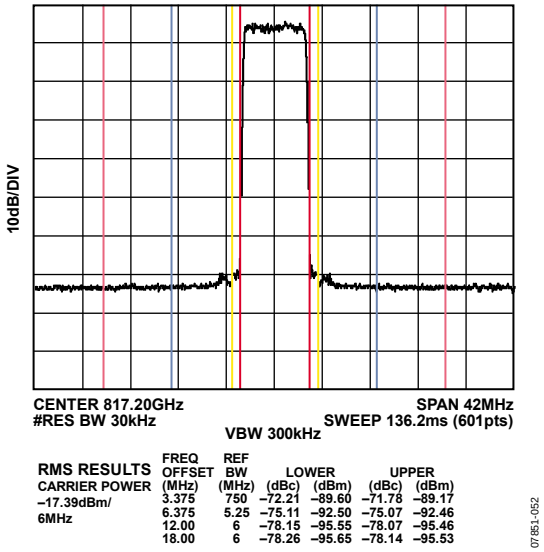


Figure 54. Single-Carrier DOCSIS Close-in ACLR Plot @ 825 MHz

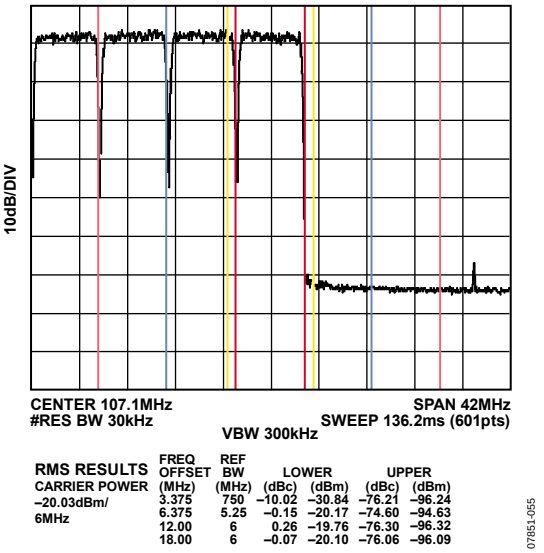


Figure 57. Single-Carrier DOCSIS Close-in ACLR Plot @ 91 MHz

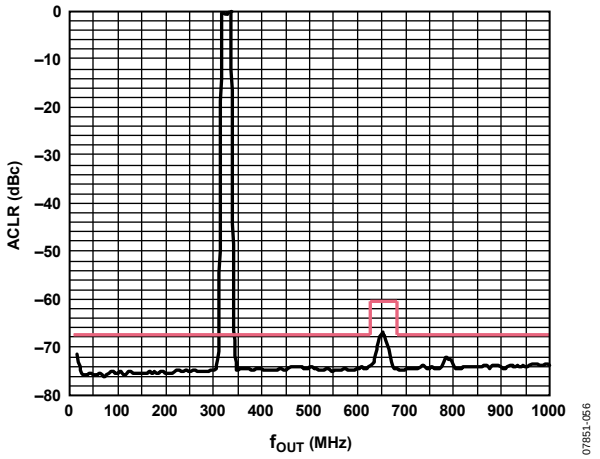


Figure 58. Four-Carrier DOCSIS ACLR Spectral Plot @ 325 MHz (DOCSIS SPEC (Red Line) Is 67 dBc ; Harmonic Exception Is 6 1dBc)

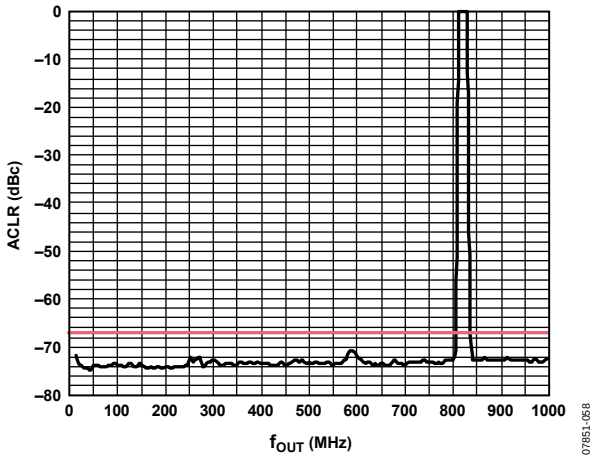


Figure 61. Four-Carrier DOCSIS ACLR Spectral Plot @ 825 MHz (DOCSIS SPEC (Red Line) Is 67 dBc ; Harmonic Exception Is 61 dBc)

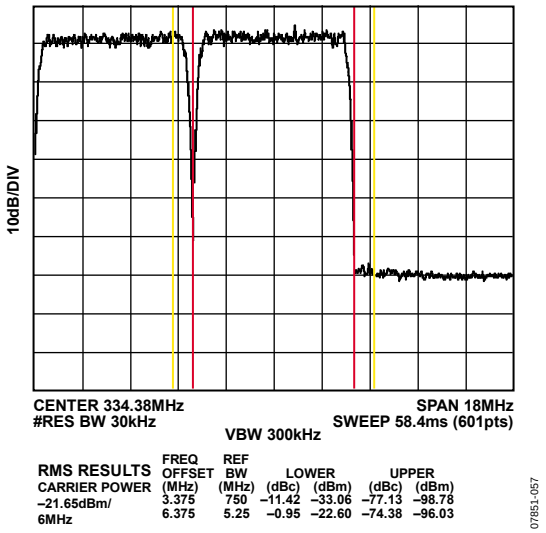


Figure 59. Four-Carrier DOCSIS Close-in ACLR Plot @ 325 MHz (Two Closest Channels)

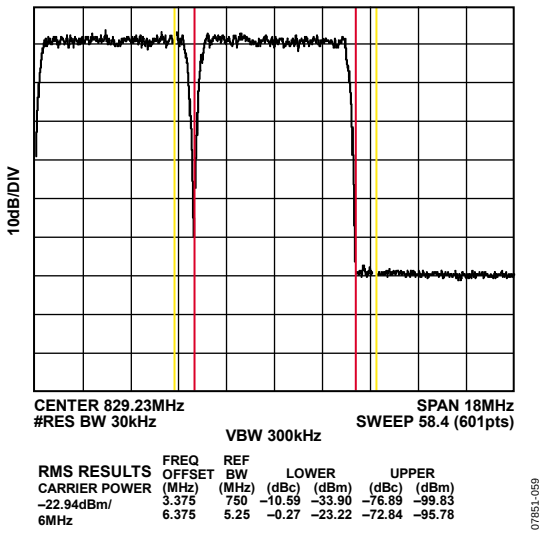


Figure 62. Four-Carrier DOCSIS Close-in ACLR Plot @ 825 MHz (Two Closest Channels)

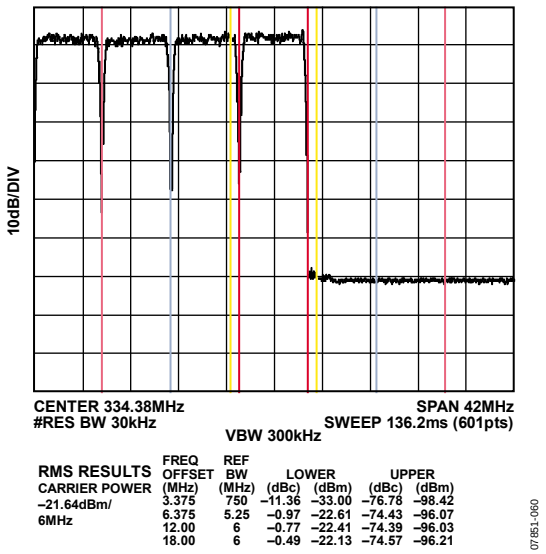


Figure 60. Single-Carrier DOCSIS Close-in ACLR Plot @ 325 MHz

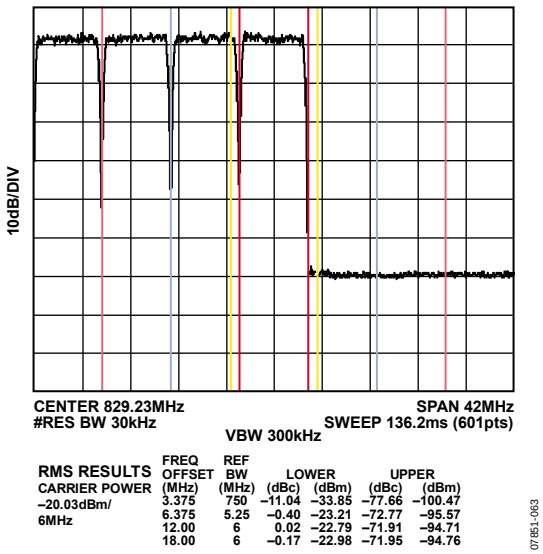


Figure 63. Single-Carrier DOCSIS Close-in ACLR Plot @ 825 MHz

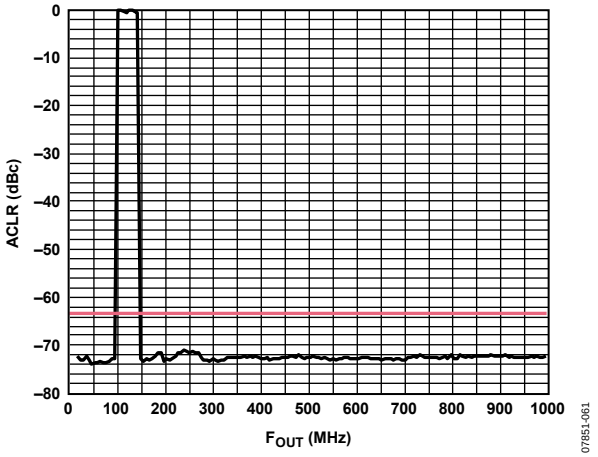


Figure 64. Eight-Carrier DOCSIS ACLR Spectral Plot @ 100 MHz (DOCSIS SPEC (Red Line) Is 63 dBc; Harmonic Exception Is 54 dBc)

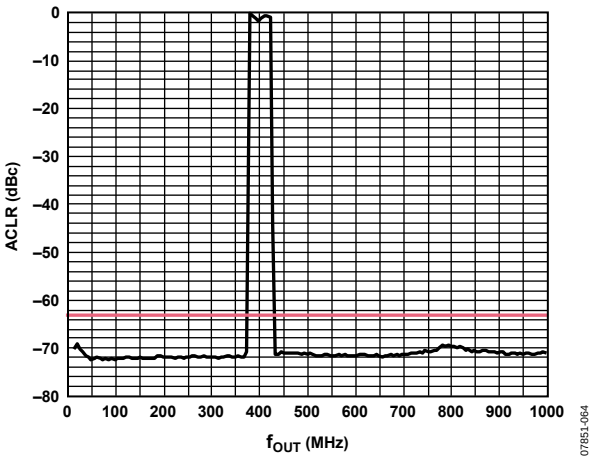


Figure 65. Eight-Carrier DOCSIS ACLR Spectral Plot @ 400 MHz (DOCSIS SPEC (Red Line) Is 63 dBc; Harmonic Exception Is 54 dBc)

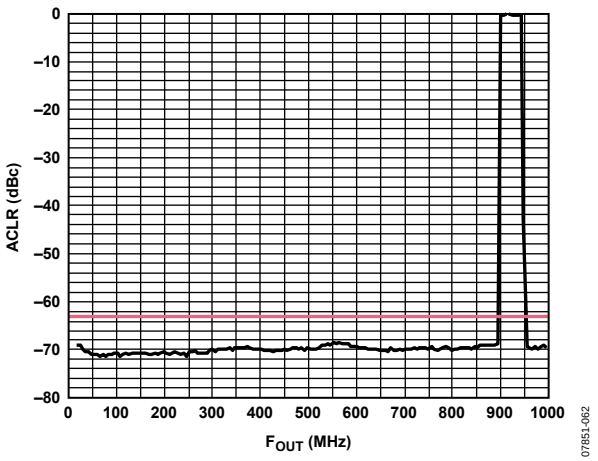


Figure 66. Eight-Carrier DOCSIS ACLR Spectral Plot @ 900 MHz (DOCSIS SPEC (Red Line) Is 63 dBc; Harmonic Exception Is 54 dBc)

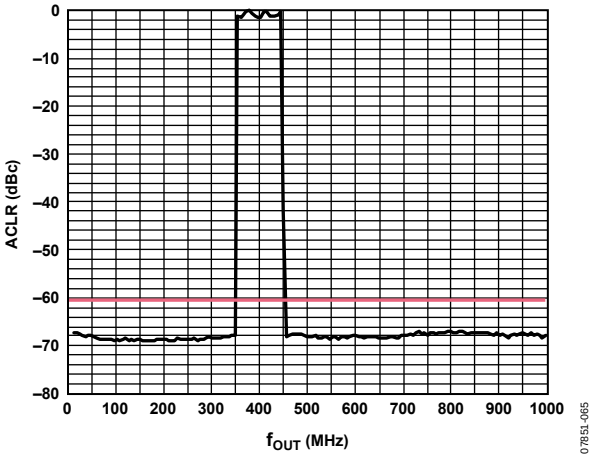


Figure 67. 16-Carrier DOCSIS ACLR Spectral Plot @ 400 MHz (DOCSIS SPEC (Red Line) Is 60 dBc ; Harmonic Exception Is 48 dBc)

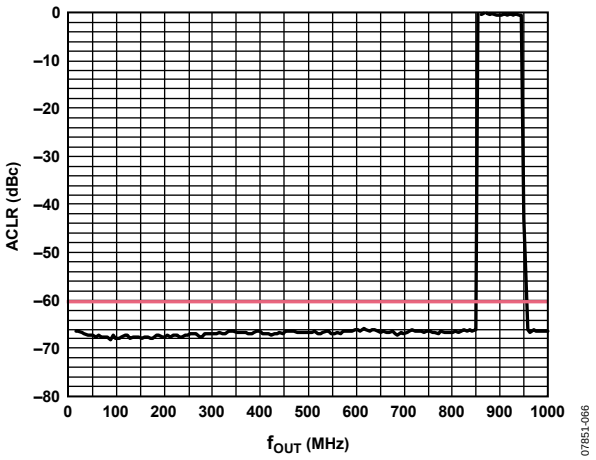


Figure 68. 16-Carrier DOCSIS ACLR Spectral Plot @ 900 MHz (DOCSIS SPEC (Red Line) Is 60 dBc; Harmonic Exception Is 48 dBc)

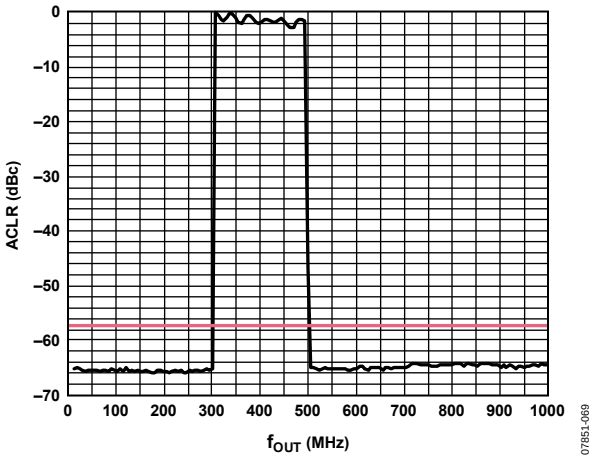


Figure 69. 32-Carrier DOCSIS ACLR Spectral Plot @ 400 MHz (DOCSIS SPEC (Red Line) Is 57 dBc; Harmonic Exception Is 42 dBc)

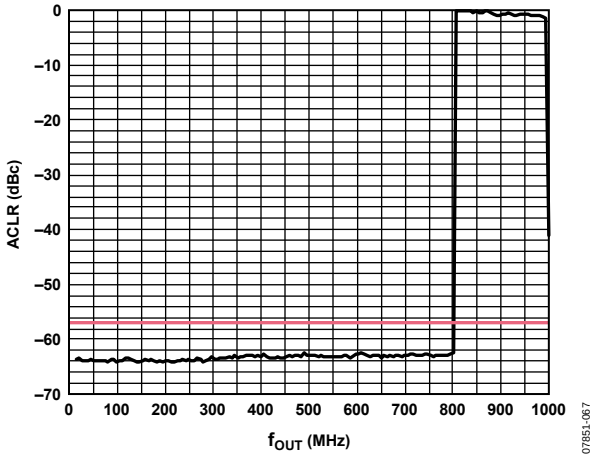


Figure 70. 32-Carrier DOCSIS ACLR Spectral Plot @ 900 MHz (DOCSIS SPEC (Red Line) Is 57 dBc; Harmonic Exception Is 42 dBc)

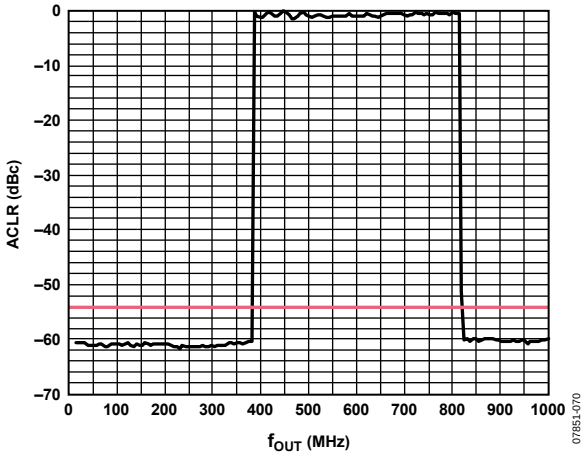


Figure 72. 72-Carrier DOCSIS ACLR Spectral Plot @ 700 MHz (DOCSIS SPEC (Red Line) Is 54 dBc; Harmonic Exception Is 35 dBc)

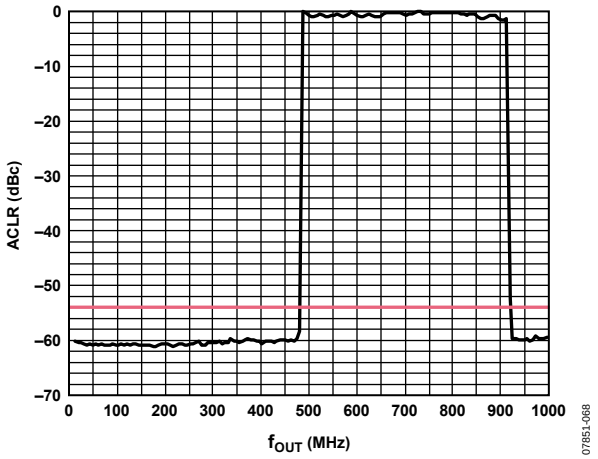


Figure 71. 72-Carrier DOCSIS ACLR Spectral Plot @ 600 MHz (DOCSIS SPEC (Red Line) Is 54 dBc ; Harmonic Exception Is 35 dBc)

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
The maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
The measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called the offset error. For IOUTP, 0 mA output is expected when the inputs are all 0s. For IOUTN, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1 minus the output when all inputs are set to 0.

Output Compliance Range
The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Spurious-Free Dynamic Range
The difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Noise Spectral Density (NSD)
NSD is the converter noise power per unit of bandwidth. This is usually specified in dBm/Hz in the presence of a 0 dBm full-scale signal.

Adjacent Channel Leakage Ratio (ACLR)
The adjacent channel leakage (power) ratio is a ratio, in dBc, between the measured power within a channel relative to its adjacent channels.

Modulation Error Ratio (MER)
Modulated signals create a discrete set of output values referred to as a constellation. Each symbol creates an output signal corresponding to one point on the constellation. MER is a measure of the discrepancy between the average output symbol magnitude and the rms error magnitude of the individual symbol.

Intermodulation Distortion (IMD)
IMD is the result of two or more signals at different frequencies mixing together. Many products are created according to the formula aF1± bF2, where a and b are integer values.

THEORY OF OPERATION

The AD9739 is a 14-bit DAC that operates at an update rate of up to 2.5 GSPS. Due to internal timing requirements, the minimum allowable sample rate is 800 MSPS. Input data is sampled through two 14-bit LVDS ports that are internally multiplexed. Each port has its own data inputs, but both ports share a common DCI input. The LVDS inputs meet the IEEE-1596 reduced swing specification with the exception of input hysteresis, which is not guaranteed over all process corners. Each DCI input runs at one-quarter the input data rate in a double data rate (DDR) format. Each edge of DCI is used to transfer data into the AD9739.

The DACCLK_N/DACCLK_P inputs directly drive the DAC core to minimize clock jitter. The DACCLK signal is divided by 4 then output as the DCO for each port. The DCO signal can be used to clock the data source. The DAC expects DDR LVDS data (DB0[13:0], DB1[13:0]), with each channel aligned with the single DDR data input clock (DCI).

Control of the AD9739 functions is via a serial peripheral interface (SPI).

SERIAL PERIPHERAL INTERFACE

The AD9739 serial port is a flexible, synchronous serial communications port, allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including the Motorola® SPI and the Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9739. Most significant bit first (MSB-first) or least significant bit first (LSB-first) transfer formats are supported. The AD9739 serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for input/output (SDIO/SDO).

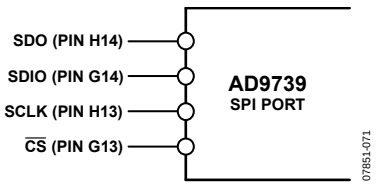


Figure 73. AD9739 SPI Port

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a communication cycle with the AD9739. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9739 coincident with the first eight SCLK rising edges. The instruction byte provides the AD9739 serial port controller with information about the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9739.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9739 and the system controller. Phase 2 of the communication cycle is a transfer of one byte only. Single-byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte. $\overline{CS}$ (chip select) can be raised after each sequence of eight bits (except the last byte) to stall the bus. The serial transfer resumes when $\overline{CS}$ is lowered. Stalling on nonbyte boundaries resets the SPI.

INSTRUCTION MODE (8-BIT INSTRUCTION)

The instruction byte is shown in the following table.

MSB							LSB
I7	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**
R/W	A6	A5	A4	A3	A2	A1	A0

R/W, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation, the data transfer cycle. A6 to A0 (Bit 6 through Bit 0 of the instruction byte) determine which register is accessed during the data transfer portion of the communications cycle.

SERIAL INTERFACE PORT PIN DESCRIPTIONS

SCLK—Serial Clock

The serial clock pin is used to synchronize data to and from the AD9739 and to run the internal state machines. The maximum frequency of SCLK is 20 MHz. All data input to the AD9739 is registered on the rising edge of SCLK. All data is driven out of the AD9739 on the rising edge of SCLK.

$\overline{CS}$—Chip Select

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDO and SDIO pins go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

SDIO—Serial Data I/O

Data is always written into the AD9739 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by SDIO_DIR at Register 0x00, Bit 7. The default is Logic 0, which configures the SDIO pin as unidirectional.

SDO—Serial Data Out

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9739 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB TRANSFERS

The AD9739 serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by LSB/MSB at Register 0x00, Bit 6. The default is MSB first (LSB/MSB = 0). When LSB/MSB = 0 (MSB first), the instruction and data bytes must be written from the most significant bit to the least significant bit.

When LSB/MSB = 1 (LSB first), the instruction and data bytes must be written from the least significant bit to the most significant bit.

SERIAL PORT CONFIGURATION

The AD9739 serial port configuration is controlled by Register 0x00, Bits[7:5]. Note that the configuration changes immediately upon writing to the last bit of the register. When setting the software reset (Register 0x00, Bit 5), all registers are set to their default values except Register 0x00, which remains unchanged.

In the event of unexpected programming sequences, the AD9739 SPI can become inaccessible. For example, if user code inadvertently changes the LSB/MSB bit, the following bits experience unexpected results. The SPI can be returned to a known state by writing an incomplete byte (1 to 7 bits) of all 0s followed by three bytes of 0x00. This returns to the MSB-first instructions (Register 0 x00 = 0x00) so that the device can be reinitialized.

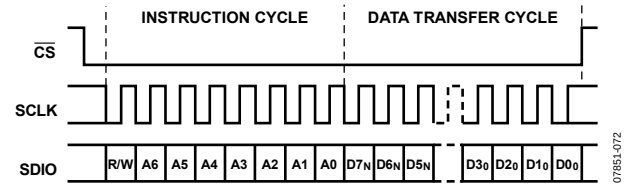


Figure 74. Serial Register Interface Timing, MSB-First Write

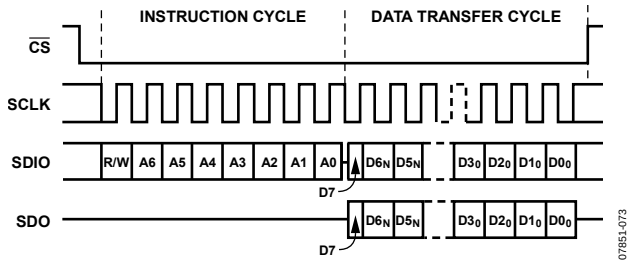


Figure 75. Serial Register Interface Timing, MSB-First Read

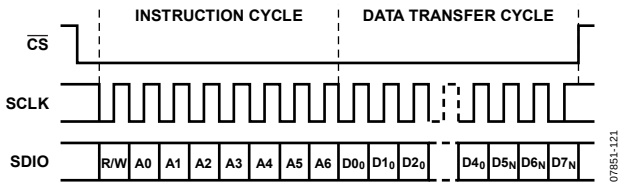


Figure 76. Serial Register Interface Timing, LSB-First Write

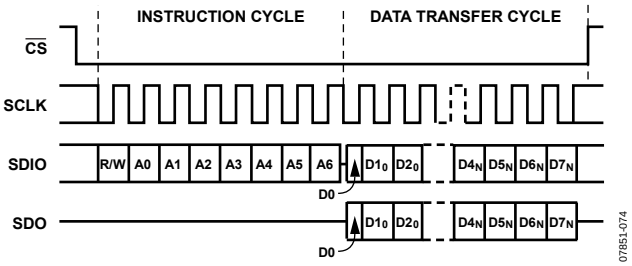


Figure 77. Serial Register Interface Timing, LSB-First Read

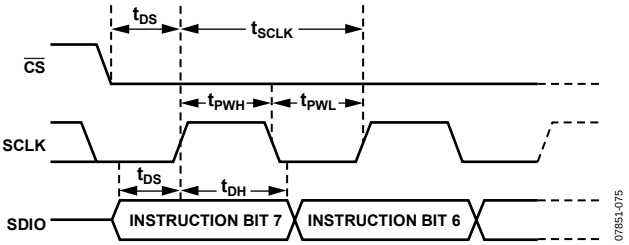


Figure 78. Timing Diagram for an SPI Register Write

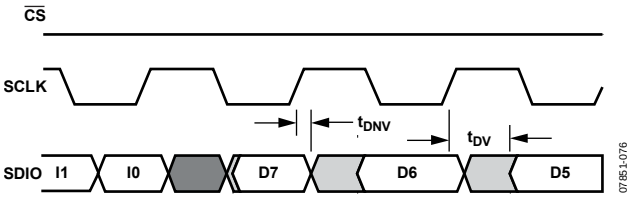


Figure 79. Timing Diagram for an SPI Register Read

After the last instruction bit is written to the SDIO pin, the driving signal must be set to a high impedance in time for the bus to turn around. The serial output data from the AD9739 is enabled by the falling edge of SCLK. This causes the first output data bit to be shorter than the remaining data bits, as shown in Figure 79. To assure proper reading of data, read the SDIO or SDO pin prior to changing the SCLK from low to high. Due to the more complex multibyte protocol, multiple AD9739 devices cannot be daisy-chained on the SPI bus. Multiple DACs should be controlled by independent $\overline{CS}$ signals.

SPI REGISTER MAP

Table 7.

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Mode	0x00	SDIO_DIR	LSB/MSB	Reset	N/A	N/A	N/A	N/A	N/A	0x00
Power-Down	0x01	N/A	N/A	LVDS_DCO_PD	LVDS_RCVR_PD	N/A	N/A	CLK_REC_PD	DAC_BIAS_PD	0x00
CNT_CLK_Dis	0x02	N/A	N/A	N/A	N/A	CLKGEN_PD	N/A	REC_CNT_CLK	MU_CNT_CLK	0x03
IRQ_En	0x03	N/A	N/A	SYNC_LST_EN	SYNC_LCK_EN	MULST_EN	MULCK_EN	RCV_LST_EN	RCV_LCK_EN	0x00
IRQ_Req	0x04	N/A	N/A	SYNC_LST_IRQ	SYNC_LCK_IRQ	MULST_IRQ	MULCK_IRQ	RCVLST_IRQ	RCVLCK_IRQ	0x00
RSVD	0x05	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
FSC_1	0x06	FSC[7]	FSC[6]	FSC[5]	FSC[4]	FSC[3]	FSC[2]	FSC[1]	FSC[0]	0x00
FSC_2	0x07	Sleep	N/A	N/A	N/A	N/A	N/A	FSC[9]	FSC[8]	0x02
Dec_CNT	0x08	N/A	N/A	N/A	N/A	N/A	N/A	DAC_DEC[1]	DAC_DEC[0]	0x00
RSVD	0x09	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
LVDS_CNT	0x0A	N/A	N/A	N/A	N/A	HNDOFF_CHK_RST	N/A	LVDS_Bias[1]	LVDS_Bias[0]	0x00
DIG_STAT	0x0B	HNDOFF_Fall[3]	HNDOFF_Fall[2]	HNDOFF_Fall[1]	HNDOFF_Fall[0]	HNDOFF_Rise[3]	HNDOFF_Rise[2]	HNDOFF_Rise[1]	HNDOFF_Rise[0]	RNDM
LVDS_STAT1	0x0C	SUP/HLD_Edge1	N/A	DCI_PHS3	DCI_PHS1	DCI_PRE_PH2	DCI_PRE_PH0	DCI_PST_PH2	DCI_PST_PH0	RNDM
LVDS_STAT2	0x0D	SUP/HLD_SYNC	SUP/HLD_Edge0	SYNC_SAMP1	SYNC_SAMP0	LVDS1_HI	LVDS1_LO	LVDS0_HI	LVDS0_LO	RNDM/0
RSVD	0x0E	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
RSVD	0x0F	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
LVDS_REC_CNT1	0x10	SYNC_FLG_RST	SYNC_LOOP_ON	SYNC_MST/SLV	SYNC_CNT_ENA	N/A	RCVR_FLG_RST	RCVR_LOOP_ON	RCVR_CNT_ENA	0x42
LVDS_REC_CNT2	0x11	SMP_DEL[1]	SMP_DEL[0]	FINE_DEL_MID[3]	FINE_DEL_MID[2]	FINE_DEL_MID[1]	FINE_DEL_MID[0]	RCVR_GAIN[1]	RCVR_GAIN[0]	0xDD
LVDS_REC_CNT3	0x12	SMP_DEL[9]	SMP_DEL[8]	SMP_DEL[7]	SMP_DEL[6]	SMP_DEL[5]	SMP_DEL[4]	SMP_DEL[3]	SMP_DEL[2]	0x29
LVDS_REC_CNT4	0x13	DCI_DEL[3]	DCI_DEL[2]	DCI_DEL[1]	DCI_DEL[0]	FINE_DEL_SKW[3]	FINE_DEL_SKW[2]	FINE_DEL_SKW[1]	FINE_DEL_SKW[0]	0x71
LVDS_REC_CNT5	0x14	CLKDIVPH[1]	CLKDIVPH[0]	DCI_DEL[9]	DCI_DEL[8]	DCI_DEL[7]	DCI_DEL[6]	DCI_DEL[5]	DCI_DEL[4]	0x0A
LVDS_REC_CNT6	0x15	SYNC_GAIN[1]	SYNC_GAIN[0]	SYNCOUT_PH[1]	SYNCOUT_PH[0]	LCKTHR[3]	LCKTHR[2]	LCKTHR[1]	LCKTHR[0]	0x42
LVDS_REC_CNT7	0x16	N/A	SYNCO_DEL[6]	SYNCO_DEL[5]	SYNCO_DEL[4]	SYNCO_DEL[3]	SYNCO_DEL[2]	SYNCO_DEL[1]	SYNCO_DEL[0]	0x00
LVDS_REC_CNT8	0x17	SYNCSH_DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_REC_CNT9	0x18	SYNCSH_DEL[8]	SYNCSH_DEL[7]	SYNCSH_DEL[6]	SYNCSH_DEL[5]	SYNCSH_DEL[4]	SYNCSH_DEL[3]	SYNCSH_DEL[2]	SYNCSH_DEL[1]	0x00
LVDS_REC_STAT1	0x19	SMP_DEL[1]	SMP_DEL[0]	N/A	N/A	SMP_FINE_DEL[3]	SMP_FINE_DEL[2]	SMP_FINE_DEL[1]	SMP_FINE_DEL[0]	0xC7
LVDS_REC_STAT2	0x1A	SMP_DEL[9]	SMP_DEL[8]	SMP_DEL[7]	SMP_DEL[6]	SMP_DEL[5]	SMP_DEL[4]	SMP_DEL[3]	SMP_DEL[2]	0x29
LVDS_REC_STAT3	0x1B	DCI_DEL[1]	DCI_DEL[0]	N/A	N/A	SYNCOUTPH[1]	SYNCOUTPH[0]	CLKDIVPH[1]	CLKDIVPH[0]	0xC0
LVDS_REC_STAT4	0x1C	DCI_DEL[9]	DCI_DEL[8]	DCI_DEL[7]	DCI_DEL[6]	DCI_DEL[5]	DCI_DEL[4]	DCI_DEL[3]	DCI_DEL[2]	0x29
LVDS_REC_STAT5	0x1D	FINE_DEL_PST[3]	FINE_DEL_PST[2]	FINE_DEL_PST[1]	FINE_DEL_PST[0]	FINE_DEL_PRE[3]	FINE_DEL_PRE[2]	FINE_DEL_PRE[1]	FINE_DEL_PRE[0]	0x86
LVDS_REC_STAT6	0x1E	N/A	SYNCO_DEL[6]	SYNCO_DEL[5]	SYNCO_DEL[4]	SYNCO_DEL[3]	SYNCO_DEL[2]	SYNCO_DEL[1]	SYNCO_DEL[0]	0x00

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
LVDS_ REC_STAT7	0x1F	SYNCSH_ DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_ REC_STAT8	0x20	SYNCSH_ DEL[8]	SYNCSH_ DEL[7]	SYNCSH_ DEL[6]	SYNCSH_ DEL[5]	SYNCSH_ DEL[4]	SYNCSH_ DEL[3]	SYNCSH_ DEL[2]	SYNCSH_ DEL[1]	0x00
LVDS_ REC_STAT9	0x21	SYNC_TRK _ON	SYNC_INIT _ON	SYNC_LST _LCK	SYNC_LCK	RCVR_TRK _ON	RCVR_FE_ ON	RCVR_LST_ LCK	RCVR_LCK	0x00
CROSS_ CNT1	0x22	N/A	N/A	N/A	DIR_P	CLKP_ OFFSET[3]	CLKP_ OFFSET[2]	CLKP_ OFFSET[1]	CLKP_ OFFSET[0]	0x00
CROSS_ CNT2	0x23	N/A	N/A	N/A	DIR_N	CLKN_ OFFSET[3]	CLKN_ OFFSET[2]	CLKN_ OFFSET[1]	CLKN_ OFFSET[0]	0x00
PHS_DET	0x24	N/A	N/A	PHS_DET AUTO_EN	CMP_BST	Bias[3]	Bias[2]	Bias[1]	Bias[0]	0x00
MU_DUTY	0x25	MU_DUTY AUTO_EN	POS/NEG	ADJ[5]	ADJ[4]	ADJ[3]	ADJ[2]	ADJ[1]	ADJ[0]	0x00
MU_CNT1	0x26	N/A	Slope	Mode[1]	Mode[0]	Read	Gain[1]	Gain[0]	Enable	0x42
MU_CNT2	0x27	MUDEL[0]	SrchMode [1]	SrchMode [0]	SetPhs[4]	SetPhs[3]	SetPhs[2]	SetPhs[1]	SetPhs[0]	0x40
MU_CNT3	0x28	MUDEL[8]	MUDEL[7]	MUDEL[6]	MUDEL[5]	MUDEL[4]	MUDEL[3]	MUDEL[2]	MUDEL[1]	0x00
MU_CNT4	0x29	Search_Tol	Retry	ContRst	Guard[4]	Guard[3]	Guard[2]	Guard[1]	Guard[0]	0x0B
MU_STAT1	0x2A	N/A	N/A	N/A	N/A	N/A	N/A	MU_LOST	MU_LKD	0x00
RSVD	0x2B	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
RSVD	0x2C	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
ANA_CNT1	0x32	HDRM[7]	HDRM[6]	HDRM[5]	HDRM[4]	HDRM[3]	HDRM[2]	HDRM[1]	HDRM[0]	0xCA
ANA_CNT2	0x33	N/A	N/A	N/A	N/A	N/A	N/A	MSEL[1]	MSEL[0]	0x03
RSVD	0x34	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
PART ID	0x35	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	0x40

SPI REGISTERS

Reading these registers returns previously written values for all defined register bits, unless otherwise noted.

Table 8. Mode Register (Register 0x00)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode	0x00	00	SDIO_DIR	LSB/MSB	Reset	N/A	N/A	N/A	N/A	N/A

[1]The two-digit number is the decimal representation of the address.

Table 9. Mode Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
SDIO_DIR	Read/write	0: input only, per SPI standard. 1: bidirectional, per SPI standard.	0
LSB/MSB	Read/write	0: MSB first, per SPI standard. 1: LSB first, per SPI standard. Change the LSB/MSB order in single-byte instructions only to avoid erratic behavior due to bit order errors.	0
Reset	Read/write	0: default. Bit is in the inactive state. 1: all programmable bits return to their default state except Register 0x00, which is unaffected by the software reset. The software reset remains in effect until this bit is set to 0 (inactive state).	0

Table 10. Power-Down Register (Register 0x01)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Power-Down	0x01	01	N/A	N/A	LVDS_DCO_PD	LVDS_RCVR_PD	N/A	N/A	CLK_REC_PD	DAC_BIAS_PD

[1]The two-digit number is the decimal representation of the address.

Table 11. Power-Down Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
LVDS_DCO_PD	Read/write	0: DCO enabled. 1: DCO disabled.	0
LVDS_RCVR_PD	Read/write	0: LVDS receiver enabled. 1: LSB receiver powered down.	0
CLK_REC_PD	Read/write	0: internal clock receiver enabled. 1: internal clock receiver powered down.	0
DAC_BIAS_PD	Read/write	0: DAC bias circuitry enabled. 1: DAC bias circuitry powered down.	0

Table 12. Controller Clock Disable Register (Register 0x02)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT_CLK_Dis	0x02	02	N/A	N/A	N/A	N/A	CLKGEN_PD	N/A	REC_CNT_CLK	MU_CNT_CLK

[1]The two-digit number is the decimal representation of the address.

Table 13. Controller Clock Disable Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
CLKGEN_PD	Read/write	0: clocks enabled. 1: clocks disabled.	0
REC_CNT_CLK	Read/write	0: clock to LVDS receiver controller disabled. 1: clock to LVDS receiver controller enabled.	0
MU_CNT_CLK	Read/write	0: clock to mu controller disabled. 1: clock to mu controller enabled.	0

Table 14. IRQ Registers (Register 0x03, Register 0x04)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQ_En	0x03	03	N/A	N/A	SYNC_LST_EN	SYNC_LCK_EN	MULST_EN	MULCK_EN	RCV_LST_EN	RCV_LCK_EN
IRQ_Req	0x04	04	N/A	N/A	SYNC_LST_IRQ	SYNC_LCK_IRQ	MULST_IRQ	MULCK_IRQ	RCVLST_IRQ	RCVLCK_IRQ

[1]The two-digit number is the decimal representation of the address.

Table 15. IRQ Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
SYNC_LST_EN	Write	0: reset SYNC_LST_IRQ and disable future SYNC_LST_IRQ. 1: enable SYNC_LST_IRQ request.	0
SYNC_LCK_EN	Write	0: reset SYNC_IRQ and disable future SYNC_LCK_IRQ. 1: enable SYNC_IRQ request.	0
MULST_EN	Write	0: reset MULST_IRQ and disable future MULST_IRQ. 1: enable MULST_IRQ request.	0
MULCK_EN	Write	0: reset MULCK_IRQ and disable future MULCK_IRQ. 1: enable the MULCK_IRQ request.	0
RCV_LST_EN	Write	0: reset the RCVLST_IRQ and disable future RCVLST_IRQ. 1: enable the RCVLST_IRQ request.	0
RCV_LCK_EN	Write	0: reset the RCV_IRQ interrupt and disable future MULCK_IRQ. 1: enable RCV_IRQ request.	0
SYNC_LST_IRQ	Read	0: the sync controller has not lost lock. 1: the sync controller has lost lock and an interrupt has occurred.	0
SYNC_LCK_IRQ	Read	0: the sync controller is unlocked. 1: the sync controller has achieved lock and an interrupt has occurred.	0
MULST_IRQ	Read	0: the mu controller has not lost lock. 1: the mu controller has lost lock and an interrupt has occurred.	0

Bit Name	Read/Write	Description	Reset Value for Write Register
MULCK_IRQ	Read	0: the mu controller is unlocked. 1: the mu controller has achieved lock and an interrupt has occurred.	0
RCVLST_IRQ	Read	0: the RCV controller has not lost lock. 1: the RCV controller has lost lock and an interrupt has occurred.	0
RCVLCK_IRQ	Read	0: the RCV controller is unlocked. 1: the RCV controller has achieved lock and an interrupt has occurred.	0

Table 16. Full-Scale Current Registers (Register 0x06, Register 0x07)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSC_1	0x06	06	FSC[7]	FSC[6]	FSC[5]	FSC[4]	FSC[3]	FSC[2]	FSC[1]	FSC[0]
FSC_2	0x07	07	Sleep	N/A	N/A	N/A	N/A	N/A	FSC[9]	FSC[8]

[1]The two-digit number is the decimal representation of the address.

Table 17. Full Scale Output Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
Sleep	Read/write	0: enable DAC output. 1: set DAC output current to 0 mA.	0
FSC[9:0]	Read/write	0x000: 10 mA full-scale output current. 0x200: 20 mA full-scale output current. 0x3FF: 30 mA full-scale output current. See the Voltage Reference section for full details.	0x200

Table 18. Decoder Control Register (Register 0x08)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Dec_CNT	0x08	08	N/A	N/A	N/A	N/A	N/A	N/A	DAC_DEC[1]	DAC_DEC[0]

[1]The two-digit number is the decimal representation of the address.

Table 19. Decoder Control/Status Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
DAC_DEC[1:0]	Read/write	0x0: normal mode. 0x1: return to zero mode. 0x2: analog mix mode. 0x3: flip mode.	0x0

Table 20. LVDS Control/Status Registers (Register 0x0A, Register 0x0B, Register 0x0C, Register 0x0D)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit2	Bit 1	Bit 0
LVDS_CNT	0x0A	10	N/A	N/A	N/A	N/A	HNDOFF_ CHK_RST	N/A	LVDS_ Bias[1]	LVDS_ Bias[0]
DIG_STAT	0x0B	11	HNDOFF_ Fall[3]	HNDOFF_ Fall[2]	HNDOFF_ Fall[1]	HNDOFF_ Fall[0]	HNDOFF_ Rise[3]	HNDOFF_ Rise[2]	HNDOFF_ Rise[1]	HNDOFF_ Rise[0]
LVDS_STAT1	0x0C	12	SUP/HLD_ Edge1	N/A	DCI_PHS3	DCI_PHS1	DCI_PRE_ PH2	DCI_PRE_ PH0	DCI_PST_ PH2	DCI_PST_ PH0
LVDS_STAT2	0x0D	13	SUP/HLD_ SYNC	SUP/HLD_ Edge0	SYNC_ SAMP1	SYNC_ SAMP0	LVDS1_HI	LVDS1_LO	LVDS0_HI	LVDS0_LO

[1]The two-digit number is the decimal representation of the address.

Table 21. LVDS Control/Status Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
HNDOFF_CHK_RST	Read/write	0: default. Bit is in the inactive state. 1: resets the handoff errors in Register 0x0B.	0x00
LVDS_Bias[1:0]	Read/write	0x0: 360 µA bias current. 0x1: 460 µA bias current. 0x2: 560 µA bias current 0x3: 660 µA bias current.	0x0
HNDOFF_Fall[3:0]	Read	0: there are no timing violations in the falling edges between the delay lines. 1: there is a timing violation in the falling edges between the delay lines.	0
HNDOFF_Rise[3:0]	Read	0: there are no timing violations in the rising edges between the delay lines. 1: there is a timing violation in the rising edges between the delay lines.	0
SUP/HLD_Edge1	Read	Sample second phase of clock divider with setup/hold delay line.	0
DCI_PHS3	Read	0: divider phases aligned correctly. 1: divider phases aligned incorrectly.	0
DCI_PHS1	Read	0: divider phases aligned incorrectly. 1: divider phases aligned correctly.	0
DCI_PRE_PH2	Read	0: the DCI signal is aligned with the Phase 2 edge. 1: the DCI signal is slightly before the Phase 2 edge.	0
DCI_PRE_PH0	Read	0: the DCI signal is aligned with the Phase 0 edge. 1: the DCI signal is slightly before the Phase 0 edge.	0
DCI_PST_PH2	Read	0: the DCI signal is aligned with the Phase 2 edge. 1: the DCI signal is slightly after the Phase 2 edge.	0
DCI_PST_PH0	Read	0: the DCI signal is aligned with the Phase 0 edge. 1: the DCI signal is slightly after the Phase 0 edge.	0
SUP/HLD_SYNC	Read	Sample SYNC_IN with setup/hold delay line (should be between the first phase and the second phase).	0
SUP/HLD_Edge0	Read	Sample first phase of clock divider with setup/hold delay line.	0
SYNC_SAMP1	Read	SYNC_IN sample of clock divider Phase 1.	0
SYNC_SAMP0	Read	SYNC_IN sample of clock divider Phase 0.	0
LVDS1_HI	Read	One or more LVDS inputs on Port 1 are above the input voltage limits of the IEEE reduce link specification.	0
LVDS1_LO	Read	One or more LVDS inputs on Port 1 are below the input voltage limits of the IEEE reduce link specification.	0
LVDS0_HI	Read	One or more LVDS inputs on Port 0 are above the input voltage limits of the IEEE reduce link specification.	0
LVDS0_LO	Read	One or more LVDS inputs on Port 0 are below the input voltage limits of the IEEE reduce link specification.	0

Table 22. LVDS Receiver Control Registers (Register 0x10, Register 0x11, Register 0x12, Register 0x13, Register 0x14, Register 0x15, Register 0x16, Register 0x17, Register 0x18)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDS_ REC_CNT1	0x10	16	SYNC_ FLG_RST	SYNC_ LOOP_ON	SYNC_ MST/SLV	SYNC_ CNT_ENA	N/A	RCVR_ FLG_RST	RCVR_ LOOP_ON	RCVR_ CNT_ENA
LVDS_ REC_CNT2	0x11	17	SMP_DEL[1]	SMP_DEL [0]	FINE_DEL_ MID[3]	FINE_DEL_ MID[2]	FINE_DEL_ MID[1]	FINE_DEL_ MID[0]	RCVR_GAIN[1]	RCVR_GAIN[0]
LVDS_ REC_CNT3	0x12	18	SMP_DEL[9]	SMP_DEL[8]	SMP_DEL[7]	SMP_DEL[6]	SMP_DEL[5]	SMP_DEL[4]	SMP_DEL[3]	SMP_DEL[2]
LVDS_ REC_CNT4	0x13	19	DCI_DEL[3]	DCI_DEL[2]	DCI_DEL[1]	DCI_DEL[0]	FINE_DEL_ SKW[3]	FINE_DEL_ SKW[2]	FINE_DEL_ SKW[1]	FINE_DEL_ SKW[0]
LVDS_ REC_CNT5	0x14	20	CLKDIVPH[1]	CLKDIVPH[0]	DCI_DEL[9]	DCI_DEL[8]	DCI_DEL[7	DCI_DEL[6]	DCI_DEL[5]	DCI_DEL[4]
LVDS_ REC_CNT6	0x15	21	SYNC_GAIN [1]	SYNC_GAIN [0]	SYNCOUT_ PH[1]	SYNCOUT_ PH[0]	LCKTHR[3]	LCKTHR[2]	LCKTHR[1]	LCKTHR[0]
LVDS_ REC_CNT7	0x16	22	N/A	SYNCO_ DEL[6]	SYNCO_ DEL[5]	SYNCO_ DEL[4]	SYNCO_ DEL[3]	SYNCO_ DEL[2]	SYNCO_ DEL[1]	SYNCO_ DEL[0]
LVDS_ REC_CNT8	0x17	23	SYNCSH_ DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
LVDS_ REC_CNT9	0x18	24	SYNCSH_ DEL[8]	SYNCSH_ DEL[7]	SYNCSH_ DEL[6]	SYNCSH_ DEL[5]	SYNCSH_ DEL[4]	SYNCSH_ DEL[3]	SYNCSH_ DEL[2]	SYNCSH_ DEL[1]

[1]The two-digit number is the decimal representation of the address.

Table 23. LVDS Receiver Control Register Bit Descriptions

Bit Name	Read/Write	Description
SYNC_FLG_RST	Write	Write high then low to reset flags set by the sync controller.
SYNC_LOOP_ON	Read/write	0: sync controller will not loop or generate an IRQ when an error has occurred. 1: sync controller will generate an IRQ and restart and return to track mode as previous.
SYNC_MST/SLV	Read/write	0: sync controller is in slave mode. 1: sync controller is in master mode.
SYNC_CNT_ENA	Read/write	0: sync controller is not enabled. 1: sync controller is enabled.
RCVR_FLG_RST	Write	Write high then low to reset flags set by the receiver controller.
RCVR_LOOP_ON	Read/write	0: receiver controller will not loop or generate an IRQ when an error has occurred. 1: receiver controller will generate an IRQ and restart and return to track mode as previous.
RCVR_CNT_ENA	Read/write	0: receiver controller is not enabled. 1: receiver controller is enabled.
RCVR_GAIN[1:0]	Read/write	Sets the receiver sample tracking gain (optimal value is 1).
SYNC_GAIN[1:0]	Read/write	Sets the sync tracking gain (optimal value is 1).
SMP_DEL[9:0]	Read/write	Sets the sample delay value (only valid when the data receiver controller is disabled; maximum sample delay value is 332 or 0x14C). When the data receiver controller is enabled, this represents the starting point for the search (optimal value is 166 or 0xA6).
FINE_DEL_MID[3:0]	Read/write	Sets the fine delay line mid value (optimal value is 7).
DCI_DEL[9:0]	Read/write	Sets the DCI delay value (only valid when the data receiver controller is disabled; maximum DCI delay value is 332 or 0x14C). When the data receiver controller is enabled, this represents the starting point for the search (optimal value is 166 or 0xA6).
FINE_DEL_SKW[3:0]	Read/write	Sets the distance between the DCI pre and post sampling.
LCKTHR[3:0]	Read/write	Sets the difference between the sample and DCI delays to lock (optimal value is 2).
CLKDIVPH[1:0]	Read/write	Sets the clock divider phase (only valid when the sync controller is disabled).
SYNCO_DEL[6:0]	Read/write	Sets the sync output delay value (only valid when the sync controller is disabled).
SYNCSH_DEL[8:0]	Read/write	Sets the sync setup and hold delay value (only valid when the sync controller is disabled).

Table 24. LVDS Receiver Status Registers (Register 0x19, Register 0x1A, Register 0x1B, Register 0x1C, Register 0x1D, Register 0x1E, Register 0x1F, Register 0x20, Register 0x21)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDS_ REC_STAT1	0x19	25	SMP_DEL[1]	SMP_DEL[0]	N/A	N/A	SMP_FINE _DEL[3]	SMP_FINE _DEL[2]	SMP_FINE _DEL[1]	SMP_FINE _DEL[0]
LVDS_ REC_STAT2	0x1A	26	SMP_DEL[9]	SMP_DEL[8]	SMP_DEL[7]	SMP_DEL[6]	SMP_DEL[5]	SMP_DEL[4]	SMP_DEL[3]	SMP_DEL[2]
LVDS_ REC_STAT3	0x1B	27	DCI_DEL[1]	DCI_DEL[0]	N/A	N/A	SYNCOUT PH[1]	SYNCOUT PH[0]	CLKDIV PH[1]	CLKDIV PH[0]
LVDS_ REC_STAT4	0x1C	28	DCI_DEL[9]	DCI_DEL[8]	DCI_DEL[7]	DCI_DEL[6]	DCI_DEL[5]	DCI_DEL[4]	DCI_DEL[3]	DCI_DEL[2]
LVDS_ REC_STAT5	0x1D	29	FINE_DEL_ PST[3]	FINE_DEL_ PST[2]	FINE_DEL_ PST[1]	FINE_DEL_ PST[0]	FINE_DEL_ PRE[3]	FINE_DEL_ PRE[2]	FINE_DEL_ PRE[1]	FINE_DEL_ PRE[0]
LVDS_ REC_STAT6	0x1E	30	N/A	SYNCO_ DEL[6]	SYNCO_ DEL[5]	SYNCO_ DEL[4]	SYNCO_ DEL[3]	SYNCO_ DEL[2]	SYNCO_ DEL[1]	SYNCO_ DEL[0]
LVDS_ REC_STAT7	0x1F	31	SYNCSH_ DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	N/A
LVDS_ REC_STAT8	0x20	32	SYNCSH_ DEL[8]	SYNCSH_ DEL[7]	SYNCSH_ DEL[6]	SYNCSH_ DEL[5]	SYNCSH_ DEL[4]	SYNCSH_ DEL[3]	SYNCSH_ DEL[2]	SYNCSH_ DEL[1]
LVDS_ REC_STAT9	0x21	33	SYNC_TRK_ ON	SYNC_INIT_ ON	SYNC_LST _LCK	SYNC_LCK	RCVR_TRK_ ON	RCVR_FE_ ON	RCVR_LST_ LCK	RCVR_LCK

[1]The two-digit number is the decimal representation of the address.

Table 25. LVDS Receiver Status Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
SMP_DEL[9:0]	Read	Readback of the present SMP_DEL value. In tracking mode, it represents the current valid SMP_DEL setting. In manual mode, it is a readback of the value written to SMP_DEL[9:0] in Register 17 and Register 18.	0
SMP_FINE_DEL[3:0]	Read	Readback of the sample fine delay line value (this is the same as FINE_MID_DEL).	0
SYNCOUTPH[1:0]	Read	Readback of the present SYNC_OUT phase selection.	0
CLKDIVPH[1:0]	Read	Readback of the present CLK divider phase rotation.	0
DCI_DEL[9:0]	Read	Readback of the present DCI_DEL value. In tracking mode, it represents the current valid DCI_DEL setting. In manual mode, it is a readback of the value written to DCI_DEL[9:0] in Register 13 and Register 14.	0
FINE_DEL_PRE[3:0]	Read	Present fine delay setting for the pre DCI window search delay line.	0
FINE_DEL_PST[3:0]	Read	Present fine delay setting for the post DCI window search delay line.	0
SYNCO_DEL[6:0]	Read	Readback of the present SYNCO_DEL value. In tracking mode, it represents the current value of the SYNCO_DEL setting. In manual mode, it is a readback of the value written to SYNCO_DEL[6:0] in Register 16.	0
SYNCSH_DEL[8:0]	Read	Readback of the present SYNCSH_DEL value. In tracking mode, it represents the current value of the SYNCSH_DEL setting. In manual mode, it is a readback of the value written to SYNCSH_DEL[8:0] in Register 17 and Register 18.	0
SYNC_TRK_ON	Read	0: with the sync controller enabled, tracking mode has not been established. 1: with the sync controller enabled, tracking mode has been established.	0
SYNC_INIT_ON	Read	1: indicates that the sync controller is in initialize mode.	0
SYNC_LST_LCK	Read	0: sync lock has not been lost. 1: sync lock has been lost at some point.	0
SYNC_LCK	Read	0: the sync controller is not locked. 1: the sync controller is locked.	0
RCVR_TRK_ON	Read	0: with the receiver controller enabled, tracking mode has not been established. 1: with the receiver controller enabled, tracking mode has been established.	0

Bit Name	Read/Write	Description	Reset Value for Write Register
RCVR_FE_ON	Read	0: indicates that the FINDEDGE state machine is not active. 1: indicates that the FINDEDGE state machine is active.	0
RCVR_LST_LCK	Read	0: lock has not been lost. 1: lock has been lost at some point.	0
RCVR_LCK	Read	0: the receiver controller is not locked. 1: the receiver controller is locked.	0

Table 26. Cross Controller Registers (Register 0x22, Register 0x23)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CROSS_CNT1	0x22	34	N/A	N/A	N/A	DIR_P	CLKP_OFFSET[3]	CLKP_OFFSET[2]	CLKP_OFFSET[1]	CLKP_OFFSET[0]
CROSS_CNT2	0x23	35	N/A	N/A	N/A	DIR_N	CLKN_OFFSET[3]	CLKN_OFFSET[2]	CLKN_OFFSET[1]	CLKN_OFFSET[0]

[1]The two-digit number is the decimal representation of the address.

Table 27. Cross Controller Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
CLKP_OFFSET[3:0]	Read/write	0x0: programmable to vary the common-mode voltage for DACCLKP (for best ac performance, the optimal setting is 15).	0x0
DIR_P	Read/Write	O: common-mode voltage on DACCLK_P decreases with the programmed value of CLKP_OFFSET[3:0]. 1: common-mode voltage on DACCLK_P increases with the programmed value of CLKP_OFFSET[3:0] (for the best ac, the optimal setting is 0).	0
CLKN_OFFSET[3:0]	Read/write	0x0: programmable to vary the common-mode voltage for DACCLKN (for best ac performance, the optimal setting is 15).	0x0
DIR_N	Read/Write	O: common-mode voltage on DACCLK_N decreases with the programmed value of CLKN_OFFSET[3:0]. 1: common-mode voltage on DACCLK_N increases with the programmed value of CLKN_OFFSET[3:0] (for the best ac, the optimal setting is 0).	0

Table 28. MU Controller Registers (Register 0x24, Register 0x25, Register 0x26, Register 0x27, Register 0x28, Register 0x29, Register 0x2A)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PHS_DET	0x24	36	N/A	N/A	PHS_DETAUTO_EN	CMP_BST	Bias[3]	Bias[2]	Bias[1]	Bias[0]
MU_DUTY	0x25	37	MU_DUTYAUTO_EN	POS/NEG	ADJ[5]	ADJ[4]	ADJ[3]	ADJ[2]	ADJ[1]	ADJ[0]
MU_CNT1	0x26	38	N/A	Slope	Mode[1]	Mode[0]	Read	Gain[1]	Gain[0]	Enable
MU_CNT2	0x27	39	MUDEL[0]	SrchMode[1]	SrchMode[0]	SetPhs[4]	SetPhs[3]	SetPhs[2]	SetPhs[1]	SetPhs[0]
MU_CNT3	0x28	40	MUDEL[8]	MUDEL[7]	MUDEL[6]	MUDEL[5]	MUDEL[4]	MUDEL[3]	MUDEL[2]	MUDEL[1]
MU_CNT4	0x29	41	Search_Tol	Retry	ContRst	Guard[4]	Guard[3]	Guard[2]	Guard[1]	Guard[0]
MU_STAT1	0x2A	42	N/A	N/A	N/A	N/A	N/A	N/A	MU_LOST	MU_LKD

[1]The two-digit number is the decimal representation of the address.

Table 29. MU Controller Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
PHS_DET AUTO_EN	Read/write	0: no action. 1: enables phase detector correction (recommended to always enable).	0
CMP_BST	Read/write	0: no action. 1: enables the phase detector comparator boost (only valid if PHS_DET AUTO_EN is enabled; recommended to always enable).	0
BIAS[3:0]	Read/write	Manual control of the phase detector boost bias (only valid if CMP_BST is disabled).	0
MU_DUTY AUTO_EN	Read/write	0: no action. 1: enables the mu controller duty correction circuitry (recommended to always enable).	0
POS/NEG	Read/write	0: decreases the mu controller clock duty cycle (optimal setting). 1: increases the mu controller clock duty cycle.	0
ADJ[5:0]	Read/write	Manual adjust of the mu controller clock duty cycle (only valid when MU_DUTY_AUTO_EN is disabled).	0
Enable	Read/write	0: the mu controller is disabled. 1: the mu controller is enabled.	0
Gain[1:0]	Read/write	Sets the mu controller tracking gain (0x01 optimal setting).	0x01
Read	Read/write	0: no action. 1: read the current value of mu delay (reads the value the controller locks if enable is set high or reads the value written into MUDEL[0:8] if enable is set low).	0
Mode[1:0]	Read/write	Sets the mode in which the mu controller functions. 0x0: search and track (optimal setting). 0x1: track only. 0x2: search only. 0x3: invalid.	0x0
Slope	Read/write	0: the mu controller locks on the negative phase slope (optimal setting for best ac performance). 1: the mu controller locks on the positive phase slope.	1
SetPhs[4:0]	Read/write	Sets the phase that the mu controller locks onto (maximum value is 16; optimal setting for best ac performance is 6).	
SrchMode[1:0]	Read/write	Sets the mode in which the mu controller searches for the desired phase from the specified starting mu delay value. 0x0: down. 0x1: up. 0x2: down/up (optimal setting). 0x3: invalid.	0x2
MUDEL[8:0]	Read/write	With enable set to 0, this value represents the value that the mu delay will be set to. With enable set to 1, this value represents the mu delay value at which the controller will begin its search. The maximum mu delay value is 432 or 0x1B0 (it is recommended to set this value to the midpoint to begin the search (216)). With enable set to 0 and read set to 1, this reads back the value that was written into the register to lock to. With enable set to 1 and read set to 1, this value reads back the value that the mu controller locked to.	0x0
Guard[4:0]	Read/write	Sets a GB from the beginning and end of the mu delay line in which the mu controller will not enter into unless it does not find a valid phase outside the GB (optimal value is Decimal 11 or 0x0B).	0x0
ContRst	Read/write	Controls whether the controller resets or continues if it does not find the desired phase. 0x0: continue (optimal setting). 0x1: reset.	0x0

Bit Name	Read/Write	Description	Reset Value for Write Register
Retry	Read/write	0x0: if the correct value is not found, the search stops. 0x1: if the correct value is not found, the search begins again.	0x0
Search_Tol	Read/write	0x0: not exact (can find a phase within two values of the desired phase). 0x1: finds the exact phase that is targeted (optimal setting).	0x0
Mu_LOST	Read	0x0: mu controller has not lost lock. 0x1: mu controller has lost lock.	0x0
Mu_LKD	Read	0x0: mu controller is not locked. 0x1: mu controller is locked.	0x0

Table 30. Analog Controller Registers (Register 0x32, Register 0x33)

Register Name	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANA_CNT1	0x32	50	HDRM[7]	HDRM[6]	HDRM[5]	HDRM[4]	HDRM[3]	HDRM[2]	HDRM[1]	HDRM[0]
ANA_CNT2	0x33	51	N/A	N/A	N/A	N/A	N/A	N/A	MSEL[1]	MSEL[0]

[1]The two-digit number is the decimal representation of the address.

Table 31. Analog Controller Register Bit Descriptions

Bit Name	Read/Write	Description	Reset Value for Write Register
MSEL[1:0]	Write	0x0: mirror roll-off frequency control = bypass. 0x1: mirror roll-off frequency control = narrowest bandwidth. 0x2: mirror roll-off frequency control = medium bandwidth. 0x3: mirror roll-off frequency control = widest bandwidth. See the plot in the Analog Control Registers section.	0x03
HDRM[7:0]	Write	0xCA: output stack headroom control. HDRM[7:4]: set the reference offset from AVDD33 (VCAS centering). HDRM[3:0]: set the overdrive (current density) trim (temperature tracking).	0xCA

APPLICATIONS INFORMATION

ANALOG MODES OF OPERATION

The AD9739 uses the quad-switch architecture shown in Figure 80, which can be configured to operate in one of the following three modes via the serial peripheral interface: normal mode, RZ mode, and analog mix mode.

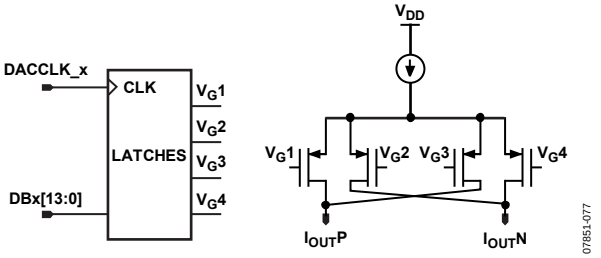


Figure 80. AD9739 Quad-Switch Architecture

The quad-switch architecture masks the code-dependent glitches that occur in a conventional two-switch DAC. Figure 81 shows the waveforms for a conventional DAC and the quad-switch DAC. In the two-switch architecture, when a switch transition occurs and D_1 and D_2 are in different states, a glitch occurs. But, if D_1 and D_2 happen to be at the same state, the switch transitions, and no glitches occur. This code-dependent glitching causes an increased amount of distortion in the DAC. In quad-switch architecture (no matter what the codes are), there are always two switches transitioning at each half clock cycle, thus eliminating the code-dependent glitches but, in the process, creating a constant glitch at 2 × DACCLK_x.

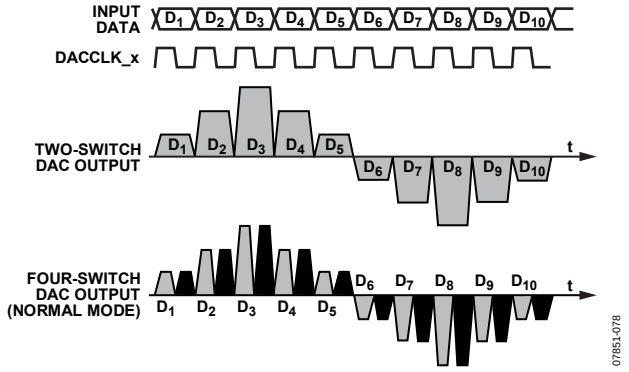


Figure 81. Two-Switch and Quad-Switch DAC Waveforms

The quad-switch architecture can also be easily configured to perform an analog mix or return-to-zero (RZ) function. In the mix mode, the output is effectively chopped at twice the DAC sample rate. This has the effect of reducing the power of the fundamental signal while increasing the power of the images centered around the DAC sample rate, thus improving the dynamic range of the higher frequency signals.

The RZ mode is similar to the analog mix mode, except that the intermediate data samples are replaced with midscale values rather than inverting. Figure 82 shows the DAC waveforms for both the mix mode and RZ modes.

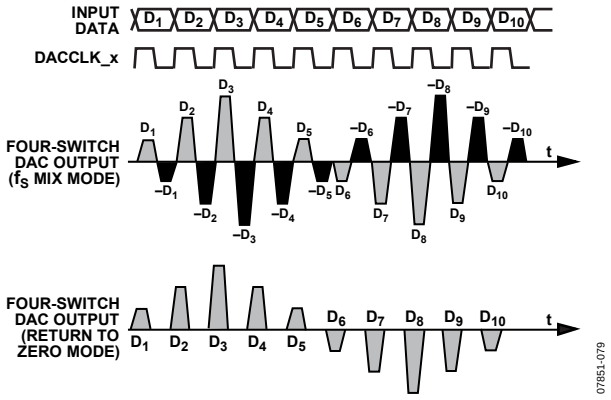


Figure 82. Mix Mode and RZ DAC Waveforms

This ability to change modes in the AD9739 makes it suitable for both CMTS and UMTS applications. The user can place a carrier anywhere in the first three Nyquist zones, depending on the operating mode selected. Switching between the analog modes reshapes the sinc roll-off inherent at the DAC output. The performance and maximum amplitude in all three Nyquist zones are impacted by this sinc roll-off, depending on where the carrier is placed, as shown in Figure 83.

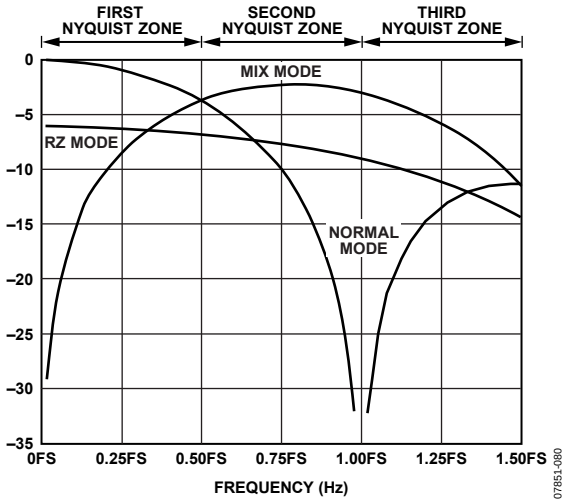


Figure 83. Sinc Roll-Off for Each Analog Operating Mode

LVDS DATA PORT INTERFACE

The AD9739 contains two parallel LVDS input ports consisting of 14 differential LVDS signals DB[13:0]. In addition to the LVDS data lines, there are four other LVDS signals: SYNC_IN_x, SYNC_OUT_x, DATACLOCK_OUT (DCO_x), and DATACLK_IN (DCI_x). A top level diagram of the data receiver and controller is shown in Figure 84.

The timing optimization for both ports is performed by using a single DCI, and clocking of the external digital signal generator (such as FPGA and ASIC) is done using a single DCO.

The SYNC_IN_x and SYNC_OUT_x signals are used to synchronize multiple parts (see the Synchronization Controller section for more information). Each data port runs internally at half the speed of the DACCLK_x, and the two ports are subsequently multiplexed together to achieve the full DAC update rate.

Maximizing the opening of the eye in the DCI_x and data signals improves the reliability of the data port interface. The two sources of degradation that reduce the eye in the DCI_x and data signals are the jitter on these signals and the skew between them. Therefore, it is recommended that the DCI_x be generated in the same manner as the data signals with the same output driver and data line routing. DCI_x can be implemented as a 17th data line with an alternating (010101…) bit sequence.

The data receiver behaves like a shift register with a variable delay from one register to the next. The data receiver uses the clocks to the rising edge of the DCI_x to determine the proper data sampling time. Upon enabling the data receiver controller, the circuit searches for rising edges in both directions, selecting the closest rising edge. Upon finding the DCI_x rising edge, the receiver controller enters tracking mode. In tracking mode, the pre- and post-delay lines traverse the DCI_x edge to maintain lock and track variations. For proper circuit operation, the DCI_x and data inputs must maintain a minimum skew (dependent on frequency). The data receiver controller should be enabled after the synchronization controller and mu controller indicate a locked state.

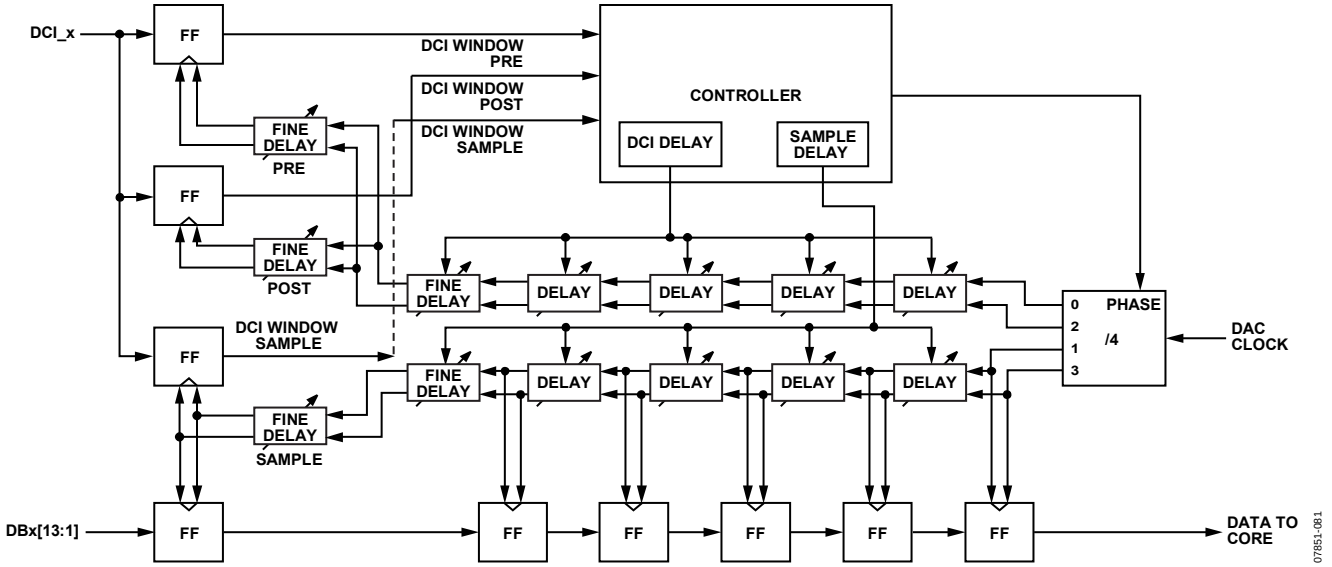


Figure 84. Top Level Diagram of the Data Receiver and Controller

CLOCKING THE AD9739

To provide the required signal swing for the internal clock receiver of the AD9739, it is necessary to use an external clock buffer chip to drive the DACCLK_P and DACCLK_N inputs. The recommended clock buffer for this application is the ADCLK914. This is an ultrafast clock buffer capable of providing 1.9 V out of each side into a 50 Ω load terminated to VCC (3.3 V) for a total differential swing of 3.8 V. This buffer also provides very low jitter, 100 FS random jitter, which is important for optimal ac performance in the AD9739.

A functional block diagram of the ADCLK914 is shown in Figure 85. Figure 86 shows the recommended schematic for the ADCLK914/AD9739 interface. See the ADCLK914 data sheet for more information.

For optimal ac performance out of the AD9739, the recommended minimum differential peak-to-peak voltage is approximately 1.4 VPP. The maximum allowable clock frequency is 2.5 GSPS and, due to internal timing requirements for the part, the minimum allowable clock frequency is 800 MSPS.

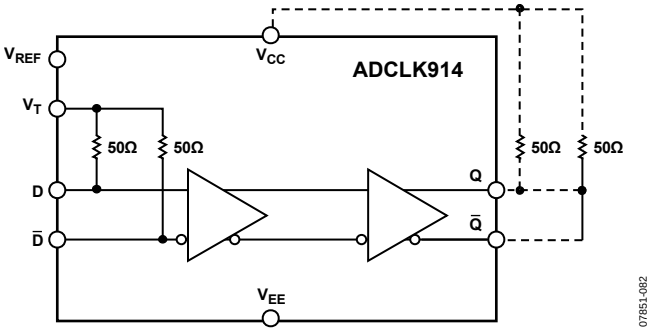


Figure 85. ADCLK914 Functional Block Diagram

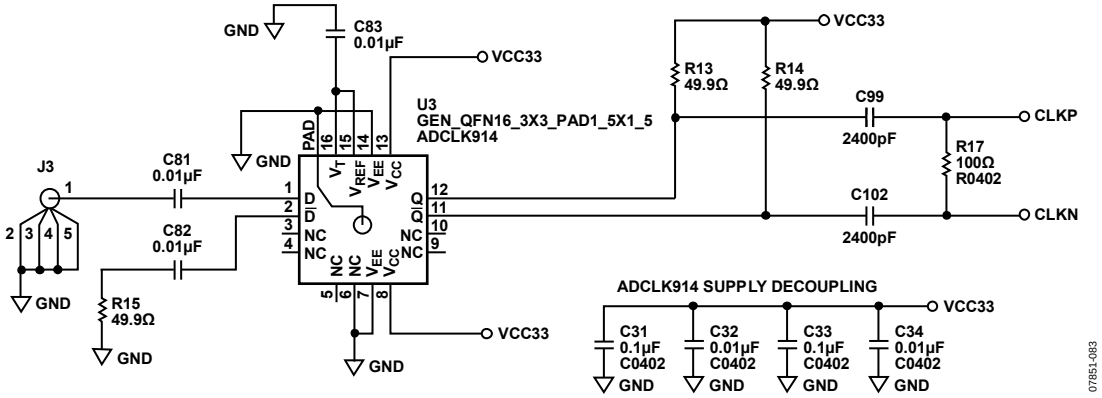


Figure 86. Recommended ADLCK914/AD9739 Interface Circuit

Clock Phase Noise Affects on AC Performance

The quality of the clock source driving the ADCLK914 determines the achievable ACLR performance for the AD9739. Table 32 summarizes the close-in ACLR for an eight-carrier DOCSIS signal at 920 MHz with respect to various phase noise profiles.

Table 32. Eight-Carrier DOCSIS Close-In ACLR Performance at 920 MHz for Various Phase Noise Profiles[1]

Band	Phase Noise Profile 1	Phase Noise Profile 2	Phase Noise Profile 3	Phase Noise Profile 4	Spec
750 kHz to 6 MHz	−68.5	−65	−61.1	−56	−59.3
6 MHz to 12 MHz	−68	−66.5	−64	−60	−61.8
12 MHz to 18 MHz	−68	−67.5	−67.3	−67.6	−64

[1]All ACLR numbers are specified in decibels relative to the carrier (dBc).

Table 33 shows the phase noise at various offsets for each profile.

Table 33. Phase Noise Summary for Each Profile[1]

Offset	Profile 1	Profile 2	Profile 3	Profile 4
1 kHz	−111.3	−109.3	−109.25	−107.5
10 kHz	−117.4	−115.9	−114.6	−114
100 kHz	−123.7	−120.3	−117.3	−114.4
1 MHz	−141.2	−125.8	−122	−115.6
10 MHz	−150.4	−147.2	−124.6	−117.9
100 MHz	−150.4	−150.3	−150.6	−150.6

[1]All phase noise numbers are specified in dBc/Hz.

To still meet the close-in ACLR requirements for the eight-carrier DOCSIS, the phase noise found in Profile 3 is the minimum requirement necessary.

APPLYING DATA TO THE AD9739

As explained in the LVDS Data Port Interface section, each data port runs internally at half the speed of the DACCLK_x, and the two ports are subsequently multiplexed together to achieve the full DAC update rate. If the user is creating a data file to load into the AD9739, this data file must be deinterleaved and applied to each port, as shown in Table 34.

Table 34. Application of Deinterleaved Files to Ports

Original Data File	Apply to DB0[13:0]	Apply to DB1[13:0]
DB0	Yes	No
DB1	No	Yes
DB2	Yes	No
DB3	No	Yes
DB4	Yes	No
DB5	No	Yes

A graphical representation of this can be seen in Figure 87. If the data pattern generator (DPG2) is being used to apply data to the part, the deinterleaving process can be done automatically via the software. Thus, the user can apply a single data file using the DPG2 and allow the software to do the deinterleaving and apply the correct data to each port.

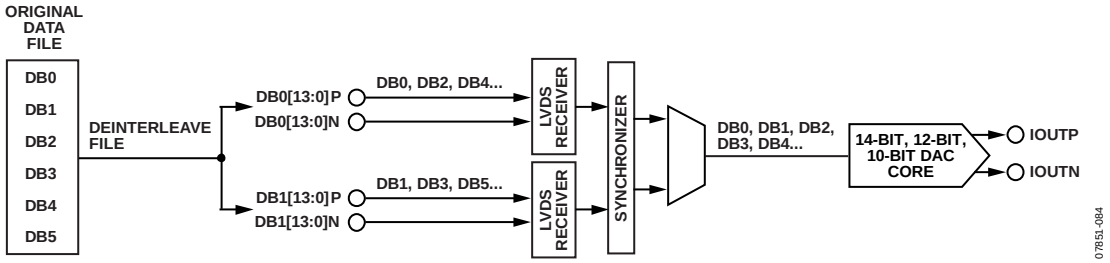


Figure 87. Graphical Representation of How to Present Data to the AD9739

MU DELAY CONTROLLER

The mu delay controller adjusts timing between the digital and analog blocks. The mu delay controller maintains phase relational information between the digital and analog clock domains. The control system continuously adjusts the mu delay to maintain the desired phase relationship between the digital and analog sections. A top level diagram of the mu delay controller within the DAC is shown in Figure 88.

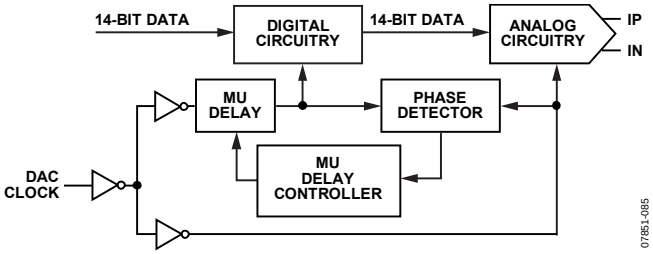


Figure 88. Mu Delay Controller Block Diagram

The mu delay controller has two modes of operation: initial phase search and phase tracking. In the phase search mode, the controller looks for the initial mu delay value to use before going into tracking mode. In tracking mode, the controller makes adjustments to the initial mu delay value to keep the phase at the desired value. The initial phase search is required because there may be multiple mu delay settings that give the desired phase, but the device may not operate correctly at all of the mu delay values.

MU CONTROL OPERATION

The mu delay controller is enabled via Register 0x26, Bit 0. Before enabling the controller, it is important to turn on both the phase comparator boost (Register 0x24, Bits[5:4]) and the mu delay controller duty cycle correction circuitry (Register 0x25, Bit 7). Both of these functions allow for more robust operation of the mu delay controller over the entire operating speed of the part. There are three modes of operation for the mu controller specified by the Mode[1:0], Bits[5:4] in Register 0x26, which are as follows:

- Search and track (0x0) (optimal setting)
- Track only (0x1)
- Search only (0x2)

Search Mode

The search algorithm begins at a specified mu delay value set via MUDEL[8:0] (MUDEL [0], Bit 7 in Register 0x27 and MUDEL[8:1], Bits[7:0] in Register 0x28). Even though there are nine bits of resolution for this delay line value, the maximum allowable mu delay is 432 (decimal). The optimal point to begin the search is in the middle of the delay line, that is, at approximately 216.

The initial search algorithm works by sweeping through different mu delay values until the desired phase is measured, which is specified by SetPhs, Bits[4:0] in Register 0x27, with the maximum allowable phase being 16. When the desired phase is measured, the slope of the phase measurement is calculated and compared against the desired slope, which is specified by the Slope bit in Register 0x26. A positive slope occurs when the measured phase increases as the mu delay increases. A negative slope occurs when the phase decreases as the mu delay increases.

For optimal ac performance, the desired setting for the search is a negative slope and a phase value of 6. If everything matches, the search algorithm is finished. The Search_Tol bit (Register 0x29, Bit 7) can be used to specify the accuracy of the search as follows:

- Not exact (0x0)—can find a phase within two values of the desired phase
- Exact (0x1)—finds the exact phase specified (optimal setting)

Figure 89 shows a typical plot of the mu phase vs. the mu delay line value at 2.4 GSPS. Starting at the selected mu delay value, the search direction can be specified via SrchMode[1:0], Bits[6:5] found in Register 0x27. There are three possible choices for the search.

- Down only (0x0)
- Up only (0x1)
- Alternating up and down (0x2) (optimal setting)

If the mode is alternating, the search proceeds in both directions until a programmable guard band is reached in one of the directions, as specified by Guard[4:0], Bits[4:0] in Register 0x29. When the guard band is reached, the search continues, only in the opposite direction. If the desired phase is not found before the guard band is reached in the second direction, then the search changes back to the alternating mode and continues looking in the guard band. The search fails if the mu delay controller reaches the endpoints. If the controller does not find the desired phase during the search, ContRst, Bit 5 in Register 0x29 determines the corrective action as follows:

- Continue (0x0)—continues to search (optimal setting)
- Reset (0x1)

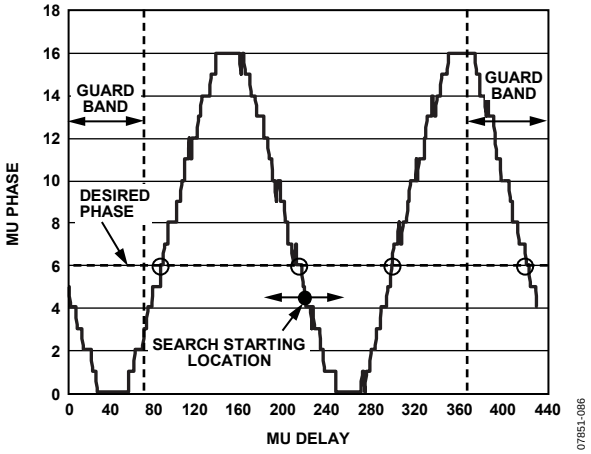


Figure 89. Typical Mu Phase Characteristic Plot @ 2.4 GSPS

To determine the correct slope, the controller measures the slope by first incrementing and then decrementing the mu delay value until any of the following happens:

- The phase changes by 2.
- The phase is equal to 16 (the maximum value).
- The phase is equal to 0 (the minimum value).
- The mu delay is 431 (the maximum value).
- The mu delay is 0 (the minimum value).

After both incrementing and then decrementing the mu delay value, the values of the measured phases are compared to determine if the slope matches the desired slope. To consider the slope valid, the positive direction phase and the negative direction phase must be on opposite sides of the desired phase. Figure 90 and Figure 91 contain examples of valid and invalid phase choice.

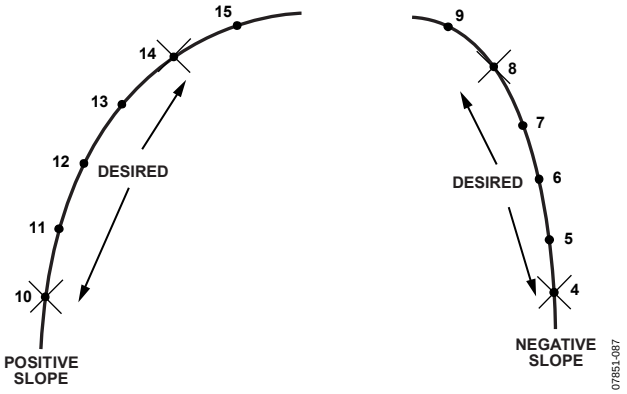


Figure 90. Valid Positive and Negative Slope Phase Examples

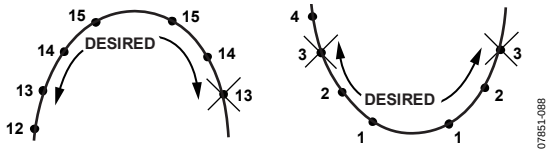


Figure 91. Invalid Slope Phase Examples

Track Mode

In tracking mode, a simple control loop is used to increment by 1, decrement by 1, or not change the mu delay value, depending on the measured phase. The control loop uses the desired slope to determine if the mu delay should be incremented or decremented. No attempt is made to determine if the actual slope has changed or is still valid.

Two status bits, MU_LKD (Register 0x2A, Bit 0) and MU_LOST (Register 0x2A, Bit 1) are available to the user to signal proper operation of the control loop. If the current phase is more than five steps away from the desired phase, the MU_LKD bit is cleared, and the MU_LOST bit is set if the lock acquired was previously set. Furthermore, if lock is lost, the controller has the option of remaining in the tracking loop or resetting and starting the search again.

Mu Delay and Phase Readback

By setting the read bit high (Register 0x26, Bit 3), the user can read back the mu delay value that the controller locked to by reading the MUDEL[8:0] bits and the phase it locked to by reading back the SetPhs[4:0] bits. These no longer read back the value the search started at or the desired phase. The MUDEL[8:0] bits should now read back the mu delay line value the controller locked to and the phase it locked to. The typical locking time for the mu controller is approximately 180 K DAC cycles (at 2 GSPS ~ 75 µs).

Operating the Mu Controller Manually

To manually control the mu delay, the user must sweep through all of the mu delay values and the record phase value at each value of MUDEL, as shown in Figure 89. In manual mode, it is recommended to enable the phase comparator boost (Register 0x24, Bits[5:4]) and the mu delay controller duty cycle correction circuitry (Register 0x25, Bit 7). Every time the MUDEL value is stepped, the read bit must be set high to read the corresponding phase for the specified mu delay line value. It is not possible to keep the read bit high and continuously read back the phase value. As is the case with auto mode, the optimal ac performance occurs at a negative slope and a phase of 6; therefore, when the curve is complete, choose the MUDEL value that corresponds to this condition and write that value into the MUDEL[8:0] bits.

Instead of manually sweeping through all of the mu delay values, it is possible to set the Mode[1:0] bits to 0x2 and search only for the mu delay value for the specified phase. In this case, the mu enable bit must be set high to perform the search.

The user then needs to occasionally monitor the phase and make adjustments to maintain an optimal phase relationship. Another option is to set the Mode[1:0] bits to 0x1 to allow the controller to track only from the specified mu delay value. In this case, the mu enable bit must be set high to perform the tracking.

Calculating Mu Delay Line Step Size

Stepping through all of the mu delay line values and plotting mu phase vs. mu delay not only allows the user to find the optimal mu delay value but also allows the user to determine the mu delay line step size. To calculate the step size, take one full cycle of the mu phase curve and divide the period of the DAC clock by this delta. From Figure 89, the two transition points are approximately 56 and 270, providing a delta of approximately 214 steps. Therefore, the mu delay line step size is

$$\frac{1}{\frac{2.4e9}{24}} = 1.95\,\text{ps}$$

Or approximately 2 ps/step. If the mu delay controller is enabled, this value allows the user to calculate how much drift is in their system (in picoseconds) with respect to the DAC clock period over temperature.

SYNCHRONIZATION CONTROLLER

A top level diagram of the synchronization circuitry and controller is shown in Figure 92. The synchronization circuitry requires a sync signal into the DAC (SYNC_IN_x) to set the clock divider. The frequency of the SYNC_IN_x signal must be 1/4 the DACCLK_x frequency (that is, for DACCLK_x = 2.5 GSPS, the SYNC_IN_x signal must be 625 MSPS). The SYNC_IN_x signal can be provided externally; however, it is recommended to use the SYNC_OUT_x signal provided by the master DAC through a fanout chip to all DACs in the system (including the master). Using the SYNC_OUT_x signal from the DAC allows for continuous adjustment over temperature for proper SYNC_IN_x position. The synchronization circuitry has two modes of operation, master and slave. In master mode, the sync operation starts an initialization phase that determines the proper position of the SYNC _IN_x signal by adjusting the SYNC_ OUT_x delay line. When the SYNC_IN_x position is locked, the master selects the correct SYNC_OUT_x phase (and, consequently, SYNC_IN_x). After SYNC_IN_x is placed in the center of the sampling window, and the appropriate phase is selected, the clock divider phase is adjusted, and the master controller enters tracking mode to maintain the SYNC_IN_x position across temperature.

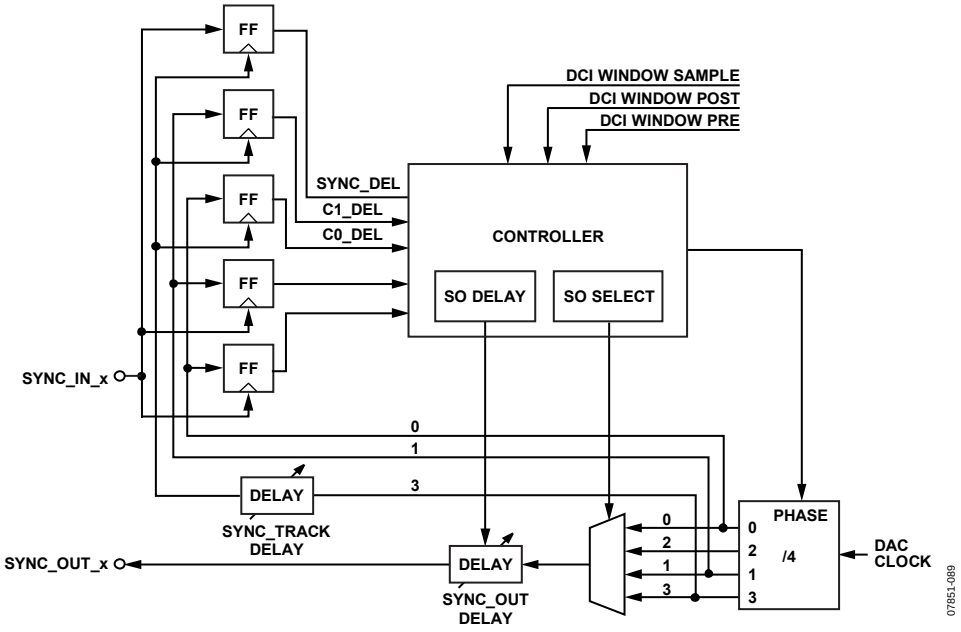


Figure 92. Top Level Block Diagram of Synchronization Circuitry and Controller

Operation in Master Mode

Setting Register 0x10, Bit 5 high sets the controller to master mode. This enables the sync logic to enter an initialization phase that adjusts the SYNC_OUT_x delay. By moving the SYNC_OUT_x delay, the SYNC_IN_x sampling point is moved and the edge transitions of Phase 0 and Phase 1 clocks can be determined. After the edges are found, the SYNC_OUT_x delay line is adjusted such that the SYNC_IN_x sampling point is now placed in the center, away from the edge transitions, as shown in Figure 93.

The sync controller also attempts to automatically select a phase for the SYNC_OUT_x signal that is closest to the DCI. This operation is performed to eliminate the arbitrary phase relationship of the clock divider upon power-up. After the SYNC_OUT_x delay is set and the phase is determined, the master performs a clock divider phase rotation and enters tracking mode.

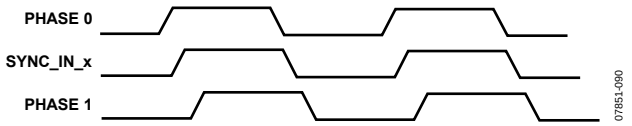


Figure 93. Optimal Placement of SYNC_IN_X

In tracking mode, the master cycles the sync track delay line and stores the delay values for the first phase edge, the SYNC_IN_x edge, and the second phase edge. These signals are only stored internally and are not accessible via the SPI. Ideally, the SYNC_IN_x position is exactly between two phases. The controller automatically adjusts the SYNC_OUT_x delay to keep the SYNC_IN_x edge centered. This operation is continuously performed in the background, and the SYNC_OUT_x delay line is adjusted to maintain proper positioning. The controller loop is shown in Figure 94.

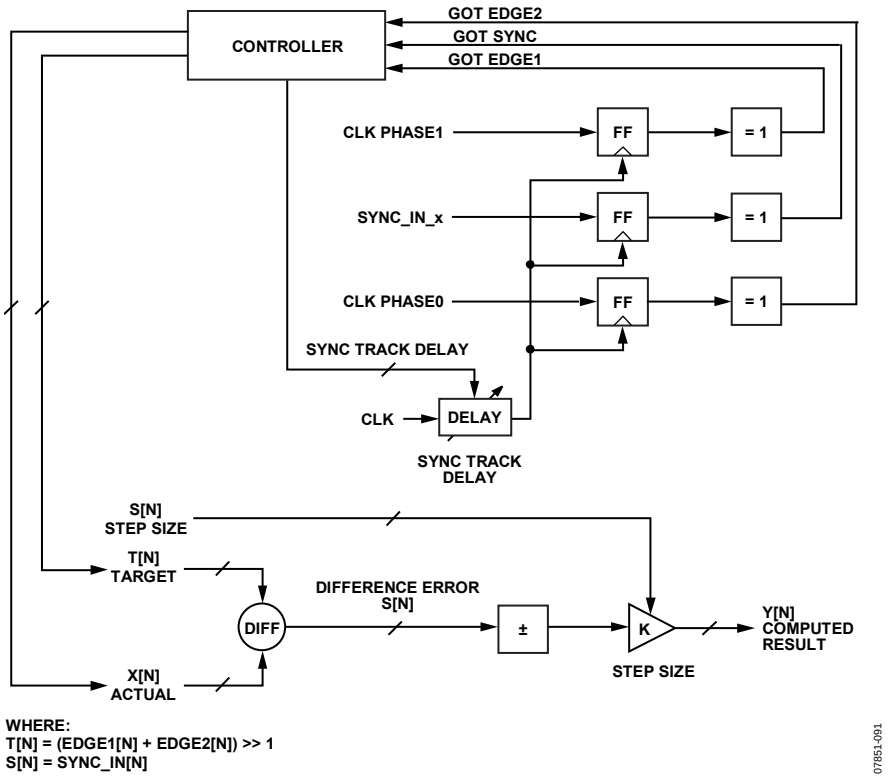


Figure 94. Synchronization Controller Track Mode Computation Block Diagram

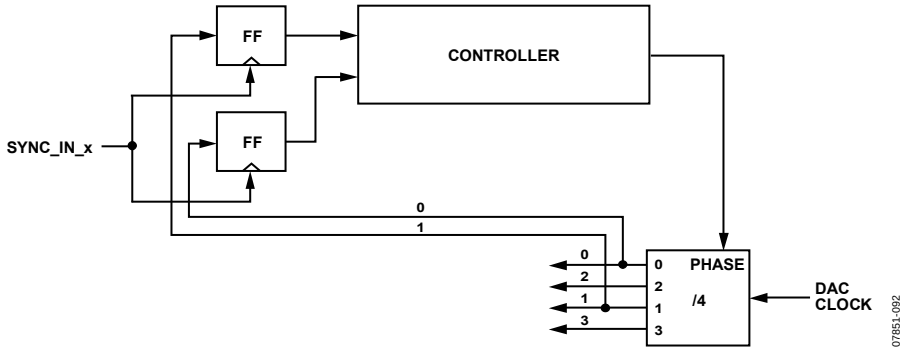


Figure 95. Slave Mode Tracking Mode Block Diagram

Status bits are available in the SPI to verify that the synchronization controller has found lock (Register 0x21, Bit 4), that the synchronization controller has entered tracking mode (Register 0x21, Bit 7), and whether the controller has lost lock (Register 0x21, Bit 5). These bits should be polled periodically to check the status of the controller. In addition, the user can verify that the SYNC_IN clock is positioned correctly by reading back the state of SYNC_SAMP1 (Register 0x0D, Bit 5) and SYNC_SAMP0 (Register 0x0D, Bit 4). If the SYNC_IN clock is positioned correctly, SYNC_SAMP1 should read back a 1 and SYNC_SAMP0 should read back a 0.

To ensure that all of the slaves are locked on correctly to the master, verify the SYNC_SAMP1 and SYNC_SAMP0 bits to ensure that the SYNC_IN_x signal has been properly placed. To guarantee that multiple slave parts all lock correctly to one master clock, care must be taken to ensure that the skew between the DACCLK_x and SYNC_IN_x signals is not more than 200 ps. If the skew is greater than this, it is possible that not all of the slave parts will lock onto the same delay setting from the master, and additional external delay lines may need to be used to ensure that the SYNC_IN_x signals are positioned correctly.

Operation in Slave Mode

When the controller is enabled in slave mode, the synchronization logic simply samples the clock divider phases. The controller uses the sampled clock divider phases to compute a new clock divider phase rotation. This operation is shown in Figure 95. For the slave parts to track correctly, the SYNC_OUT_x signal must be controlled from the master and used as an input signal into the SYNC_IN clock.

DATA RECEIVER OPERATION IN AUTO MODE

The receiver controller is enabled by setting the RCVR_CNT_ENA bit high (Register 0x10, Bit 0). After this bit is set, the controller enters search mode. The search mode attempts to find the rising edge of the DCI by adjusting the delay line. The search begins by increasing the delay line from a user-defined starting point until the rising edge of the DCI is found. This is followed by another search, starting from the same user-defined point, decreasing the delay line until the other rising edge of the DCI is found. The controller selects the closest rising edge, and the controller then enters tracking mode. The starting delay value can be programmed via the SPI using the DCI_DEL bits found in Register 0x13 and Register 0x14, allowing the user to bias the closest edge selection. This value should also be programmed into the SMP_DEL bits found in Register 0x11 and Register 0x12. To optimize the search, it is recommended to either set the DCI_DEL bits to 0 and search up or start the DCI_DEL bits at the midpoint and search up and down.

Tracking mode uses two sampling clocks to traverse the rising edge of DCI. The pre sample clock should always sample DCI low. The post sample clock should always sample DCI high. The controller uses the samples from the pre and post registers to adjust the delay lines and maintain lock with the user DCI, as shown in Figure 96. The skew between the pre- and post-sample clocks is user adjustable via the FINE_DEL_SKW[3:0] bits (Register 0x13, Bits[3:0]). The value of the FINE_DEL_SKEW bits determines how closely the controller tracks the rising edge of DCI and, indirectly, the speed of the loop. Each step of the FINE_DEL_SKW bits is 20 ps, allowing for a total skew of 300 ps. Each of the delay lines has a 1 ns range for a total adjustment range of ±2 ns.

The tracking controller operates continuously in the background. Monitoring the status of DCI_PRE_PH0 (Register 0x0C, Bit 2) and DCI_PST_PH0 (Register 0x0C, Bit 0) allows the user to verify whether the sampling of the DCI is occurring correctly. If the delay settings are correct, the state of DCI_ PRE_PH0 should be 0 and the state of DCI_PST_PH0 should be 1.

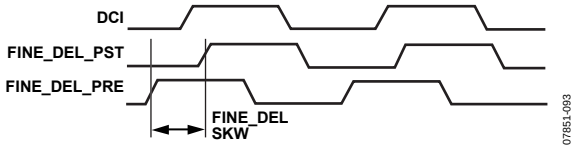


Figure 96. Pre- and Post-Delay Sampling Diagram

The search and tracking modes use Clock Phase 0 to lock onto the DCI. When the controller is locked, Clock Phase 1 is placed in the center of the data sampling period. Figure 97 shows the clock and DCI phase relationships.

The data receiver controller can be set up to loop when an error occurs by setting the RCVR_LOOP_ON bit in the SPI (Register 0x10, Bit 1). If this bit is set, the controller generates an IRQ and restart, beginning with the clock phase determination, followed

by the DCI transition detection, and then back into track mode. Status bits are available in the SPI to verify that the receiver controller has found lock (Register 0x21, Bit 0), that the receiver controller has entered tracking mode (Register 0x21, Bit 3), and whether the controller has lost lock (Register 0x21, Bit 1).

With the synchronization controller off or with the part in slave mode, the LVDS controller typically locks in 70 K DAC cycles (at 2 GSPS ~ 35 µs). The worst-case locking time is 135 K DAC cycles (at 2 GSPS ~ 67.5 µs). With the synchronization controller on and the part in master mode, the LVDS controller typically locks in 301 K DAC cycles (at 2 GSPS ~ 150 µs). The worst-case locking time is 555 K DAC cycles (at 2 GSPS ~ 277.5 µs).

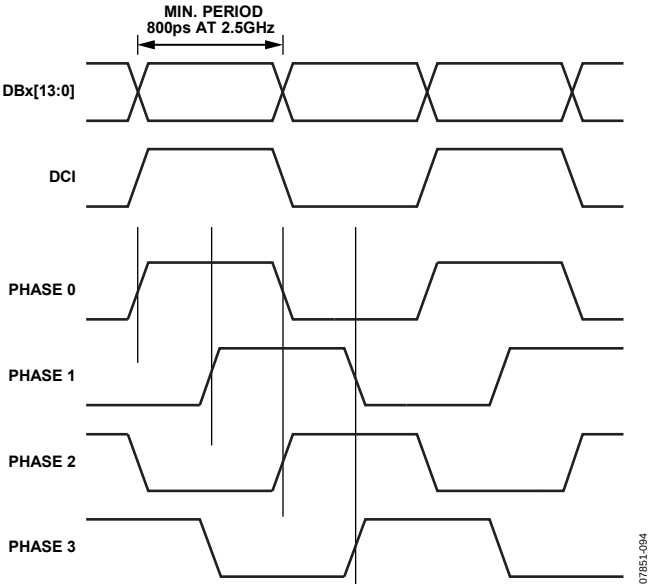


Figure 97. Phase Relationship of Clocks During Locked Receiver State

DATA RECEIVER OPERATION IN MANUAL MODE

If the receiver controller is disabled, the timing adjustments can be done manually. The user must adjust the DCI_DEL bits in Register 0x13 and Register 0x14 and monitor the DCI_PRE_PH0 bit (Register 0x0C, Bit 2) or the DCI_PST_PH0 bit (Register 0x0C, Bit 0) to determine where the DCI rising edge occurs. If there is no skew programmed in the FINE_DEL_SKW bits, then both the DCI_PRE_PH0 bit and the DCI_PST_PH0 bit transition at the same time. When the delay setting is found, the optimal value must be written to the DCI_DEL bits. This same delay value also must be applied to the SMP_DEL bits (Register 0x11 and Register 0x12) to set the proper sampling point for the Phase 1 clock, which is used to sample the incoming data into the DAC core.

Because the controller is off, there is no tracking of the DCI_x signal; therefore, the user must monitor the DCI_PST_PH0 and DCI_PRE_PH0 bits periodically to determine if the timing has shifted due to temperature or other causes. In addition to monitoring these bits, it is also important to ensure that the handoff timing between the flip flops in the data path is valid. As shown in Figure 84, the optimal sample delay value is split between these flip flops in the data path. If the timing in any one of these stages is violated, one of the status bits in Register 0x0B (HNDOFF_Fall[3:0] or HNDOFF_Rise[3:0]) reads back a value of 1. If this occurs, it is necessary to adjust the sample delay and, in turn, the DCI delay so as to not violate the timing between these flip flops. When the new sample delay value is found, the HNDOFF check bits can be reset by setting the HNDOFF_CHK_RST bit high (Register 0x0A, Bit 3).

Calculating the DCI Delay Line Step Size

To calculate the DCI delay line step size, the user must step through all the values of the DCI delay line manually and record the state of DCI_PRE_PH0. A typical plot of this measurement at 2.4 GSPS is shown in Figure 98

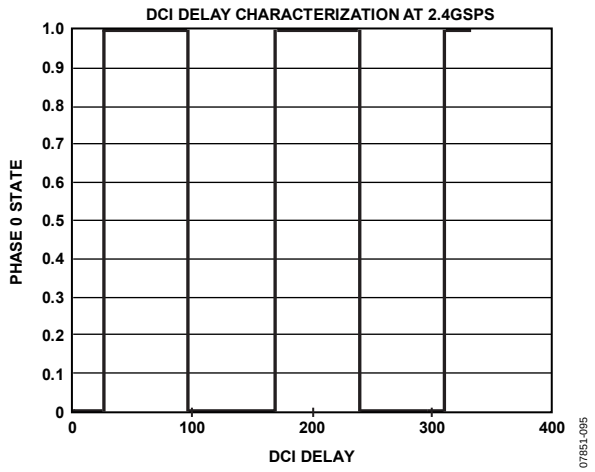


Figure 98. DCI Delay Line Step Size Measurement

To calculate the step size, take the transition points of the Phase 0 state curve and divide the period of the DCI clock (1/2 of the DAC clock rate) by this delta. As shown in Figure 98, two transition points are approximately 26 and 97, providing a delta of approximately 71 steps. Therefore, the DCI delay line step size is

$$\frac{1}{\frac{1.2e9}{71}} = 11.65\,ps$$

Or approximately 12 ps/step.

MAXIMUM ALLOWABLE DATA TIMING SKEW/JITTER

The maximum allowable skew and jitter out of an FPGA with respect to the DDR DCI clock edge on each LVDS port is calculated as

$$MaxSkew + Jitter = Period(\text{ns}) - ValidWindow(\text{ps}) - Guard$$

The minimum LVDS valid window is approximately 344 ps, as shown in Table 2, and a guard of 100 ps is recommended. Therefore, at the maximum operating frequency of 2.5 GSPS, the maximum allowable FPGA skew plus jitter is equal to

MaxSkew + *Jitter* = 800 ps – 344 ps – 100 ps

MaxSkew + *Jitter* = 456 ps

OPTIMIZING THE CLOCK COMMON-MODE VOLTAGE

To optimize the interface and handoff timing, there is an additional system that sets the common-mode voltage of the clock, which can be used to properly align the crossing point of the DACCLK_P and DACCLK_N signals to ensure that the duty cycle of the clock is set properly. Figure 99 shows how the common-mode voltage of DACCLK_P and DACCLK_N is set. Eight switches controlled by the SPI bits, CLKP_OFFSET[3:0] (Register 0x22, Bits[3:0]) and CLKN_OFFSET[3:0] (Register 0x23, Bits[3:0]), for both the DACCLK_P and DACCLK_N signals.

The DIR_P (Register 0x22, Bit 4) and DIR_N (Register 0x23, Bit 4) bits determine the direction of the adjustment. If DIR_P/DIR_N is low, the common-mode voltage decreases with the CLKP_OFFSET/CLKN_OFFSET values. If DIR_P/DIR_N is high, the common-mode voltage increases with the CLKP_OFFSET/CLKN_OFFSET values, as shown in Figure 100. When both CLKP_OFFSET and CLKN_OFFSET bits are set to zero, the feedback path forces the common-mode voltage to be set to approximately 0.9 V. The optimal ac performance occurs at a setting of −15 on both the CLKP and CLKN offset bits.

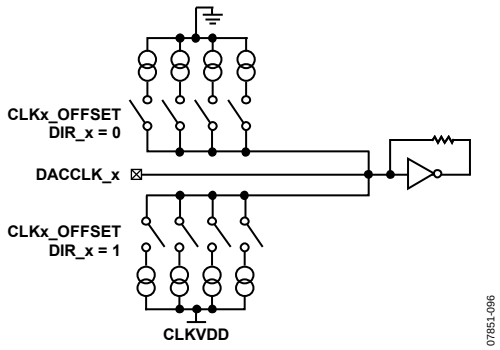


Figure 99. Clock Common-Mode Control

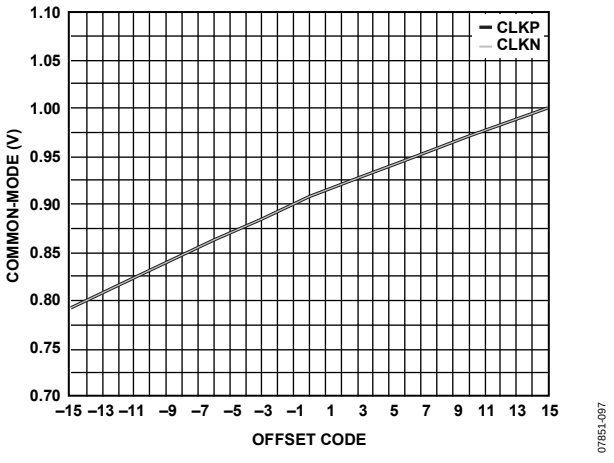


Figure 100. Common-Mode Voltage with Respect to CLKP_OFFSET/CLKN_OFFSET and DIR_P/DIR_N

ANALOG CONTROL REGISTERS

The AD9739 includes some registers for optimizing its analog performance. These registers include noise reduction in the output current mirror and output current mirror headroom adjustments.

MIRROR ROLL-OFF FREQUENCY CONTROL

Using MSEL[1:0] (Register 0x33, Bits[1:0]), the user can adjust the noise contribution of the internal current mirror to optimize the 1/f noise. Figure 101 shows the MSEL bits vs. the 1/f noise with 20 mA full-scale current into a 50 Ω resistor.

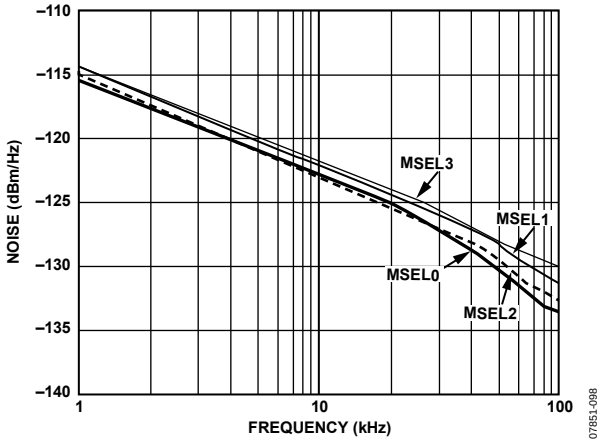


Figure 101. 1/f Noise with Respect to the MSEL Bits

VOLTAGE REFERENCE

The AD9739 output current is set by a combination of digital control bits and the I120 reference current, as shown in Figure 102.

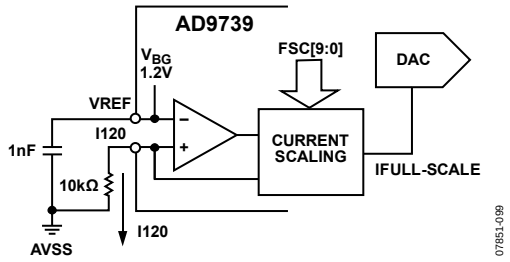


Figure 102. Voltage Reference Circuit

The reference current is obtained by forcing the band gap voltage across an external 10 kΩ resistor from I120 (Pin B14) to ground. The 1.2 V nominal band gap voltage (VREF) generates a 120 µA reference current in the 10 kΩ resistor. This current is adjusted digitally by FSC[9:0] (Register 0x06 and Register 0x07) to set the output full-scale current I_{FS}.

$$IOUTFS = 0.0226 \times FSC[9:0] + 8.5845$$

The full-scale output current range is approximately 8 mA to 31 mA for register values from 0x000 to 0x3FF. The default value of 0x200 generates 20 mA full scale. The typical range is shown in Figure 103.

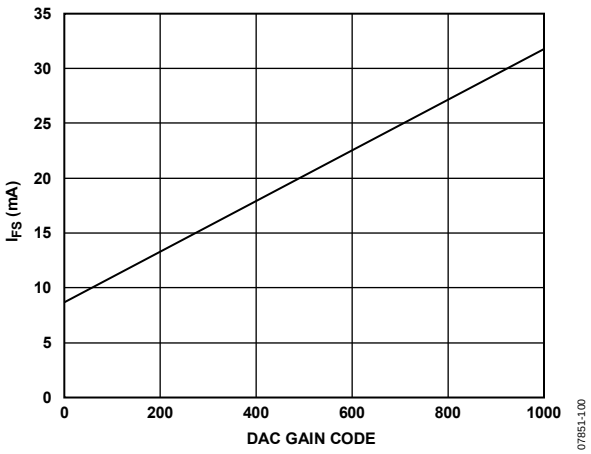


Figure 103. IFS vs. DAC Gain Code

Always connect a 10 kΩ resistor from the I120 pin to ground and use the digital controls to vary the full-scale current. The AD9739 is not a multiplying DAC. Applying an analog signal to I120 is not supported.

VREF (Pin C14) must be bypassed to ground with a 1 nF capacitor. The band gap voltage is present on this pin and can be buffered for use in external circuitry. The typical output impedance is near 5 kΩ. An external reference can be used to overdrive the internal reference by connecting it to the VREF pin (Pin C14). IPTAT (Pin D14) can be used to track the internal temperature of the chip by monitoring the output current of this pin. The output current is approximately 10 μA at 25°C with a slope of approximately 20 nA/°C.

ANALOG OUTPUTS

The AD9739 provides complementary current outputs, IOUTP and IOUTN. IOUTP provides a near full-scale current output, I_{OUTFS}, when all bits are high (DAC CODE = 16,383), while IOUTN provides the DAC dc offset. Due to the quad switch architecture, the dc offset of the AD9739 is approximately 1/16 of the DAC full-scale current. The current output appearing at IOUTP and IOUTN is a function of both the input code and the I_{OUTFS} and can be expressed as

$$IOUTP = \left(\frac{DACCODE}{16384}\right) \times I_{OUTFS} \quad (2)$$

$$IOUTN = \left(\frac{16383 - DACCODE}{16384}\right) \times I_{OUTFS} \quad (3)$$

where DAC CODE = 0 to 16,383 (decimal) and IOUTFS is found using Equation 1.

Figure 104, Figure 105, and Figure 106 contain plots for FSC[9:0] equal to 0.512 and 1023 to show the equivalent gain and offset values for the midpoints and endpoints of the full-scale gain transfer curve.

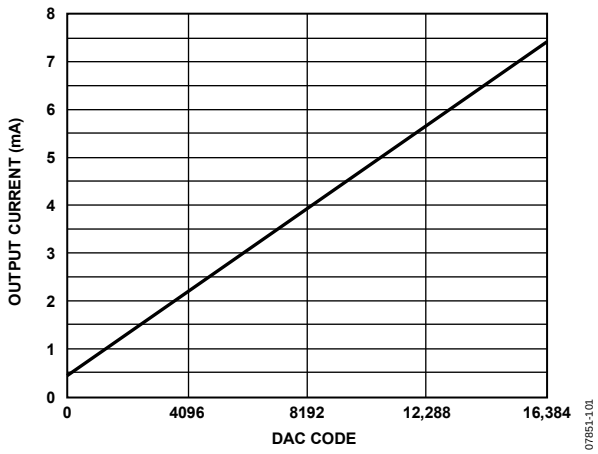


Figure 104. Gain Curve for FSC[9:0] = 0, DAC OFFSET = 0.257 mA

Figure 105. Gain Curve for FSC[9:0] = 512, DAC OFFSET = 1.228 mA

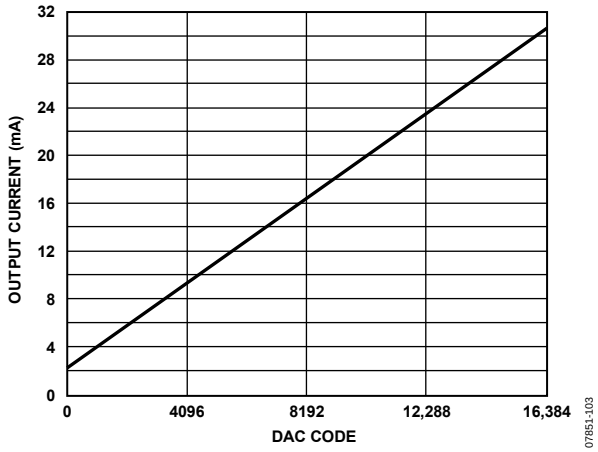


Figure 106. Gain Curve for FSC[9:0] = 1023, DAC OFFSET = 1.932 mA

The complementary current outputs can be configured for single-ended or differential operation. IOUTP and IOUTN can be converted into complementary single-ended voltage outputs using load resistors.

The differential voltage existing between IOUTP and IOUTN can also be converted to a single-ended voltage via a transformer or differential amplifier configuration. Internal to the AD9739 is a differential resistance between IOUTP and IOUTN that must be factored into the calculations for the voltage output and impedance out of the DAC. The approximate impedance between the outputs is 70 Ω.

Depending on the mode of operation and desired signal, the output stage can be configured in several ways for optimal ac performance. Figure 107 shows the optimal output network when measuring the signal in normal mode (baseband). Figure 108 shows the optimal output network when measuring the signal in mix mode (second or third Nyquist zone). The bandwidth of the ADT2T-1T-1P center tap transformer is not sufficient to support mix mode outputs; therefore, the best solution is to use the balun by itself.

Finally, when measuring DOCSIS performance, it is necessary to use a filter between the DAC and the transformer to control the impedance and help to decrease the folded back harmonics for higher frequency outputs. The optimal transformer for DOCSIS measurements is the JTX-2-10T, which is a balun and center-tapped transformer in one package. This output stage is shown in Figure 109.

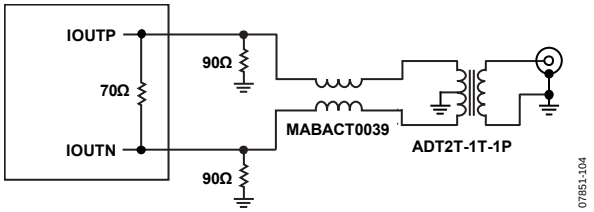


Figure 107. Recommended Transformer Output Stage for Normal Mode

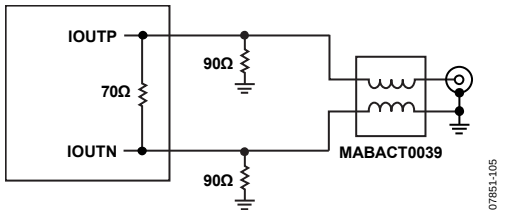


Figure 108. Recommended Transformer Output Stage for Mix Mode

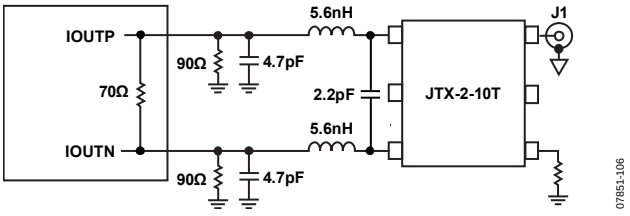


Figure 109. Recommended Transformer Output Stage for DOCSIS Measurements

INTERRUPT REQUESTS

There following six interrupt requests (IRQ) can be used for additional verification of the status of each controller.:

- Receiver locked
- Receiver lost lock
- Mu controller locked
- Mu controller lost lock
- Sync controller locked
- Sync controller lost lock

Each IRQ is enabled using the enable bits in the interrupt mask register (IMR), Register 0x03 (IRQ_En). The status of the IRQ can be measured in one of the following ways: via the SPI bits found in the interrupt service request register (IST), Register 0x04 (IRQ_Req) or using the IRQ pin (Pin F13).

If the pin is used to determine that an interrupt has occurred, it is also necessary to check Register 0x04 to determine which bit caused the interrupt because the pin can only indicate that an interrupt has occurred. To clear an IRQ, it is necessary to write a 1 to the bit in Register 0x04 that caused the interrupt. A detailed diagram of the interrupt circuitry is shown in Figure 110.

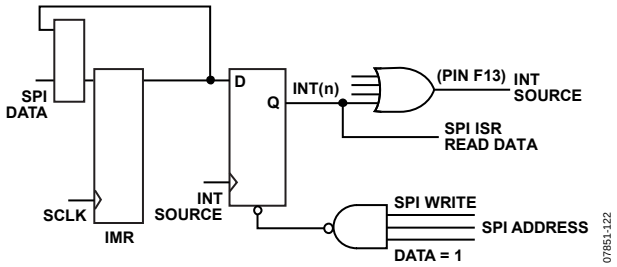


Figure 110. Interrupt Request Circuitry

RECOMMENDED START-UP SEQUENCE

The steps necessary to optimize the performance of the part and generate an output waveform are as follows:

1. Enable clocks to the controller and set the full-scale current. The registers and bits used in this step are shown in Table 35. Recommended values for the bits are in parentheses.

Table 35.

Register	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Recommended Value
CNT_CLK_Dis	0x02	02	N/A	N/A	N/A	N/A	CLKGEN_PD (0)	N/A	REC_CNT_CLK (1)	MU_CNT_CLK (1)	0x03
FSC_1	0x06	06	FSC[7] (0)	FSC[6] (0)	FSC[5] (0)	FSC[4] (0)	FSC[3] (0)	FSC[2] (0)	FSC[1] (0)	FSC[0] (0)	0x00
FSC_2	0x07	07	Sleep (0)	N/A	N/A	N/A	N/A	N/A	FSC[9] (1)	FSC[8] (0)	0x02

[1]The two-digit number is the decimal representation of the address.

2. Select the decoder mode. Recommended values for the bits are in parenthesis in Table 36, Table 37, and Table 38.

Table 36. Normal Mode

Register	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Recommended Value
Decoder_CNT	0x08	08	N/A	N/A	N/A	N/A	N/A	N/A	DAC_DEC[1] (0)	DAC_DEC[0] (0)	0x00

[1]The two-digit number is the decimal representation of the address.

Table 37. RZ Mode

Register	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Recommended Value
Decoder_CNT	0x08	08	N/A	N/A	N/A	N/A	N/A	N/A	DAC_DEC[1] (0)	DAC_DEC[0] (1)	0x01

[1]The two-digit number is the decimal representation of the address.

Table 38. Mix Mode

Register	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Recommended Value
Decoder_CNT	0x08	08	N/A	N/A	N/A	N/A	N/A	N/A	DAC_DEC[1] (1)	DAC_DEC[0] (0)	0x02

[1]The two-digit number is the decimal representation of the address.

3. Set the cross control to the optimal setting. Recommended values for the bits are in parenthesis in Table 39.

Table 39.

Register	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Recommended Value
CROS_CNT1	0x22	34	N/A	N/A	N/A	DIR_P (0)	CLKP_OFFSET [3] (1)	CLKP_OFFSET [2] (1)	CLKP_OFFSET[1] (1)	CLKP_OFFSET[0] (1)	0x0F
CROS_CNT2	0x23	35	N/A	N/A	N/A	DIR_N (0)	CLKN_OFFSET [3] (1)	CLKN_OFFSET [2] (1)	CLKN_OFFSET[1] (1)	CLKN_OFFSET [0] (1)	0x0F

[1]The two-digit number is the decimal representation of the address.

4. Enable the mu controller and ensure that it locks. Recommended values for the bits are in parenthesis in Table 40. To optimize and lock the mu controller, it is only necessary to have the DAC clock running; no data need be presented to the DAC to optimize this controller. It is recommended to write to Register 0x26 last, after all other mu controller registers in the table are written to, to ensure that the controller is set up correctly before it is enabled.

Table 40.

Register	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Recommended Value
PHS_DET	0x24	36	N/A	N/A	PHS_DET AUTO_EN (1)	CMP_BST (1)	Bias[3] (0)	Bias[2] (0)	Bias[1] (0)	Bias[0] (0)	0x30
MU_DUTY	0x25	37	MU_DUTY AUTO_EN (1)	POS/NEG (0)	ADJ[5](0)	ADJ[4] (0)	ADJ[3] (0)	ADJ[2] (0)	ADJ[1] (0)	ADJ[0] (0)	0x80
MU_CNT1	0x26	38	N/A	Slope (0)	Mode[1] (0)	Mode[0] (0)	Read (0)	Gain[1] (0)	Gain[0] (1)	Enable (1)	0x03
MU_CNT2	0x27	39	MUDEL[0] (0)	SrchMode[1] (1)	SrchMode [0] (0)	SetPhs[4] (0)	SetPhs [3] (0)	SetPhs [2] (1)	SetPhs [1] (1)	SetPhs[0] (0)	0x46
MU_CNT3	0x28	40	MUDEL[8] (0)	MUDEL[7] (1)	MUDEL[6] (1)	MUDEL[5] (0)	MUDEL [4] (1)	MUDEL[3] (1)]	MUDEL [2] (0)	MUDEL[1] (0)	0x6C
MU_CNT4	0x29	41	Search_Tol (1)	Retry (1)	ContRst (0)	Guard[4] (0)	Guard[3] (1)	Guard [2] (0)	Guard [1] (1)	Guard[0] (1)	0xCB

[1]The two-digit number is the decimal representation of the address.

The status readback bits for the mu controller, if the controller is locked, are as shown in Table 41.

Table 41.

Register	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Recommended Value
MU_STAT1	0x2A	42	N/A	N/A	N/A	N/A	N/A	N/A	MU_LOST (0)	MU_LKD (1)	0x01

[1]The two-digit number is the decimal representation of the address.

To read back the present mu delay and phase values, it is necessary to set the read bit high and then low before the values can be read back.

- Read—Register 0x26, Bit 3 (set high to read). For subsequent reads, this bit must be brought low, then high again. It cannot be left high to continuously read the MUDEL value.
- Mu delay readback—Register 0x28, Bits[7:0] and Register 0x27, Bit 7 (a total of nine bits in the readback; the maximum mu delay value is d432 or x1B0). This now represents the value the controller locked to, not the starting value of the search.
- MUD_PH_Readback, Register 0x27, Bits[4:0]—This represents the phase the controller is locked to.

There is a lower speed limit on the DAC clock. The mu controller was not designed to run at DAC clock speeds of 1 GHz and below. For applications in these frequency ranges, it is recommended that the mu controller be disabled completely.

5. If synchronizing multiple parts, enable the synchronization controller and ensure that it locks. If synchronization is not necessary, skip Step 5 and go to Step 6.

Table 42. Master Mode

Register	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Recommended Value
LVDS_REC_ CNT1	0x10	16	SYNC_ FLG_RST (0)	SYNC_ LOOP_ON (1)	SYNC_ MST/SLV (1)	SYNC_ CNT_ENA (1)	N/A	RCVR_ FLG_RST (0)	RCVR_ LOOP_ON (0)	RCVR_ CNT_ ENA (0)	0x70
LVDS_REC_ CNT6	0x15	21	SYNC_ GAIN[1] (0)	SYNC_ GAIN[0](1)	SYNCOUT_ PH[1](0)	SYNCOUT_ PH[0](0)	LCKTHR[3] (0)	LCKTHR[2] (0)	LCKTHR[1] (1)	LCKTHR[0] (0)	0x42

[1]The two-digit number is the decimal representation of the address.

Table 43. Slave Mode

Register	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Recommended Value
LVDS_REC_ CNT1	0x10	16	SYNC_ FLG_RST (0)	SYNC_ LOOP_ON (1)	SYNC_ MST/SLV (0)	SYNC_ CNT_ENA (1)	N/A	RCVR_ FLG_RST (0)	RCVR_ LOOP_ ON (1)	RCVR_ CNT_ENA (1)	0x50
LVDS_REC_ CNT6	0x15	21	SYNC_ GAIN[1](0)	SYNC_ GAIN[0](1)	SYNCOUT_ PH[1](0)	SYNCOUT_ PH[0](0)	LCKTHR[3] (0)	LCKTHR[2] (0)	LCKTHR[1] (1)	LCKTHR[0] (0)	0x42

[1]The two-digit number is the decimal representation of the address.

To verify that the sync controller is locked and tracking, the following bits must be read back:

- Register 0x21, Bit 4 (SYNC_LCK)—If the controller is locked, this bit reads back a value of 1. This is a value of 1 for the master part only. If the part is set up as a slave, this bit reads back 0.
- Register 0x21, Bit 7 (SYNC_TRK_ON)—If the controller is tracking, this bit reads back a value of 1. This is a value of 1 for the master part only. If the part is set up as a slave, this bit reads back 0.
- Register 0x21, Bit 5 (SYNC_LST_LCK)—If the controller is locked, this bit reads back a value of 0. If the controller comes out of lock, this bit reads back a value of 1. This bit is valid for the master part only.
- Register 0x0D, Bit 4 (SYNC_SAMP0)—If the controller is locked and the SYNC_IN signal is positioned correctly, this bit reads back a value of 0. This state is valid for both the master and slave parts.
- Register 0x0D, Bit 5 (SYNC_SAMP1)—If the controller is locked and the SYNC_IN signal is positioned correctly, this bit reads back a value of 1. This state is valid for both the master and slave parts.

6. Load the desired data pattern.
7. Enable the LVDS controller and ensure that it locks. If the synchronization controller is being used, keep the values from Step 5 in the registers and add the values in Table 44.

Table 44.

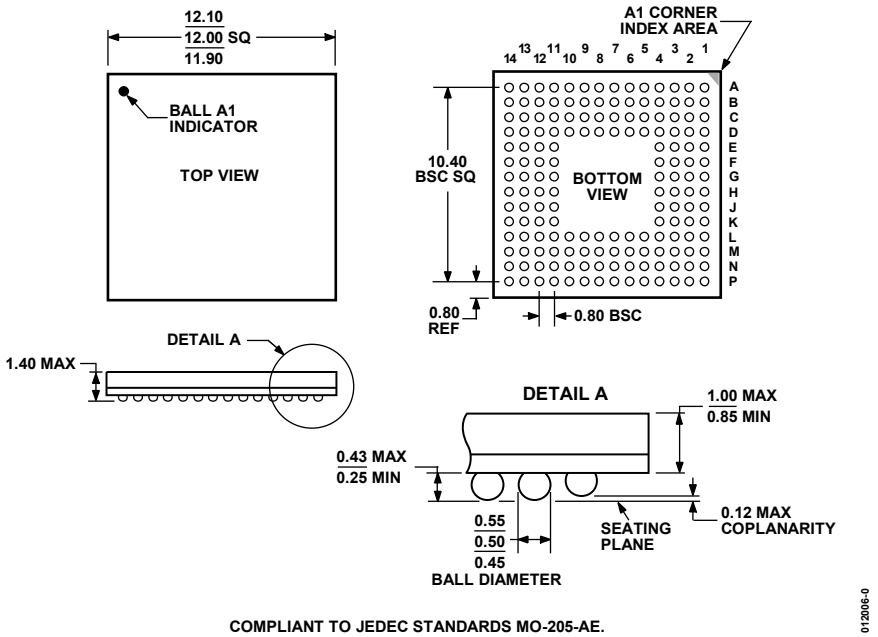
Register	Address[1]		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Recommended Value
LVDS_REC_CNT1	0x10	16	SYNC_FLG_RST (0)	SYNC_LOOP_ON (0)	SYNC_MST/SLV (0)	SYNC_CNT_ENA (0)	N/A	RCVR_FLG_RST (0)	RCVR_LOOP_ON (1)	RCVR_CNT_ENA (1)	0x03 (no sync) 0x73 (sync master) 0x53 (sync slave)
LVDS_REC_CNT2	0x11	17	SMP_DEL [1] (1)	SMP_DEL [0] (0)	FINE_DEL_MID[3] (0)	FINE_DEL_MID[2] (1)	FINE_DEL_MID[1] (1)	FINE_DEL_MID[0] (1)	RCVR_GAIN [1] (0)	RCVR_GAIN [0] (1)	0x9D
LVDS_REC_CNT3	0x12	18	SMP_DEL [9] (0)	SMP_DEL [8] (0)	SMP_DEL [7] (1)	SMP_DEL [6] (1)	SMP_DEL [5] (1)	SMP_DEL [4] (0)	SMP_DEL [3] (0)	SMP_DEL [2] (1)	0x29
LVDS_REC_CNT4	0x13	19	DCI_DEL [3] (0)	DCI_DEL [2] (1)	DCI_DEL [1] (1)	DCI_DEL [0] (0)	FINE_DEL_SKW[3] (0)	FINE_DEL_SKW[2] (0)	FINE_DEL_SKW[1] (1)	FINE_DEL_SKW[0] (0)	0x62
LVDS_REC_CNT5	0x14	20	CLKDIVPH [1]] (0)	CLKDIVPH [0] (0)	DCI_DEL[9] (0)	DCI_DEL [8] (0)	DCI_DEL [7] (1)	DCI_DEL [6] (0)	DCI_DEL [5] (1)	DCI_DEL [4] (0)	0x0A
LVDS_REC_CNT6	0x15	21	SYNC_GAIN[1](0)	SYNC_GAIN[0](1)	SYNCOUT_PH[1](0)	SYNCOUT_PH[0](0)	LCKTHR[3] (0)	LCKTHR[2] (0)	LCKTHR[1] (1)	LCKTHR[0] (0)	0x42
LVDS_REC_CNT7	0x16	22	N/A	SYNCO_DEL[6] (0)	SYNCO_DEL[5] (0)	SYNCO_DEL[4] (0)	SYNCO_DEL[3] (0)	SYNCO_DEL[2] (0)	SYNCO_DEL[1] (0)	SYNCO_DEL[0] (0)	0x00
LVDS_REC_CNT8	0x17	23	SYNCSH_DEL[0] (0)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_REC_CNT9	0x18	24	SYNCSH_DEL[8] (0)	SYNCSH_DEL[7] (0)	SYNCSH_DEL[6] (0)	SYNCSH_DEL[5] (0)	SYNCSH_DEL[4] (0)	SYNCSH_DEL[3] (0)	SYNCSH_DEL[2] (0)	SYNCSH_DEL[1] (0)	0x00

[1]The two-digit number is the decimal representation of the address.

To verify that the LVDS controller is locked, tracking, and sampling on the correct phase, the following bits must be read back:

- Register 0x21, Bit 0 (RCVR_LCK)—If the controller is locked, this bit reads back a value of 1.
- Register 0x21, Bit 3 (RCVR_TRK_ON)—If the controller is tracking this bit reads back a value of 1.
- Register 0x0C, Bit 5 (DCI_PHS3)—If the controller is locked on the correct phase and the data is sampling correctly, this bit reads back a value of 0.
- Register 0x0C, Bit 4 (DCI_PHS1)—If the controller is locked on the correct phase and the data is sampling correctly, this bit reads back a value of 1.
- Register 0x19, Bits [7:6] and Register 0x1A, Bits[7:0] (SMP_DEL[9:0])—This corresponds to the present sample delay value that the controller locked to. Continuous readback of these bits shows how the sample delay value changes to maintain proper sampling in the presence of temperature shifts in the system.
- Register 0x1B, Bits[7:6] and Register 0x1C, Bits[7:0] (DCI_DEL[9:0])—This corresponds to the present DCI delay value that the controller locked to. Continuous readback of these bits shows how the DCI value changes to maintain proper sampling in the presence of temperature shifts in the system.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-205-AE.

Figure 111. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-160-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9739BBCZ[1]	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9739BBCZRL[1]	−40°C to +85°C	160- Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9739BBC	−40°C to +85°C	160- Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9739BBCRL	−40°C to +85°C	160- Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9739-EBZ[1]		Evaluation Board for Normal Mode Evaluation	
AD9739-MIX-EBZ[1]		Evaluation Board for Mix Mode Evaluation	
AD9739-CMTS-EBZ[1]		Evaluation Board for CMTS Evaluation	

[1] Z = RoHs Compliant Part.

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