FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11436-1E

MEMORY Mobile FCRAM™

CMOS

32M Bit (2 M word × 16 bit)

Mobile Phone Application Specific Memory

MB82DP02183D-65L

CMOS 2,097,152-WORD x 16 BIT
Fast Cycle Random Access Memory
with Low Power SRAM Interface

■ DESCRIPTION

The Fujitsu MB82DP02183D is a CMOS Fast Cycle Random Access Memory (FCRAM*) with asynchronous Static Random Access Memory (SRAM) interface containing 33,554,432 storages accessible in a 16-bit format. MB82DP02183D is utilized using a Fujitsu advanced FCRAM core technology and improved integration in comparison to regular SRAM.

This MB82DP02183D is suited for mobile applications such as Cellular Handset and PDA.

*: FCRAM is a trademark of Fujitsu Limited, Japan

■ FEATURES

- Asynchronous SRAM Interface
- Fast Access Cycle Time : $t_{AA} = t_{CE} = 65$ ns Max
- 8 words Page Access Capability : $t_{PAA} = 20$ ns Max
- Low Voltage Operating Condition : $V_{DD} = +2.6$ V to $+3.5$ V
- Wide Operating Temperature : $T_A = -30$ °C to $+85$ °C
  $T_J = -30$ °C to $+90$ °C
- Byte Control by $\overline{LB}$ and $\overline{UB}$
- Low Power Consumption : $I_{DDA1} = 30$ mA Max
  $I_{DDS1} = 100$ µA Max
- Various Power Down mode : Sleep
  4M-bit Partial
  8M-bit Partial
- Shipping Form : Wafer/Chip

FUJITSU

■ PRODUCT LINEUP

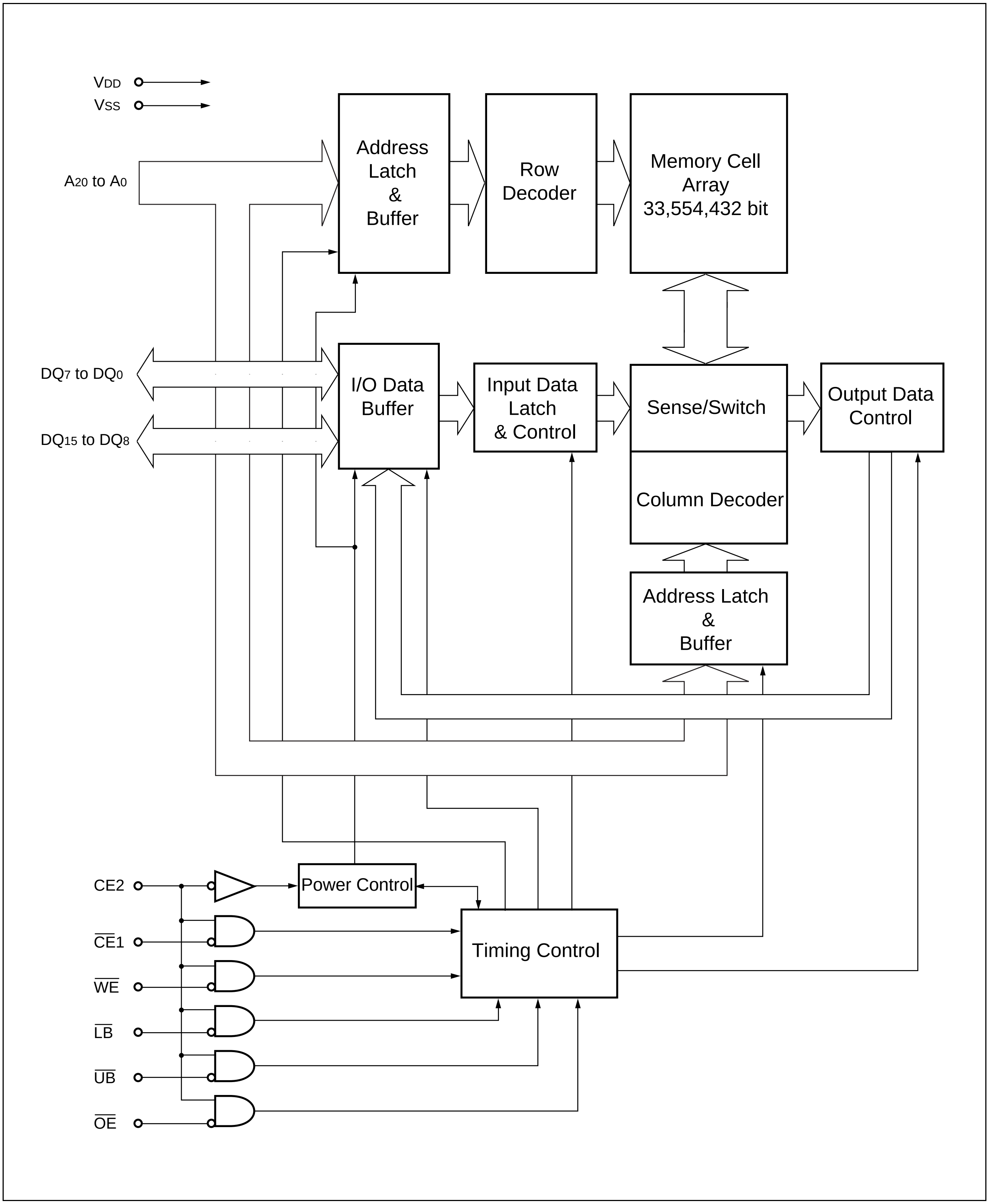
Parameter	MB82DP02183D-65L
Access Time (Max) (t_{CE}, t_{AA})	65 ns
Active Current (Max) (I_{DDA1})	30 mA
Standby Current (Max) (I_{DDS1})	100 µA
Power Down Current (Max) (I_{DDPS})	10 µA

■ PIN DESCRIPTION

Pin Name	Description
A_{20} to A_0	Address Input
$\overline{\text{CE}}$1	Chip Enable 1 (Low Active)
CE2	Chip Enable 2 (High Active)
$\overline{\text{WE}}$	Write Enable (Low Active)
$\overline{\text{OE}}$	Output Enable (Low Active)
$\overline{\text{LB}}$	Lower Byte Control (Low Active)
$\overline{\text{UB}}$	Upper Byte Control (Low Active)
DQ_7 to DQ_0	Lower Byte Data Input/Output
DQ_{15} to DQ_8	Upper Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground

Note : Refer to “■ PACKAGE FOR ENGINEERING SAMPLES” for additional pin descriptions of FBGA package supply.

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

Mode	CE2	$\overline{\text{CE1}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	A_{20} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z
Output Disable*[1]	H	L	H	H	X	X	*3	High-Z	High-Z
Output Disable (No Read)			H	L	H	H	Valid	High-Z	High-Z
Read (Upper Byte)					H	L	Valid	High-Z	Output Valid
Read (Lower Byte)					L	H	Valid	Output Valid	High-Z
Read (Word)					L	L	Valid	Output Valid	Output Valid
No Write			L	H*[4]	H	H	Valid	Invalid	Invalid
Write (Upper Byte)					H	L	Valid	Invalid	Input Valid
Write (Lower Byte)					L	H	Valid	Input Valid	Invalid
Write (Word)					L	L	Valid	Input Valid	Input Valid
Power Down*[2]	L	X	X	X	X	X	X	High-Z	High-Z

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance

*1 : Should not be kept this logic condition longer than 1 µs.

*2 : Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.
Data retention depends on the selection of Power Down Program. Refer to "■ Power Down" for the detail.

*3 : Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

*4 : $\overline{\text{OE}}$ can be V_{IL} during Write operation if the following conditions are satisfied;
(1) Write pulse is initiated by $\overline{\text{CE1}}$. Refer to "(12) READ/WRITE Timing #1-1 ($\overline{\text{CE1}}$ Control)" in "■ TIMING DIAGRAMS".
(2) $\overline{\text{OE}}$ stays V_{IL} during Write cycle.

■ POWER DOWN

Power Down

The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in power down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from power down mode.

This device has three power down modes, Sleep, 4M-bit Partial and 8M-bit Partial. The selection of power down mode can be programmed by series of read/write operation. Each mode has following data retention features.

Mode	Data Retention	Retention Address
Sleep (default)	No	N/A
4M-bit Partial	4M bits	00000h to 3FFFFh
8M-bit Partial	8M bits	00000h to 7FFFFh

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

Power Down Program Sequence

The program requires total six read/write operations with unique address. Between each read/write operation requires that device be in standby mode. Following table shows the detail sequence.

Cycle #	Operation	Address	Data
1st	Read	1FFFFFh (MSB)	Read Data (RDa)
2nd	Write	1FFFFFh	RDa
3rd	Write	1FFFFFh	RDa
4th	Write	1FFFFFh	Don’t care (X)
5th	Write	1FFFFFh	X
6th	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address (MSB).
The second and third cycles are to write to MSB. If the second or third cycle is written into the different address, the program is cancelled and the data written by the second or third cycle is valid as a normal write operation. It is recommended to write back the data (RDa) read by first cycle to MSB in order to secure the data.
The forth and fifth cycle is to write to MSB. The data of forth and fifth cycle are don’t-care. If the forth or fifth cycle is written into different address, the program is also cancelled but write data may not be written as normal write operation.
The last cycle is to read from a specific address key for power down mode selection. And read data (RDb) is invalid.
Once this program sequence is performed from a Partial mode to the other Partial mode, the written data stored in a memory cell array may be lost. So, it should perform this program prior to regular read/write operation if Partial power down mode is used.

Address Key

The address key has following format.

Mode	Address			
	A_{20}	A_{19}	A_{18} to A_0	Hexadecimal
Sleep (default)	1	1	1	1FFFFFh
4M-bit Partial	1	0	1	17FFFFh
8M-bit Partial	0	1	1	0FFFFFh

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value		Unit
		Min	Max	
Voltage of V_{DD} Supply Relative to V_{SS}*	V_{DD}	– 0.5	+ 3.6	V
Voltage at Any Pin Relative to V_{SS}*	V_{IN}, V_{OUT}	– 0.5	+ 3.6	V
Short Circuit Output Current	I_{OUT}	– 50	+ 50	mA
Storage Temperature	T_{STG}	– 55	+ 125	°C

* : All voltages are referenced to V_{SS}.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Supply Voltage*1, *2	$V_{DD\ (31)}$	3.1	3.5	V
	$V_{DD\ (26)}$	2.6	3.1	V
	V_{SS}	0	0	V
High Level Input Voltage *1, *2, *3	$V_{IH\ (31)}$	$V_{DD} \times 0.8$	$V_{DD} + 0.2$ (≤ 3.6)	V
	$V_{IH\ (26)}$	$V_{DD} \times 0.8$	$V_{DD} + 0.2$	V
Low Level Input Voltage *1, *4	V_{IL}	– 0.3	$V_{DD} \times 0.2$	V
Ambient Temperature	T_A	– 30	+ 85	°C
Junction Temperature	T_J	– 30	+90	°C

*1 : All voltages are referenced to V_{SS}.

*2 : This device supports both $V_{DD(31)}$ and $V_{DD(26)}$ voltage ranges on an identical device. V_{DD} range is divided into two ranges as $V_{DD(31)}$ and $V_{DD(26)}$ on the table due to V_{IH} varied according to V_{DD} supply voltage.

*3 : Maximum DC voltage on input and I/O pins is V_{DD} + 0.2 V. During voltage transitions, inputs may overshoot to V_{DD} + 1.0 V for the period of up to 5 ns.

*4 : Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, inputs may undershoot V_{SS} to -1.0 V for the period of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test conditions		Value		Unit
				Min	Max	
Input Leakage Current	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{DD}$		–1.0	+1.0	µA
Output Leakage Current	I_{LO}	$0\text{ V} \leq V_{OUT} \leq V_{DD}$, Output Disable		–1.0	+1.0	µA
Output High Voltage Level	V_{OH}	$V_{DD} = V_{DD}$ Min, $I_{OH} = -0.5$ mA		2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 1$ mA		—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	$V_{DD} = V_{DD\ (26)}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $CE2 \leq 0.2$ V	Sleep	—	10	µA
	I_{DDP4}		4 M-bit partial	—	45	µA
	I_{DDP8}		8 M-bit partial	—	55	µA
V_{DD} Standby Current	I_{DDS}	$V_{DD} = V_{DD\ (26)}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = CE2 = V_{IH}$		—	1.5	mA
	I_{DDS1}	$V_{DD} = V_{DD\ (26)}$ Max, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{DD} - 0.2$ V, $\overline{CE}1 = CE2 \geq V_{DD} - 0.2$ V		—	100	µA
V_{DD} Active Current	I_{DDA1}	$V_{DD} = V_{DD\ (26)}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0$ mA	t_{RC}/t_{WC} = Min	—	30	mA
	I_{DDA2}		$t_{RC}/t_{WC} = 1$ µs	—	3	mA
V_{DD} Page Read Current	I_{DDA3}	$V_{DD} = V_{DD\ (26)}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0$ mA, t_{PRC} = Min		—	10	mA

Notes :
- All voltages are referenced to V_{SS}.
- I_{DD} depends on the output termination, load conditions, and AC characteristics.
- After power on, initialization following POWER-UP timing is required. DC characteristics are guaranteed after the initialization.
- I_{DDPS}, I_{DDP4}, I_{DDP8} and I_{DDS1} might be higher for up to 200ms after POWER-UP or power down/standby mode entry.

2. AC CHARACTERISTICS

(1) READ OPERATION

(At recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Read Cycle Time	t_{RC}	65	1000	ns	*1, *2
$\overline{\text{CE}}$1 Access Time	t_{CE}	—	65	ns	*3
$\overline{\text{OE}}$ Access Time	t_{OE}	—	40	ns	*3
Address Access Time	t_{AA}	—	65	ns	*3, *5
$\overline{\text{LB}}$, $\overline{\text{UB}}$ Access Time	t_{BA}	—	30	ns	*3
Page Address Access Time	t_{PAA}	—	20	ns	*3, *6
Page Read Cycle Time	t_{PRC}	20	1000	ns	*1, *6, *7
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{\text{CE}}$1 Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
$\overline{\text{OE}}$ Low to Output Low-Z	t_{OLZ}	10	—	ns	*4
$\overline{\text{LB}}$, $\overline{\text{UB}}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{\text{CE}}$1 High to Output High-Z	t_{CHZ}	—	12	ns	*3
$\overline{\text{OE}}$ High to Output High-Z	t_{OHZ}	—	12	ns	*3
$\overline{\text{LB}}$, $\overline{\text{UB}}$ High to Output High-Z	t_{BHZ}	—	12	ns	*3
Address Setup Time to $\overline{\text{CE}}$1 Low	t_{ASC}	–5	—	ns	
Address Setup Time to $\overline{\text{OE}}$ Low	t_{ASO}	10	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5, *8
Address Hold Time from $\overline{\text{CE}}$1 High	t_{CHAH}	–6	—	ns	*9
Address Hold Time from $\overline{\text{OE}}$ High	t_{OHAH}	–6	—	ns	
$\overline{\text{WE}}$ High to $\overline{\text{OE}}$ Low Time for Read	t_{WHOL}	10	1000	ns	*10
$\overline{\text{CE}}$1 High Pulse Width	t_{CP}	10	—	ns	

*1 : Maximum value is applicable if $\overline{\text{CE}}$1 is kept at Low without change of address input of A_{20} to A_3.

*2 : Address should not be changed within a minimum t_{RC}.

*3 : The output load 50 pF.

*4 : The output load 5 pF.

*5 : Applicable to A_{20} to A_3 when $\overline{\text{CE}}$1 is kept at Low.

*6 : Applicable only to A_2, A_1 and A_0 when $\overline{\text{CE}}$1 is kept at Low for the page address access.

*7 : In case Page Read Cycle is continued with keeping $\overline{\text{CE}}$1 stays Low, $\overline{\text{CE}}$1 must be brought to High within 4 µs. In other words, Page Read Cycle must be closed within 4 µs.

*8 : Applicable when at least two of address inputs among applicable are switched from the previous state.

*9 : t_{RC} (Min) and t_{PRC} (Min) must be satisfied.

*10 : If the actual value of t_{WHOL} is shorter than specified minimum values, the actual t_{AA} of following Read may become longer by the amount of subtracting the actual value from the specified minimum value.

(2) WRITE OPERATION

(At recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Write Cycle Time	t_{WC}	65	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*3
$\overline{\text{CE}}$1 Write Pulse Width	t_{CW}	40	—	ns	*3
$\overline{\text{WE}}$ Write Pulse Width	t_{WP}	40	—	ns	*3
$\overline{\text{LB}}$, $\overline{\text{UB}}$ Write Pulse Width	t_{BW}	40	—	ns	*3
$\overline{\text{LB}}$, $\overline{\text{UB}}$ Byte Mask Setup Time	t_{BS}	– 5	—	ns	*4
$\overline{\text{LB}}$, $\overline{\text{UB}}$ Byte Mask Hold Time	t_{BH}	– 5	—	ns	*5
Write Recovery Time	t_{WR}	0	—	ns	*6
$\overline{\text{CE}}$1 High Pulse Width	t_{CP}	10	—	ns	
$\overline{\text{WE}}$ High Pulse Width	t_{WHP}	10	1000	ns	
$\overline{\text{LB}}$, $\overline{\text{UB}}$ High Pulse Width	t_{BHP}	10	1000	ns	
Data Setup Time	t_{DS}	12	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{\text{OE}}$ High to $\overline{\text{CE}}$1 Low Setup Time for Write	t_{OHCL}	–5	—	ns	*7
$\overline{\text{OE}}$ High to Address Setup Time for Write	t_{OES}	0	—	ns	*8
$\overline{\text{LB}}$ and $\overline{\text{UB}}$ Write Pulse Overlap	t_{BWO}	40	—	ns	

*1 : Maximum value is applicable if $\overline{\text{CE}}$1 is kept at Low without any address change.

*2 : Minimum value must be equal or greater than the sum of write pulse (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WR}).

*3 : Write pulse is defined from High to Low transition of $\overline{\text{CE}}$1, $\overline{\text{WE}}$, $\overline{\text{LB}}$ or $\overline{\text{UB}}$, whichever occurs last.

*4 : Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of $\overline{\text{CE}}$1 or $\overline{\text{WE}}$ whichever occurs last.

*5 : Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of $\overline{\text{CE}}$1 or $\overline{\text{WE}}$ whichever occurs first.

*6 : Write recovery is defined from Low to High transition of $\overline{\text{CE}}$1, $\overline{\text{WE}}$, $\overline{\text{LB}}$ or $\overline{\text{UB}}$, whichever occurs first.

*7 : If $\overline{\text{OE}}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other word, $\overline{\text{OE}}$ must be brought to High within 5 ns after $\overline{\text{CE}}$1 is brought to Low.

*8 : If $\overline{\text{OE}}$ is Low after new address input, read cycle is initiated. In other word, $\overline{\text{OE}}$ must be brought to High at the same time or before new address valid.

(3) POWER DOWN PARAMETERS

(At recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit	Note
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	65	—	ns	
$\overline{\text{CE}}$1 High Hold Time following CE2 High after Power Down Exit [Sleep mode only]	t_{CHH}	300	—	µs	*1
$\overline{\text{CE}}$1 High Hold Time following CE2 High after Power Down Exit [not in Sleep mode]	t_{CHHP}	65	—	ns	*2
$\overline{\text{CE}}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns	*1

*1 : Applicable also to power-up.

*2 : Applicable when 4M-bit and 8M-bit Partial mode is programmed.

(4) OTHER TIMING PARAMETERS

(At recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit	Note
		Min	Max		
$\overline{\text{CE}}$1 High to $\overline{\text{OE}}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{\text{CE}}$1 High to $\overline{\text{WE}}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	µs	
$\overline{\text{CE}}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time	t_T	1	25	ns	*2

*1 : Some data might be written into any address location if t_{CHWX}(Min) is not satisfied.

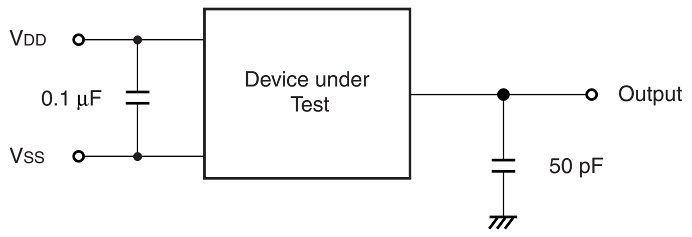
*2 : The Input Transition Time (t_T) at AC testing is 5 ns as shown in below. If actual t_T is longer than 5 ns, it may violate AC specification of some timing parameters.

(5) AC TEST CONDITIONS

(At recommended operating conditions unless otherwise noted.)

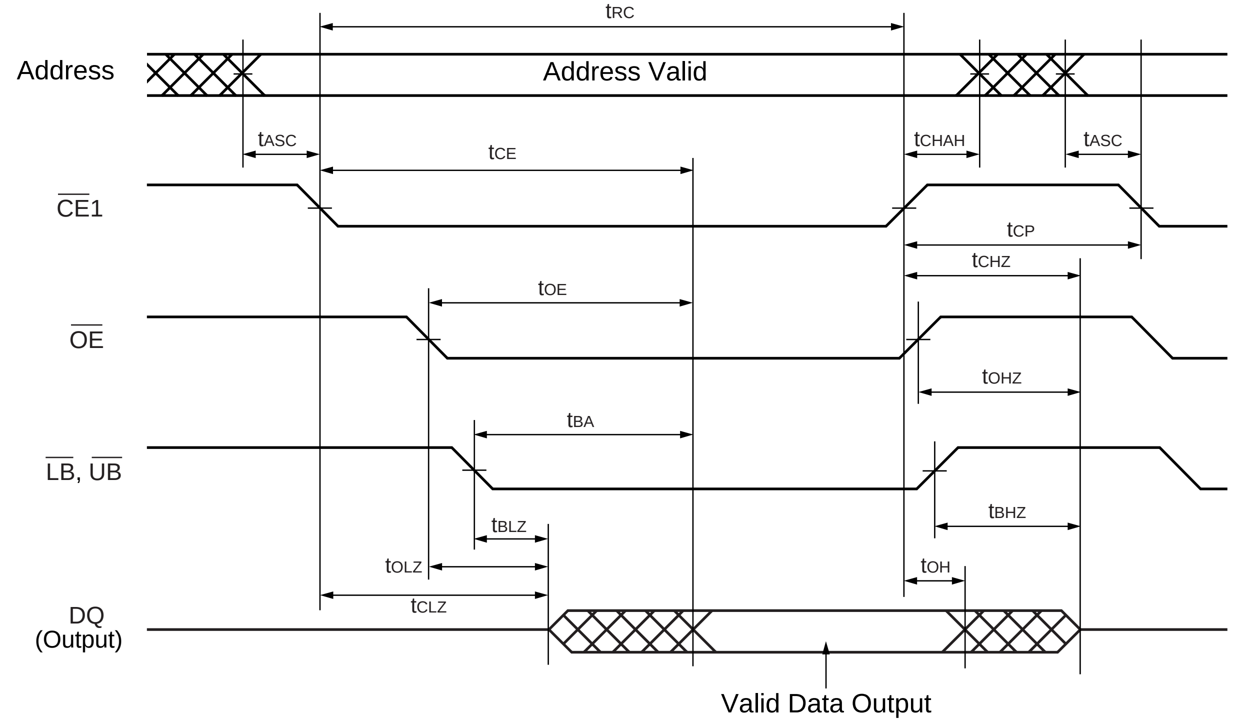
Description	Symbol	Test Setup	Value	Unit	Note
Input High Level	V_{IH}	—	$V_{DD} \times 0.8$	V	
Input Low Level	V_{IL}	—	$V_{DD} \times 0.2$	V	
Input Timing Measurement Level	V_{REF}	—	$V_{DD} \times 0.5$	V	
Input Transition Time	t_T	Between V_{IL} and V_{IH}	5	ns	

- AC MEASUREMENT OUTPUT LOAD CIRCUIT



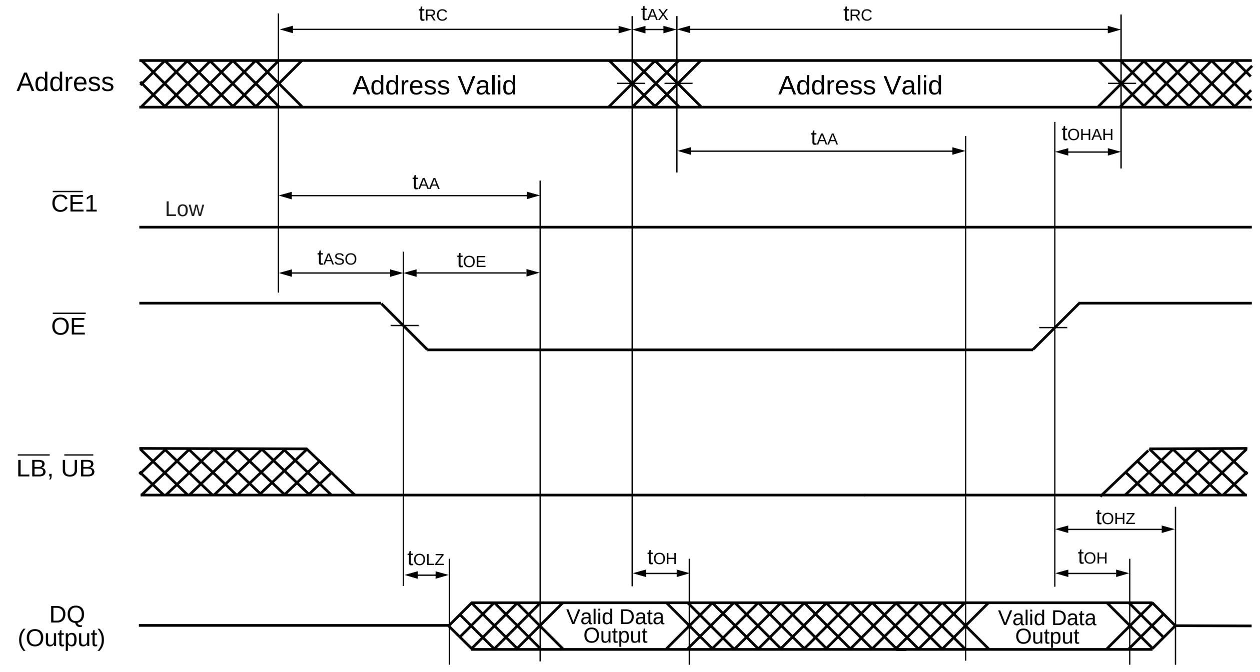
■ TIMING DIAGRAMS

(1) READ Timing #1 (Basic Timing)



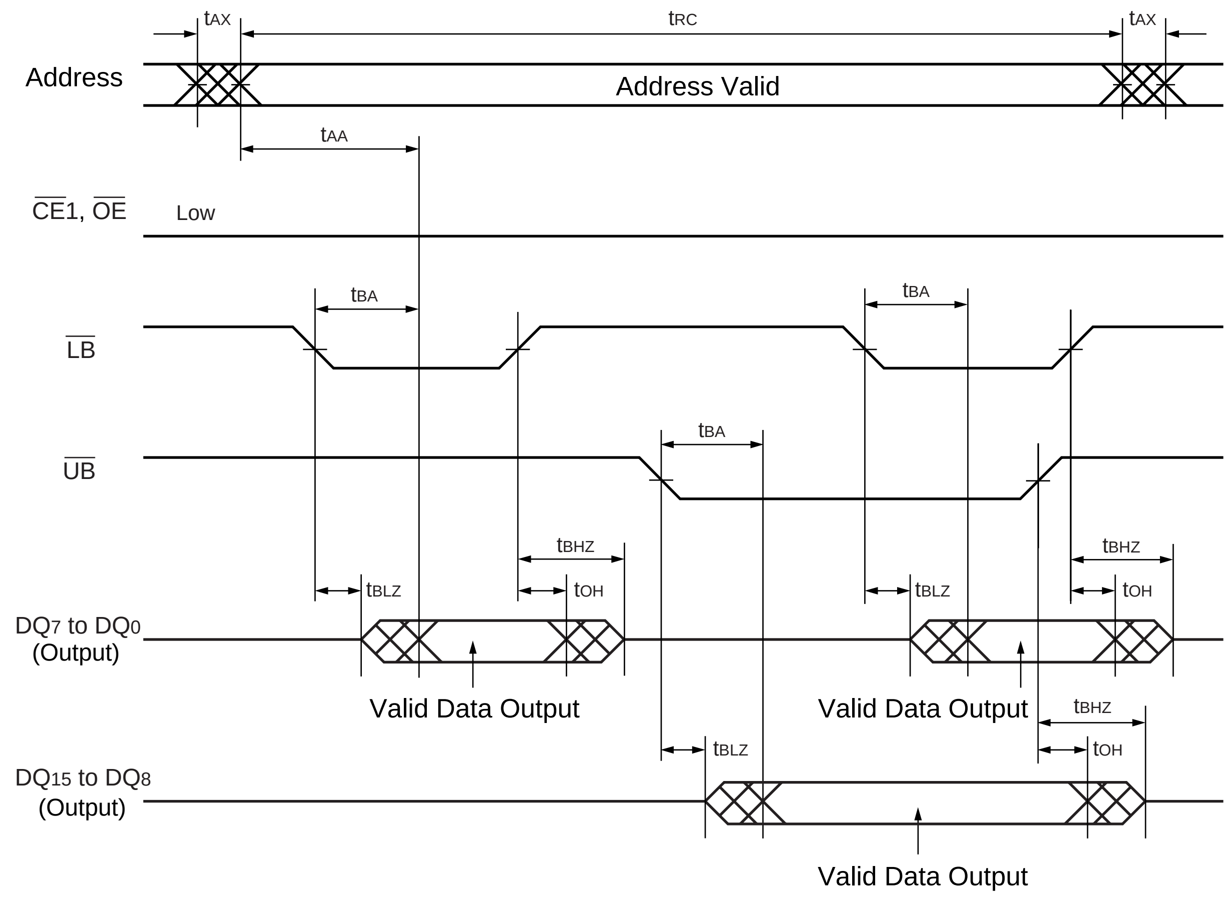
Note : This timing diagram assumes CE2 = H and WE = H.

(2) READ Timing #2 ($\overline{\text{OE}}$ & Address Access)



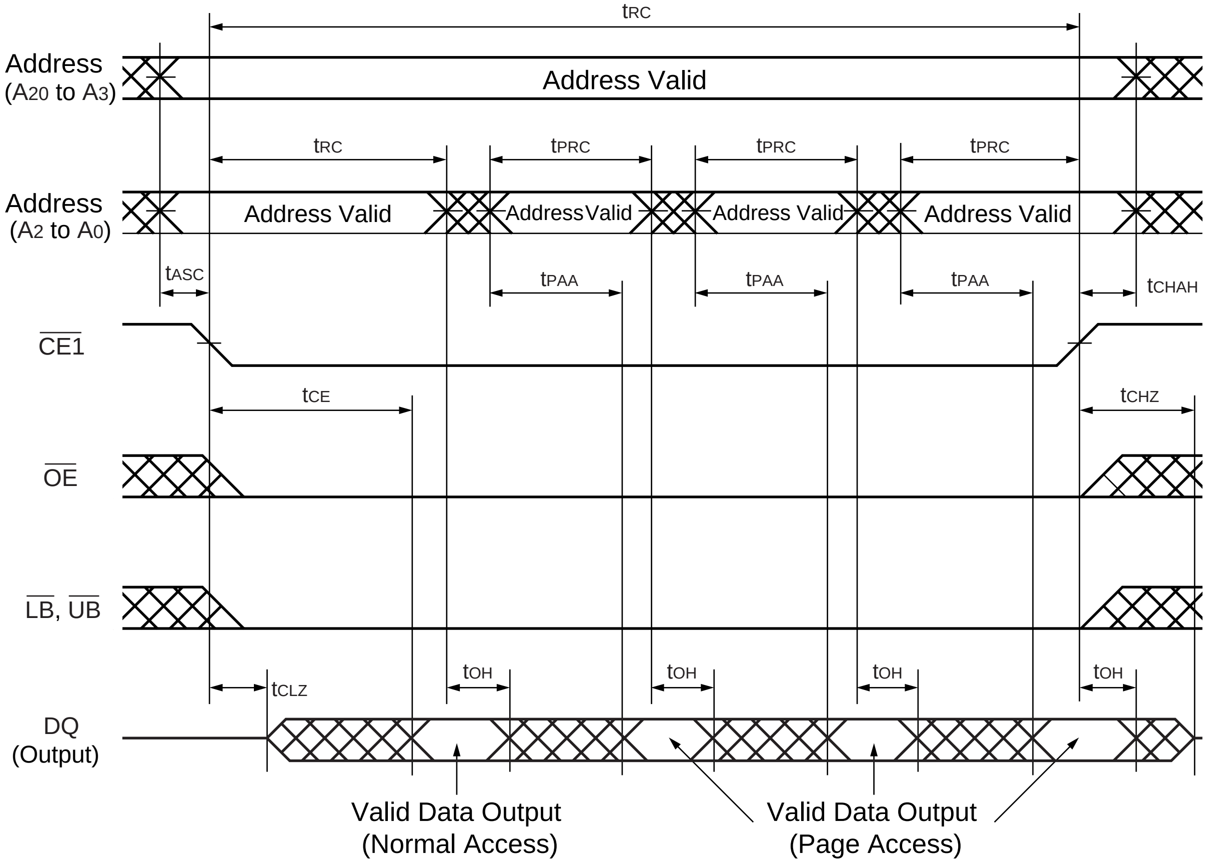
Note : This timing diagram assumes CE2 = H and $\overline{\text{WE}}$ = H.

(3) READ Timing #3 ($\overline{LB}$, $\overline{UB}$ Byte Access)



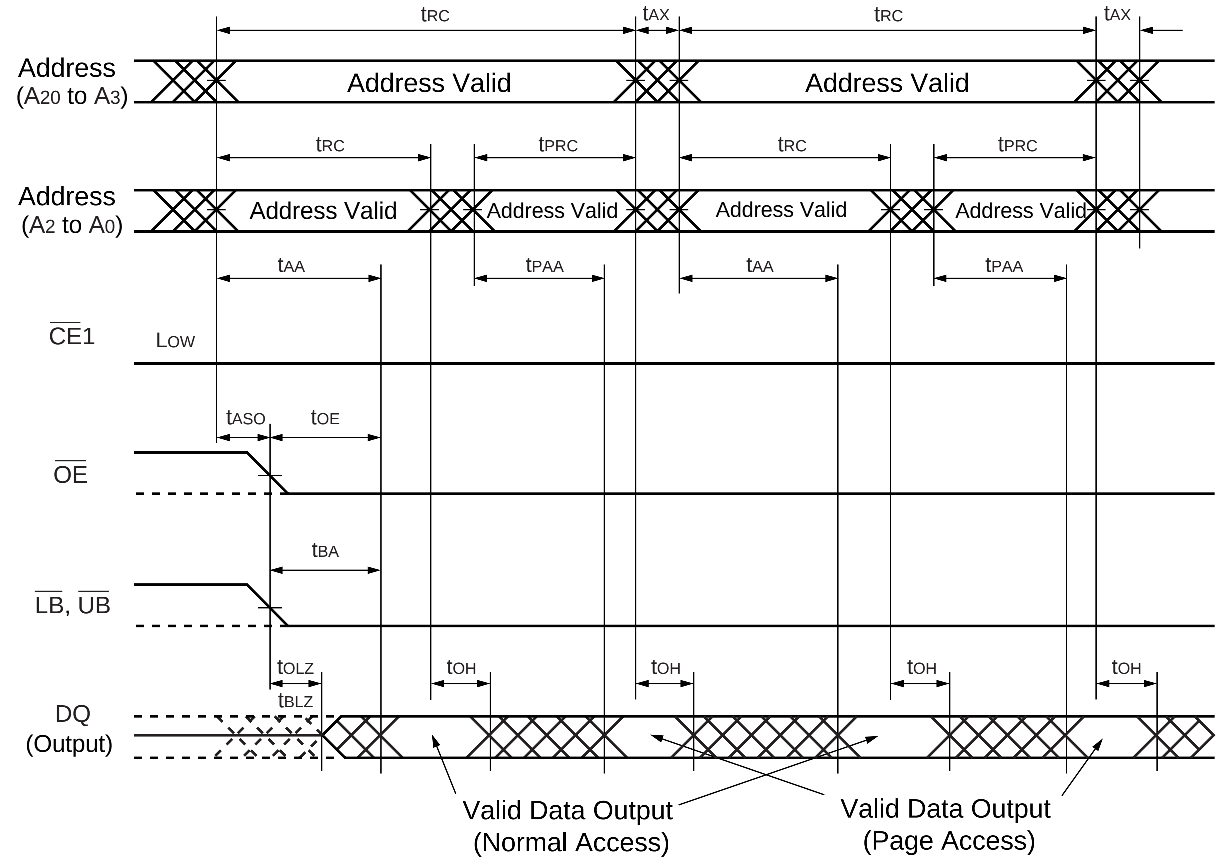
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(4) READ Timing #4 (Page Address Access after $\overline{\text{CE1}}$ Control Access)



Note : This timing diagram assumes CE2 = H and $\overline{\text{WE}}$ = H.

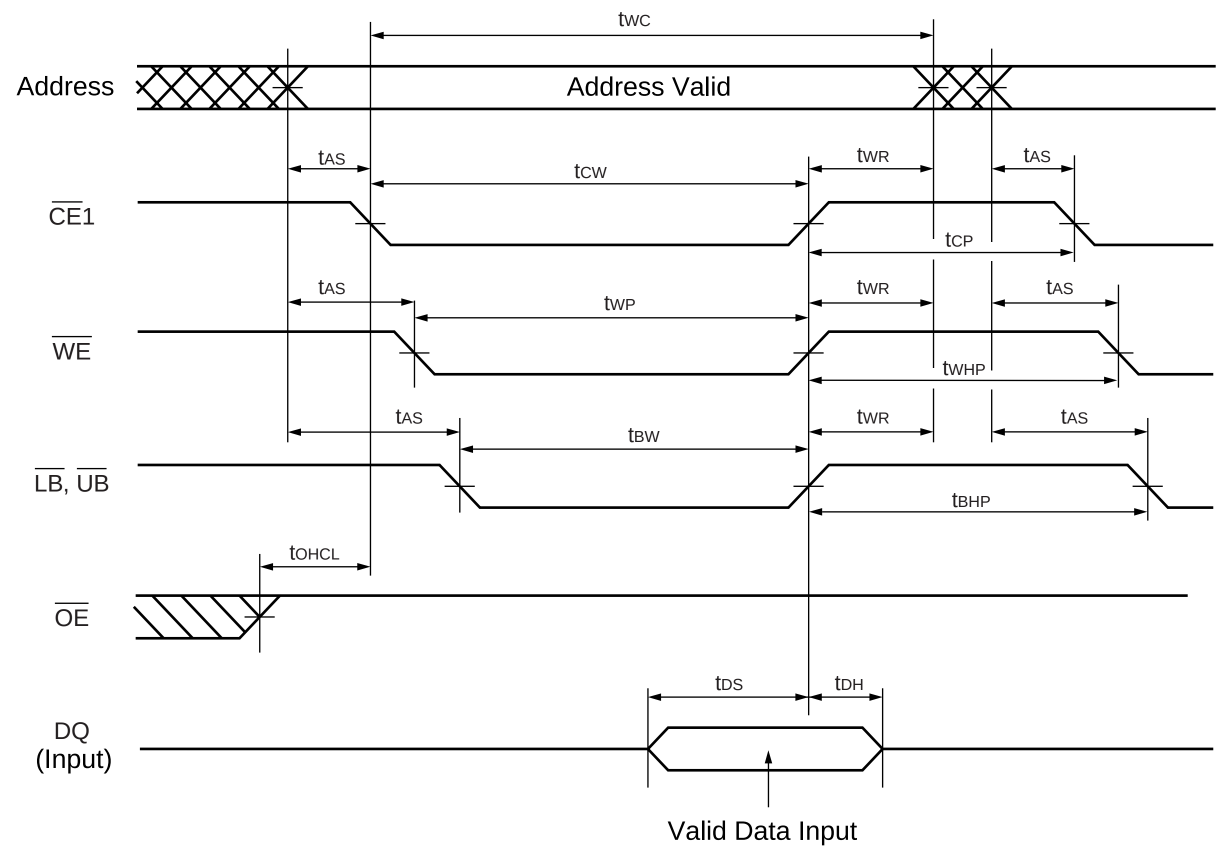
(5) READ Timing #5 (Random and Page Address Access)



Notes : • This timing diagram assumes CE2 = H and $\overline{\text{WE}}$ = H.

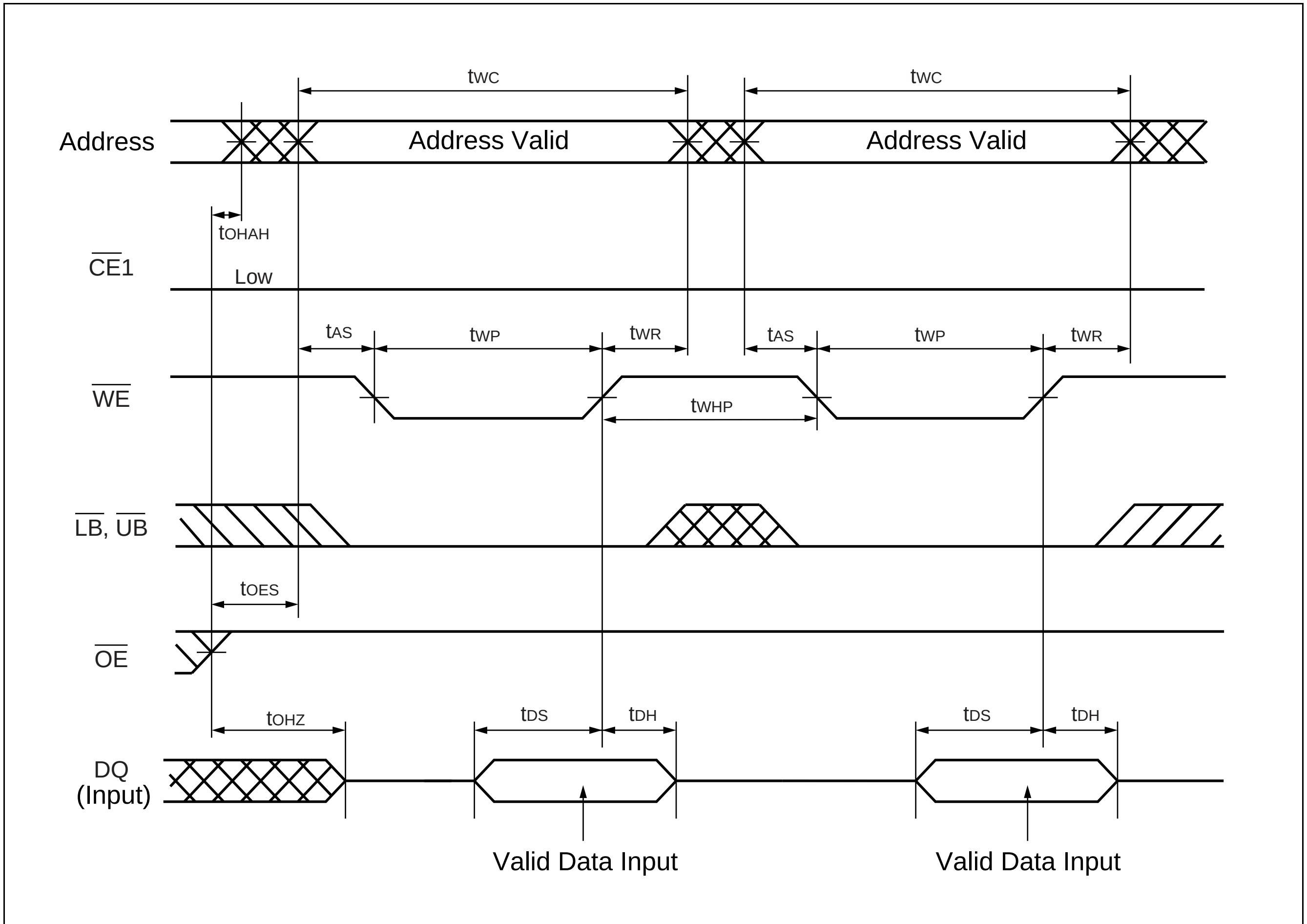
• Either or both $\overline{\text{LB}}$ and $\overline{\text{UB}}$ must be Low when both $\overline{\text{CE1}}$ and $\overline{\text{OE}}$ are Low.

(6) WRITE Timing #1 (Basic Timing)



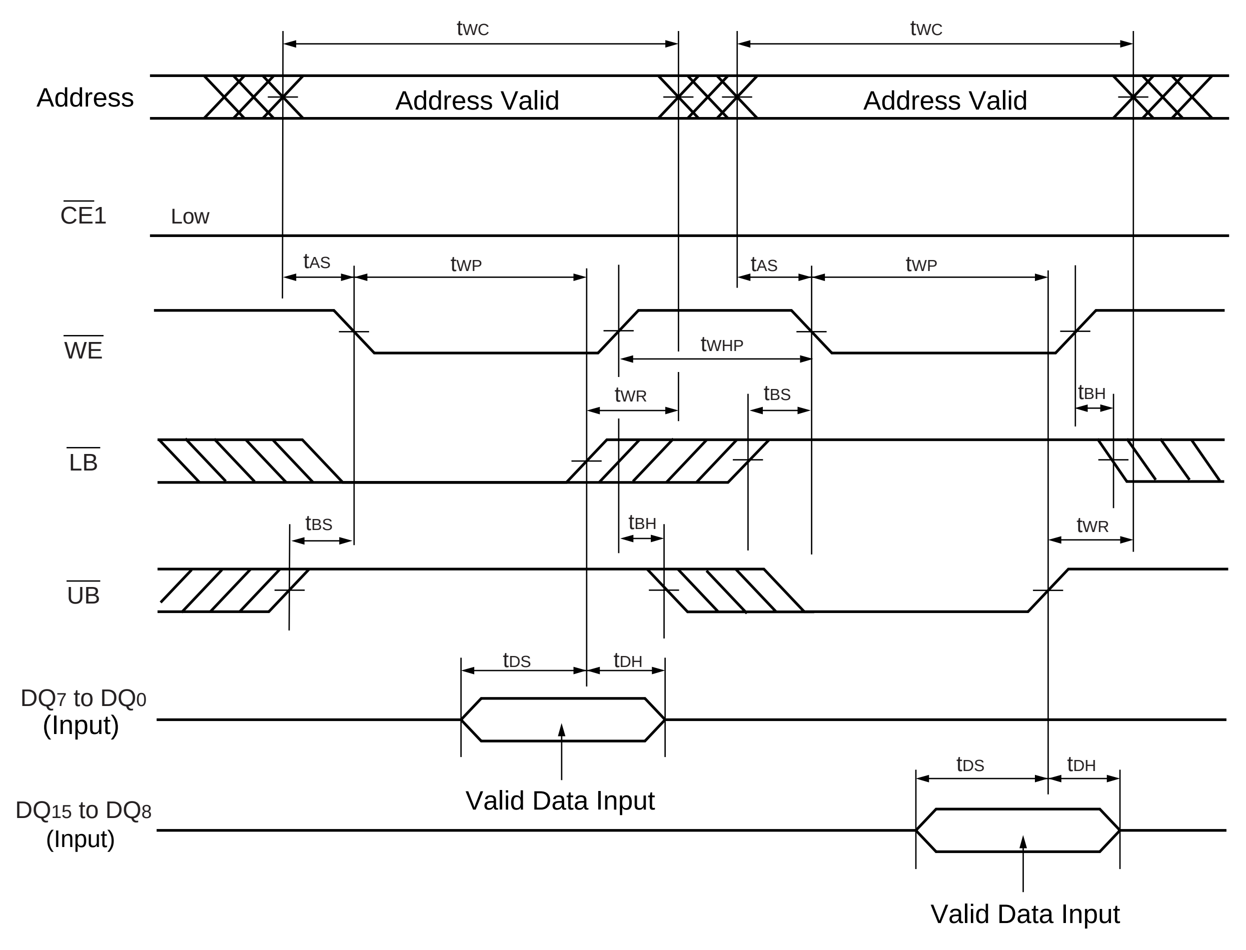
Note : This timing diagram assumes CE2 = H.

(7) WRITE Timing #2 (WE Control)



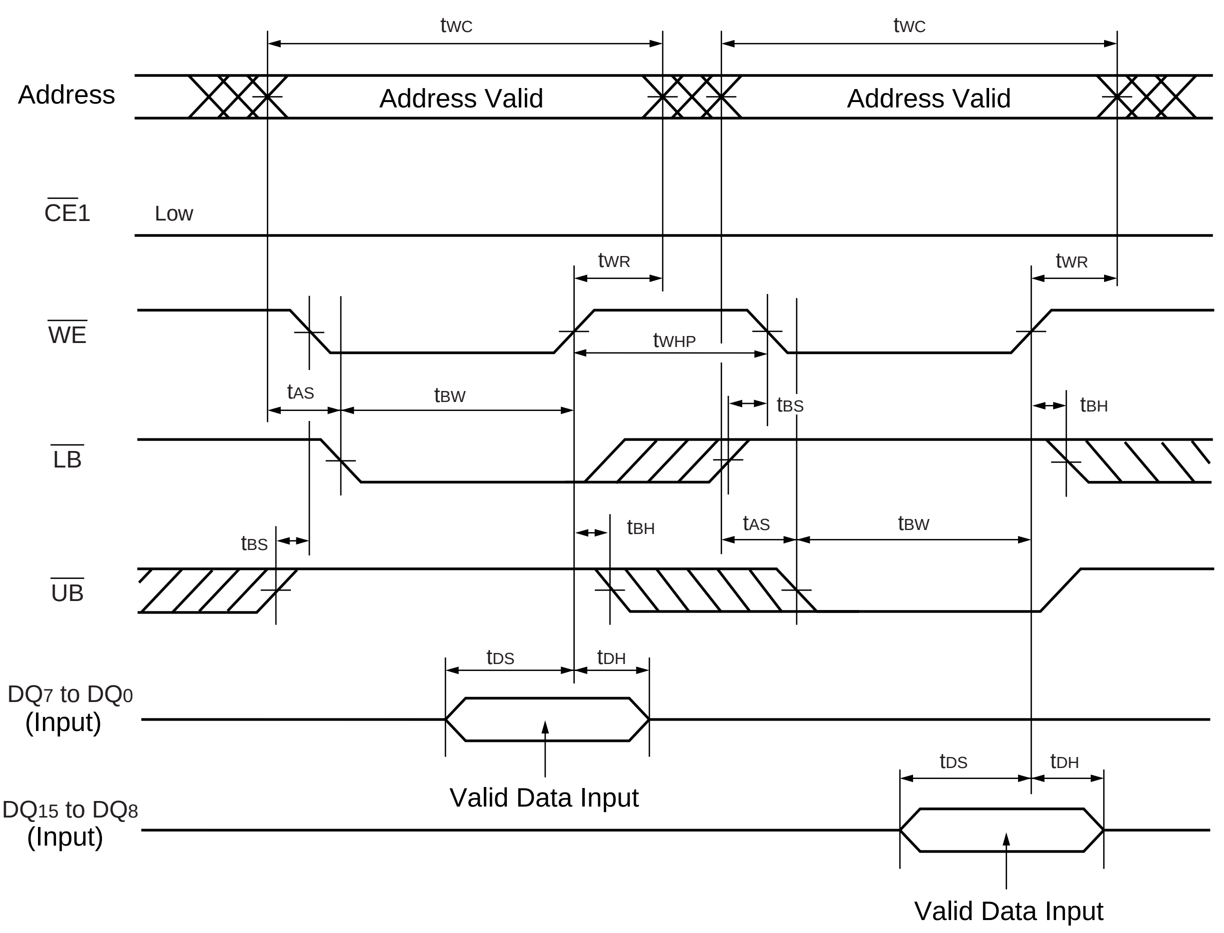
Note : This timing diagram assumes CE2 = H.

(8) WRITE Timing #3-1 (WE, LB, UB Byte Write Control)



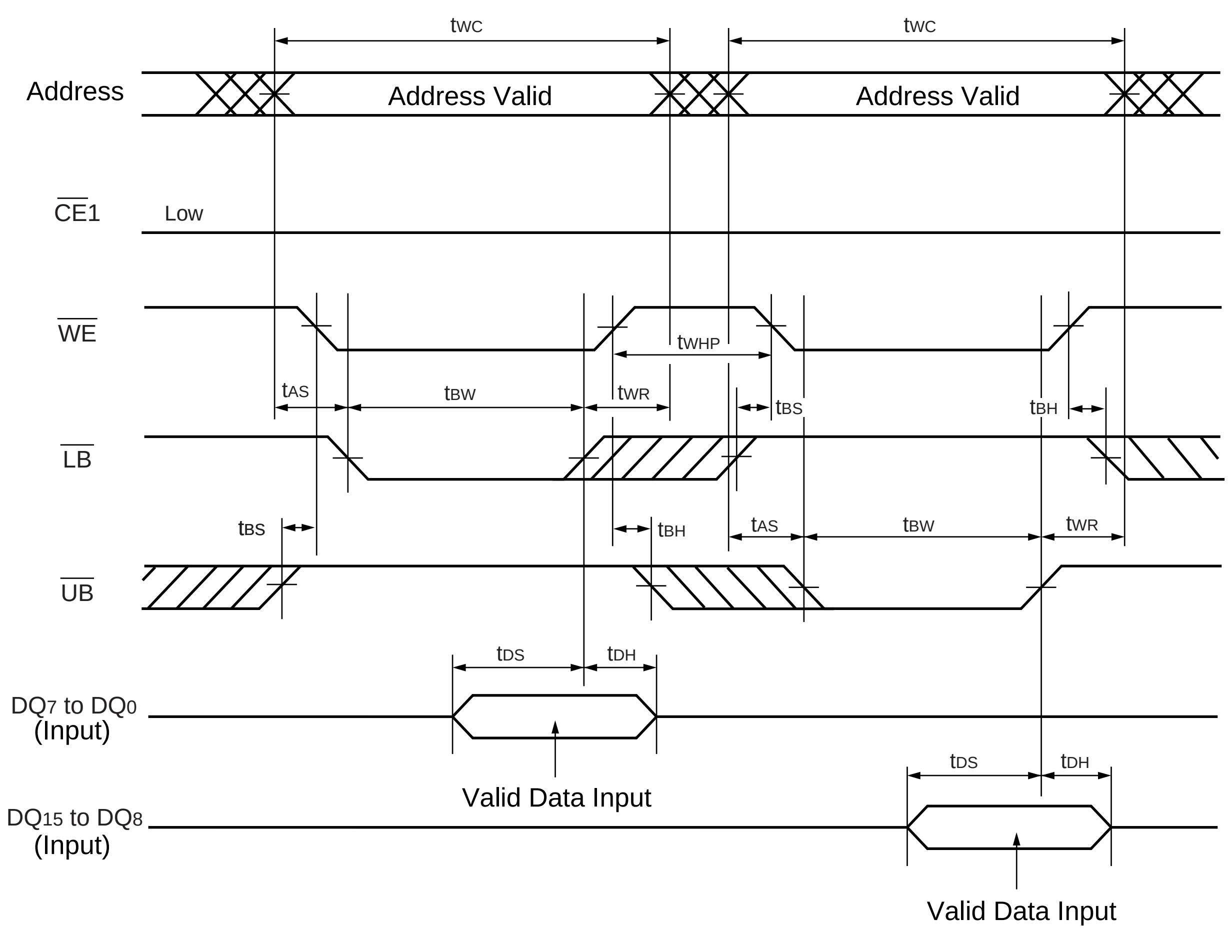
Note : This timing diagram assumes CE2 = H and OE = H.

(9) WRITE Timing #3-2 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



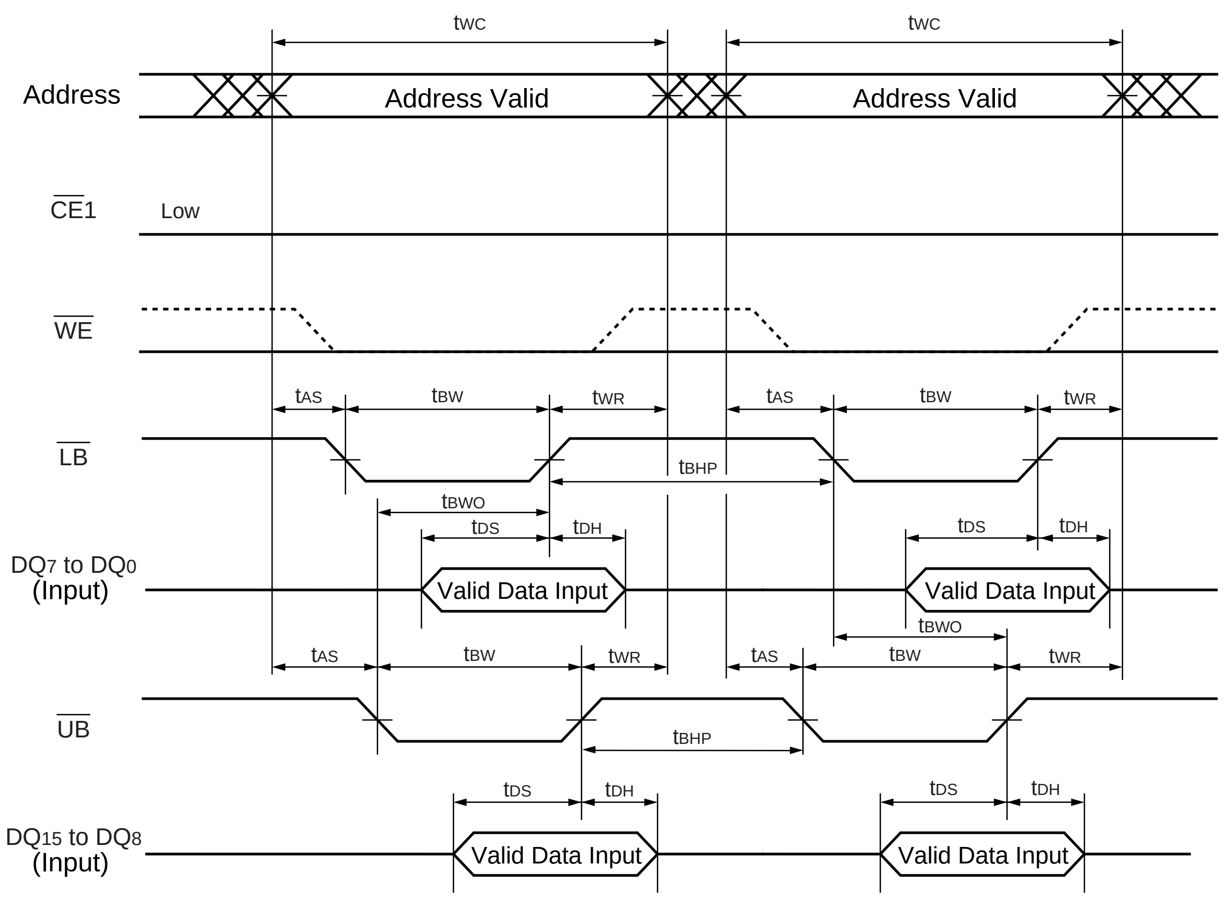
Note : This timing diagram assumes CE2 = H and $\overline{OE}$ = H.

(10) WRITE Timing #3-3 ($\overline{\text{WE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$ Byte Write Control)



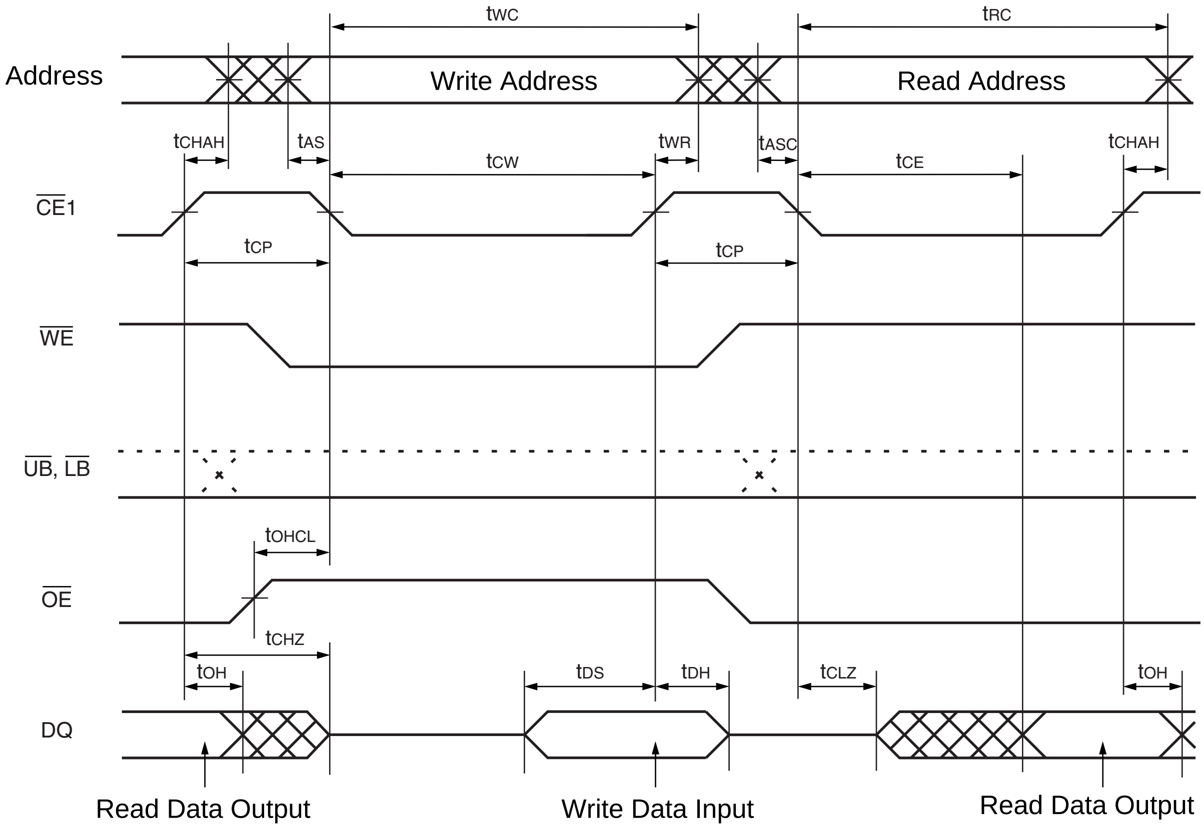
Note : This timing diagram assumes CE2 = H and $\overline{\text{OE}}$ = H.

(11) WRITE Timing #3-4 ($\overline{\text{WE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$ Byte Write Control)



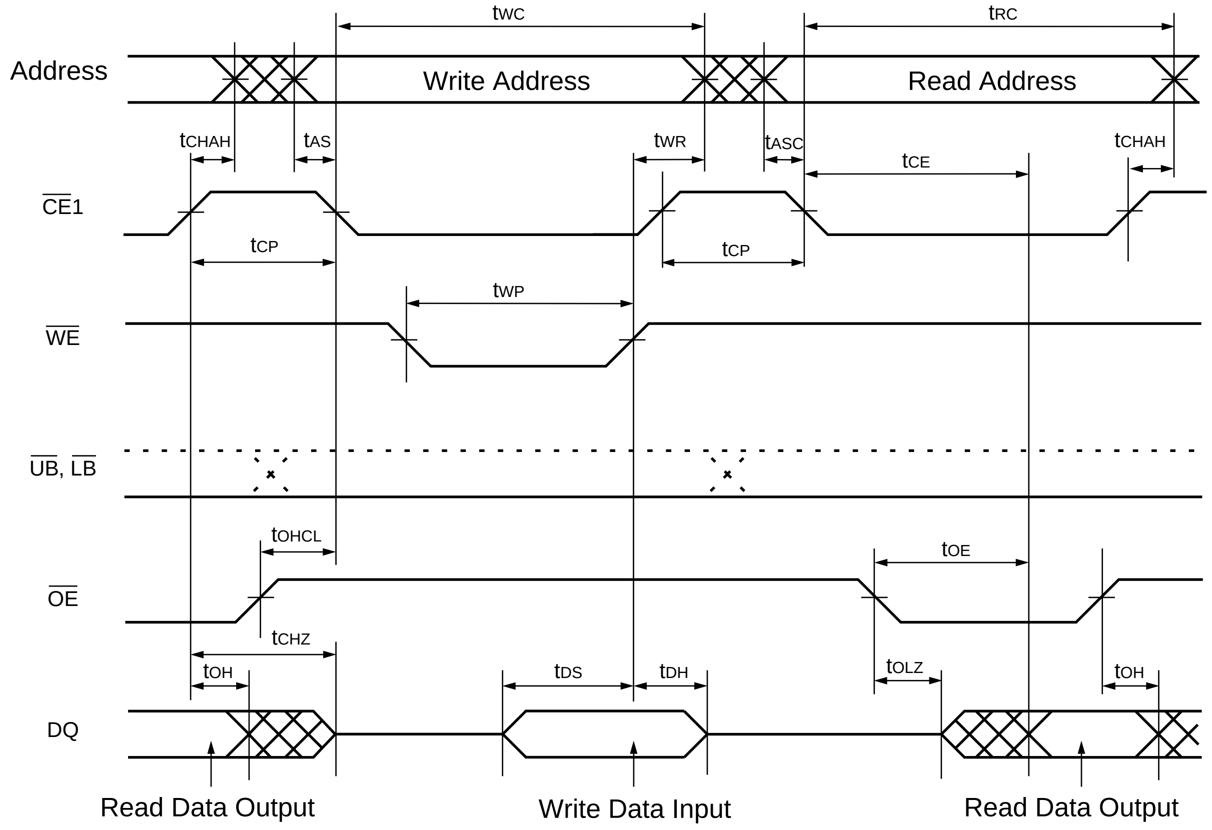
Note : This timing diagram assumes CE2 = H and $\overline{\text{OE}}$ = H.

(12) READ / WRITE Timing #1-1 (CE1 Control)



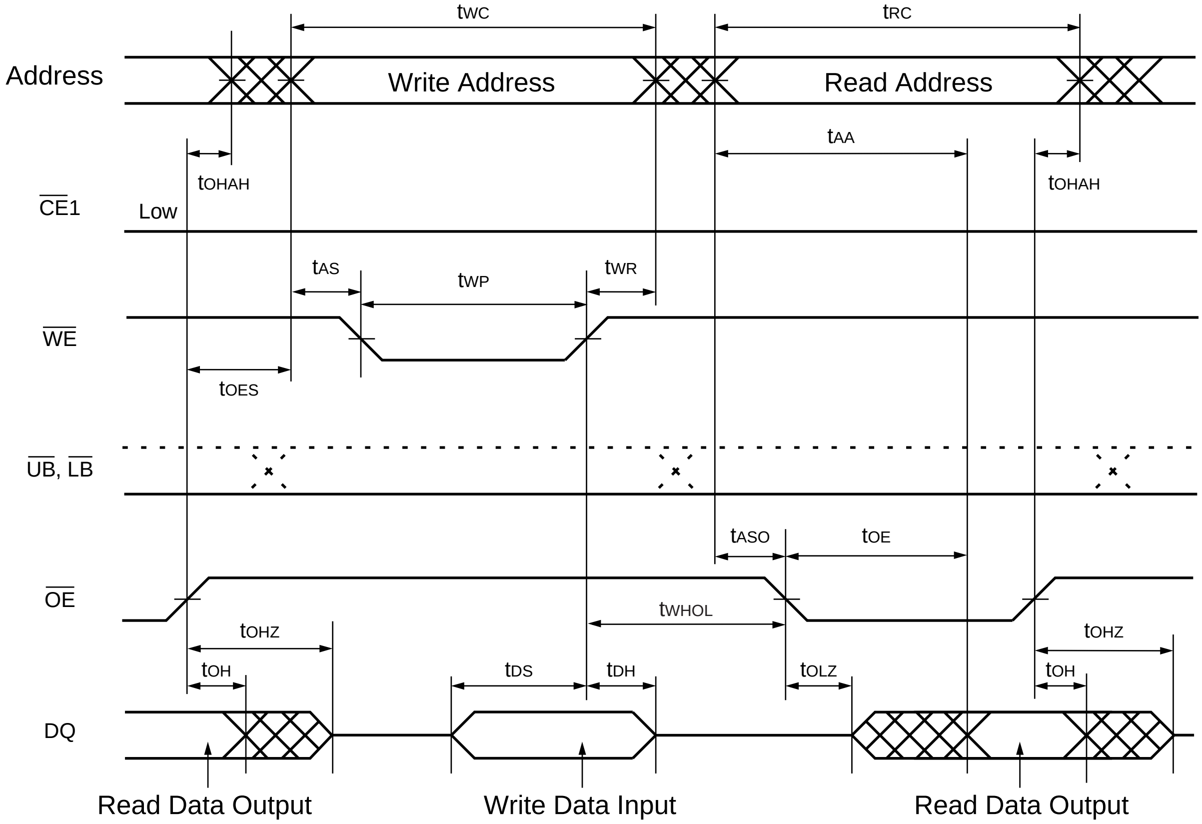
Notes : • This timing diagram assumes CE2 = H.
• Write address is valid from either CE1 or WE of last falling edge.

(13) READ / WRITE Timing #1-2 ($\overline{\text{CE}}$1, $\overline{\text{WE}}$, $\overline{\text{OE}}$ Control)



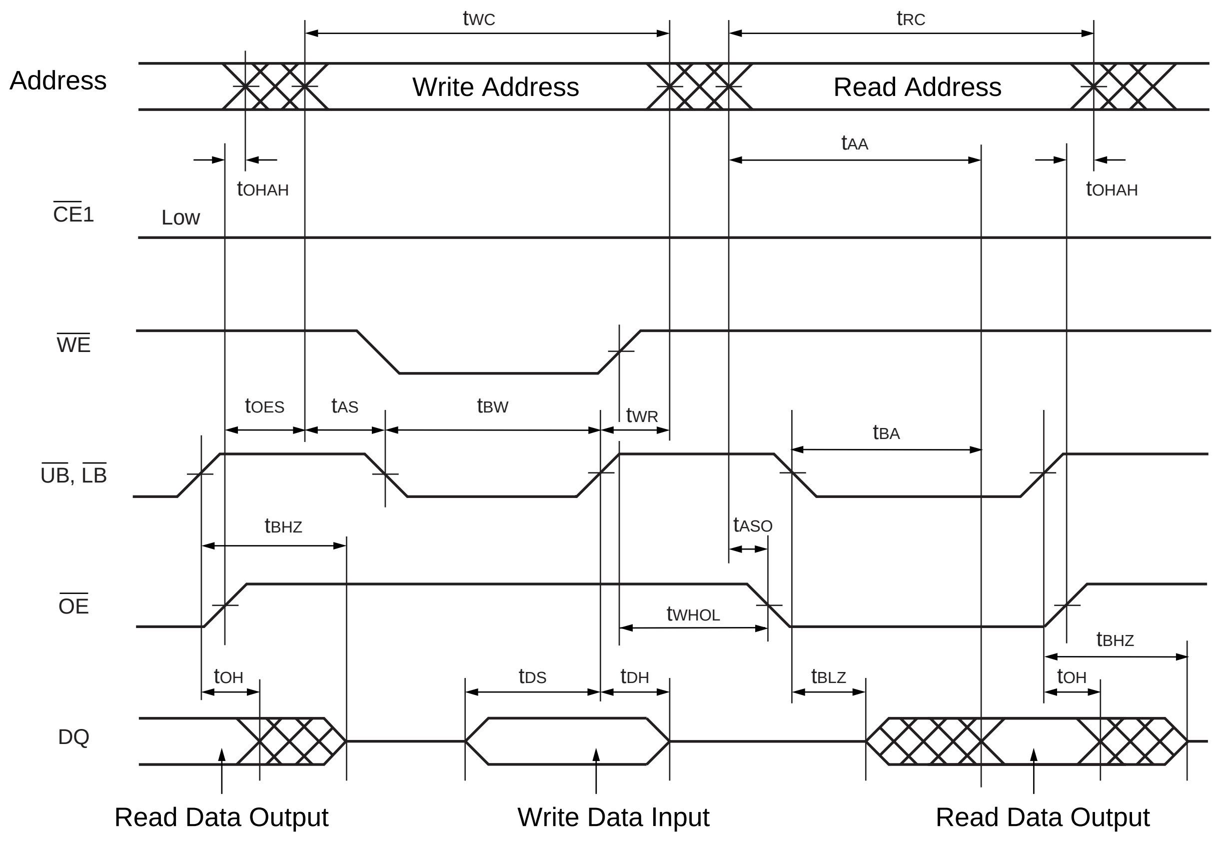
Notes :
- This timing diagram assumes CE2 = H.
- $\overline{\text{OE}}$ can be fixed Low during write operation if it is $\overline{\text{CE}}$1 controlled write at Read-Write-Read sequence.

(14) READ / WRITE Timing #2 ($\overline{\text{OE}}$, $\overline{\text{WE}}$ Control)



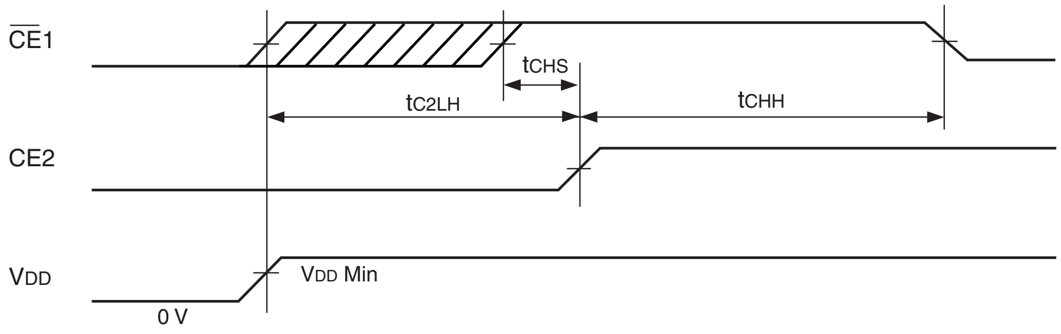
Notes :
- This timing diagram assumes CE2 = H.
- $\overline{\text{CE1}}$ can be tied to Low for $\overline{\text{WE}}$ and $\overline{\text{OE}}$ controlled operation.

(15) READ / WRITE Timing #3 ($\overline{\text{OE}}$, $\overline{\text{WE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$ Control)



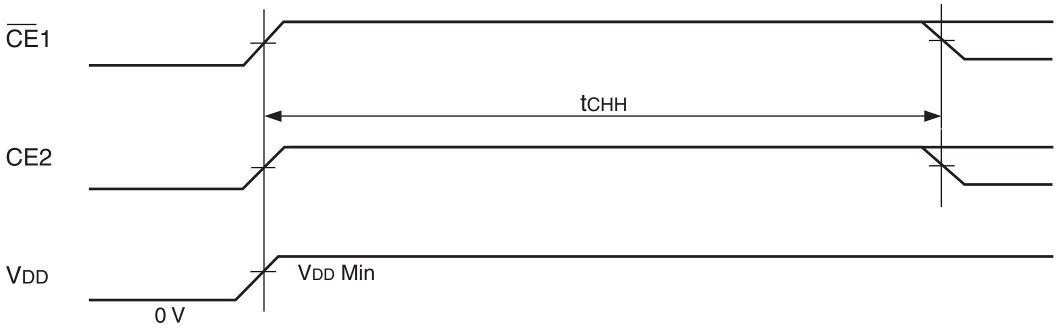
Notes :
- This timing diagram assumes CE2 = H.
- $\overline{\text{CE1}}$ can be tied to Low for $\overline{\text{WE}}$ and $\overline{\text{OE}}$ controlled operation.

(16) POWER-UP Timing #1



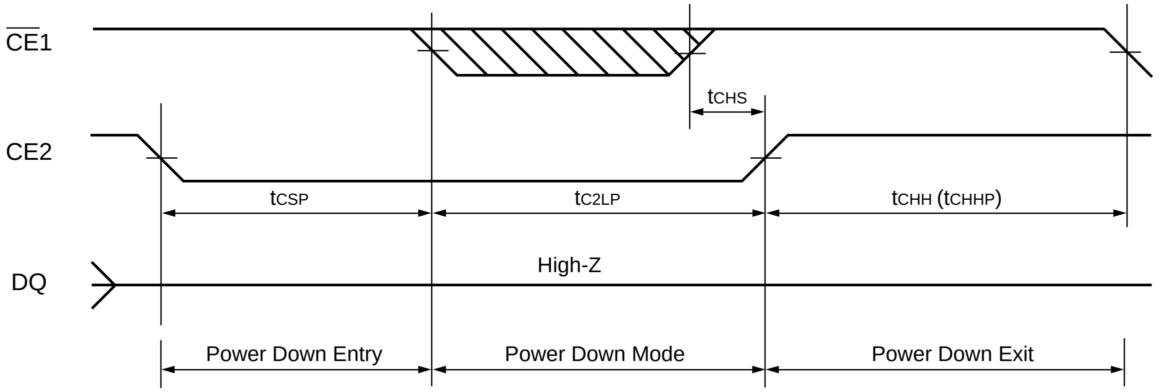
Note : The t_{C2LH} specifies after V_{DD} reaches specified minimum level.

(17) POWER-UP Timing #2



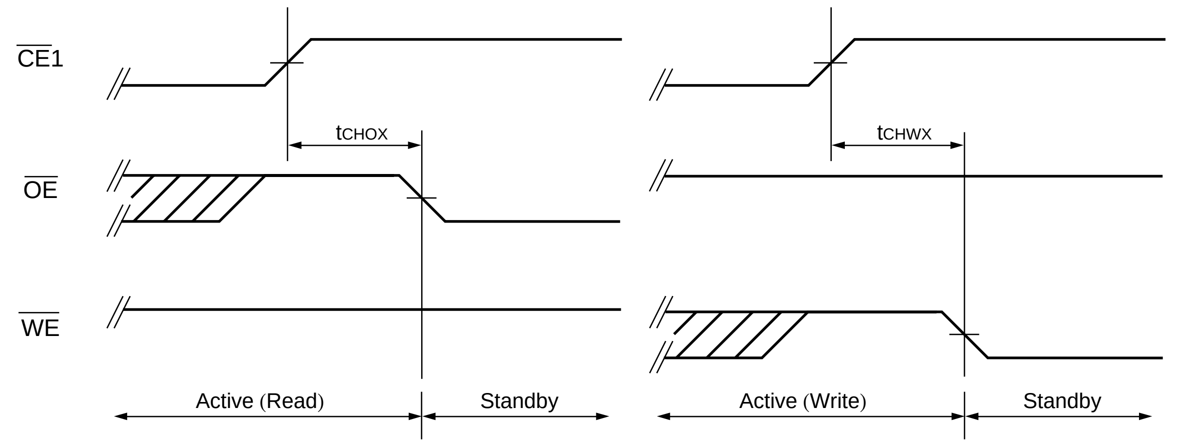
Note : The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable both $\overline{CE}1$ and CE2. If transition time of V_{DD} (from 0 V to V_{DD} Min) is longer than 50 ms, POWER-UP Timing #1 must be applied.

(18) POWER DOWN Entry and Exit Timing



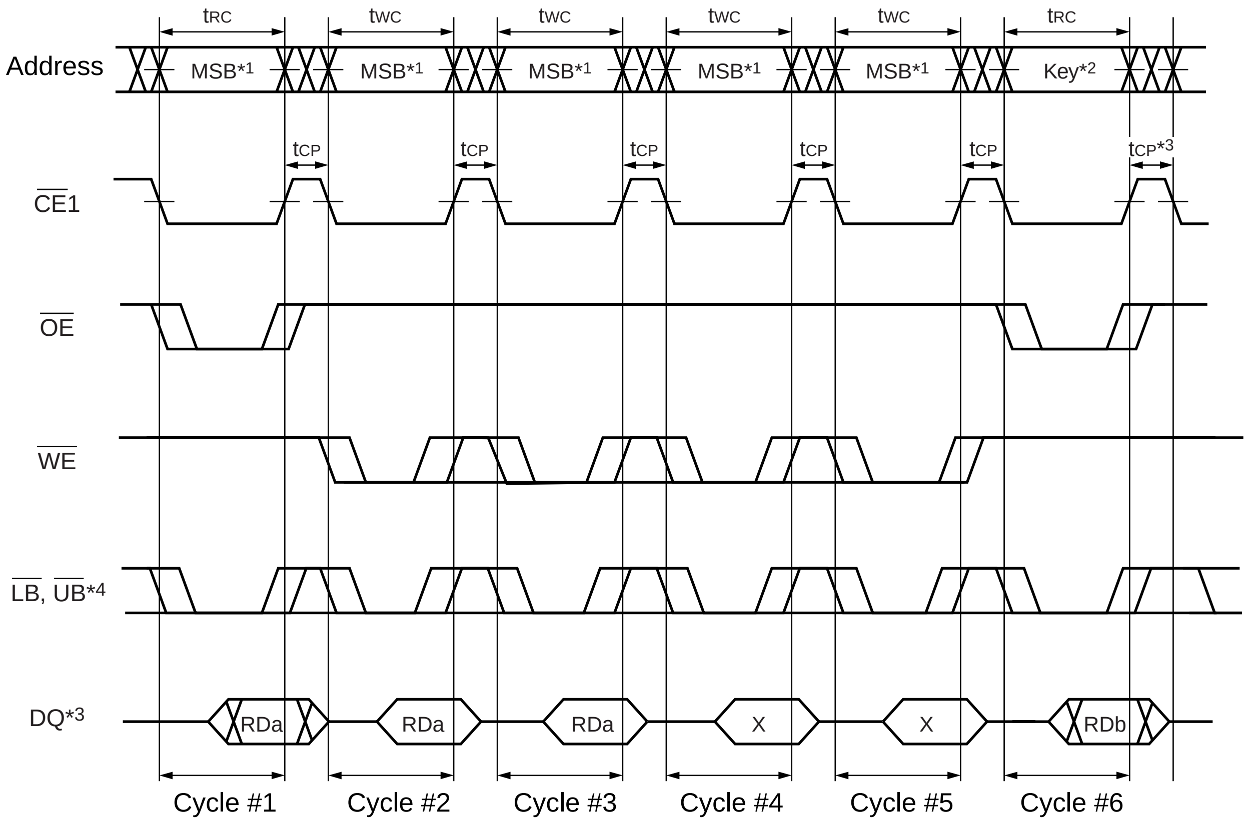
Note : This Power Down mode can be also used as a reset timing if “POWER-UP timing” above could not be satisfied and Power Down program was not performed prior to this reset.

(19) Standby Entry Timing after Read or Write



Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode.

(20) POWER DOWN PROGRAM Timing



*1 : The all address inputs must be High from Cycle #1 to #5.

*2 : The address key must confirm the format specified in "■ POWER DOWN". If not, the operation and data are not guaranteed.

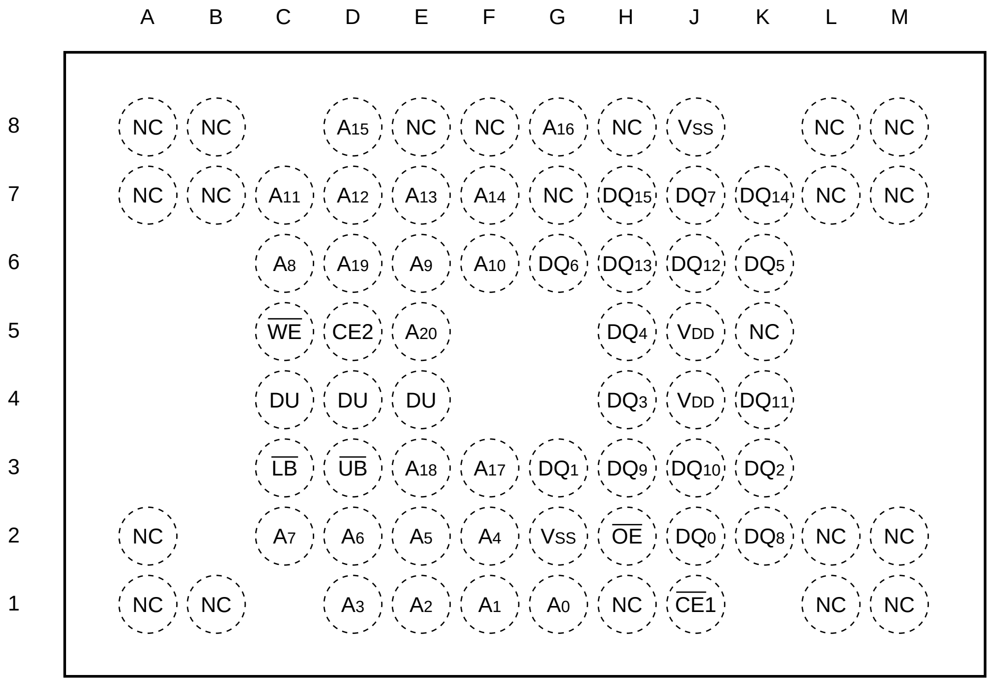
*3 : After tCP following Cycle #6, the Power Down Program is completed and returned to the normal operation.

*4 : Byte read or write is available in addition to Word read or write. At least one byte control signal ($\overline{LB}$ or $\overline{UB}$) need to be Low.

■ PACKAGE FOR ENGINEERING SAMPLES

- Pin Assignment

(TOP VIEW)



	A	B	C	D	E	F	G	H	J	K	L	M
8	NC	NC		A_{15}	NC	NC	A_{16}	NC	V_{SS}		NC	NC
7	NC	NC	A_{11}	A_{12}	A_{13}	A_{14}	NC	DQ_{15}	DQ_7	DQ_{14}	NC	NC
6			A_8	A_{19}	A_9	A_{10}	DQ_6	DQ_{13}	DQ_{12}	DQ_5		
5			$\overline{WE}$	CE2	A_{20}			DQ_4	V_{DD}	NC		
4			DU	DU	DU			DQ_3	V_{DD}	DQ_{11}		
3			$\overline{LB}$	$\overline{UB}$	A_{18}	A_{17}	DQ_1	DQ_9	DQ_{10}	DQ_2		
2	NC		A_7	A_6	A_5	A_4	V_{SS}	$\overline{OE}$	DQ_0	DQ_8	NC	NC
1	NC	NC		A_3	A_2	A_1	A_0	NC	$\overline{CE1}$		NC	NC

(BGA-71P-M03)

- Pin Description

Pin Name	Description
A_{20} to A_0	Address Input
$\overline{CE1}$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
DQ_7 to DQ_0	Lower Byte Data Input/Output
DQ_{15} to DQ_8	Upper Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connection
DU	Don’t Use

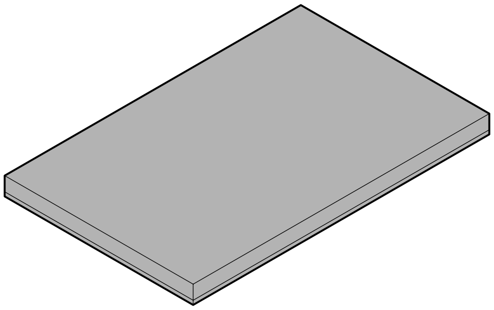
- Package Capacitance

(f = 1 MHz, T_A = +25 °C)

Parameter	Symbol	Test conditions	Value			Unit
			Min	**Typ**	**Max**	
Address Input Capacitance	C_{IN1}	V_{IN} = 0 V	—	—	5	pF
Control Input Capacitance	C_{IN2}	V_{IN} = 0 V	—	—	5	pF
Data Input/Output Capacitance	$C_{I/O}$	V_{IO} = 0 V	—	—	8	pF

- Package View

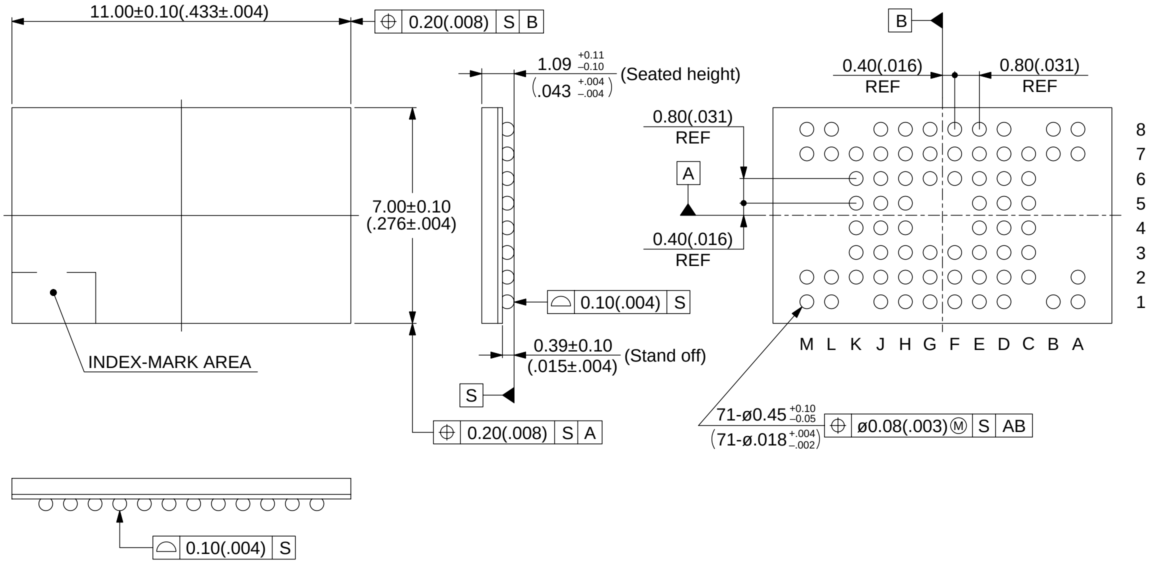
71-ball plastic FBGA



(BGA-71P-M03)

- Package Dimension

71-ball plastic FBGA
(BGA-71P-M03)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

■ BONDING PAD INFORMATION

Please contact local FUJITSU representative for pad layout and pad coordinate information.

■ ORDERING INFORMATION

Part Number	Shipping Form	Remarks
MB82DP02183D-65LWT	Wafer	

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