CEP61A2/CEB61A2

N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

■ 20V, 57A, $R_{DS(ON)}$ = 12mΩ @V_{GS} = 4.5V.

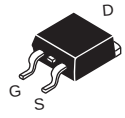
$R_{DS(ON)}$ = 20mΩ @V_{GS} = 2.5V.

■ Super high dense cell design for extremely low $R_{DS(ON)}$.

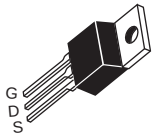
■ High power and current handing capability.

■ Lead free product is acquired.

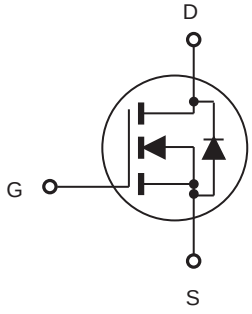
■ TO-220 & TO-263 package.



CEB SERIES
TO-263(DD-PAK)



CEP SERIES
TO-220



ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	57	A
Drain Current-Pulsed [a]	I_{DM}	228	A
Maximum Power Dissipation @ T_C = 25°C	P_D	94	W
- Derate above 25°C		0.63	W/°C
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.6	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

查询"CEB61A2"供应商

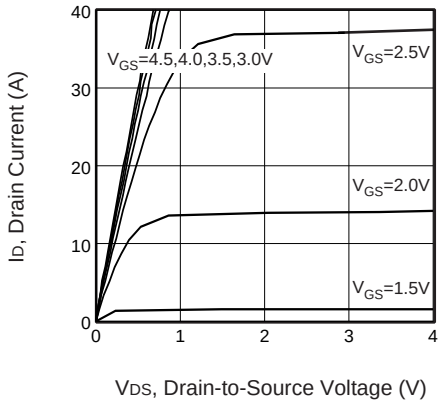


Figure 1. Output Characteristics

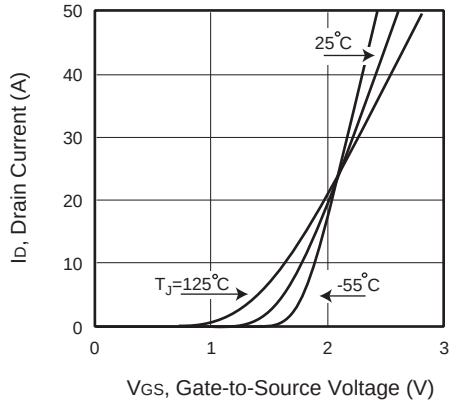


Figure 2. Transfer Characteristics

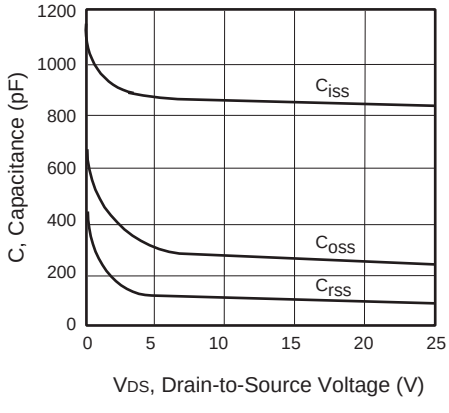


Figure 3. Capacitance

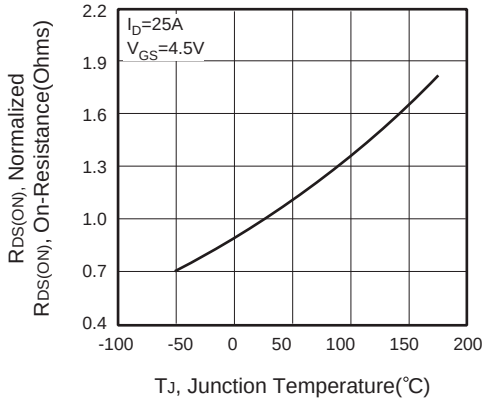


Figure 4. On-Resistance Variation with Temperature

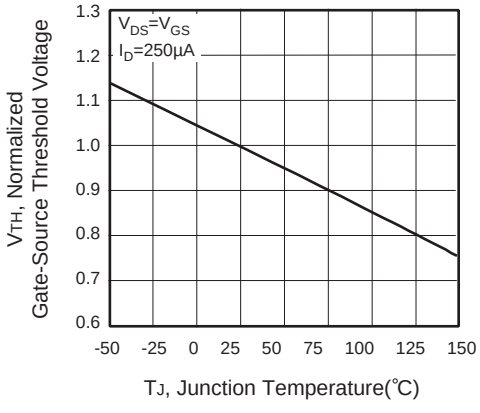


Figure 5. Gate Threshold Variation with Temperature

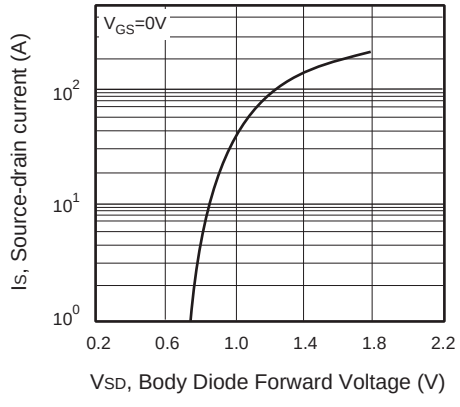


Figure 6. Body Diode Forward Voltage Variation with Source Current

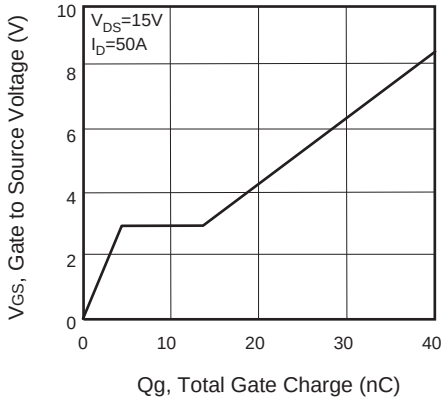


Figure 7. Gate Charge

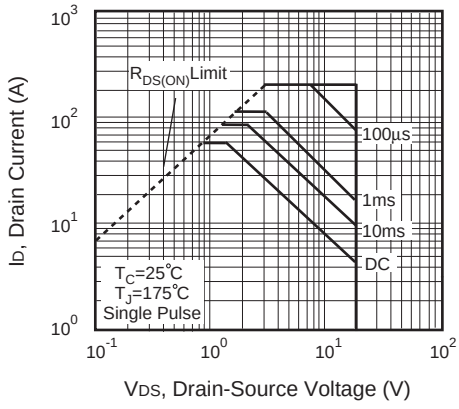


Figure 8. Maximum Safe Operating Area

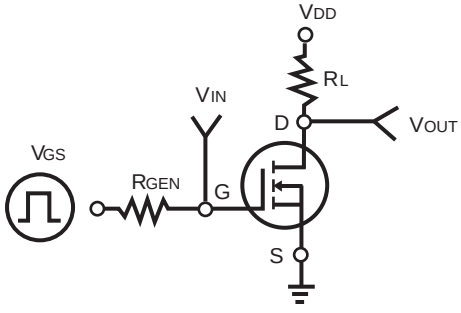


Figure 9. Switching Test Circuit

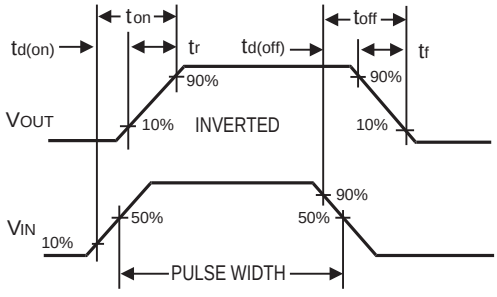


Figure 10. Switching Waveforms

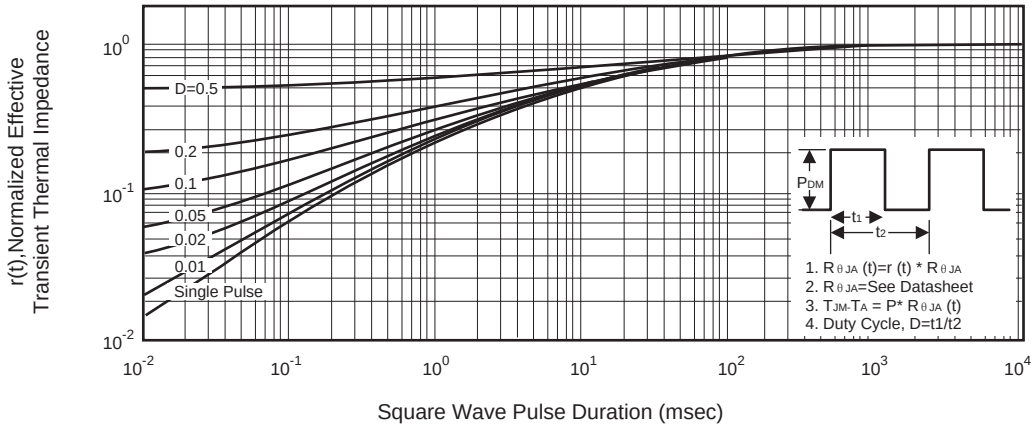


Figure 11. Normalized Thermal Transient Impedance Curve