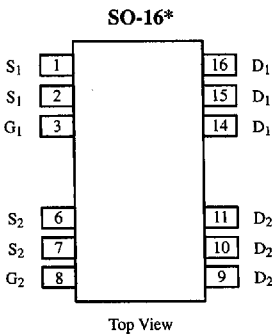


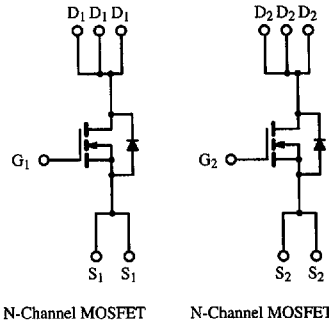
**Dual N-Channel Enhancement-Mode MOSFET**

**Product Summary**

V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
50	0.05 @ V <sub>GS</sub> = 10 V	± 5.3
	0.07 @ V <sub>GS</sub> = 4.5 V	± 4.5



\*Conforms to standard SO-16 dimensions



**Absolute Maximum Ratings (T<sub>A</sub> = 25°C Unless Otherwise Noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	50	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25°C	± 5.3
		T <sub>A</sub> = 70°C	± 4.2
Pulsed Drain Current	I <sub>DM</sub>	± 20	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	2.5	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25°C	2.5
		T <sub>A</sub> = 70°C	1.6
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>sig</sub>	-55 to 150	°C

**Thermal Resistance Ratings**

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	50	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1211. A SPICE Model data sheet is available for this product (FaxBack document #5106).

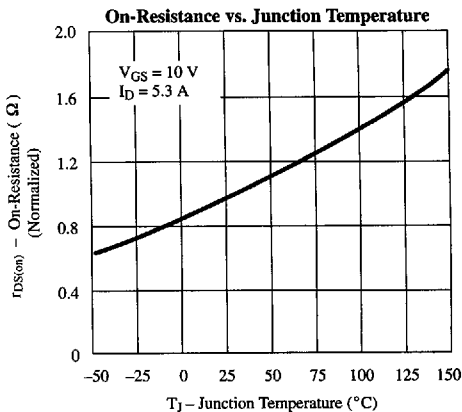
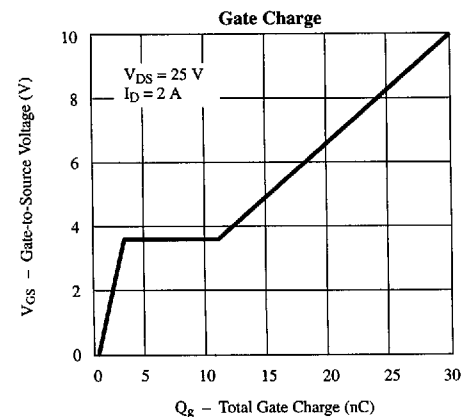
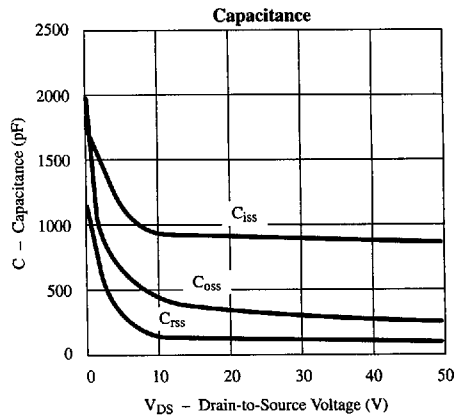
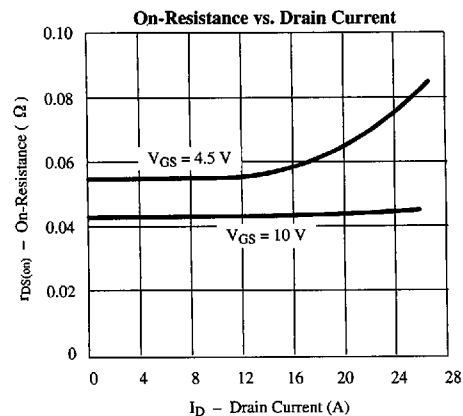
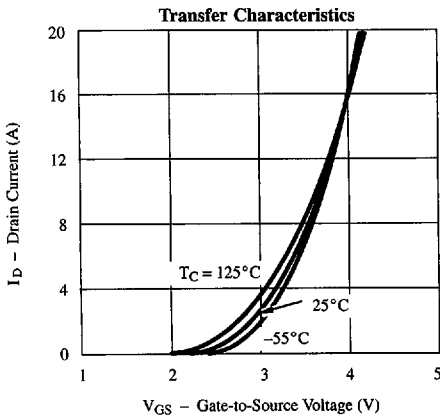
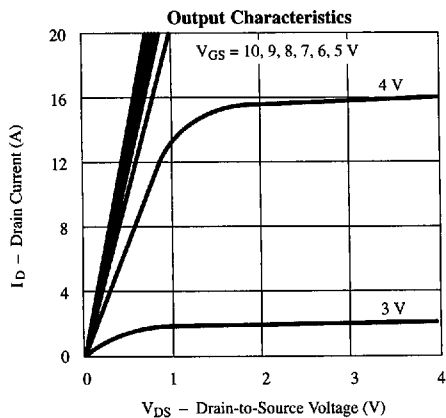
**Specifications ( $T_J = 25^\circ\text{C}$  Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$			2	$\mu\text{A}$
		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			A
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 5.3 \text{ A}$		0.042	0.05	$\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 4.5 \text{ A}$		0.055	0.07	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}, I_D = 5.3 \text{ A}$		11		S
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_S = 1.5 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V
<b>Dynamic<sup>a</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 25 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$		30	50	nC
Gate-Source Charge	$Q_{gs}$			2.5		
Gate-Drain Charge	$Q_{gd}$			9.4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25 \text{ V}, R_L = 25 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		17	40	ns
Rise Time	$t_r$			30	60	
Turn-Off Delay Time	$t_{d(off)}$			95	150	
Fall Time	$t_f$			55	100	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 1.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		130		

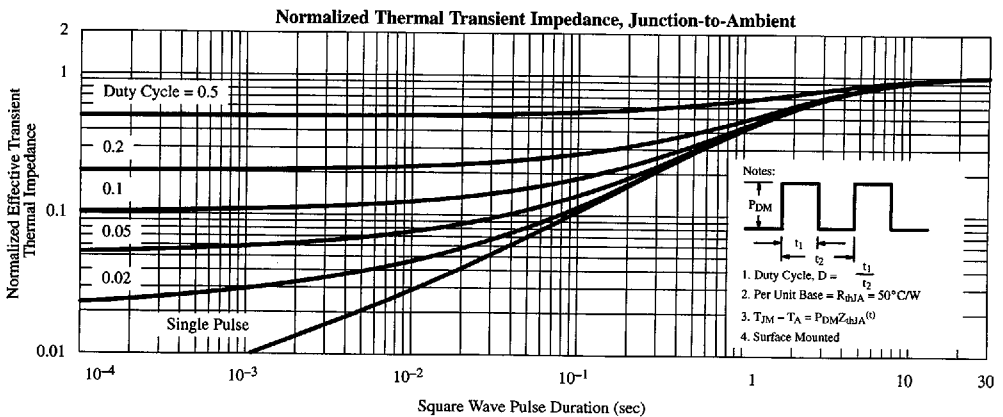
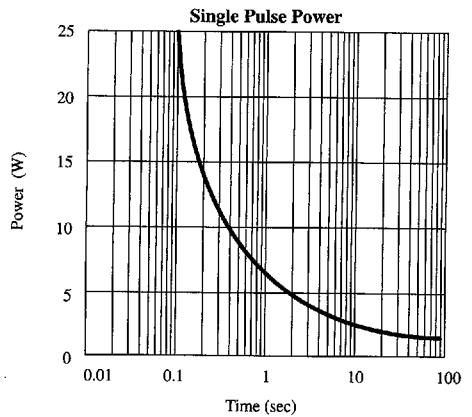
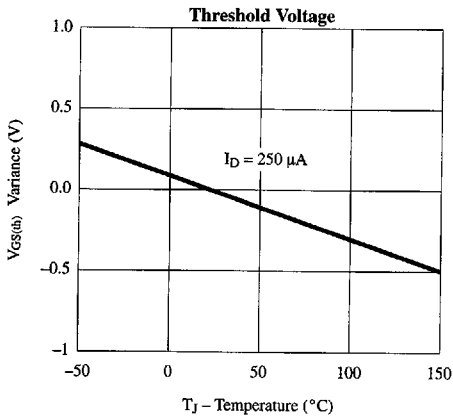
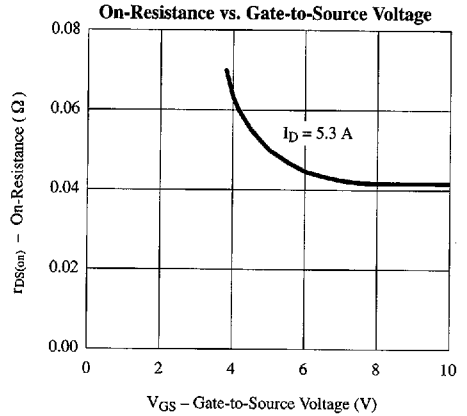
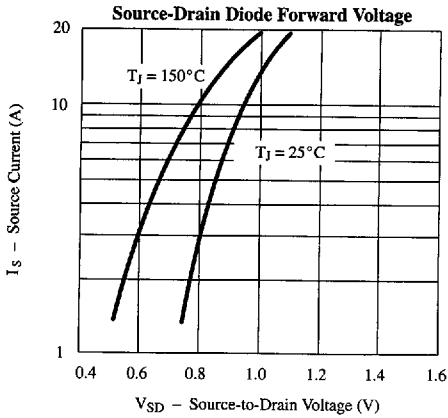
Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

**Typical Characteristics (25°C Unless Otherwise Noted)**

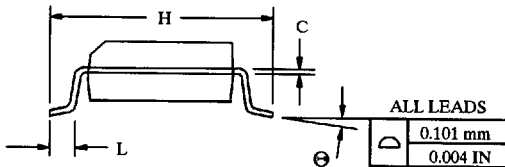
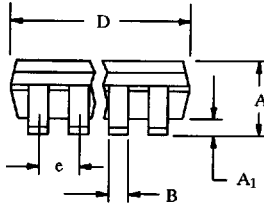
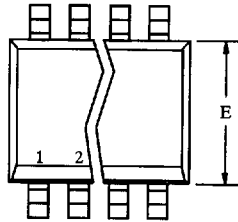


**Typical Characteristics (25°C Unless Otherwise Noted)**



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## SO Package (Y Suffix), 8-16 Leads



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	
A <sub>1</sub>	0.10	0.20	0.004	
B	0.35	0.45	0.014	
C	0.18	0.23	0.007	
D-8	4.60	5.20	0.181	
D-14	8.35	8.95	0.329	
D-16	9.60	10.20	0.378	
E	3.55	4.05	0.140	
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	
L	0.60	0.80	0.024	
Θ	0°	8°	0°	