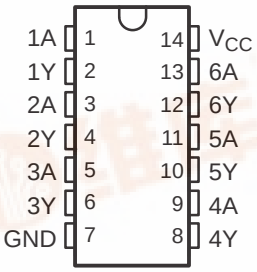
HEX SCHMITT-TRIGGER INVERTERS

Check for Samples: SN54LVC14A, SN74LVC14A

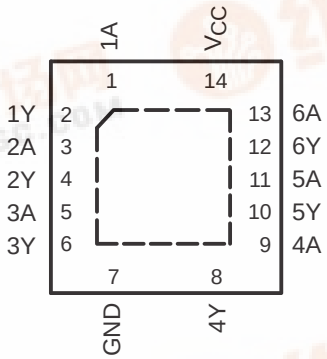
FEATURES

- **Operate From 1.65 V to 3.6 V**
- **Specified From –40°C to 85°C, –40°C to 125°C, and –55°C to 125°C**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 6.4 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

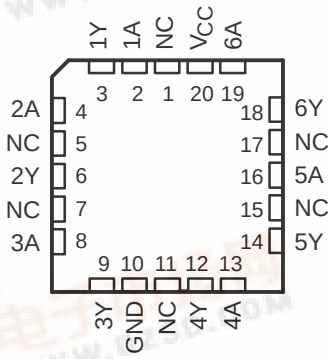
SN54LVC14A . . . J OR W PACKAGE
SN74LVC14A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN74LVC14A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC14A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V V_{CC} operation.

Ordering Information

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC14ARGYR	LC14A
–40°C to 125°C	SOIC – D	Tube of 50	SN74LVC14AD	LVC14A
		Reel of 2500	SN74LVC14ADRG3	
		Reel of 250	SN74LVC14ADT	
	SOP – NS	Reel of 2000	SN74LVC14ANSR	LVC14A
	SSOP – DB	Reel of 2000	SN74LVC14ADBR	LC14A
	TSSOP – PW	Tube of 90	SN74LVC14APW	LC14A
		Reel of 2000	SN74LVC14APWRG3	
		Reel of 250	SN74LVC14APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC14ADGVR	LC14A
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC14AJ	SNJ54LVC14AJ
	CFP – W	Tube of 150	SNJ54LVC14AW	SNJ54LVC14AW
	LCCC – FK	Tube of 55	SNJ54LVC14AFK	SNJ54LVC14AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

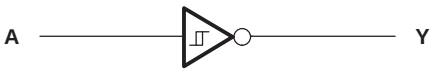
The devices contain six independent inverters and perform the Boolean function $Y = \overline{A}$.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Table 1. FUNCTION TABLE (EACH INVERTER)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Output voltage range(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance	D package (4)		86	°C/W
		DB package(4)		96	
		DGV package(4)		127	
		NS package(4)		76	
		PW package(4)		113	
		RGY package(5)		47	
T_{stg}	Storage temperature range		–65	150	°C
P_{tot}	Power dissipation	T_A = –40°C to 125°C(6) (7)		500	mW

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.
(6) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
(7) For the DB, DGV, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

Recommended Operating Ooditions(1)

			SN54LVC14A		UNIT
			–55 TO 125°C		
			MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions(1)

			SN74LVC14A						UNIT
			T_A = 25°C		–40 TO 85°C		–40 TO 125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V_I	Input voltage		0	5.5	0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4		–4		–4	mA
		V_{CC} = 2.3 V		–8		–8		–8	
		V_{CC} = 2.7 V		–12		–12		–12	
		V_{CC} = 3 V		–24		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4		4		4	mA
		V_{CC} = 2.3 V		8		8		8	
		V_{CC} = 2.7 V		12		12		12	
		V_{CC} = 3 V		24		24		24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LVC14A –55 TO 125°C			UNIT
			MIN	TYP	MAX	
V_{T+} Positive-going threshold		2.7 V	0.8		2	V
		3 V	0.9		2	
		3.6 V	1.1		2	
V_{T-} Negative-going threshold		2.7 V	0.4		1.4	V
		3 V	0.6		1.5	
		3.6 V	0.8		1.7	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		2.7 V	0.3		1.1	V
		3 V	0.3		1.2	
		3.6 V	0.3		1.2	
V_{OH}	I_{OH} = –100 μA	2.7 V to 3.6 V	V_{CC} – 0.2			V
	I_{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I_{OH} = –24 mA	3 V	2.2			
V_{OL}	I_{OL} = 100 μA	2.7 V to 3.6 V			0.2	V
	I_{OL} = 12 mA	2.7 V			0.4	
	I_{OL} = 24 mA	3 V			0.55	
I_I	V_I = 5.5 V or GND	3.6 V			±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	3.6 V			10	μA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		5(1)		pF

(1) T_A = 25°C

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN74LVC14A						UNIT
			T_A = 25°C			–40 TO 85°C		–40 TO 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going threshold		1.65 V	0.4		1.3	0.4	1.3	0.4	1.3	V
		1.95 V	0.6		1.5	0.6	1.5	0.6	1.5	
		2.3 V	0.8		1.7	0.8	1.7	0.8	1.7	
		2.5 V	0.8		1.7	0.8	1.7	0.8	1.7	
		2.7 V	0.8		2	0.8	2	0.8	2	
		3 V	0.9		2	0.9	2	0.9	2	
		3.6 V	1.1		2	1.1	2	1.1	2	
V_{T-} Negative-going threshold		1.65 V	0.15		0.85	0.15	0.85	0.15	0.85	V
		1.95 V	0.25		0.95	0.25	0.95	0.25	0.95	
		2.3 V	0.4		1.2	0.4	1.2	0.4	1.2	
		2.5 V	0.4		1.2	0.4	1.2	0.4	1.2	
		2.7 V	0.4		1.4	0.4	1.4	0.4	1.4	
		3 V	0.6		1.5	0.6	1.5	0.6	1.5	
		3.6 V	0.8		1.7	0.8	1.7	0.8	1.7	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		1.65 V	0.1		1.15	0.1	1.15	0.1	1.15	V
		1.95 V	0.15		1.25	0.15	1.25	0.15	1.25	
		2.3 V	0.25		1.3	0.25	1.3	0.25	1.3	
		2.5 V	0.25		1.3	0.25	1.3	0.25	1.3	
		2.7 V	0.3		1.1	0.3	1.1	0.3	1.1	
		3 V	0.3		1.2	0.3	1.2	0.3	1.2	
		3.6 V	0.3		1.2	0.3	1.2	0.3	1.2	
V_{OH}	I_{OH} = –100 μA	1.65 V to 3.6 V	V_{CC} – 0.2			V_{CC} – 0.2		V_{CC} – 0.3		V
	I_{OH} = –4 mA	1.65 V	1.29			1.2		1.05		
	I_{OH} = –8 mA	2.3 V	1.9			1.7		1.65		
	I_{OH} = –12 mA	2.7 V	2.2			2.2		2.05		
		3 V	2.4			2.4		2.25		
	I_{OH} = –24 mA	3 V	2.3			2.2		2		
V_{OL}	I_{OL} = 100 μA	1.65 V to 3.6 V			0.1		0.2		0.3	V
	I_{OL} = 4 mA	1.65 V			0.24		0.45		0.6	
	I_{OL} = 8 mA	2.3 V			0.3		0.7		0.75	
	I_{OL} = 12 mA	2.7 V			0.4		0.4		0.6	
	I_{OL} = 24 mA	3 V			0.55		0.55		0.8	
I_I	V_I = 5.5 V or GND	3.6 V			±1		±5		±20	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	3.6 V			1		10		40	μA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500		500		5000	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		5						pF

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54LVC14A		UNIT
				–55 TO 125°C		
				MIN	MAX	
t_{pd}	A	Y	2.7 V		7.5	ns
			3.3 V ± 0.3 V	1	6.4	

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

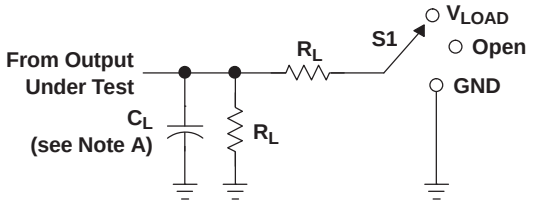
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74LVC14A							UNIT
				T_A = 25°C			–40 TO 85°C		–40 TO 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.8 V ± 0.15 V	1	5	10.5	1	11	1	13	ns
			2.5 V ± 0.2 V	1	3.4	7.3	1	7.8	1	10	
			2.7 V	1	3.6	7.3	1	7.5	1	9.5	
			3.3 V ± 0.3 V	1	3.2	6.2	1	6.4	1	8	
$t_{sk(o)}$			3.3 V ± 0.3 V			1		1		1.5	ns

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	f = 10 MHz	1.8 V	11	pF
			2.5 V	12	
			3.3 V	15	

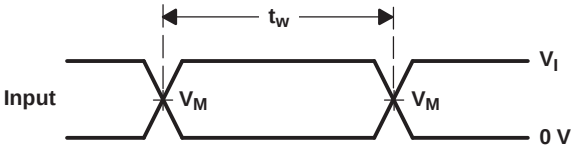
Parameter Measurement Information



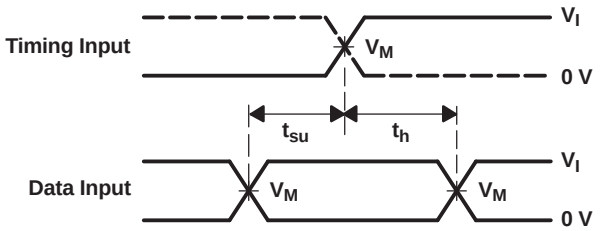
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

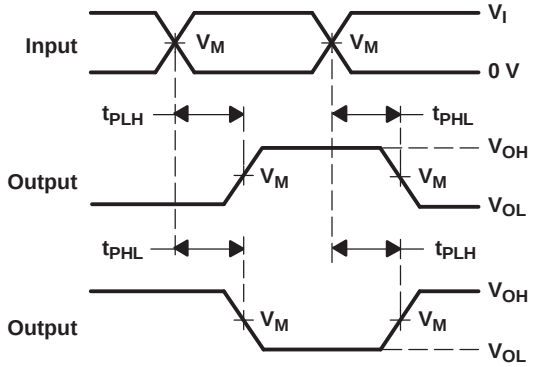
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



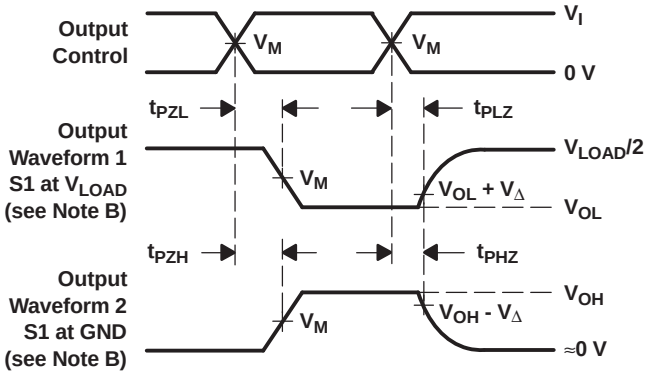
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
5962-9761501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg
5962-9761501QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg
5962-9761501QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg
5962-9761501V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg
5962-9761501VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg
5962-9761501VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg
SN74LVC14AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74LVC14ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADRG3	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260
SN74LVC14ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260

TEXAS INSTRUMENTS

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
SN74LVC14ADT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ADTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74LVC14APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14APWRG3	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260
SN74LVC14APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
SN74LVC14ARGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
SN74LVC14ARGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260

www.ti.com

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
SNJ54LVC14AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg
SNJ54LVC14AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg
SNJ54LVC14AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.t
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate inf
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical an
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for releas

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Cu

OTHER QUALIFIED VERSIONS OF SN54LVC14A, SN54LVC14A-SP, SN74LVC14A :

- Catalog: SN74LVC14A, SN54LVC14A
- Automotive: SN74LVC14A-Q1, SN74LVC14A-Q1

www.ti.com

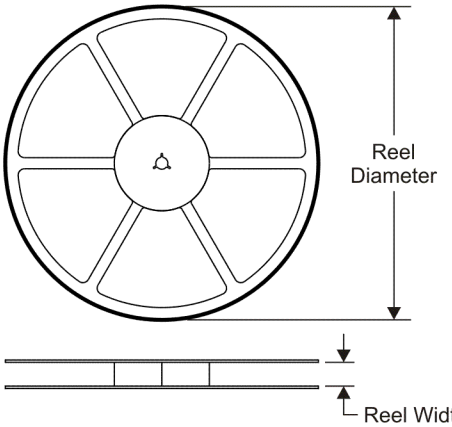
- Enhanced Product: SN74LVC14A-EP, SN74LVC14A-EP
- Military: SN54LVC14A
- Space: SN54LVC14A-SP

NOTE: Qualified Version Definitions:

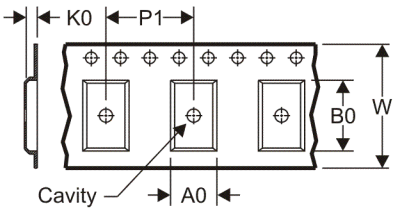
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

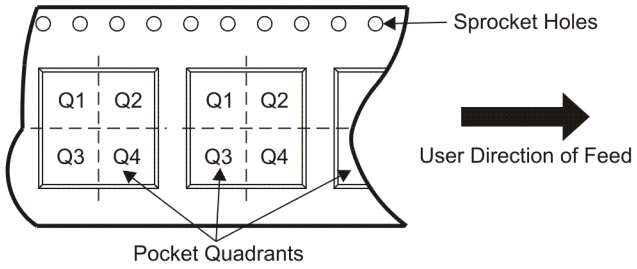


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

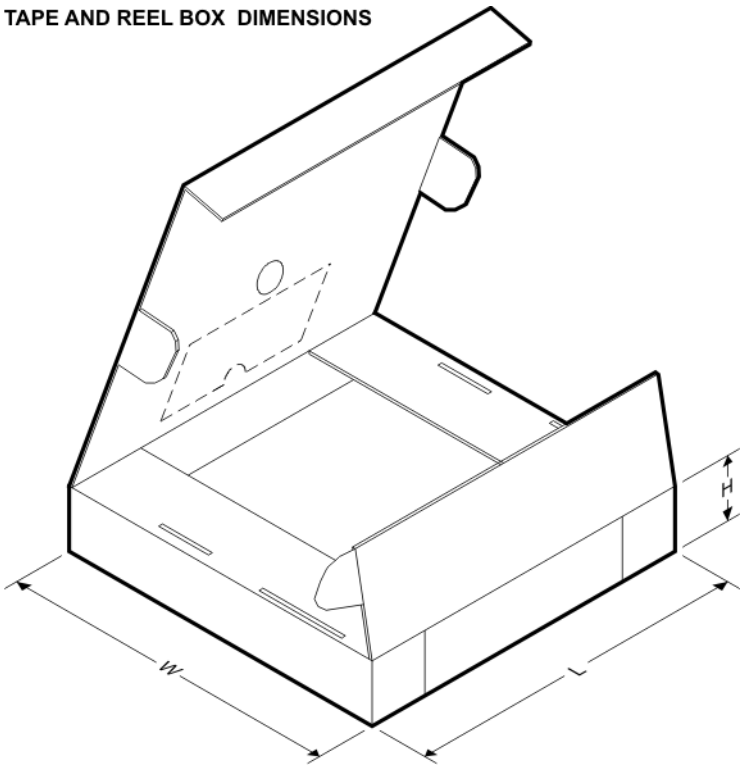
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC14ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVC14ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC14ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC14ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC14APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14APWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LVC14APWRG3	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LVC14APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC14ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

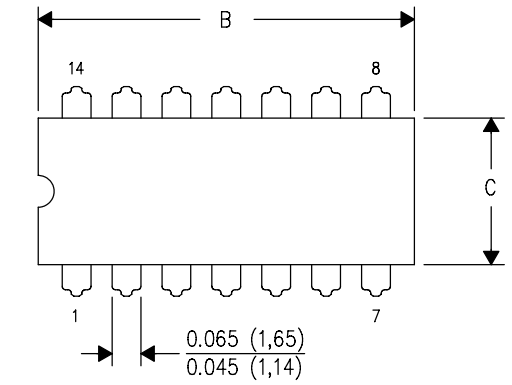


*All dimensions are nominal

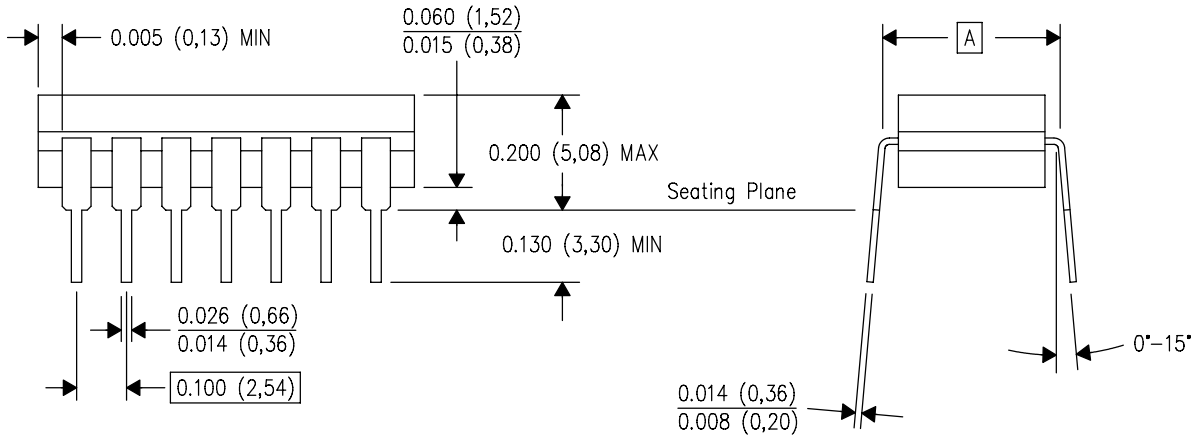
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC14ADBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74LVC14ADGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
SN74LVC14ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LVC14ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVC14ADT	SOIC	D	14	250	346.0	346.0	33.0
SN74LVC14ANSR	SO	NS	14	2000	346.0	346.0	33.0
SN74LVC14APWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74LVC14APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC14APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC14APWT	TSSOP	PW	14	250	346.0	346.0	29.0
SN74LVC14ARGYR	VQFN	RGY	14	3000	346.0	346.0	29.0

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



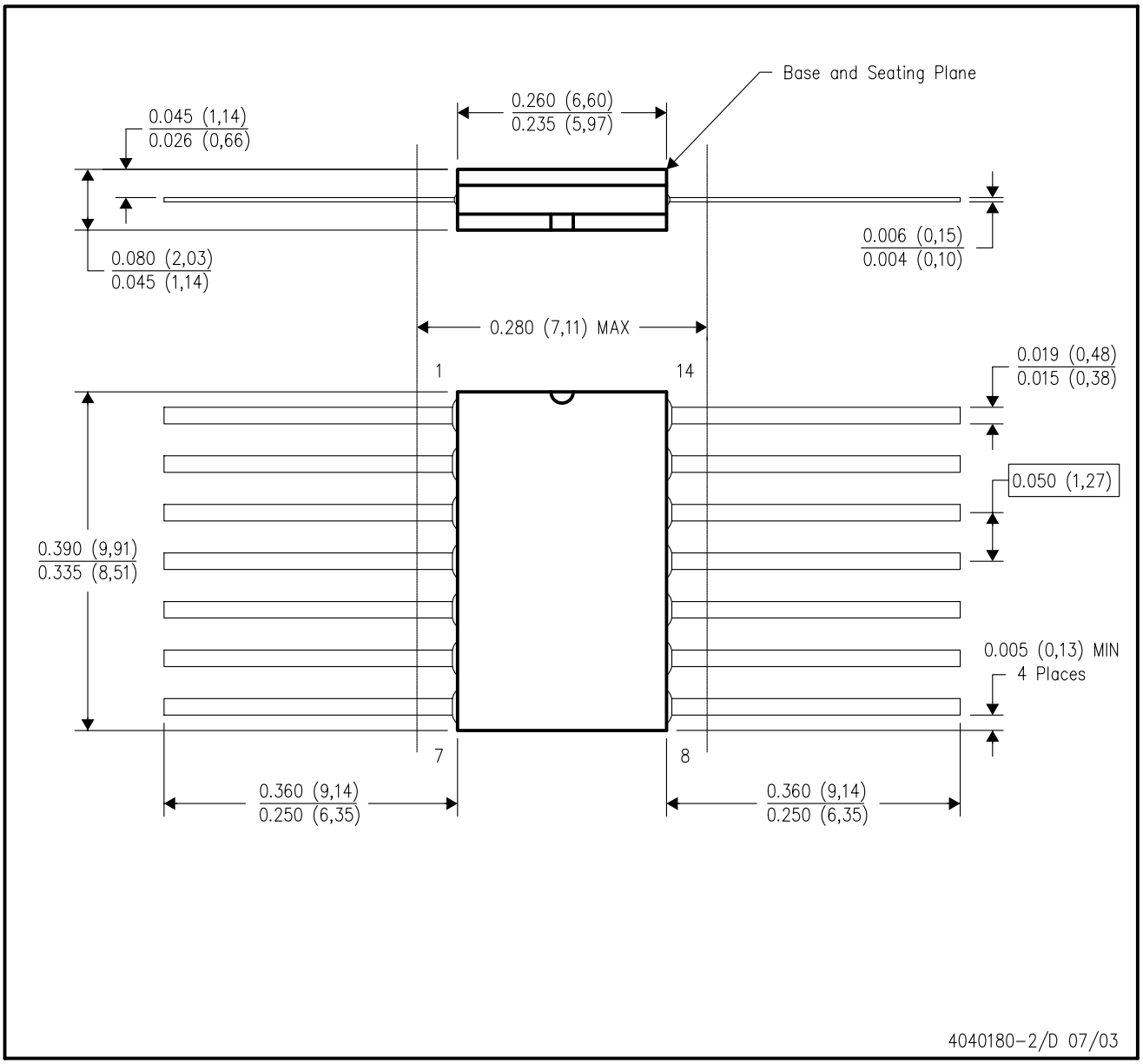
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

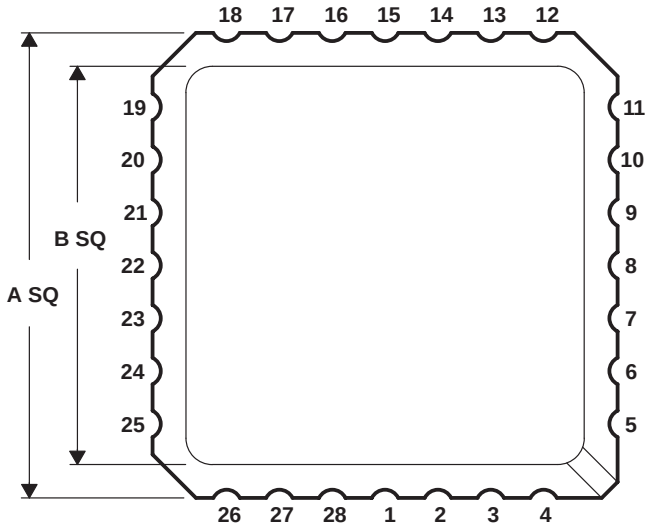
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



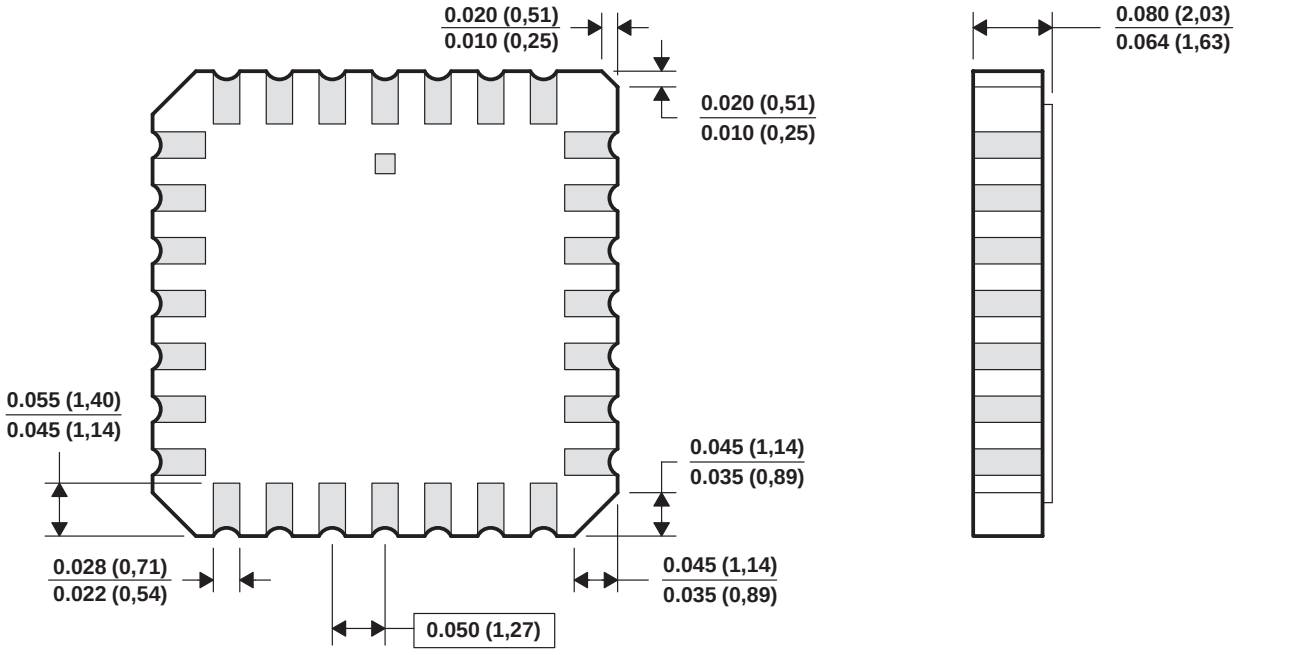
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

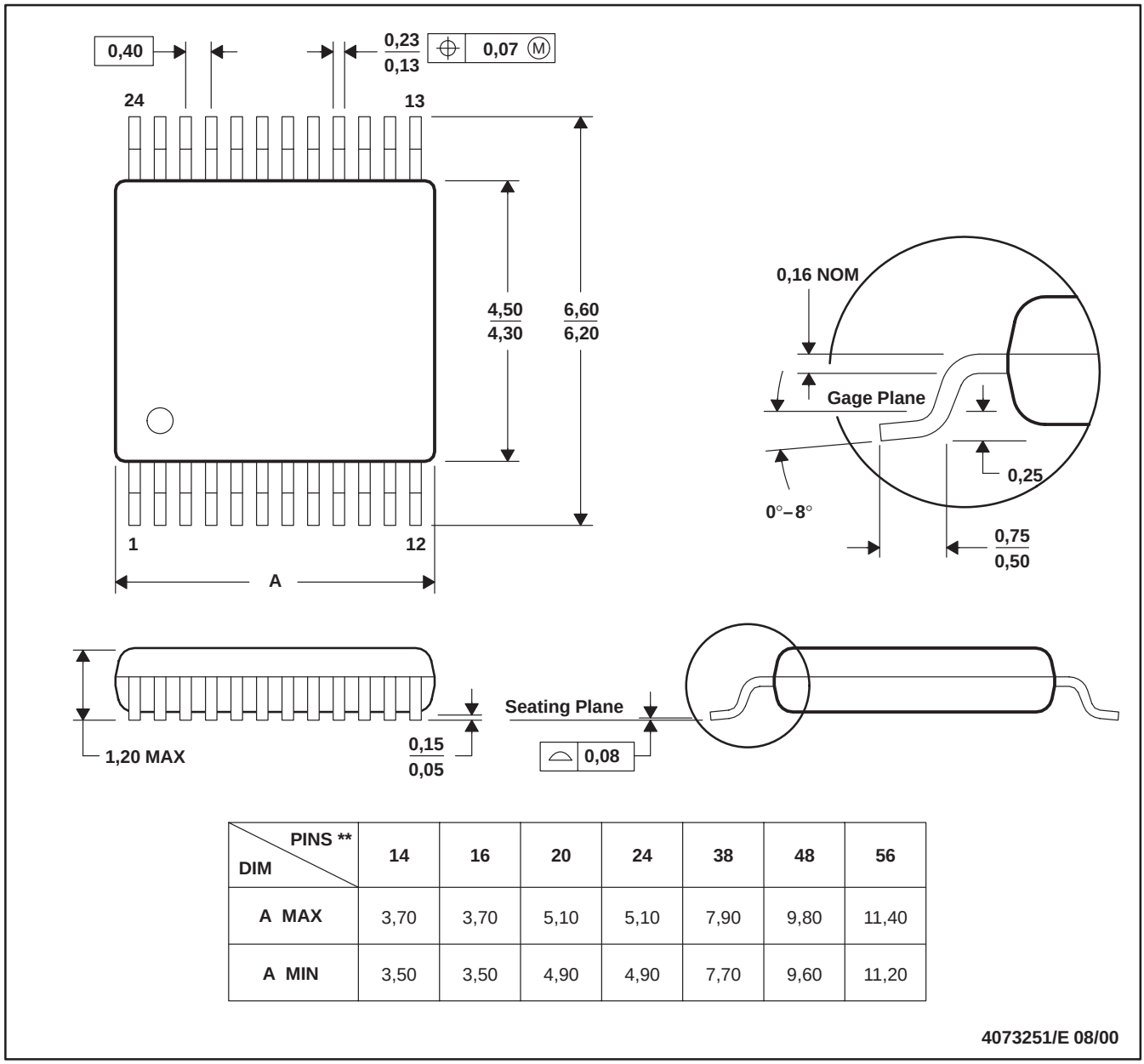


4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

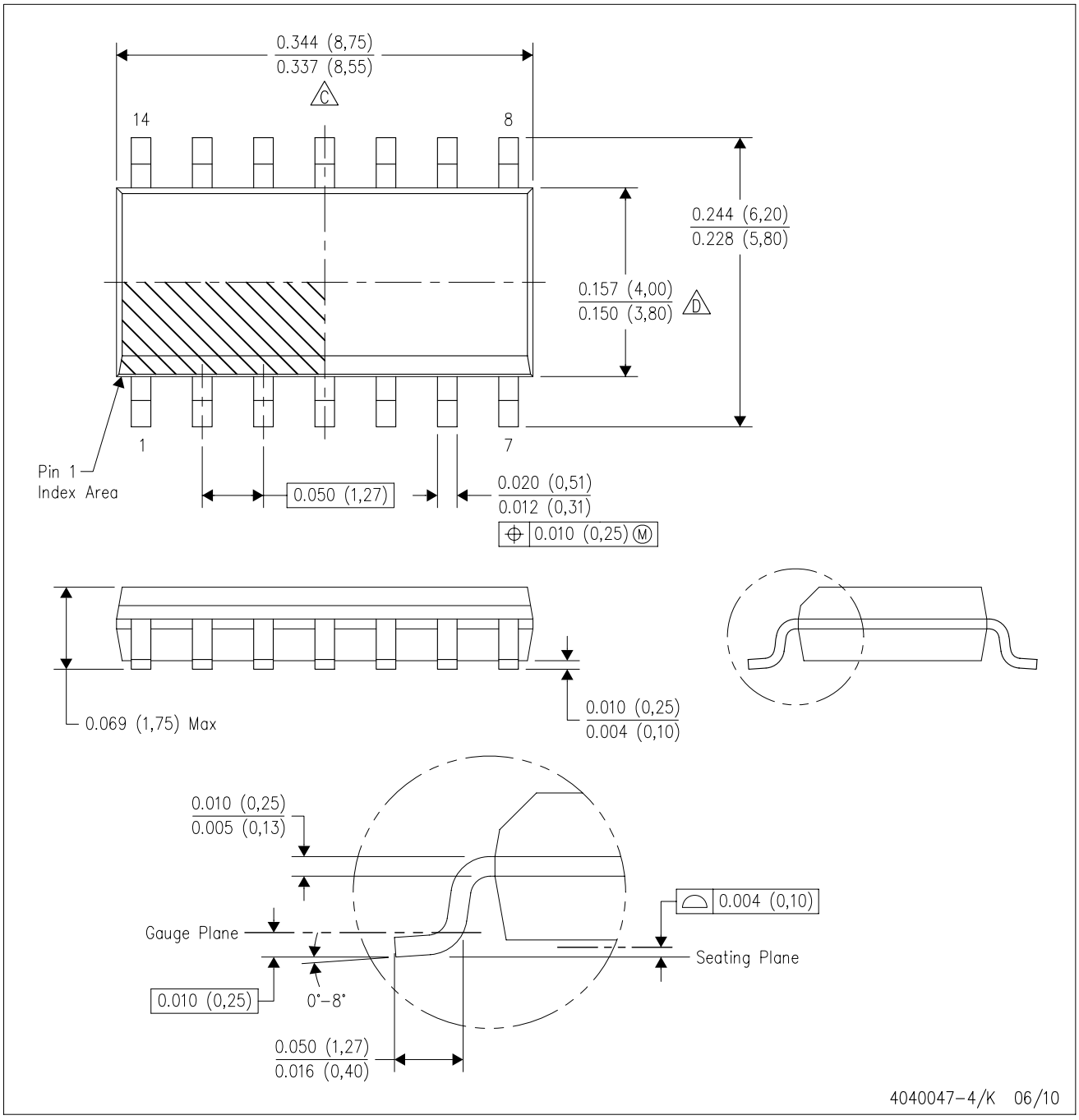
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

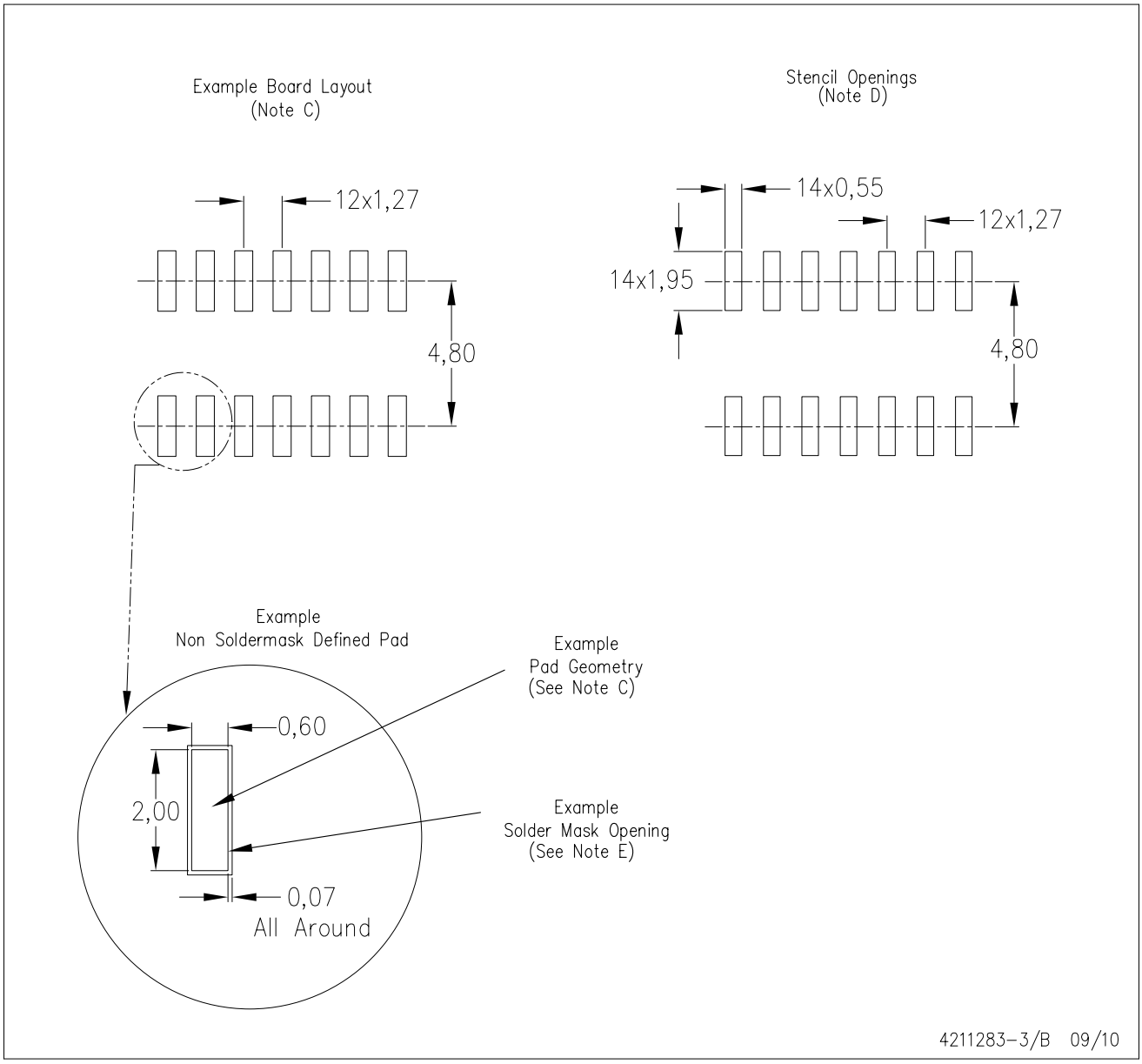
D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



4040047–4/K 06/10

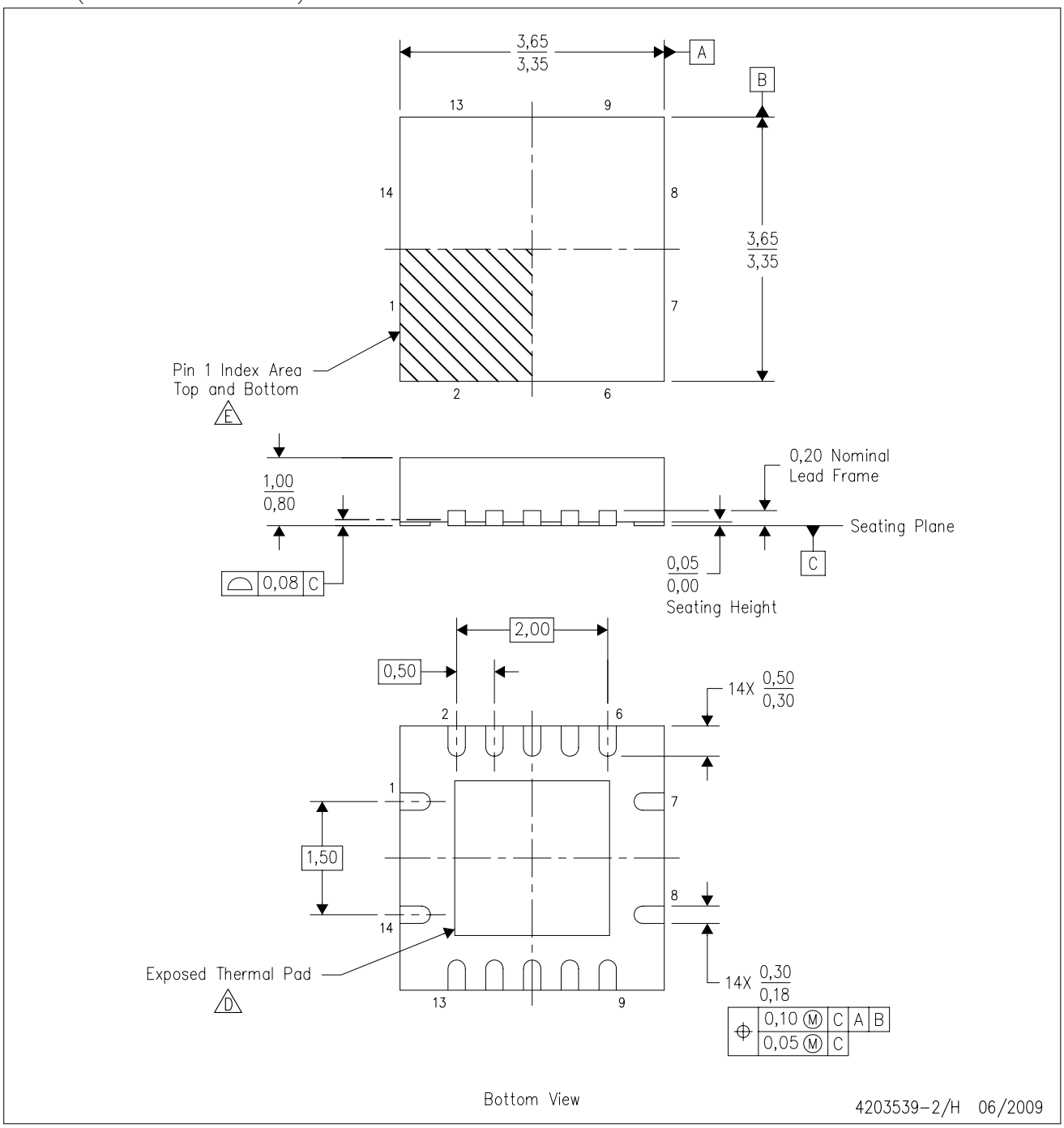
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BA.

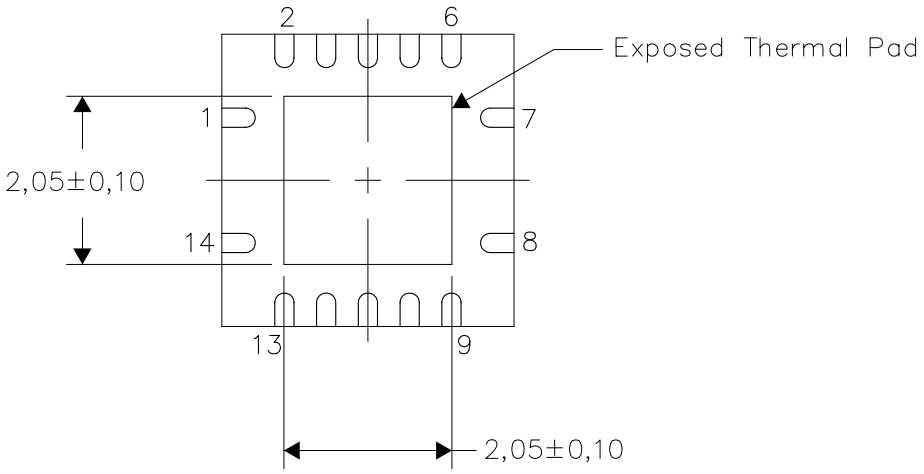
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

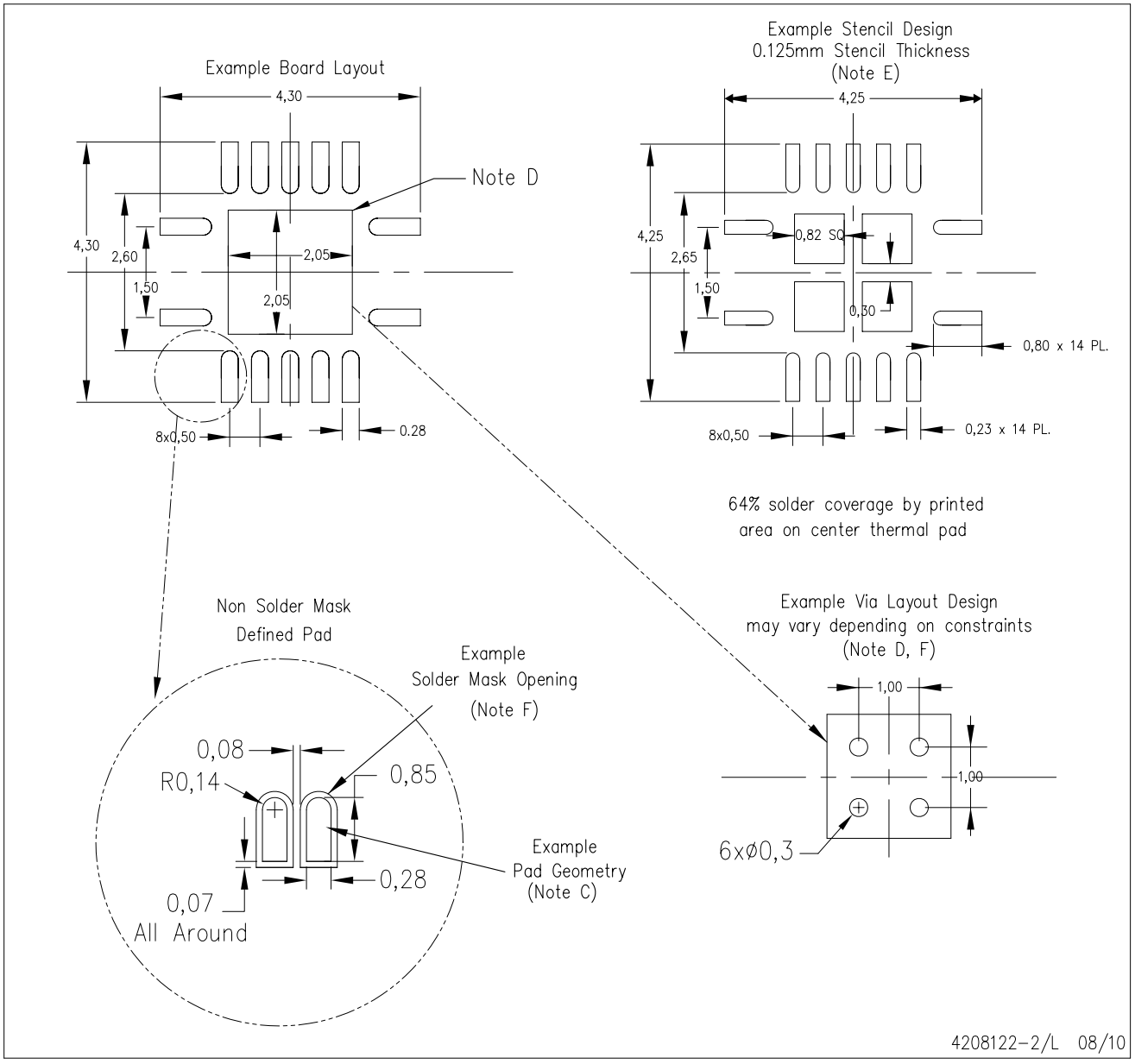


Bottom View

NOTES: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

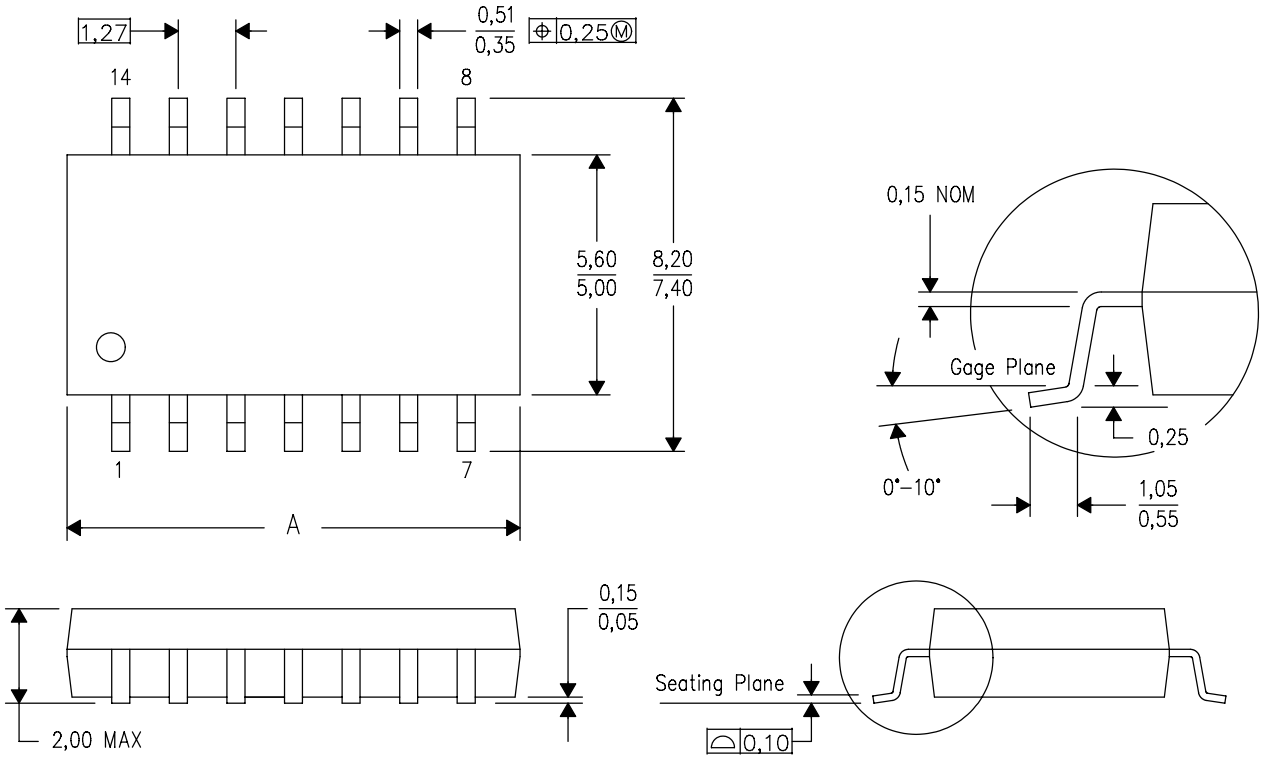


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



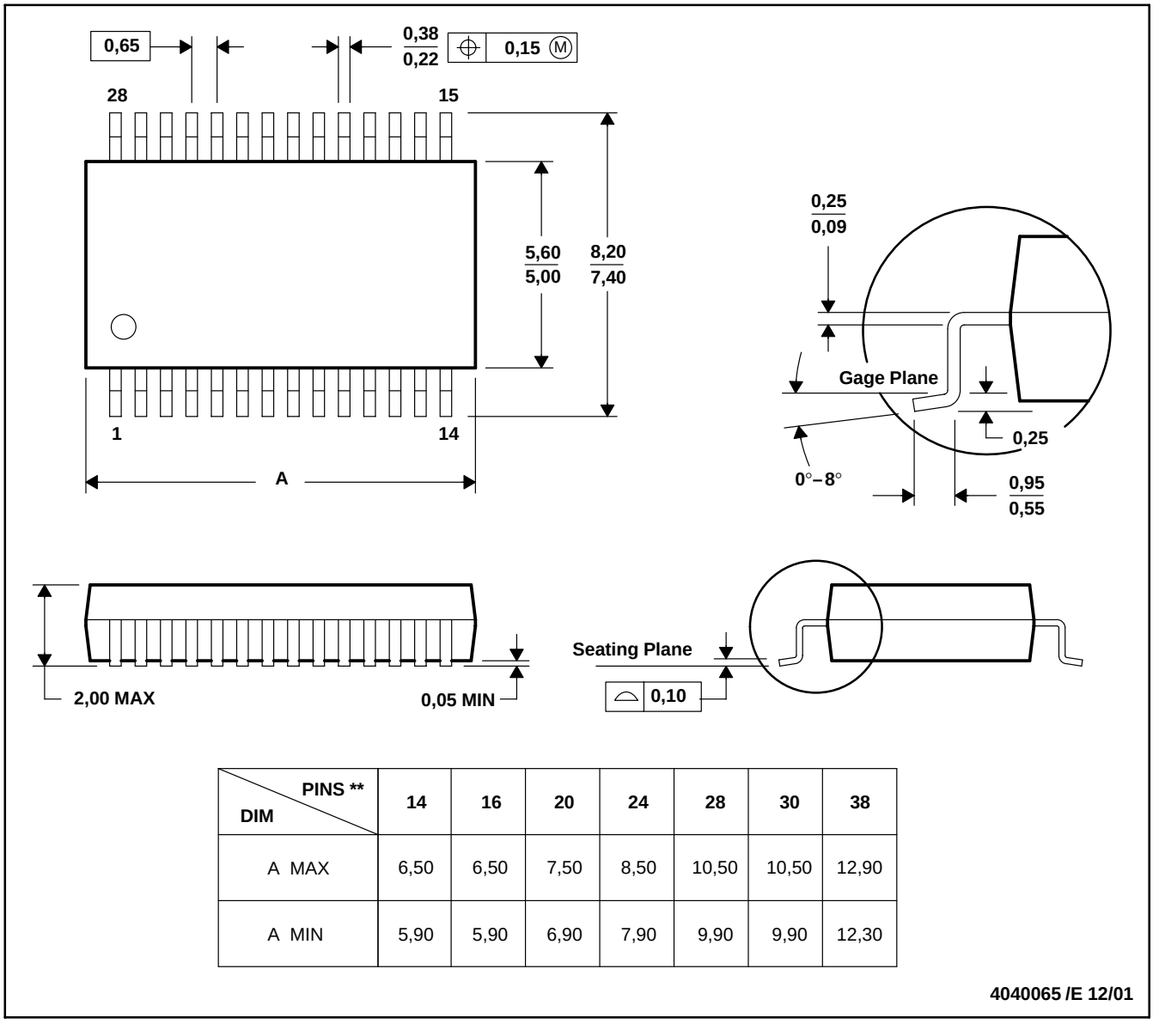
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



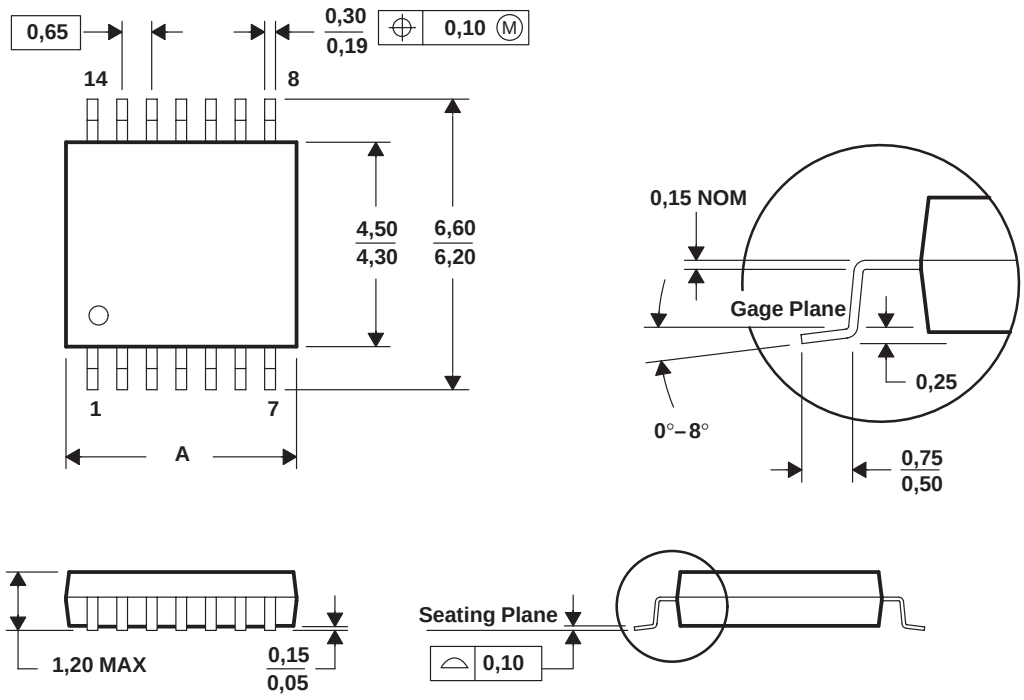
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

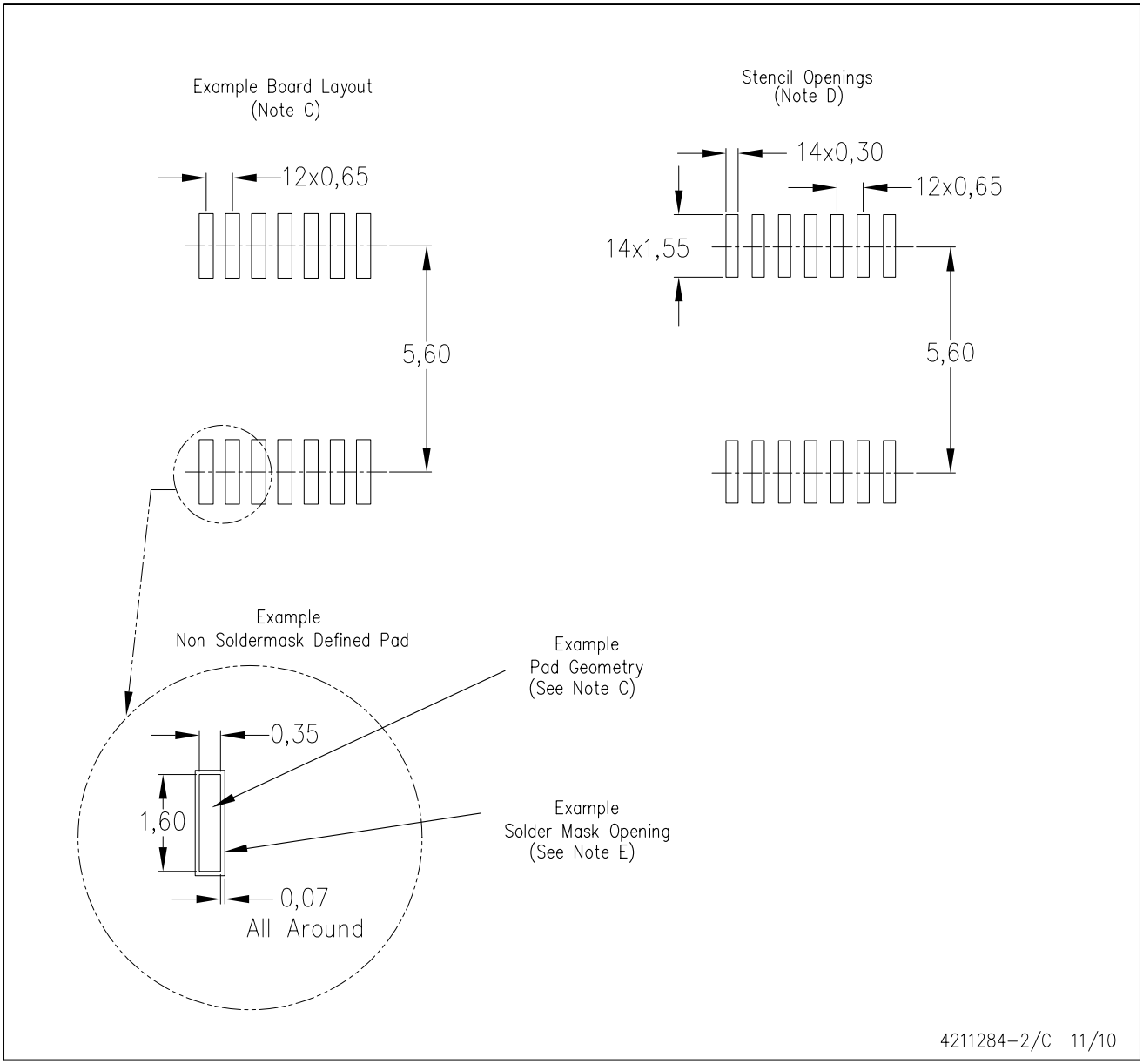


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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