September 2005

LMH6574
4:1 High Speed Video Multiplexer

General Description

The LMH™6574 is a high performance analog multiplexer optimized for professional grade video and other high fidelity high bandwidth analog applications. The output amplifier selects any one of four buffered input signals based on the state of the two address bits. The LMH6574 provides a 400 MHz bandwidth at 2 V_{PP} output signal levels. Multimedia and high definition television (HDTV) applications can benefit from the LMH6574's 0.1 dB bandwidth of 150 MHz and its 2200 V/µs slew rate.

The LMH6574 supports composite video applications with its 0.02% and 0.05˚ differential gain and phase errors for NTSC and PAL video signals while driving a single, back terminated 75Ω load. An 80 mA linear output current is available for driving multiple video load applications.

The LMH6574 gain is set by external feedback and gain set resistors for maximum flexibility.

The LMH6574 is available in the 14 pin SOIC package.

Features

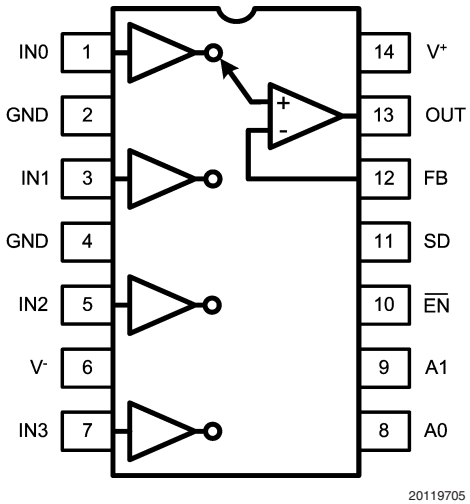
- 500 MHz, 500 mV –3 dB bandwidth, A_V = 2
- 400 MHz, 2V_{PP} –3 dB bandwidth, A_V = 2
- 8 ns channel switching time
- 70 dB channel to channel isolation @ 10 MHz
- 0.02%, 0.05˚ diff. gain, phase
- 0.1 dB gain flatness to 150 MHz
- 2200 V/µs slew rate
- Wide supply voltage range: 6V (±3V) to 12V (±6V)
- –68 dB HD2 @ 5 MHz
- –84 dB HD3 @ 5 MHz

Applications

- Video router
- Multi input video monitor
- Instrumentation / Test equipment
- Receiver IF diversity switch
- Multi Channel A/D Driver
- Picture in Picture video switch

Connection Diagram

14-Pin SOIC



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Top View

Truth Table

A1	A0	$\overline{EN}$	SD	OUT
1	1	0	0	CH 3
1	0	0	0	CH2
0	1	0	0	CH1
0	0	0	0	CH 0
X	X	1	0	Disable
X	X	X	1	Shutdown

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
14-Pin SOIC	LMH6574MA	LH6574MA	55 Units/Rail	M14A
	LMH6574MAX		2.5k Units Tape and Reel	

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	(Note 4)
Human Body Model	2000V
Machine Model	200V
Supply Voltage ($V^+ - V^-$)	13.2V
I_{OUT} (Note 3)	130 mA
Signal & Logic Input Pin Voltage	±(V_S+0.6V)
Signal & Logic Input Pin Current	±20 mA
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Soldering Information	
Infrared or Convection (20 sec)	235 ˚C
Wave Soldering (10 sec)	260 ˚C

Operating Ratings (Note 1)

Operating Temperature	−40 ˚C to 85 ˚C	
Supply Voltage Range	6V to 12V	
Thermal Resistance		
Package	(θ_{JA})	(θ_{JC})
14-Pin SOIC	130˚C/W	40˚C/W

±5V Electrical Characteristics

V_S = ±5V, R_L = 100Ω, A_V = 2 V/V, R_F = 575 Ω, T_J = 25 ˚C, Unless otherwise specified. **Bold** numbers specify limits at temperature extremes.

Symbol	Parameter	Conditions (Note 2)	Min	Typ	Max	Units
Frequency Domain Performance						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		500		MHz
LSBW	−3 dB Bandwidth	V_{OUT} = 2 V_{PP}		400		MHz
.1 dBBW	0. 1 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		150		MHz
DG	Differential Gain	R_L = 150Ω, f = 4.43 MHz		0.02		%
DP	Differential Phase	R_L = 150Ω, f = 4.43MHz		0.05		deg
XTLK	Channel to Channel Crosstalk	All Hostile, 5 MHz		−85		dB
Time Domain Response						
TRS	Channel to Channel Switching Time	Logic Transition to 90% Output		8		ns
	Enable and Disable Times	Logic Transition to 90% or 10% Output		10		ns
TRL	Rise and Fall Time	4V Step		2.4		ns
TSS	Settling Time to 0.05%	2V Step		17		ns
OS	Overshoot	2V Step		5		%
SR	Slew Rate	4V Step		2200		V/µs
Distortion						
HD2	2nd Harmonic Distortion	2 V_{PP} , 5 MHz		−68		dBc
HD3	3rd Harmonic Distortion	2 V_{PP} , 5 MHz		−84		dBc
IMD	3rd Order Intermodulation Products	10 MHz, Two Tones 2 V_{PP} at Output		−80		dBc
Equivalent Input Noise						
VN	Voltage	>1 MHz, Input Referred		5		nV $\sqrt{Hz}$
ICN	Current	>1 MHz, Input Referred		5		pA/ $\sqrt{Hz}$
Static, DC Performance						
CHGM	Channel to Channel Gain Difference	DC, Difference in Gain Between Channels		±0.005	±0.032 **±0.035**	%
VIO	Input Offset Voltage (Note 5)	V_{IN} = 0V		1	±20 **±25**	mV
DVIO	Offset Voltage Drift			30		µV/˚C
IBN	Input Bias Current (Notes 7, 5)	V_{IN} = 0V		−3	±5 **±5.6**	µA
DIBN	Bias Current Drift			11		nA/˚C
	Inverting Input Bias Current	Pin 12, Feedback Point, V_{IN} = 0V		−7	±10 **±13**	
PSRR	Power Supply Rejection Ratio (Note 5)	DC, Input Referred	47 **45**	54		dB

±5V Electrical Characteristics (Continued)

V_S = ±5V, R_L = 100Ω, A_V = 2 V/V, R_F = 575 Ω, T_J = 25 ˚C, Unless otherwise specified. **Bold** numbers specify limits at temperature extremes.

Symbol	Parameter	Conditions (Note 2)	Min	Typ	Max	Units
ICC	Supply Current (Note 5)	No Load		13	16 **18**	mA
	Supply Current Disabled(Note 5)	$\overline{ENABLE}$>2V		4.7	5.8 **5.9**	mA
	Supply Current Shutdown	SHUTDOWN > 2V		1.8	2.5 **2.6**	mA
VIH	Logic High Threshold(Note 5)	Select & Enable Pins (SD & $\overline{EN}$)	2.0			V
VIL	Logic Low Threshold (Note 5)	Select & Enable Pins (SD & $\overline{EN}$)			0.8	V
IiL	Logic Pin Input Current Low (Note 7)	Logic Input = 0V Select & Enable Pins (SD & $\overline{EN}$)	–2.9 **-8.5**	–1		µA
IiH	Logic Pin Input Current High (Note 7)	Logic Input = 2.0V, Select & Enable Pins (SD & $\overline{EN}$)		47	68 **72.5**	µA
Miscellaneous Performance						
RIN+	Input Resistance			5		kΩ
CIN	Input Capacitance			0.8		pF
ROUT	Output Resistance	Output Active, ($\overline{EN}$ and SD < 0.8 V)		0.04		Ω
ROUT	Output Resistance	Output Disabled, ($\overline{EN}$ or SD > 2V)		3000		Ω
COUT	Output Capacitance	Output Disabled, ($\overline{EN}$ or SD > 2V)		3.1		pF
VO	Output Voltage Range	No Load	±3.54 **±3.53**	±3.7		V
VOL		R_L = 100Ω	±3.18 **±3.17**	±3.5		V
CMIR	Input Voltage Range		±2.5	±2.6		V
IO	Linear Output Current (Notes 5, 7)	V_{IN} = 0V	+60 -70 **+50** **–60**	±80		mA
ISC	Short Circuit Current (Note 3)	V_{IN} = ±2V, Output Shorted to Ground		±230		mA

±3.3V Electrical Characteristics

V_S = ±3.3V, R_L = 100Ω, A_V = 2 V/V, R_F = 575 Ω; Unless otherwise specified.

Symbol	Parameter	Conditions (Note 2)	Min	Typ	Max	Units
Frequency Domain Performance						
SSBW	–3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		475		MHz
LSBW	–3 dB Bandwidth	V_{OUT} = 2.0 V_{PP}		375		MHz
0.1 dBBW	0.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		100		MHz
GFP	Peaking	DC to 200 MHz		0.4		dB
XTLK	Channel to Channel Crosstalk	All Hostile, f = 5 MHz		–85		dBc
Time Domain Response						
TRL	Rise and Fall Time	2V Step		2		ns
TSS	Settling Time to 0.05%	2V Step		20		ns
OS	Overshoot	2V Step		5		%
SR	Slew Rate	2V Step		1400		V/µs
Distortion						
HD2	2nd Harmonic Distortion	2 V_{PP}, 10 MHz		–67		dBc
HD3	3rd Harmonic Distortion	2 V_{PP}, 10 MHz		–87		dBc

±3.3V Electrical Characteristics (Continued)

V_S = ±3.3V, R_L = 100Ω, A_V = 2 V/V, R_F = 575 Ω; Unless otherwise specified.

Symbol	Parameter	Conditions (Note 2)	Min	Typ	Max	Units
Static, DC Performance						
VIO	Input Offset Voltage	V_{IN} = 0V		-5		mV
IBN	Input Bias Current (Note 7)	V_{IN} = 0V		-3		µA
PSRR	Power Supply Rejection Ratio	DC, Input Referred		49		dB
ICC	Supply Current	No Load		12		mA
VIH	Logic High Threshold	Select & Enable Pins (SD & $\overline{EN}$)	1.3			V
VIL	Logic Low Threshold	Select & Enable Pins (SD & $\overline{EN}$)			0.4	V
Miscellaneous Performance						
RIN+	Input Resistance			5		kΩ
CIN	Input Capacitance			0.8		pF
ROUT	Output Resistance			0.06		Ω
VO	Output Voltage Range	No Load		±2		V
VOL		R_L = 100Ω		±1.8		V
CMIR	Input Voltage Range			±1.2		V
IO	Linear Output Current	V_{IN} = 0V		±60		mA
ISC	Short Circuit Current	V_{IN} = ±1V, Output Shorted to Ground		±150		mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Section for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

Note 3: The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150˚C). See the Power Dissipation section of the Application Section for more details. A short circuit condition should be limited to 5 seconds or less.

Note 4: Human Body model, 1.5 kΩ in series with 100 pF. Machine model, 0Ω In series with 200 pF.

Note 5: Parameters guaranteed by electrical testing at 25˚C.

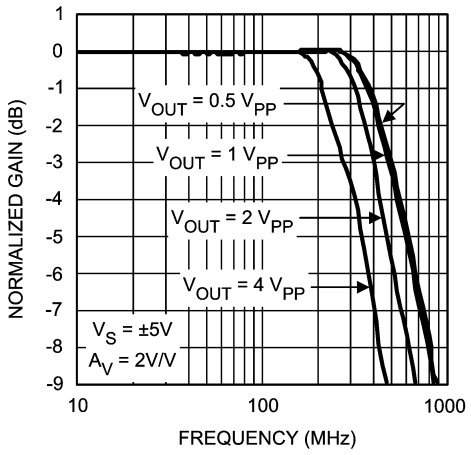
Note 6: Parameters guaranteed by design.

Note 7: Positive Value is current into device.

Typical Performance Characteristics

V_s = ±5V, R_L = 100Ω, A_V = 2, R_F = R_G = 575Ω; unless otherwise specified.

Frequency Response vs. V_{OUT}



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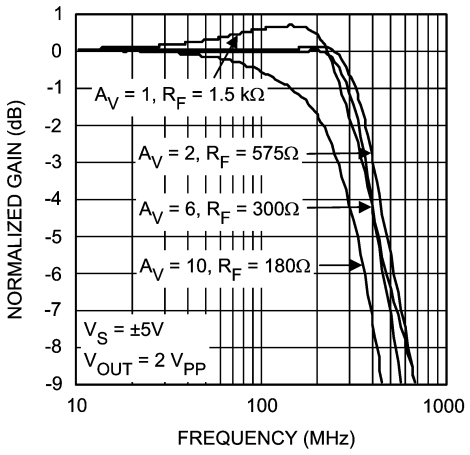
Frequency Response vs. Gain



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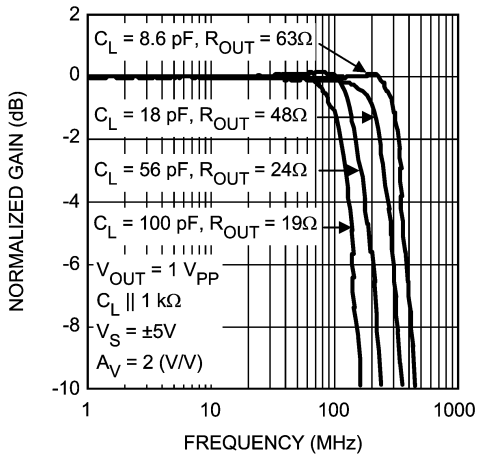
Frequency Response vs. Capacitive Load



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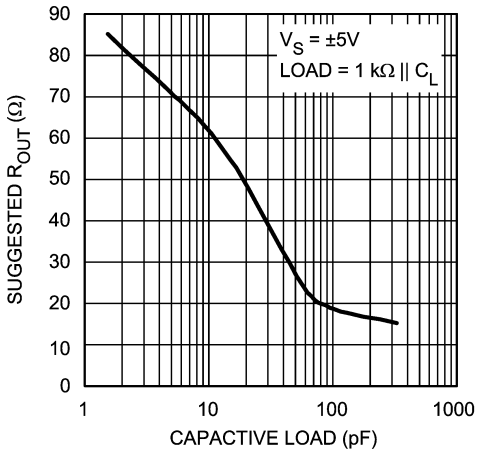
Suggested R_{OUT} vs. Capacitive Load



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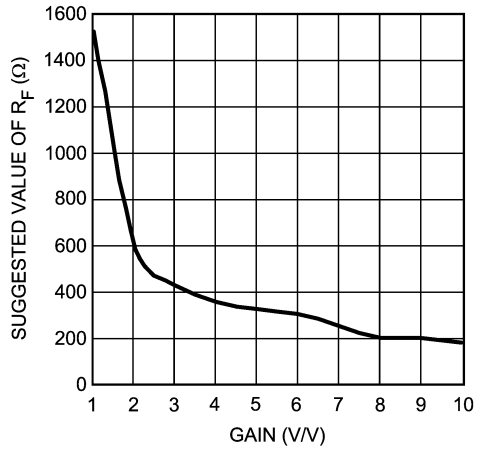
Suggested Value of R_F vs. Gain



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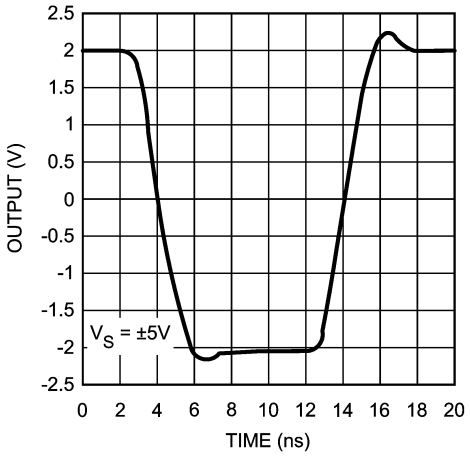
Pulse Response $4V_{PP}$



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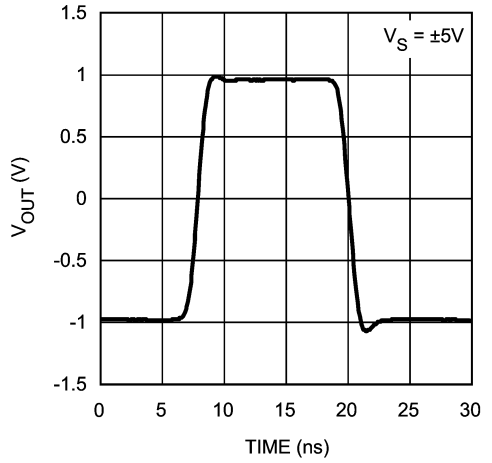
Typical Performance Characteristics V_s = ±5V, R_L = 100Ω, A_V = 2, R_F = R_G = 575Ω; unless otherwise specified. (Continued)

Pulse Response $2V_{PP}$



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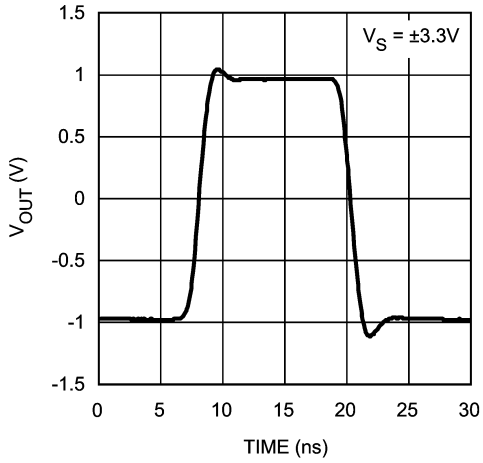
Pulse Response $2V_{PP}$



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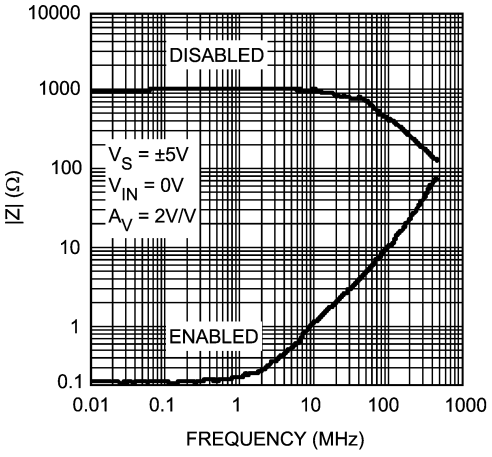
Closed Loop Output Impedance



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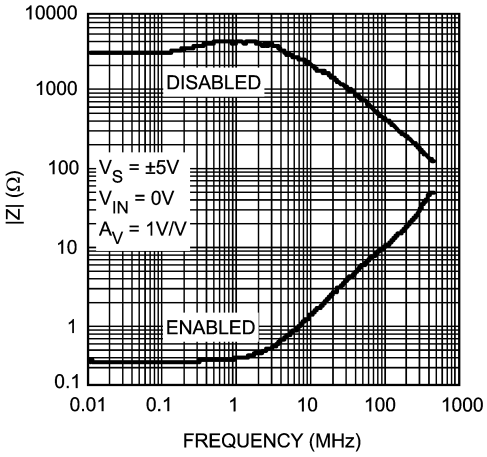
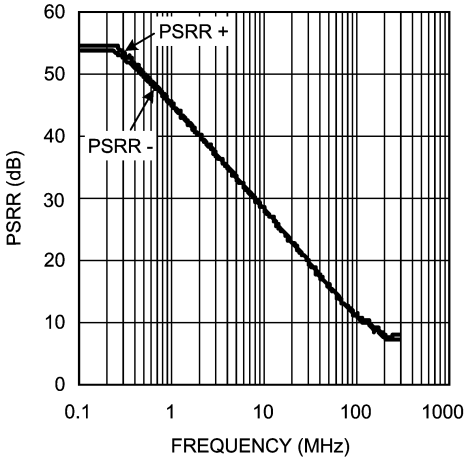
Closed Loop Output Impedance



20119709

PSRR vs. Frequency



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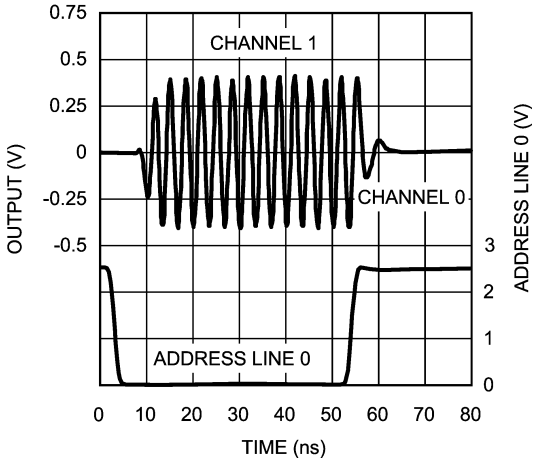
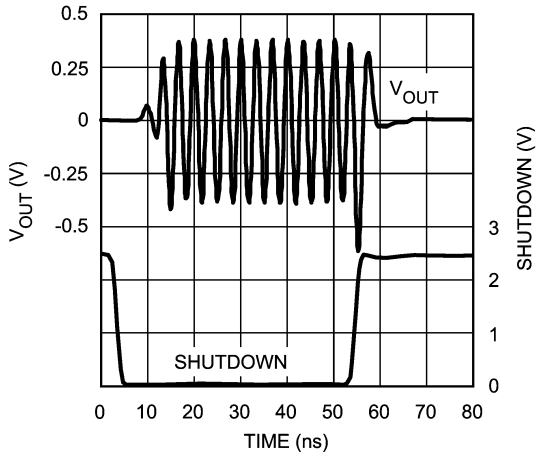
Channel Switching



20119716

Typical Performance Characteristics V_s = ±5V, R_L = 100Ω, A_V = 2, R_F = R_G = 575Ω; unless otherwise specified, (continued)

SHUTDOWN Switching



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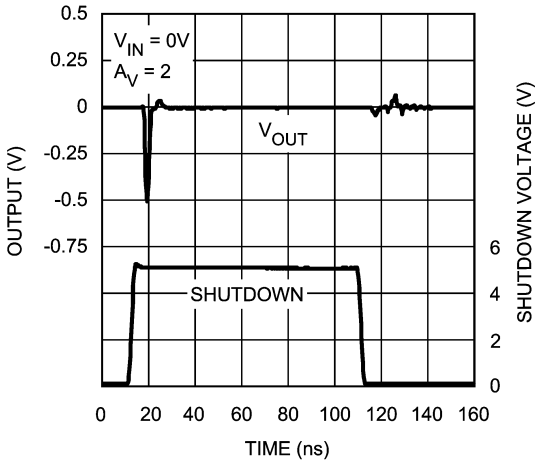
Shutdown Glitch



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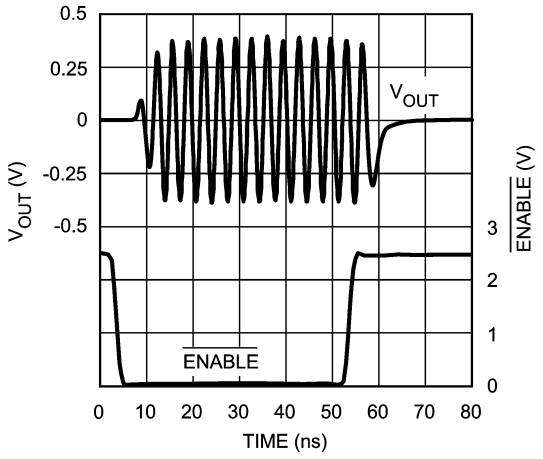
$\overline{\text{ENABLE}}$ Switching



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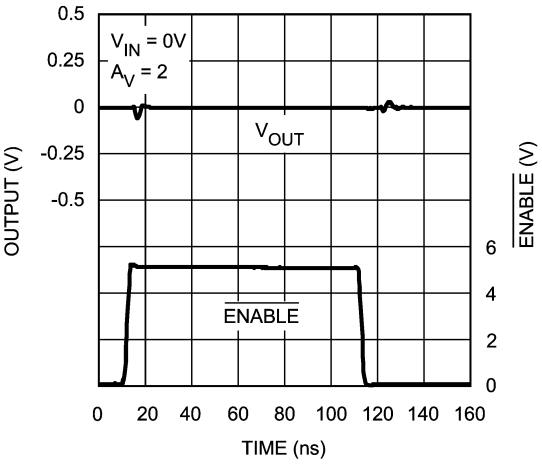
Disable Glitch



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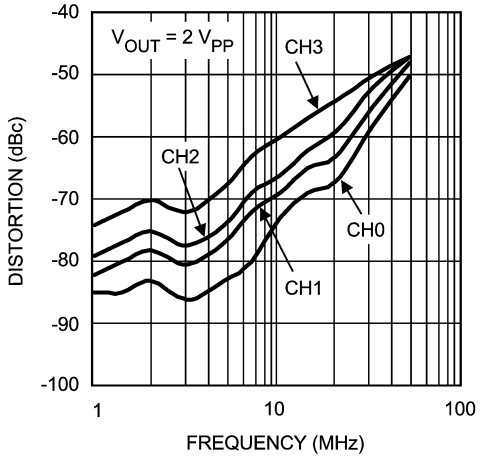
HD2 vs. Frequency



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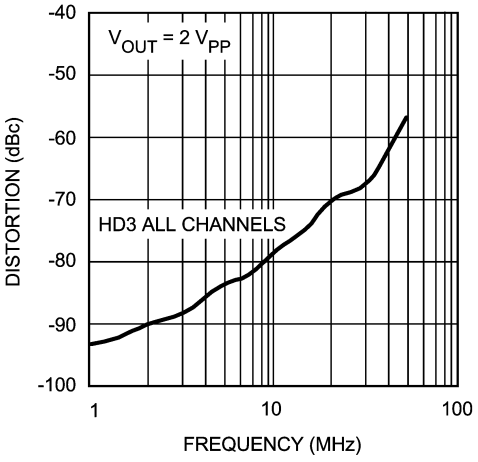
HD3 vs. Frequency



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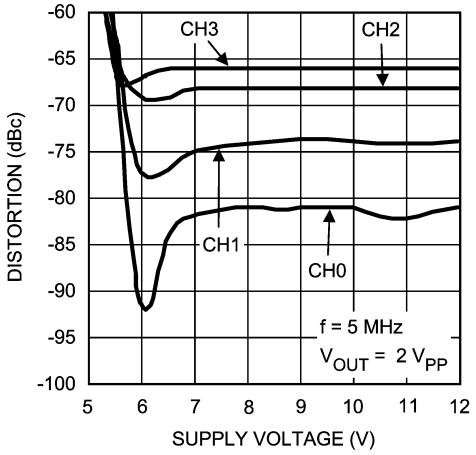
Typical Performance Characteristics V_s = ±5V, R_L = 100Ω, A_V = 2, R_F = R_G = 575Ω; unless otherwise specified (Continued)

HD2 vs. V_S



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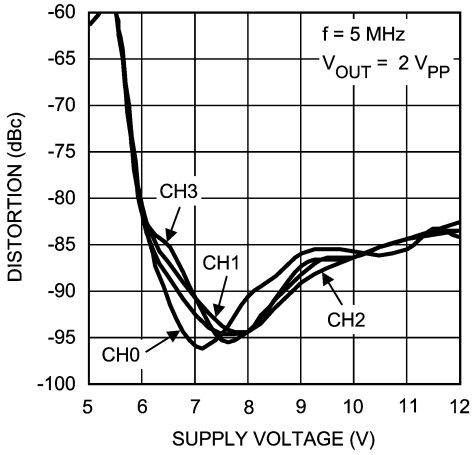
HD3 vs. V_S



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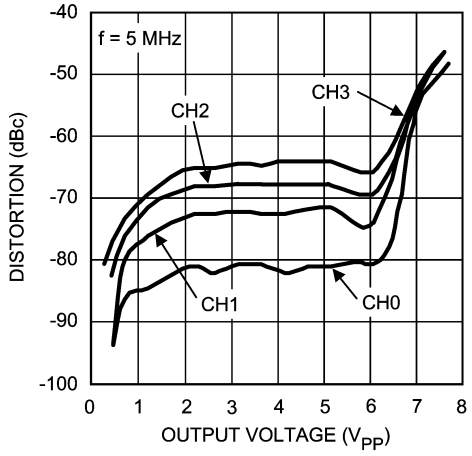
HD2 vs. V_{OUT}



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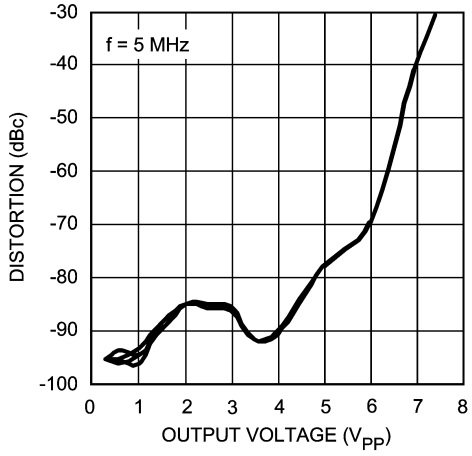
HD3 vs. V_{OUT}



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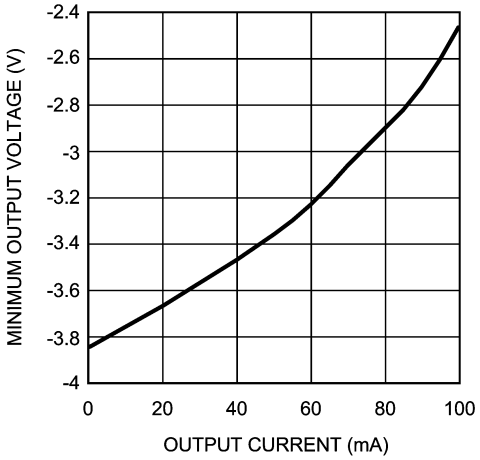
Minimum V_{OUT} vs. I_{OUT}(Note 7)



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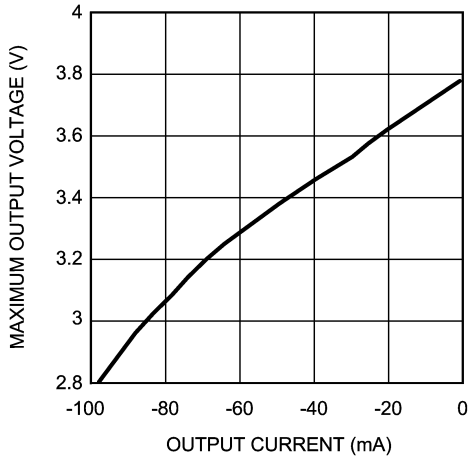
Maximum V_{OUT} vs. I_{OUT}(Note 7)



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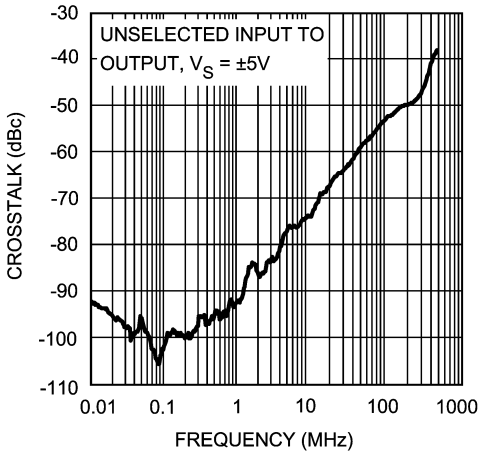
Typical Performance Characteristics V_s = ±5V, R_L = 100Ω, A_V = 2, R_F = R_G = 575Ω; unless otherwise specified. (Continued)

Crosstalk vs. Frequency



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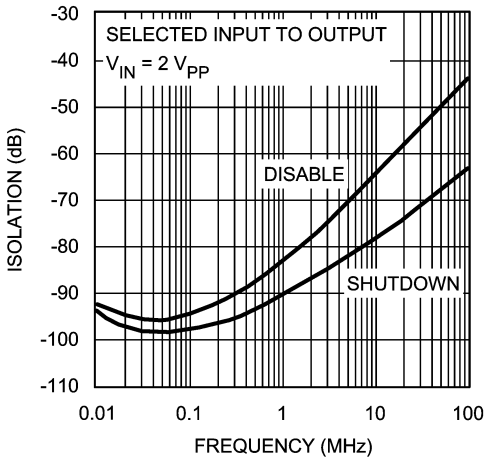
Off Isolation



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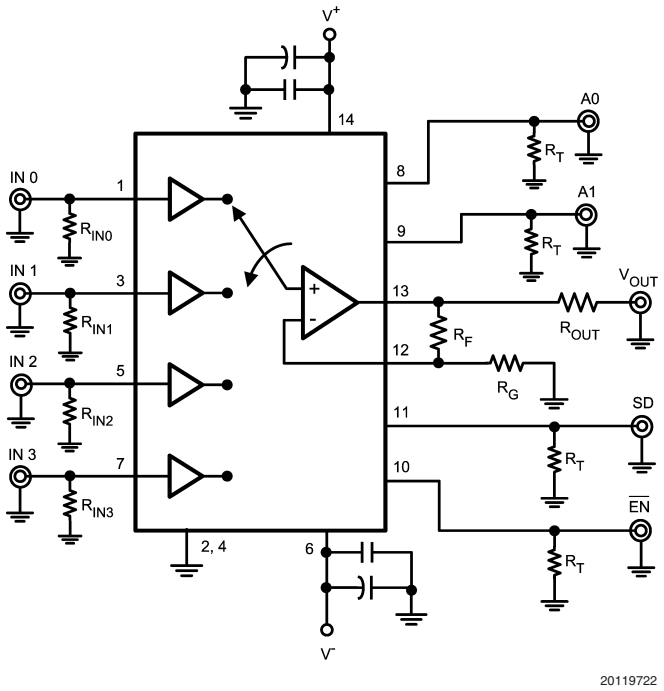


FIGURE 1. Typical Application

The LMH6574 is a high-speed 4:1 analog multiplexer, optimized for very high speed and low distortion. With selectable gain and excellent AC performance, the LMH6574 is ideally suited for switching high resolution, presentation grade video signals. The LMH6574 has no internal ground reference. Single or split supply configurations are both possible. The LMH6574 features very high speed channel switching and disable times. When disabled the LMH6574 output is high impedance making MUX expansion possible by combining multiple devices. See “Multiplexer Expansion” section below.

VIDEO PERFORMANCE

The LMH6574 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. *Figure 1* shows a typical configuration for driving a 75Ω. Cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

FEEDBACK RESISTOR SELECTION

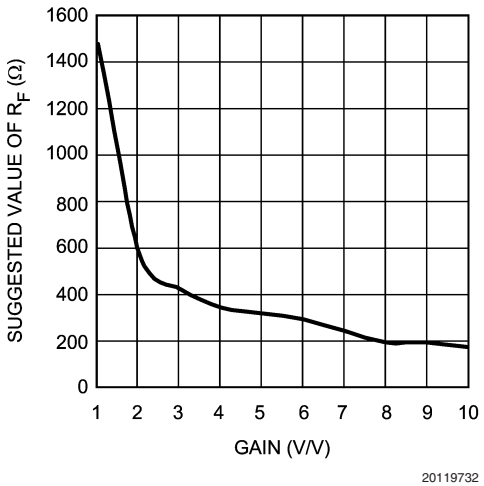


FIGURE 2. Suggested R_F vs. Gain

Application Notes (Continued)

The LMH6574 has a current feedback output buffer with gain determined by external feedback (R_F) and gain set (R_G) resistors. With current feedback amplifiers, the closed loop frequency response is a function of R_F. For a gain of 2 V/V, the recommended value of R_F is 575Ω. For other gains see the chart "Suggested R_F vs Gain". Generally, lowering R_F from the recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below the recommended value will cause overshoot, ringing and, eventually, oscillation.

Since all applications are slightly different it is worth some experimentation to find the optimal R_F for a given circuit. For more information see Application Note OA-13 which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The impedance looking into pin 12 is approximately 20Ω. This allows for good bandwidth at gains up to 10 V/V. When used with gains over 10 V/V, the LMH6574 will exhibit a "gain bandwidth product" similar to a typical voltage feedback amplifier. For gains of over 10 V/V consider selecting a high performance video amplifier like the LMH6720 to provide additional gain.

SD vs. $\overline{EN}$

The LMH6574 has both shutdown and disable capability. The shutdown feature affects the entire chip, whereas the disable function only affects the output buffer. When in shutdown mode, minimal power is consumed. The shutdown function is very fast, but causes a very brief spike of about 400 mV to appear on the output. When in shutdown mode the LMH6574 consumes only 1.8 mA of supply current. For maximum input to output isolation use the shutdown function.

The $\overline{EN}$ pin only disables the output buffer which results in a substantially reduced output glitch of only 50 mV. While disabled the chip consumes 4.7 mA, considerably more than when shutdown. This is because the input buffers are still active. For minimal output glitch use the $\overline{EN}$ pin. Also, care should be taken to ensure that, while in the disabled state, the voltage differential between the active input buffer (the one selected by pins A0 and A1) and the output pin stays less than 2V. As the voltage differential increases, input to output isolation decreases. Normally this is not an issue. See the section on MULTIPLEXER EXPANSION for further details.

To reduce the output glitch when using the SD pin, switch the $\overline{EN}$ pin at least 10 ns before switching the SD pin. This can be accomplished by using an RC delay circuit between the two pins if only one control signal is available.

Logic inputs "SD" and "$\overline{EN}$" will revert to the "High", while "A_0" and "A_1" will revert to the "Low" state when left floating.

MULITPLEXER EXPANSION

Figure 3 shows an 8:1 MUX using two LMH6574's.

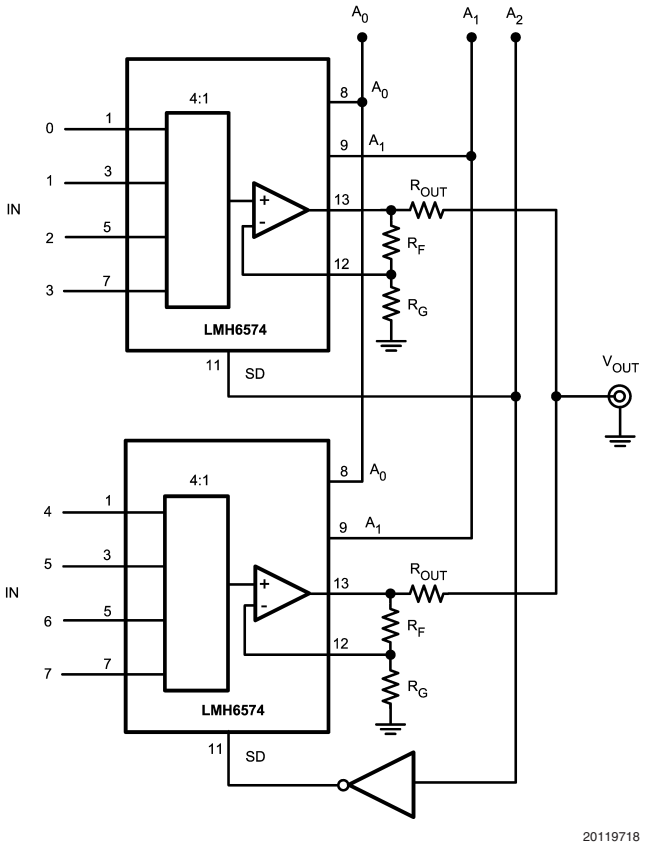


FIGURE 3. 8:1 MUX USING TWO LMH6574's

Application Notes (Continued)

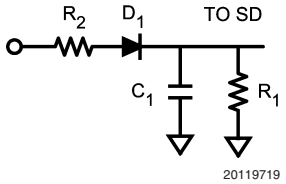


FIGURE 4. Delay Circuit Implementation

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added, to drive the SHUTDOWN pin of each device. *Figure 4* shows one possible approach to this delay circuit. The delay circuit shown will delay SHUTDOWN's H to L transitions (R_1 and C_1 decay) but won't delay its L to H transition. R_2 should be kept small compared to R_1 in order to not reduce the SHUTDOWN voltage and to produce little or no delay to SHUTDOWN.

With the SHUTDOWN pin putting the output stage into a high impedance state, several LMH6574's can be tied together to form a larger input MUX. However, there is a loading effect on the active output caused by the unselected devices. The circuit in *Figure 5* shows how to compensate for this effect. For the 16:1 MUX function shown in *Figure 5* below the gain error would be about –0.8 dB, or about 9%. In the circuit in *Figure 5*, resistor ratios have been adjusted to compensate for this gain error. By adjusting the gain of each multiplexer circuit the error can be reduced to the tolerance of the resistors used (1% in this example).

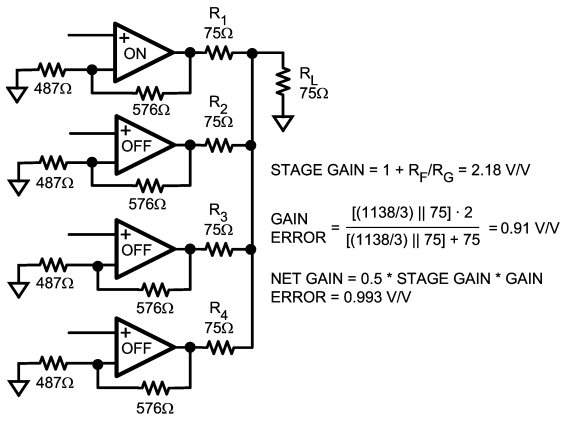


FIGURE 5. Multiplexer Gain Compensation

Disabling of the LMH6574 using the $\overline{EN}$ pin is not recommended for use when doing multiplexer expansion. While disabled, If the voltage between the selected input and the chip output exceeds approximately 2V the device will begin to enter a soft breakdown state. This will show up as reduced input to output isolation. The signal on the non-inverting input of the output driver amplifier will leak through to the inverting input, and then to the output through the feedback resistor. The worst case is a gain of 1 configuration where the non inverting input follows the active input buffer and (through the feedback resistor) the inverting input follows the voltage driving the output stage. The solution for this is to use shutdown mode for multiplexer expansion.

Other Applications

The LMH6574 could support a multi antenna receiver with up to four separate antennas. Monitoring the signal strength of all 4 antennas and connecting the strongest signal to the final IF stage would provide effective spacial diversity.

For direction finding, the LMH6574 could be used to provide high speed sampling of four separate antennas to a single DSP which would use the information to calculate the direction of the received signal.

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. *Figure 6* shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The chart "Suggested R_{OUT} vs. Cap Load" gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

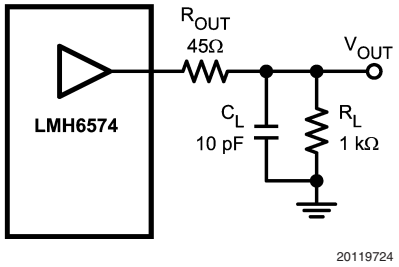


FIGURE 6. Decoupling Capacitive Loads

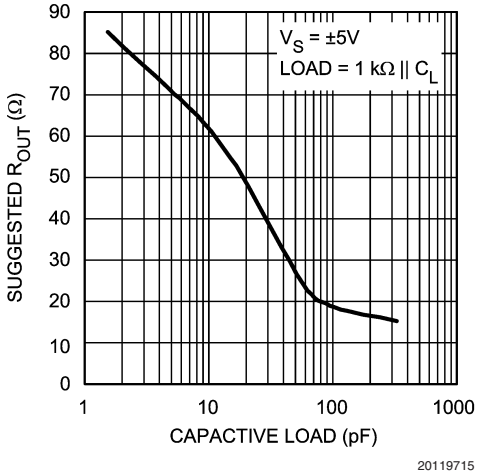


FIGURE 7. Suggested R_{OUT} vs. Capacitive Load

Other Applications (Continued)

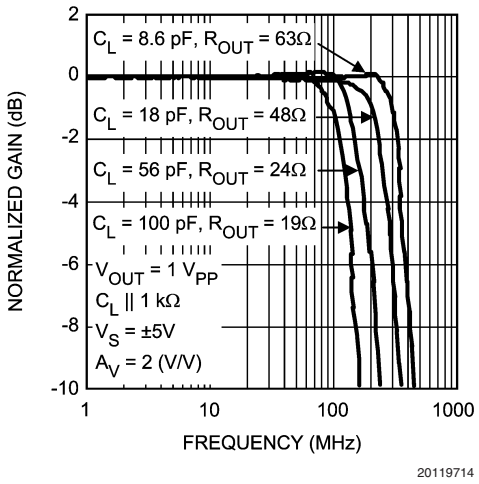


FIGURE 8. Frequency Response vs. Capacitive Load

LAYOUT CONSIDERATIONS

Whenever questions about layout arise, use the evaluation board as a guide. The LMH730276 is the evaluation board supplied with samples of the LMH6574. To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. In *Figure 1*, the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01 µF and 0.1 µF ceramic capacitors for each supply bypass.

POWER DISSIPATION

The LMH6574 is optimized for maximum speed and performance in the small form factor of the standard SOIC package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6574:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}^* (V_S)$, where $V_S = V^+ - V^-$.
2. Calculate the RMS power dissipated in the output stage: P_D (rms) = rms $((V_S - V_{OUT}) * I_{OUT})$, where V_{OUT} and I_{OUT} are the voltage across and the current through the external load and V_S is the total supply voltage.
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMH6574 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150^\circ - T_{AMB})/ \theta_{JA}$, where T_{AMB} = Ambient temperature (˚C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (˚C/W). For the SOIC package θ_{JA} is 130 ˚C/W.

ESD PROTECTION

The LMH6574 is protected against electrostatic discharge (ESD) on all pins. The LMH6574 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6574 is driven by a large signal while the device is powered down the ESD diodes will conduct . The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

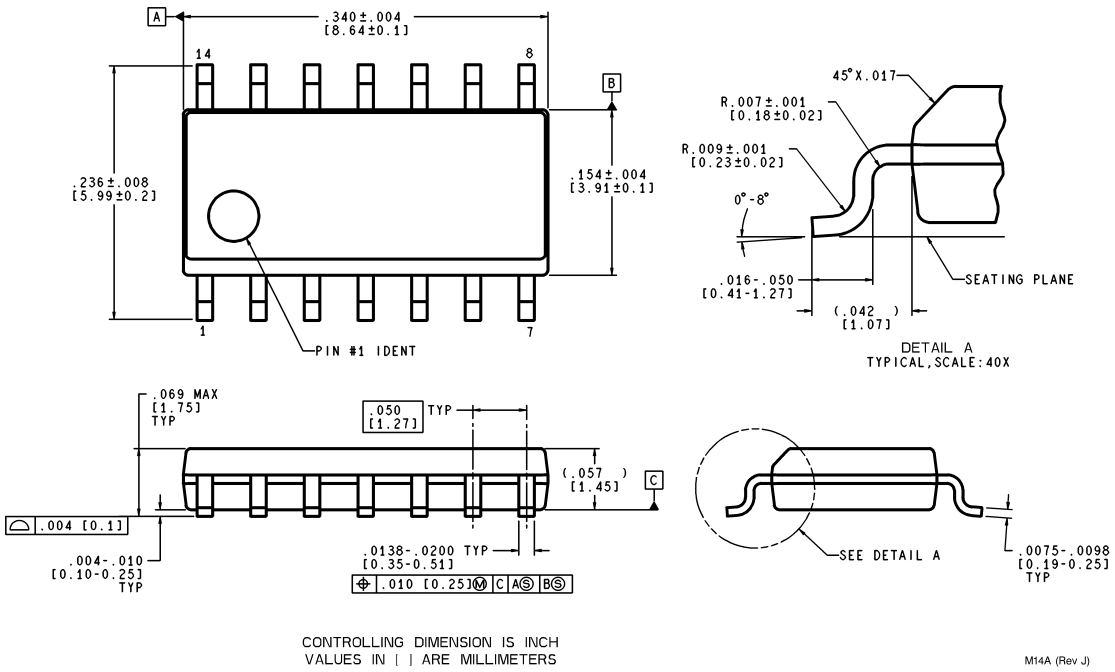
EVALUATION BOARDS

National Semiconductor provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the data sheet plots were measured with this board.

Device	Package	Evaluation Board
LMH6574	SOIC	LMH730276

An evaluation board can be shipped when a sample request is placed with National Semiconductor. Samples can be ordered on the National web page. (www.national.com)

Physical Dimensions inches (millimeters) unless otherwise noted



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