Wireless Power Transmitter Manager

Check for Samples: bq500110

FEATURES

- **Intelligent Control of the Power Transfer between Base Station and Mobile Device**
- **Conforms to Version 1.0 of the Wireless Power Consortium (WPC) Transmitter Specifications**
- **Demodulates and Decodes WPC Complaint Message Packets from the Power Receiving Device Over the Same Wireless Link that Transfers Electrical Power**
- **Implements closed-loop Power Transfer PID Control by modulating frequency of the Voltage on the Transmitting Coil**
- **Operating Modes Status Indicators**

APPLICATIONS

- **WPC Compliant Contactless Charging Stations**
- **Other Wireless Power Base Stations and Transmitters**

DESCRIPTION

The bq500110 integrates most of the logic function required to control Wireless Power Transfer and facilitate communication in the single channel WPC compliant contactless charging base station. The bq500110 is an intelligent device that periodically pings surrounding environment for available devices to be powered while minimizing the idle power; monitors all communication from the mobile device being wirelessly powered; adjusts power applied to the transmitter coil per information received from the powered device. The bq500110 also manages fault conditions associated with power transfer and controls status signal (LEDs) to indicate operating modes.

The bq500110 comes in the area saving 48-pin, 7mm x 7mm QFN package and operates over temperature range from -40°C to 110°C.

ORDERING INFORMATION(1)

OPERATING TEMPERATURE RANGE, T_A	ORDERABLE PART NUMBER	PIN COUNT	SUPPLY	PACKAGE	TOP SIDE MARKING
-40°C to 110°C	BQ500110RGZR	48 pin	Reel of 2500	QFN	bq500110
	BQ500110RGZT	48 pin	Reel of 250	QFN	bq500110

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	VALUE		UNIT
	MIN	MAX	
Voltage applied at V33D to DGND	–0.3	3.8	V
Voltage applied at V33A to AGND	–0.3	3.8	V
Voltage applied to any pin (2)	–0.3	3.8	V
Storage temperature, T_{STG}	–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to GND.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V	Supply voltage during operation, V33D, V33A	3.0	3.3	3.6	V
T_A	Operating free-air temperature range (1)	–40		125	°C
T_J	Junction temperature (1)			125	°C

(1) When operating continuously, the bq500110's typical power consumption causes a 15°C temperature rise from ambient.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SUPPLY CURRENT						
I_{V33A}	Supply current	V33A = 3.3 V		8	15	mA
I_{V33D}		V33D = 3.3 V		42	55	
I_{V33D}		V33D = 3.3 V while storing configuration parameters in flash memory		53	65	
INTERNAL REGULATOR CONTROLLER INPUTS/OUTPUTS						
V33	3.3-V linear regulator	Emitter of NPN transistor	3.25	3.3	3.6	V
V33FB	3.3-V linear regulator feedback			4	4.6	
I_{V33FB}	Series pass base drive	V_{IN} = 12 V; current into V33FB pin		10		mA
Beta	Series NPN pass device		40			
EXTERNALLY SUPPLIED 3.3 V POWER						
V33D	Digital 3.3-V power	T_A = 25°C	3		3.6	V
V33A	Analog 3.3-V power	T_A = 25°C	3		3.6	V
V33Slew	V33 slew rate	V33 slew rate between 2.3V and 2.9V, V33A = V33D	0.25			V/ms
ANALOG INPUTS V_IN, I_IN, TEMP_IN, I_COIL, LED_MODE, PMOD_THR						
V_OPEN	Voltage indicating open on a current bias enabled pin	LED_MODE, PMOD_THR open	2.37			V
V_SHORT	Voltage indicating a short on a current bias enabled pin	LED_MODE, PMOD_THR short to ground			0.36	V
V_{ADC_RANGE}	Measurement range for voltage monitoring	Inputs: ADC-VIN, ADC-IIN, ADC-IOUTA, ADC-IOUTB	0		2.5	V
INL	ADC integral nonlinearity		-2.5		2.5	mV
I_{lkg}	Input leakage current	3V applied to pin			100	nA
R_{IN}	Input impedance	Ground reference	8			MΩ

ELECTRICAL CHARACTERISTICS (continued)

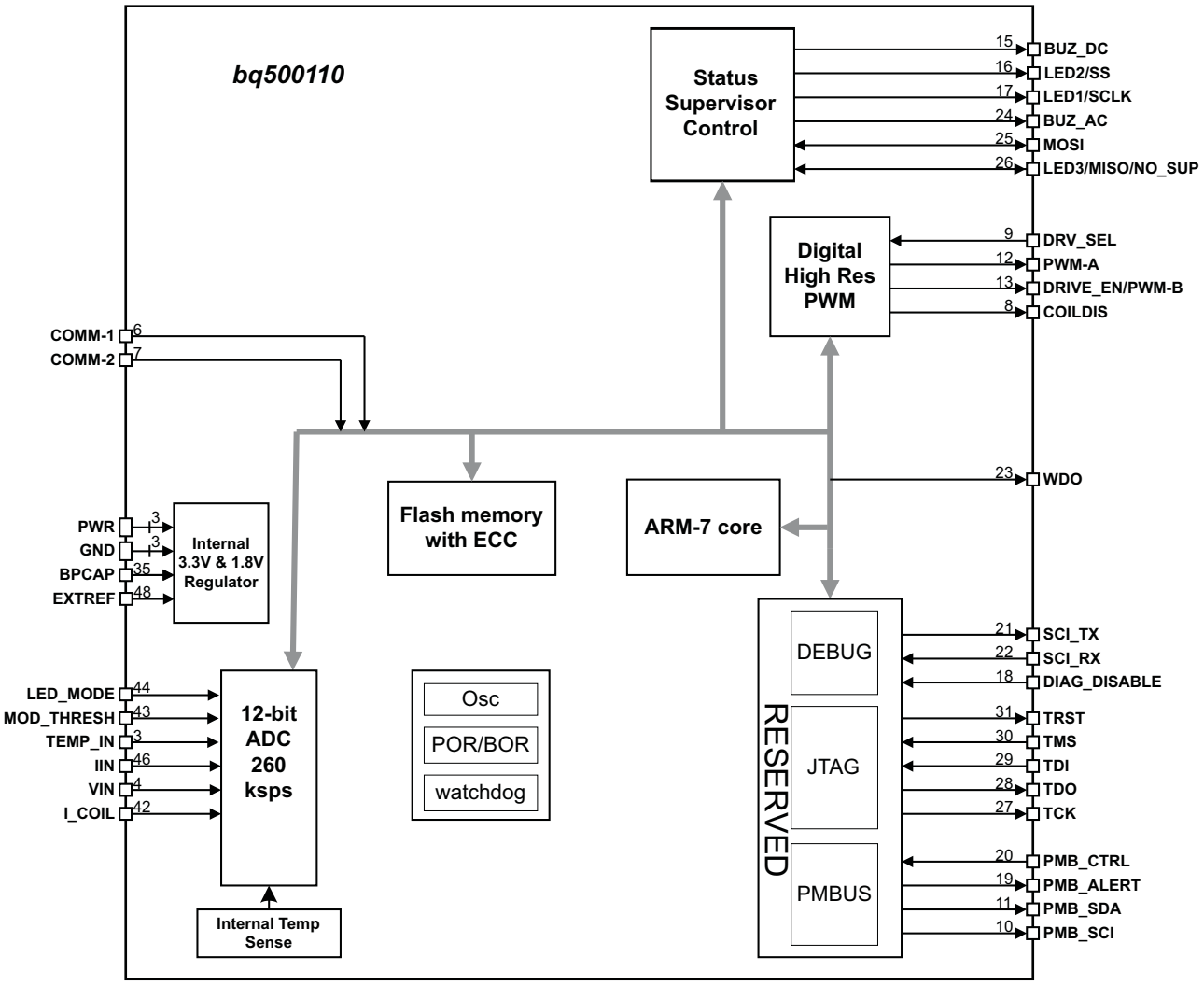
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Input capacitance				10	pF
DIGITAL INPUTS/OUTPUTS						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA (1), V33D = 3 V			DGND1 +0.25	V
V_{OH}	High-level output voltage	I_{OH} = -6 mA (2), V33D = 3 V	V33D -0.6V			V
V_{IH}	High-level input voltage	V33D = 3V	2.1		3.6	V
V_{IL}	Low-level input voltage	V33D = 3.5 V			1.4	V
I_{OH}(MAX)	Output high source current				4	mA
I_{OL}(MAX)	Output low sink current				4	mA
SYSTEM PERFORMANCE						
V_{RESET}	Voltage where device comes out of reset	V33D Pin	2.3		2.4	V
t_{RESET}	Pulse width needed for reset	$\overline{RESET}$ pin	2			µs
F_{SW}	Switching Frequency		110		205	kHz
t_{detect}	Time to detect presence of device requesting power				0.6	sec
$t_{retention}$	Retention of configuration parameters	T_J = 25°C	100			Years
Write_Cycles	Number of nonvolatile erase/write cycles	T_J = 25°C	20			K cycles

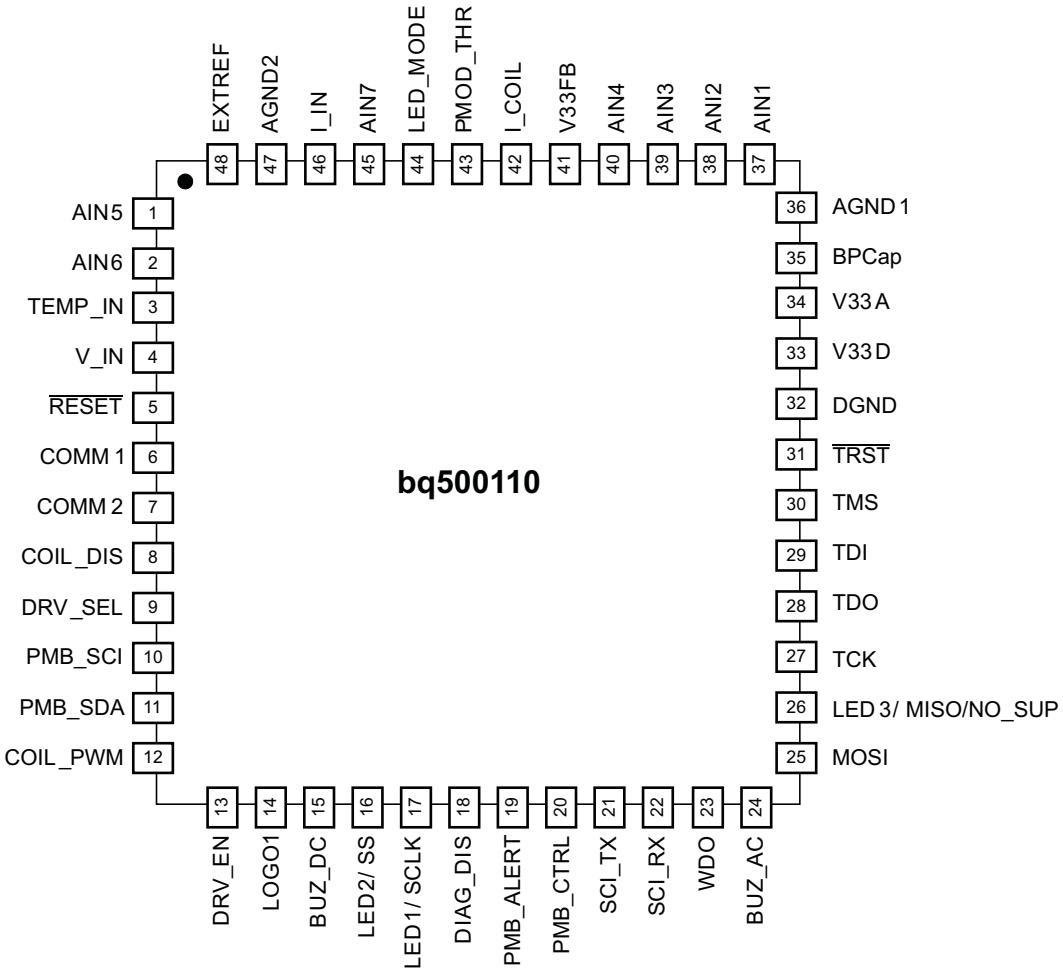
(1) The maximum I_{OL}, for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified.
(2) The maximum I_{OH}, for all outputs combined, should not exceed 48 mA to hold the maximum voltage drop specified.
(3) With default device calibration. PMBus calibration can be used to improve the regulation tolerance.
(4) Time from close of error ADC sample window to time when digitally calculated control effort (duty cycle) is available. This delay must be accounted for when calculating the system dynamic response. Includes EADC conversion time.

DEVICE INFORMATION

Functional Block Diagram



48-PIN QFN PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
1	AIN5	I	Connect this pin to GND
2	AIN6	I	Connect this pin to GND
3	TEMP_IN	I	Thermal protection Input
4	V_IN	I	Input-voltage ADC Input
5	$\overline{\text{RESET}}$	I	Device reset
6	COMM1	I	Primary communication channel
7	COMM2	I	Alternate communication channel
8	COIL_DIS	I	Coil disable
9	DRV_SEL	I	Gate Driver mode select
10	PMB_SCI	I/O	Optional programming I/O. Pull up to V_{CC} via 5.1kΩ resistor.
11	PMB_SDA	I/O	Optional programming I/O. Pull up to V_{CC} via 5.1kΩ resistor.
12	COIL_PWM	O	PWM Output
13	DRV_EN	O	PWM Enable Output
14	LOGO1	O	Optional Logic Output. Leave this pin floating.
15	BUZ_DC	O	DC Buzzer Output
16	LED2 / SS	O	LED Drive Output 2 / Slave Select output

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
17	LED1 / SCLK	O	LED Drive Output 1 / Serial Clock Output
18	DIAG_DIS	I/O	Disable Diagnostic Output. Leave this pin floating to inhibit diagnostic.
19	PMB_ALERT	I/O	Optional Programming I/O. Connect to GND.
20	PMB_CTRL	I/O	Optional programming I/O. Pull up to V_{CC} via 5.1kΩ resistor.
21	SCI-TX	I/O	Optional Programming I/O. Leave floating.
22	SCI-RX	I/O	Optional Programming I/O. Leave floating.
23	WDO	O	External Watchdog Output
24	BUZ_AC	O	AC Buzzer Output
25	MOSI	I/O	Master Out Slave In
26	LED3/MISO/NO_SUP	I/O	LED Drive Output 3 / Master In Slave Out / Select stand alone operation (no supervisor)
27	TCK	I/O	Optional Programming I/O. Leave floating.
28	TDO	I/O	Optional Programming I/O. Leave floating.
29	TDI	I/O	Optional programming I/O. Pull up to V_{CC} via 5.1kΩ resistor.
30	TMS	I/O	Optional programming I/O. Pull up to V_{CC} via 5.1kΩ resistor.
31	$\overline{\text{TRST}}$	I/O	Optional programming I/O. Pull to GND via 10kΩ resistor.
32	DGND	—	Digital GND
33	V33D	—	Digital Core 3.3V Supply
34	V33A	—	Analog 3.3V Supply
35	BPCAP	—	1.8V Bypass Capacitor Connect Pin
36	AGND	—	Analog GND
37	AN1	I	Reserved Analog Input. Connect this pin to GND.
38	AN2	I	Reserved Analog Input. Connect this pin to GND.
39	AN3	I	Reserved Analog Input. Connect this pin to GND.
40	AN4	I	Reserved Analog Input. Connect this pin to GND.
41	V33FB	I	3.3V Linear-Regulator Feedback Input. Leave this pin floating.
42	I_COIL	I	Coil Current Input
43	PMOD_THR	I	Input to Program Metal Object Detection Threshold
44	LED_MODE	I	Input to Select LED Mode
45	AIN7	I	Reserved Analog Input. Connect this pin to GND.
46	I_IN	I	Transmitter Input Current
47	AGN2	—	Analog GND 2.
48	EXTREF	I	External Reference Voltage Input. Connect this Input to GND.

FUNCTIONAL OVERVIEW

Option Select Pins

At power–up, a bias current is applied to pins LED_MODE and PMOD_THR and the resulting voltage measured in order to identify the value of the attached programming resistor. The values of the operating parameters set by these pins are determined using Option Select Bins. For LED_MODE the selected bin determines the LED behavior based on LED Modes; for the PMOD_THR the selected bin sets a threshold used for parasitic metal object detection (see Metal Object Detection (MOD) section).

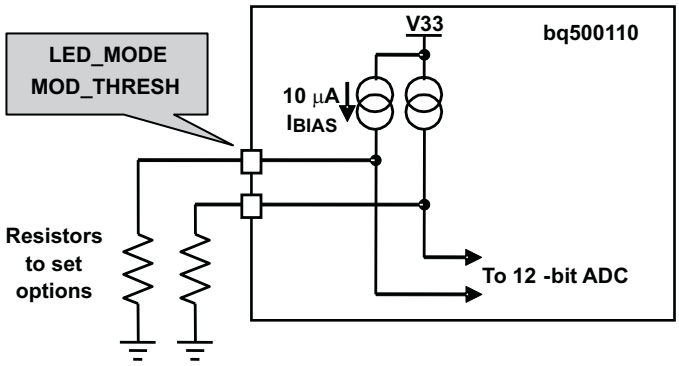


Figure 1. Option Programming

Table 1. Option Select Bins

BIN NUMBER	RESISTANCE (kΩ)	LED OPTION	PMD THRESHOLD (mW)
0	GND	0	400
1	42.2	1	500
2	48.7	2	600
3	56.2	3	700
4	64.9	4	800
5	75	5	900
6	86.6	6	1000
7	100	7	1100
8	115	8	1200
9	133	9	1300
10	154	10	1400
11	178	11	1500
12	205	12	1600
13	open	13	OFF

LED Modes

The bq500110 can directly control up to three LED outputs. They are driven based on one of twelve selectable modes. Using the resistor of the 44 pin to GND select one of the desired LED Indication scheme presented in Table 2.

Table 2. LED Modes

LED Control Option	I/O	Supervisory Register	Recommended LED Colors	Operational States										Fault Blink Period (ON time + OFF time) (ms)	PLD Blink Period (ON time + OFF time) (ms
				Initialization	Uses Operating Blink Rate			PLD Blink	Uses Fault Blink Rate			Diag LED On	Diag LED Off		
					Standby	Power Xfer	Charged	PLD Fault	Dev Fault	Sys Fault	NVM Fault				
0	26	LED1	Red	ON	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	200	200
	16	LED2	Green	ON	ON	Blink	ON	OFF	OFF	OFF	OFF	ON	OFF		
	17	LED3	Red (Pilot)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
	n/a	n/a	Pilot (Blue)	x	x	x	x	x	x	x	x	x	x		
1	17	LED1	x	x	x	x	x	x	x	x	x	x	x	x	x
	16	LED2	x	x	x	x	x	x	x	x	x	x	x		
	26	LED3	x	x	x	x	x	x	x	x	x	x	x		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
2	17	LED1	Green	OFF	OFF	ON	Blink	Blink	Blink	Blink	Blink	ON	OFF	200	200
	16	LED2	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
3	17	LED1	Red	OFF	OFF	ON	OFF	ON	ON	ON	Blink	ON	OFF	200	200
	16	LED2	Green	OFF	OFF	ON	ON	OFF	OFF	OFF	Blink	ON	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
4	17	LED1	Red	ON	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	200	200
	16	LED2	Green	ON	ON	Blink	ON	OFF	OFF	OFF	OFF	ON	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		

Table 2. LED Modes (continued)

5	17	LED1	Red	OFF	OFF	Blink	OFF	Blink	Blink	Blink	Blink	ON	OFF	200	200
	16	LED2	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
6	17	LED1	Red	OFF	OFF	OFF	OFF	Blink	Blink	Blink	Blink	ON	OFF	200	200
	16	LED2	Green	OFF	OFF	Blink	ON	OFF	OFF	OFF	OFF	ON	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
7	17	LED1	Red	OFF	OFF	ON	OFF	Blink(1)	Blink	Blink	Blink	ON	OFF	400	2000
	16	LED2	Green	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
8	17	LED1	Red	OFF	OFF	OFF	OFF	Blink(1)	Blink	Blink	Blink	ON	OFF	400	2000
	16	LED2	Green	OFF	OFF	Blink	ON	OFF	OFF	OFF	OFF	ON	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
9	17	LED1	Red	ON	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	200	200
	16	LED2	Green	ON	ON	Blink	ON	OFF	OFF	OFF	OFF	ON	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
10	17	LED1	Red	ON	OFF	Blink	OFF	Blink	Blink	Blink	Blink	ON	OFF	200	200
	16	LED2	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
11	17	LED1	Red	ON	OFF	OFF	OFF	Blink	Blink	Blink	Blink	ON	OFF	200	200
	16	LED2	Green	OFF	OFF	Blink	ON	OFF	OFF	OFF	OFF	ON	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
12	17	LED1	Red	OFF	OFF	ON	OFF	Blink(1)	Blink	Blink	Blink	ON	OFF	400	2000
	16	LED2	Green	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		
13	17	LED1	Red	OFF	OFF	OFF	OFF	Blink(1)	Blink	Blink	Blink	ON	OFF	400	2000
	16	LED2	Green	ON	OFF	Blink	ON	OFF	OFF	OFF	OFF	ON	OFF		
	26	LED3	not used	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	n/a	n/a	Pilot (Blue)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON		

Thermal Protection

The bq500110 can provide thermal protection to the transmitter. The external NTC resistor can be placed in the most thermally challenged area, which usually is the center of the transmitting coil, and connected between V_{CC} and the dedicated pin 3. The threshold on the pin 3 is set 1.25V. The NTC resistor and the resistor from the pin 3 to GND create temperature sensitive divider. User has full flexibility choosing the NTC resistor and the value of the resistor from the pin 3 to GND to set the desired temperature when system shuts down.

$$R_{TEMP\_IN} = 0.6097 \times R_{NTC}(T_{MAX}) \quad (1)$$

The system will attempt to restore normal operation after approximately five minutes being in the suspended mode due to tripping the over-temperature threshold.

Audible Notification on Initiation of Power Transfer

The bq500110 is capable of activating two types of buzzers to indicate power transfer begin. The pin 15 outputs the high logic signal for 0.5s which is suitable to activate DC type buzzers with built in tone generation, other types of sound generators, or custom indication systems. The pin 24 outputs 0.2s, 4000Hz square wave signal suitable for inexpensive AC type ceramic buzzers.

Gate Driver Modes

The inner PID (proportional-integral-derivative) loop feeds the variable frequency driver, which produces a digital signal of 50% duty cycle with variable frequency. In operation, the inner PID loop calculates the necessary frequency, which is then generated by the variable frequency driver. The variable frequency is then fed into a MOSFET power train that excites the serial resonance transmitter coil.

The bq500110 can operate with several types of MOSFET gate drivers to accommodate various power train topologies. The DRV_SEL input, pin 9, selects between two modes of drive. When pin 9 is pulled to GND, the DRV_EN output, pin 13, will be driven high while the COIL_PWM output sends a square waveform to the gate driver. The most typical and suggested solution is to use a synchronous buck driver like the TPS28225 that drives n-channel upper and lower power MOSFETs with a safe dead-time.

An alternative solution that may utilize a combination of p-channel and n-channel MOSFETs can be used when input DRV_SEL input, pin 9, is pulled high to V_{CC}. In this case the outputs COIL_PWM and DRV_EN, both output the square waveforms to discrete gate drivers. The dead-time is provided by pulse duration difference between the two waveforms.

Coil Disable Signal

As the part of the WPC 1.0 compliance communication protocol, the bq500110 has the coil damping control signal that is provided on the output COIL_DIS, pin 8. The damping signal activates the MOSFET that loads the output of the half-bridge with the 100Ω resistor.

Power-On Reset

The bq500110 has an integrated power-on reset (POR) circuit that monitors the supply voltage. At power-up, the POR circuit detects the V33D rise. When V33D is greater than VRESET, the device initiates an internal startup sequence. At the end of the startup sequence, the device begins normal operation.

External Reset

The device can be forced into the reset state by an external circuit connected to the $\overline{\text{RESET}}$ pin. A logic low voltage on this pin holds the device in reset. To avoid an erroneous trigger caused by noise, a 10kΩ pull up resistor to 3.3V is recommended.

Non-Volatile Memory Error Correction Coding

The device uses Error Correcting Code (ECC) to improve data integrity and provide high reliability storage of Data Flash contents. ECC uses dedicated hardware to generate extra check bits for the user data as it is written into the Flash memory. This adds an additional six bits to each 32-bit memory word stored into the Flash array. These extra check bits, along with the hardware ECC algorithm, allow for any single bit error to be detected and corrected when the Data Flash is read. Note that the Data Flash configuration has been factory programmed and is not generally available for customization.

Metal Object Detection (MOD)

As a safety feature, the bq500110 can be configured to detect parasitic metal placed in the vicinity of the magnetic field. The bq500100 uses the power packet information (as received from the powered device) and measured transmitter input power to calculate parasitic losses in the system. When excessive power loss is detected, the device will light the red LED and provide a twenty second warning, and then will disable its PWM output. If the metal object is removed during this twenty second warning time, the normal operation will be restored. After shutdown, the bq500110 will attempt to restart normally after approximately five minutes. If the object that caused excessive power dissipation is still present in close proximity to the field, the sequence will be repeated again and again.

To facilitate parasitic loss function, the bq500110 monitors input voltage and current supplied to the coil drive circuit.

The MOD_THR pin is used to set the threshold at which the MOD is activated. The MOD operation can be disabled by selecting the highest bin(leaving the pin is left floating).

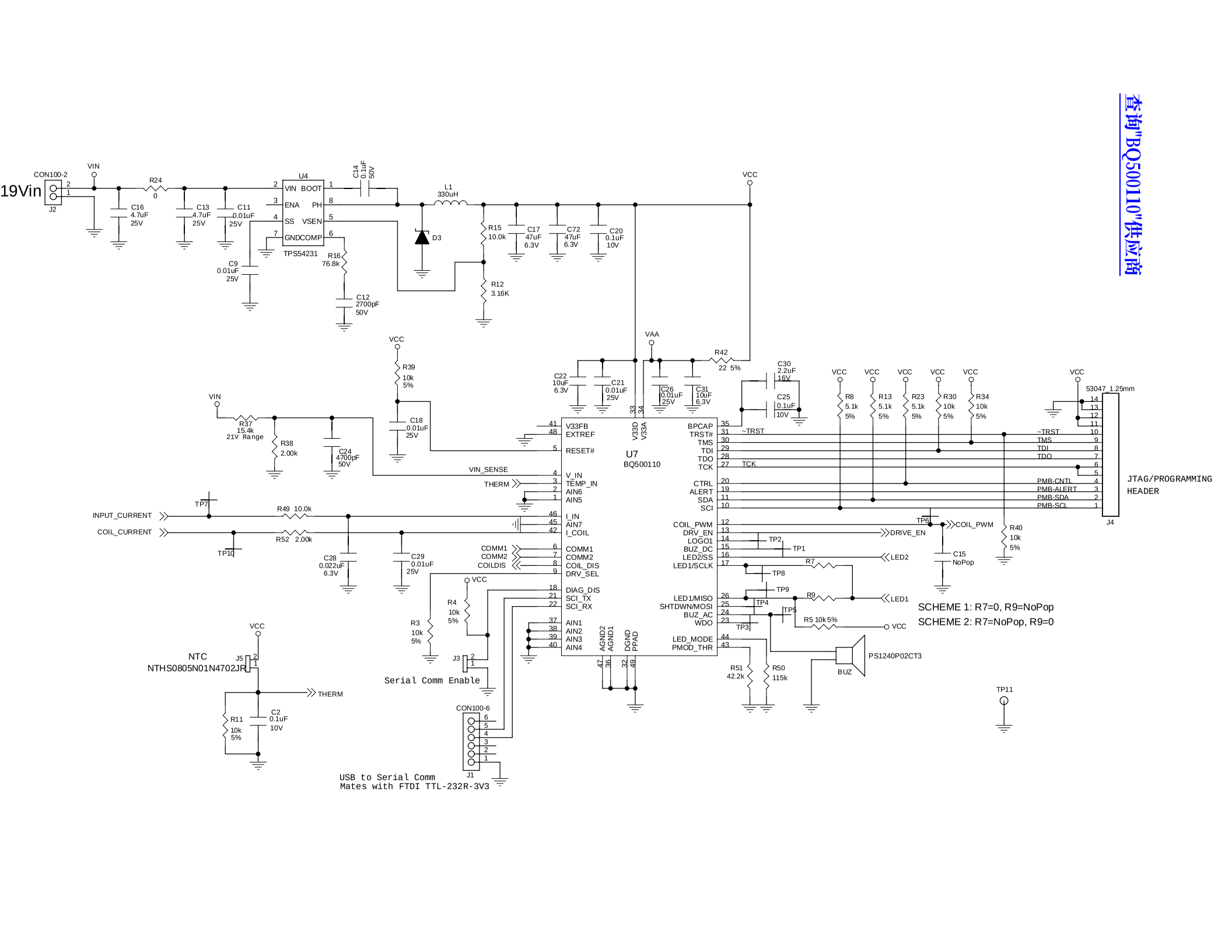
The threshold is set by Equation 2:

$$\text{Threshold} = 400\ \text{mW} + \text{Bin\_Number} \times 100\ \text{mW} \quad (2)$$

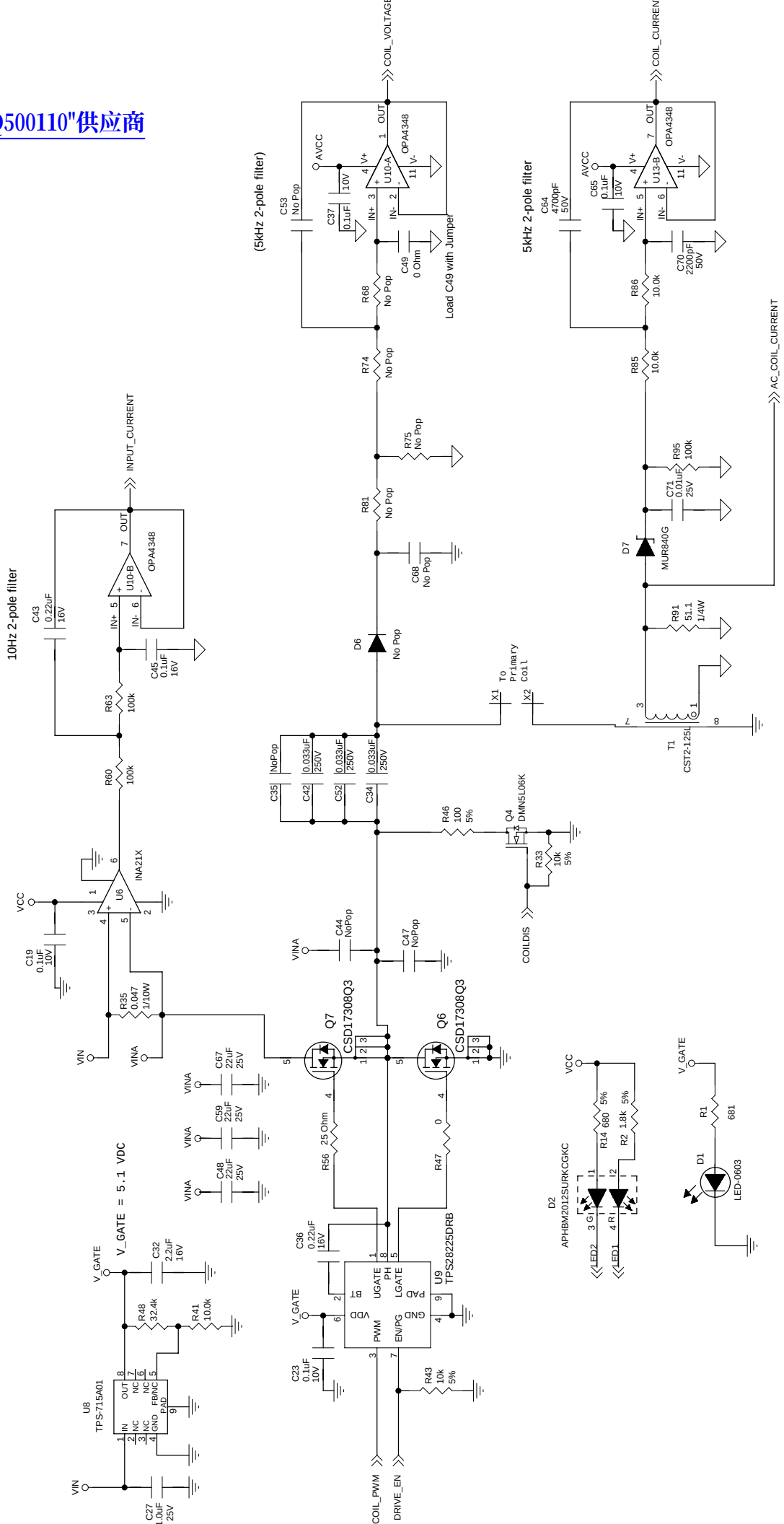
Note: The WPC Specification V1.0 does not define the requirements and thresholds for MOD feature, thus metal object detection may perform differently with different products. Therefore make your own decision when setting the threshold.

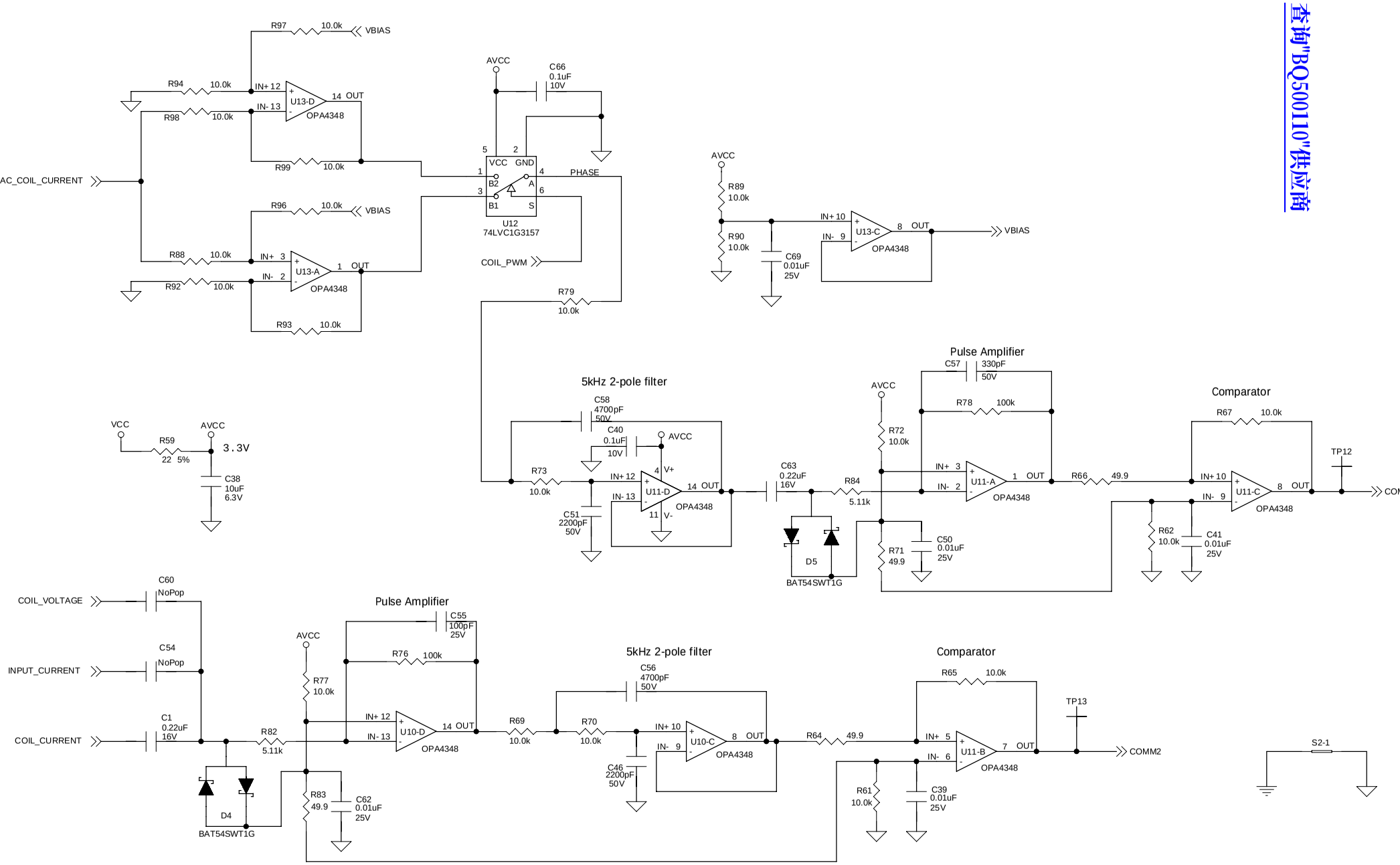
APPLICATION INFORMATION

Typical application diagrams for the WPC 1.0 compliant transmitter are shown on the following pages.


查询"BQ500110"供应商
19Vin
CON100-2
J2
VIN
R24
0
C16
4.7uF
25V
C13
4.7uF
25V
C11
0.01uF
25V
C9
0.01uF
25V
U4
VIN
BOOT
ENA
PH
SS
VSEN
GNDCOMP
TPS54231
C14
0.1uF
50V
L1
330uH
D3
R16
76.8k
C12
2700pF
50V
R15
10.0k
R12
3.16K
C17
47uF
6.3V
C72
47uF
6.3V
C20
0.1uF
10V
VCC
VAA
R42
22 5%
C22
10uF
6.3V
C21
0.01uF
25V
C26
0.01uF
25V
C31
10uF
6.3V
C30
2.2uF
16V
C25
0.1uF
10V
R39
10k
5%
C18
0.01uF
25V
R37
15.4k
21V Range
R38
2.00k
C24
4700pF
50V
VIN_SENSE
THERM
U7
BQ500110
V33FB
EXTREF
RESET#
V_IN
TEMP_IN
AIN6
AIN5
I_IN
AIN7
I_COIL
COMM1
COMM2
COIL_DIS
DRV_SEL
DIAG_DIS
SCI_TX
SCI_RX
AIN1
AIN2
AIN3
AIN4
AGND2
AGND1
DGND
PPAD
V33D
V33A
BPCAP
TRST#
TMS
TDI
TDO
TCK
CTRL
ALERT
SDA
SCI
COIL_PWM
DRV_EN
LOGO1
BUZ_DC
LED2/SS
LED1/SCLK
LED1/MISO
SHTDWN/MOSI
BUZ_AC
WDO
LED_MODE
PMOD_THR
~TRST
TCK
DRIVE_EN
LED2
LED1
VCC
R8
R13
R23
R30
R34
5.1k
5%
10k
5%
53047-1.25mm
J4
JTAG/PROGRAMMING
HEADER
PMB-CNTL
PMB-ALERT
PMB-SDA
PMB-SCL
TP6
TP2
TP1
TP8
TP9
TP4
TP5
TP3
R7
R9
R5 10k 5%
C15
NoPop
R40
10k
5%
SCHEME 1: R7=0, R9=NoPop
SCHEME 2: R7=NoPop, R9=0
INPUT_CURRENT
COIL_CURRENT
TP7
TP10
R49 10.0k
R52 2.00k
C28
0.022uF
6.3V
C29
0.01uF
25V
R4
10k
5%
R3
10k
5%
J3
Serial Comm Enable
CON100-6
J1
USB to Serial Comm
Mates with FTDI TTL-232R-3V3
NTC
NTHS0805N01N4702JR
J5
R11
10k
5%
C2
0.1uF
10V
R51
42.2k
R50
115k
PS1240P02CT3
BUZ
TP11

查询"BQ500110"供应商





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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
BQ500110RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260
BQ500110RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260

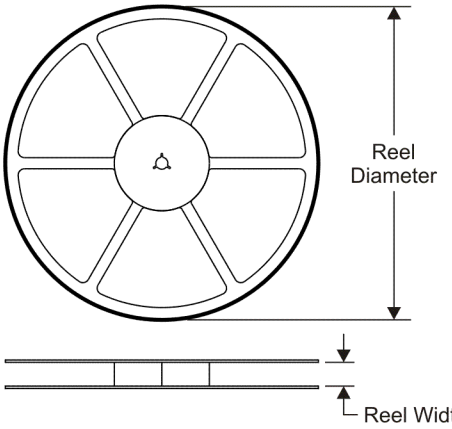
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

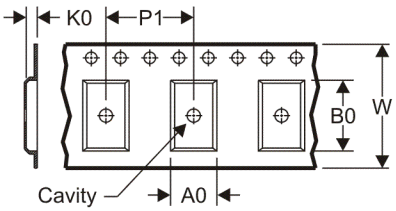
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

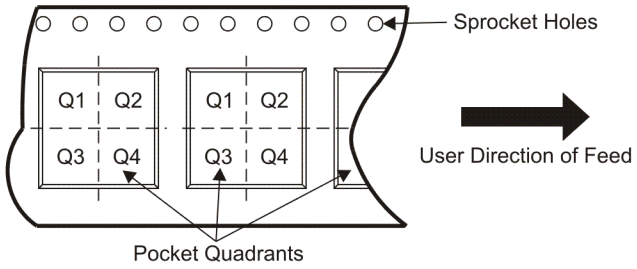


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

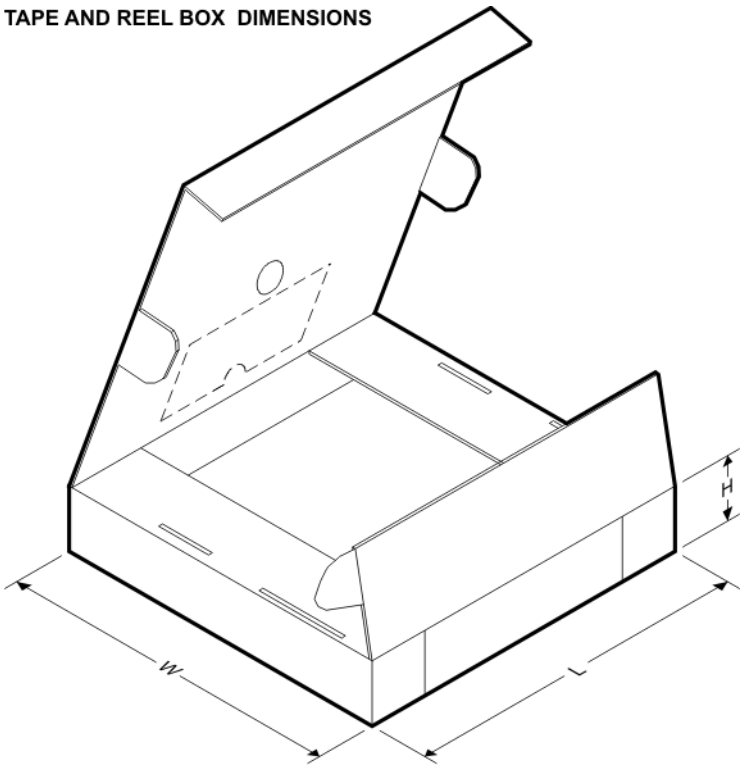
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ500110RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
BQ500110RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

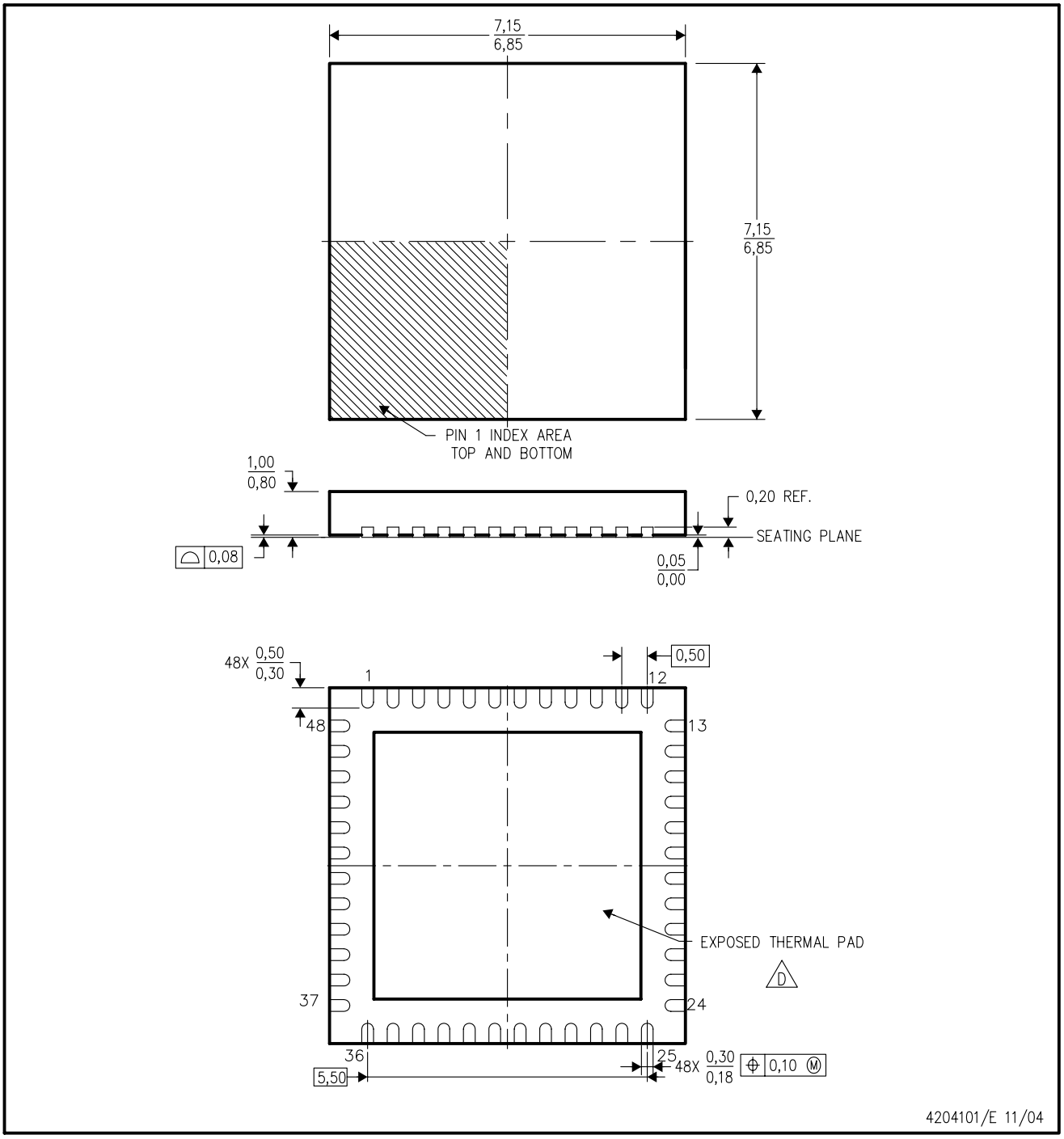
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ500110RGZR	VQFN	RGZ	48	2500	346.0	346.0	33.0
BQ500110RGZT	VQFN	RGZ	48	250	190.5	212.7	31.8

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

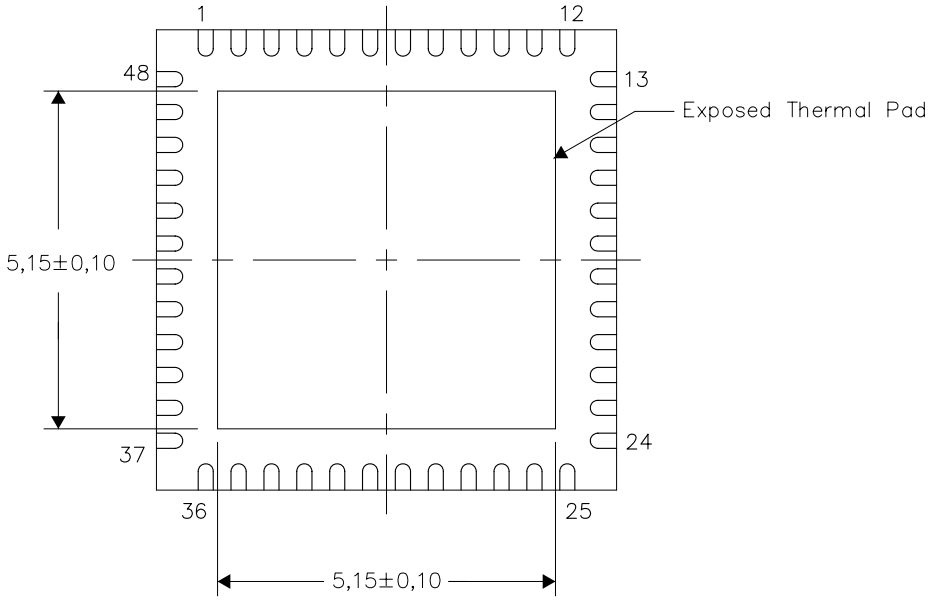
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

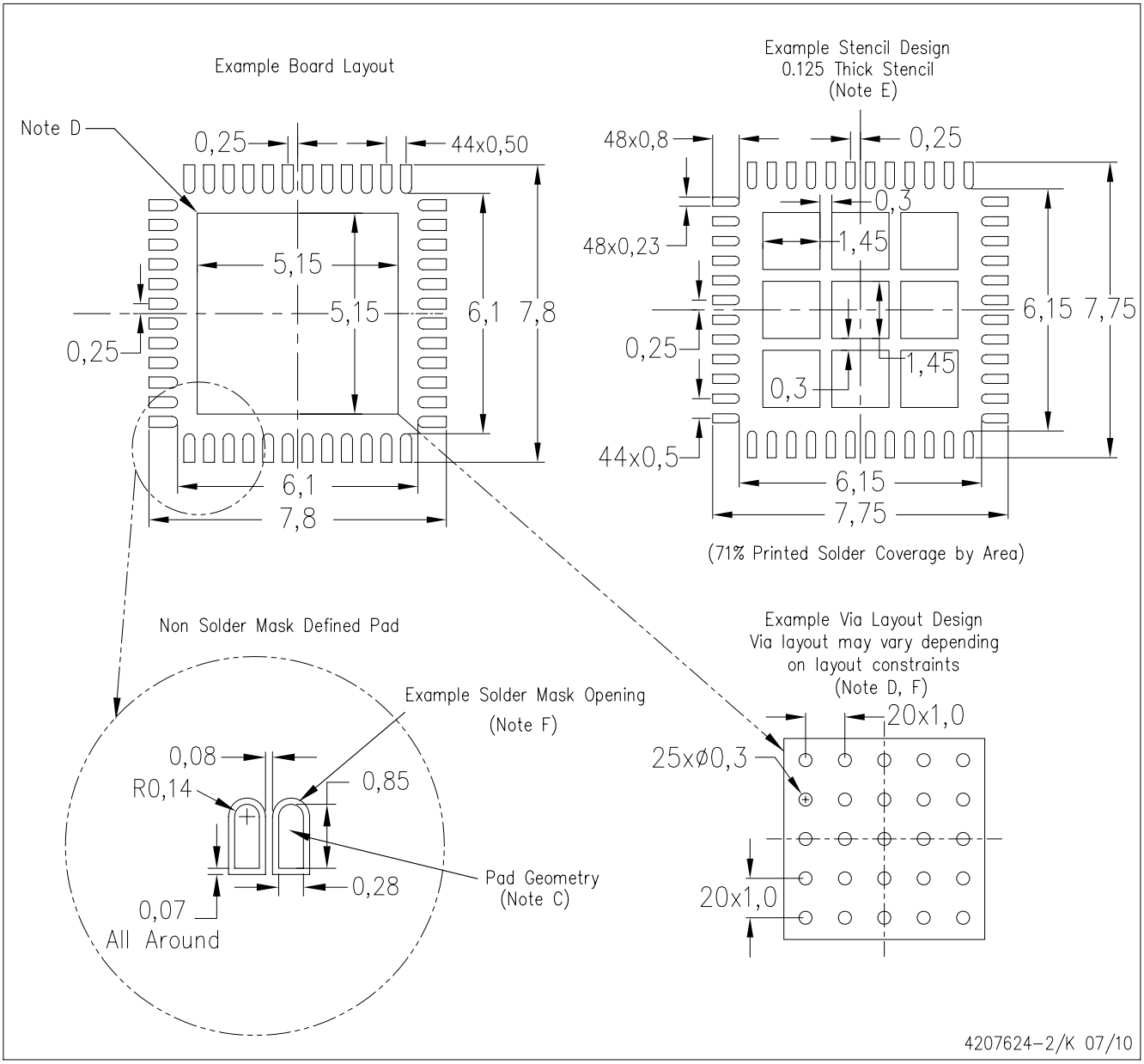


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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