Power MOSFET

30 V, 7.0 A, Single N-Channel, TSOP-6

Features

- Low R_{DS(on)}
- Low Gate Charge
- Pb-Free Package is Available

Applications

- Load Switch
- Notebook PC
- Desktop PC

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Ratin	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DSS}	30	V		
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain	Steady $T_A = 25^{\circ}C$		I _D	5.0	Α
Current (Note 1)	State	T _A = 85°C		3.6	
	t ≤ 10 s	T _A = 25°C		7.0	
Power Dissipation (Note 1)			P _D	1.0	W
				2.0	
Continuous Drain	Steady	T _A = 25°C	I _D	3.5	Α
Current (Note 2)	State	T _A = 85°C		2.5	
Power Dissipation (Note 2)	T _A = 25°C		P _D	0.5	W
Pulsed Drain Current	I _{DM}	21	Α		
Operating Junction and S	T _J , T _{STG}	–55 to 150	°C		
Source Current (Body Dio	IS	2.0	Α		
Single Pulse Drain-to-Sour ($V_{DD} = 30 \text{ V}, I_L = 10.4 \text{ A}, I_L = 1.0 \text{ mH}, R_G = 25 \Omega$)	EAS	54	mJ		
Lead Temperature for Sol (1/8" from case for 10 s)	TL	260	°C		

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	125	°C/W
Junction-to-Ambient - t ≤ 10 s (Note 1)	$R_{\theta JA}$	62.5	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	248	

- 1. Surface-mounted on FR4 board using 1 inch sq pad size
 (Cu area = 1 127 in sq [1 oz] including traces)
- (Cu area = 1.127 in sq [1 oz] including traces).
 2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0773 in sq).

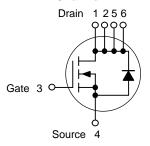


ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX	
30 V	21.5 mΩ @ 10 V	7.0 A	
00 1	30 mΩ @ 4.5 V	7.070	

N-Channel





TSOP-6 CASE 318G STYLE 1



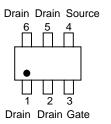
MARKING

S4 = Device Code M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping [†]		
NTGS4141NT1	TSOP-6	3000/Tape & Reel		
NTGS4141NT1G	TSOP-6 (Pb-Free)	3000/Tape & Reel		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL 4CHARAOTER STIES (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS			•				
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				18.4		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	$T_J = 25^{\circ}C$			1.0	μΑ
			T _J = 125°C			10	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, \text{ V}_{0}$	_{GS} = ±20 V			±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{I}$	_O = 250 μA	1.0		3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V,	I _D = 7.0 A		21.5	25	mΩ
		V _{GS} = 4.5 V,	I _D = 6.0 A		30	35	
Forward Transconductance	9FS	V _{DS} = 10 V,	I _D = 7.0 A		30		S
CHARGES, CAPACITANCES AND GATE RE	SISTANCE		•			•	
Input Capacitance	C _{ISS}				560		pF
Output Capacitance	C _{OSS}	$V_{GS} = 0 \text{ V, f} = V_{DS} = 0$	= 1.0 MHz, 24 V		115		1
Reverse Transfer Capacitance	C _{RSS}	v _{DS} = 24 v			75		1
Total Gate Charge	$Q_{G(TOT)}$				12		nC
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = 10 \text{ V}, V_{DS} = 15 \text{ V},$ $I_D = 7.0 \text{ A}$			0.85		1
Gate-to-Source Charge	Q_{GS}	$I_D = 7$	0 A		1.9		1
Gate-to-Drain Charge	Q_{GD}		-		3.0		1
Total Gate Charge	Q _{G(TOT)}				6.0		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 4.5 V, \	/ _{DS} = 15 V,		0.8		1
Gate-to-Source Charge	Q_{GS}	$I_D = 7$	0 A		1.85		1
Gate-to-Drain Charge	Q_{GD}		-		3.0		
Gate Resistance	R_{G}				2.8		Ω
SWITCHING CHARACTERISTICS (Note 4)	•				•	1	
Turn-On Delay Time	t _{d(ON)}				6.0		ns
Rise Time	t _r	V _{GS} = 10 V, V	'ns = 24 V.		15		
Turn-Off Delay Time	t _{d(OFF)}	$I_D = 7.0 \text{ A}, R_G = 3.0 \Omega$			18		
Fall Time	t _f				4.0		1
DRAIN - SOURCE DIODE CHARACTERIST	ics						
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	$T_J = 25^{\circ}C$		0.78	1.0	V
		$I_{S} = 2.0 \text{ A}$	T _J = 125°C		0.63		
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V}$ $dI_{S}/dt = 100 \text{ A/}\mu\text{s}, I_{S} = 2.0 \text{ A}$			15		ns
Charge Time	t _a				9.0		
Discharge Time	t _b				6.0		1

Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

查询"NTGS4141N-D"供应商

TYPICAL PERFORMANCE CURVES

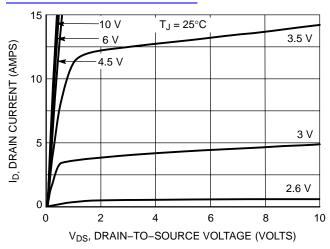


Figure 1. On-Region Characteristics

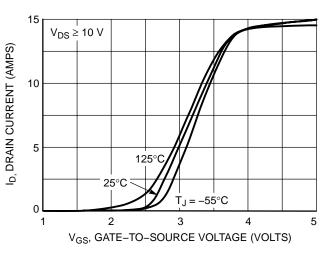


Figure 2. Transfer Characteristics

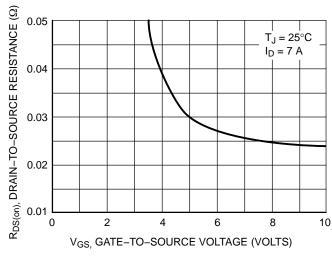


Figure 3. On-Resistance vs. Gate-to-Source Voltage

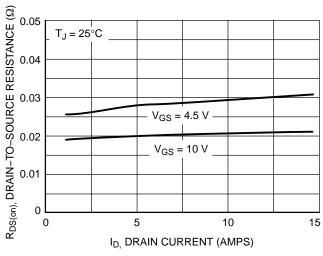


Figure 4. On–Resistance vs. Drain Current and Gate Voltage

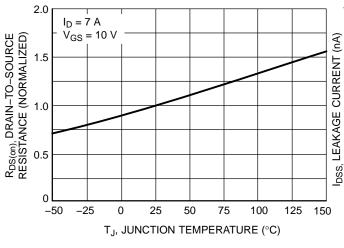


Figure 5. On–Resistance Variation with Temperature

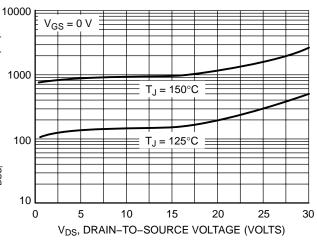
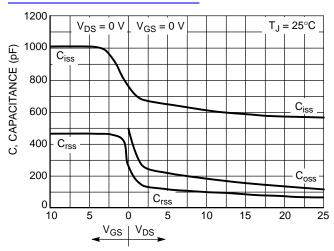


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL PERFORMANCE CURVES

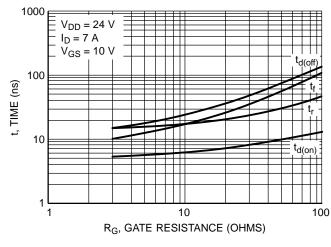


VGS GATE-TO-SOURCE VOLTAGE (V) QT 8 V_{GS} Q_{GD} $I_D = 7 A$ 2 V_{DD} = 15 V $T_J = 25^{\circ}C$ 0 2 6 12 0 10 Q_G, TOTAL GATE CHARGE (nC)

GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge





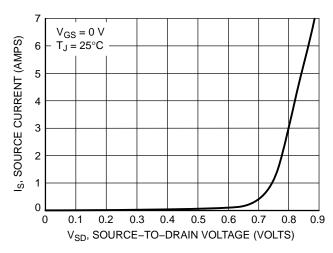


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

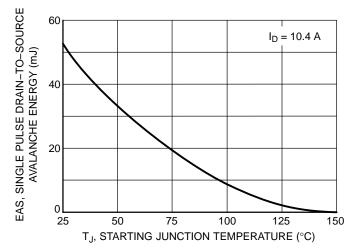
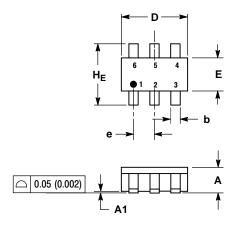


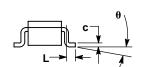
Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

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PACKAGE DIMENSIONS

TSOP-6 CASE 318G-02 ISSUE P





NOTES:

- OT LC.

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

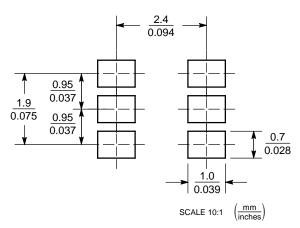
 2. CONTROLLING DIMENSION: MILLIMETER.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.90	1.00	1.10	0.035	0.039	0.043	
A1	0.01	0.06	0.10	0.001	0.002	0.004	
b	0.25	0.38	0.50	0.010	0.014	0.020	
C	0.10	0.18	0.26	0.004	0.007	0.010	
D	2.90	3.00	3.10	0.114	0.118	0.122	
Е	1.30	1.50	1.70	0.051	0.059	0.067	
е	0.85	0.95	1.05	0.034	0.037	0.041	
L	0.20	0.40	0.60	0.008	0.016	0.024	
HE	2.50	2.75	3.00	0.099	0.108	0.118	
θ	0°	_	10°	0°	_	10°	

PIN 1. DRAIN 2. DRAIN 3. GATE

- 4. SOURCE 5. DRAIN
- 6. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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