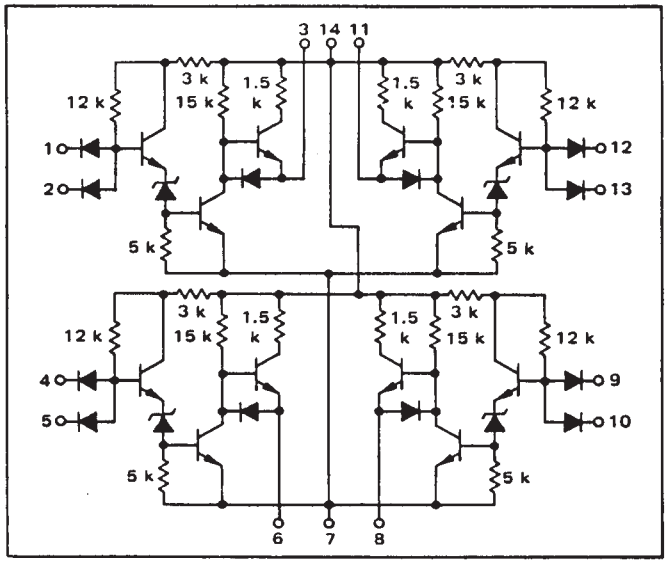
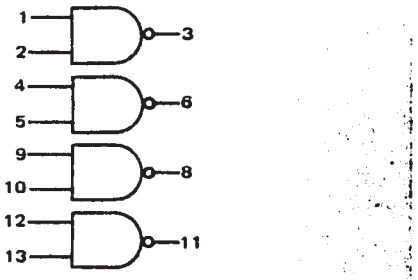
# ML672
## Quad 2-Input "Nand" Gate

**Legacy Device:** *Motorola MC672*




This device consists of four 2-input NAND gates with active output pullup.




Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High = 176 mW typ/pkg
Input Low = 52 mW typ/pkg

## ELECTRICAL CHARACTERISTICS

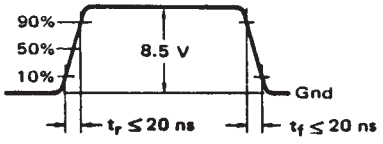
Test procedures shown are for one gate only. The other gates are tested in the same manner.

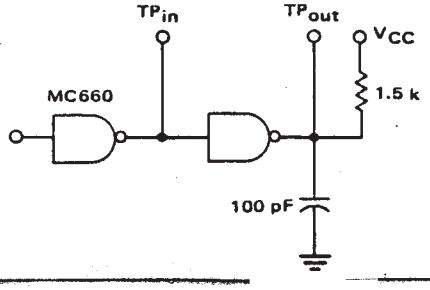
| TEST CURRENT/VOLTAGE VALUES (All Temperatures) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| mA | | Volts | | | | | | | |
| $I_{OL}$ | $I_{OH}$ | $V_{IL}$ | $V_{IH}$ | $V_F$ | $V_R$ | $V_{CEX}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ |
| 12.0 | -0.03 | 6.50 | 8.50 | 1.5 | 16.0 | 16.0 | 15.0 | 14.0 | 16.0 |

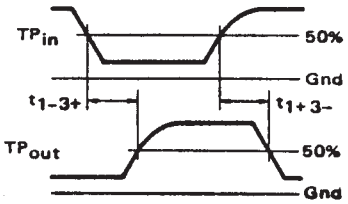
| Characteristic | Symbol | Pin Under Test | 672 Test Limits −30°C Min | −30°C Max | +25°C Min | +25°C Max | +75°C Min | +75°C Max | Unit | TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{OL}$ | $I_{OH}$ | $V_{IL}$ | $V_{IH}$ | $V_F$ | $V_R$ | $V_{CEX}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ | Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage | $V_{OL}$ | 3 | - | 1.5 | - | 1.5 | - | 1.5 | Vdc | 3 | - | - | 1.2 | - | - | - | - | 14 | - | 7 |
| | $V_{OH}$ | 3 | - | - | 12.5 | - | 12.5 | - | Vdc | - | 3 | 1 | - | - | - | - | 2 | 14 | - | 7 |
| | | 3 | - | - | 12.5 | - | 12.5 | - | Vdc | - | 3 | 2 | - | - | - | - | 1 | 14 | - | 7 |
| Short-Circuit Current | $I_{SC}$ | 3 | - | - | -6.5 | -15.0 | -6.5 | -15.0 | mAdc | - | - | - | - | - | - | - | - | - | 14 | 1.3.7 |
| Reverse Current | $I_R$ | 1 | - | - | - | 2.0 | - | 2.0 | μAdc | - | - | - | - | - | 1 | - | - | 14 | - | 2.7 |
| | | 2 | - | - | - | 2.0 | - | 2.0 | μAdc | - | - | - | - | - | 2 | - | - | 14 | - | 1.7 |
| Output Leakage Current | $I_{CEX}$ | 3 | - | - | - | 100 | - | 100 | μAdc | - | - | - | - | - | - | 3.14 | - | - | - | 1.7 |
| Forward Current | $I_F$ | 1 | - | - | - | -1.20 | - | -1.20 | mAdc | - | - | - | - | 1 | 2 | - | - | - | 14 | 7 |
| | | 2 | - | - | - | -1.20 | - | -1.20 | mAdc | - | - | - | - | 2 | 1 | - | - | - | 14 | 7 |
| Power Drain Current (Total Device) | $I_{CCL}$ | 14 | - | - | - | 6.0 | - | - | mAdc | - | - | - | - | - | - | - | - | - | 14 | 1.2.4.5.7.9. 10.12.13 |
| | $I_{CCH}$ | 14 | - | - | - | 20 | - | - | mAdc | - | - | - | - | - | - | - | - | - | 14 | 7 |
| Switching Times | | | | | | | | | | Pulse In | Pulse Out | | | | | | | | | |
| | $t_{1-3+}$ | 3 | - | - | - | 200 | - | - | ns | 1 | 3 | - | - | - | - | - | 14 | - | - | 7 |
| | $t_{1+3-}$ | 3 | - | - | - | 100 | - | - | ns | 1 | 3 | - | - | - | - | - | 14 | - | - | 7 |

Pins not listed are left open.

### SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS




f = 500 kHz
DUTY CYCLE = 50%