DisplayPort 1:1 Signal Repeater and Signal Conditioner

Check for Samples: SN75DP119

FEATURES

- **DP signal repeater**
- **Supports Data Rates up to 2.7Gbps**
- **Fixed Equalizer With 3 Selectable Settings**
- **12kV ESD HBM**
- **Temperature Range: 0..85°C**
- **14 Pin 3.5x3.5mm RGY Package or 36-Pin 6.0x6.0mm RHH Package**

APPLICATIONS

- **eDP**
- **Desktop PC**
- **Notebook PC**
- **PC Docking Station**
- **PC Standalone Video Card**

DESCRIPTION

The SN75DP119 is a 1-lane or 2-lane embedded DisplayPort (eDP) repeater that regenerates the DP high speed digital link. The device compensates for pcb related frequency loss and signal reflections. This is especially helpful in designs with long pcb traces or when there is a FET switch in the signal path.

Four levels of differential output voltage swing (V_{OD}) and any combination of pre-emphasis using these V_{OD} levels are supported. The output swing and pre-emphasis are configured through device control inputs. The available output swing levels are $300mV_{PP}$, $400mV_{PP}$, $600mV_{PP}$ or $750mV_{PP}$. Therefore, the output pre-emphasis level can be configured to 0dB, 2.0dB, 2,5dB, 3.5dB, 5.5dB, 6dB, or 8dB. This is a good solution for embedded link applications, such as the connection from the GPU to the notebook internal panel. To adjust the output signal level adaptively during link training, the implementation needs to control the device control inputs.

The SN75DP119 supports programmable integrated receiver equalization circuitry. This equalization circuitry can be used to help improve signal integrity in applications where the input link has a high level of insertion loss. The equalizer can be set to 3dB or 6dB equalization. The equalizer can also be turned off.

The SN75DP119 consumes between 64mW and 175mW depending on the selected mode of operation. The device also supports an ultra low power standby mode. In this mode, the outputs are disabled and the device draws less then 700µW of power.

The device is characterized for an extended operational temperature range from 0°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL IMPLEMENTATIONS

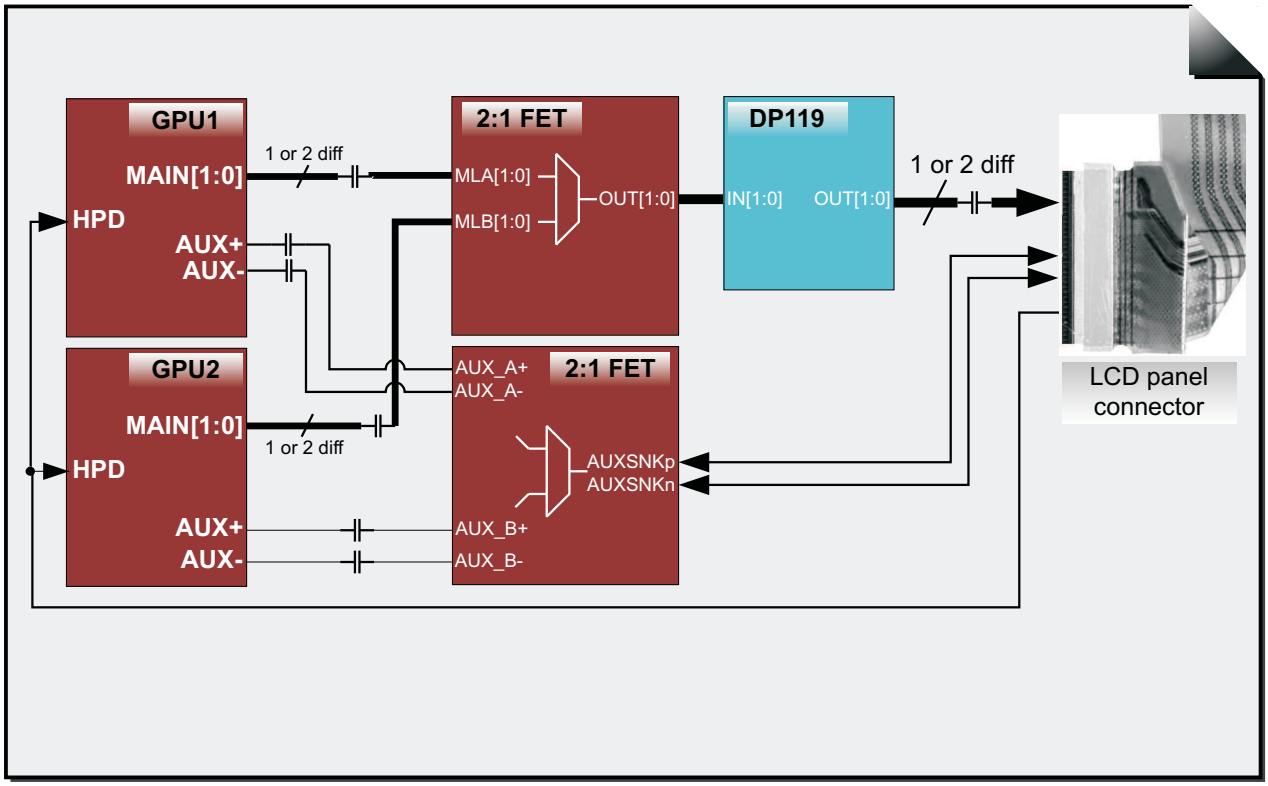


Figure 1. Typical Implementation Showing Two GPU Sources, a 2:1 FET Switch, and the DP119 as Signal Conditioner

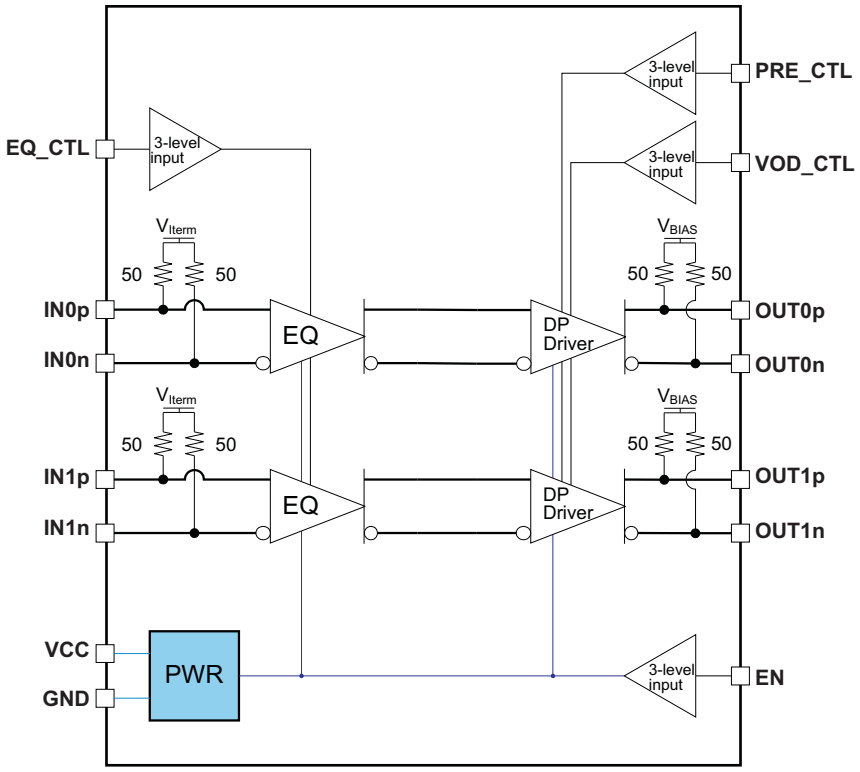


Figure 2. Device Block Diagram

PACKAGE PIN OUT

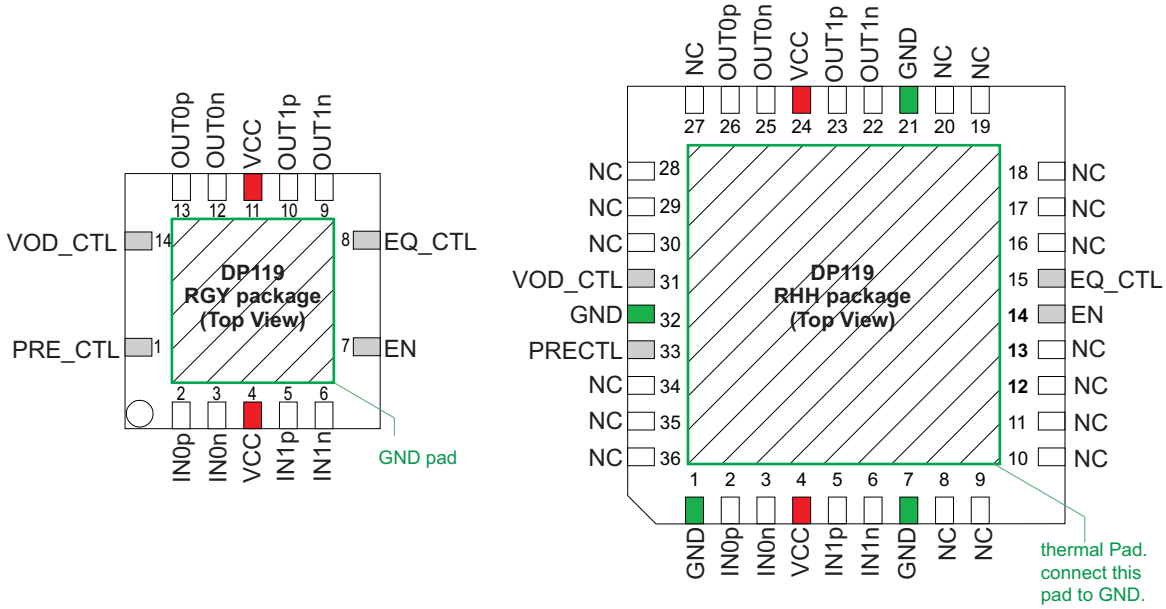


Table 1. Pin List 14-Pin RGY Package

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
IN0p/n	2, 3	OUT0p/n	13, 12	EN	7	VOD_CTL	14	pwr	4, 11
IN1p/n	5, 6	OUT1p/n	10, 9	PRE_CTL	1	EQ_CTL	8	GND	thermal pad

Table 2. Pin List 36-Pin RHH Package

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
IN0p/n	2, 3	OUT0p/n	23, 22	EN	14	VOD_CTL	31	pwr	4, 24	N.C.	8-13,16-20, 27-30, 34-36
IN1p/n	5, 6	OUT1p/n	26, 25	PRE_CTL	33	EQ_CTL	15	GND	1, 7, 21, 32 thermal pad		

PIN FUNCTIONS

PIN		DESCRIPTION
SIGNAL	I/O	
MAIN LINK INPUT PINS		
IN0p/n	I [100Ω diff]	DisplayPort Main Link Channel 0 Differential Input
IN1p/n		DisplayPort Main Link Channel 1 Differential Input
MAIN LINK OUTPUT PINS		
OUT0p/n	O [100Ω diff]	DisplayPort Main Link Channel 0 Differential Output
OUT1p/n		DisplayPort Main Link Channel 1 Differential Output
CONTROL PINS		
EN	3-level Input [CMOS]	Enable. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure the device for 1-channel mode, 2-channel mode or power down mode. EN = HIGH: Device in Normal Mode, both outputs OUT1 and OUT2 are enabled; EN = VCC/2 (input left floating): Device in Normal mode, 2nd output is disabled; EN = LOW: Device in Power Down mode. All outputs are high-impedance; Inputs are ignored
PRE_CTL	3-level Input [CMOS]	Configures the output pre-emphasis level. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure the pre-emphasis for 3 different levels. See Table 4 for configuration details.
VOD_CTL	3-level Input [CMOS]	Configures the output amplitude VOD level. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure 3 different output swing amplitudes. See Table 4 for configuration details.
EQ_CTL	3-level Input [CMOS]	Configures the EQ input setting for both differential inputs. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure the pre-emphasis for 3 different levels. EQ_CTL = LOW: 0dB (EQ turned off) EQ_CTL = VCC/2 (input left floating): 3dB fixed EQ EQ_CTL = HIGH (input tied to VCC): 6dB fixed EQ
SUPPLY AND GROUND PINS		
VCC	pwr	3.3V Supply
GND	pwr	Ground
Note: (H) Logic High: (L) Logic Low		

STATUS DETECT AND OPERATING MODES FLOW DIAGRAM

The SN75DP119 switches between the power saving and the active modes in the following way:

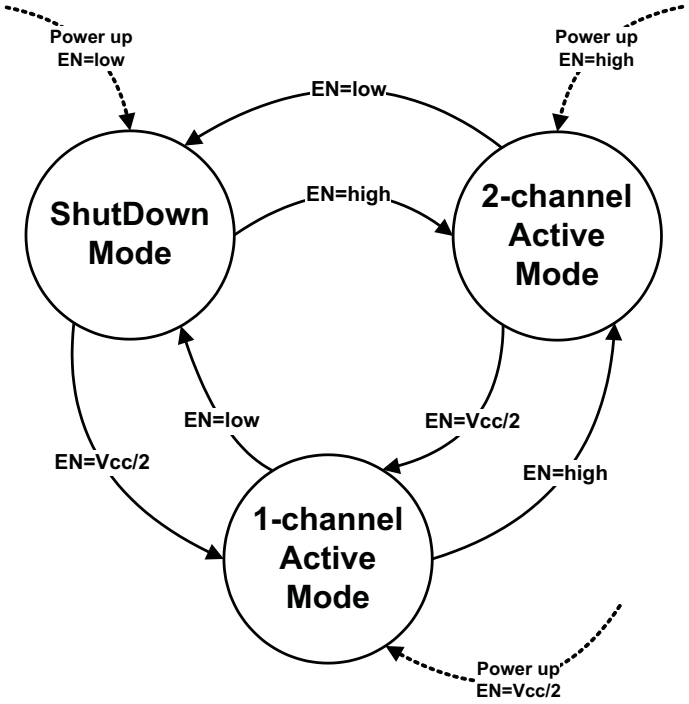


Figure 3. SN75DP119 Operational Modes Flow Chart

Table 3. Description of SN75DP119 Modes

MODE	CHARACTERISTICS	CONDITIONS
ShutDown Mode	Least amount of power consumption (all circuitry turned off); outputs are high-impedance	EN is low
2- channel Active Mode	Data transfer (normal operation); The device outputs OUTx represents the data received on the input INx. The input EQ and output pre-emphasis and output swing voltage level are controlled through the external control pins.	EN is high (both main link outputs enabled)
1-channel Active Mode	Data transfer (normal operation); The device output OUT0 represents the data received on the input IN0. The 2nd channel (IN1 and OUT1) are disabled. The input EQ and output pre-emphasis and output swing voltage level are controlled through the external control pins.	EN is VCC/2 (only main link channel 0 enabled)

PRE-EMPHASIS AND VOD OUTPUT SWING SETINGS

The SN75DP119 allows configuring output pre-emphasis and output swing through the external control inputs. The following options are valid:

Table 4. Pre-Emphasis and V_{OD} Output Swing Configuration

	PRE_CTL = LOW	PRE_CTL = VCC/2 (INPUT LEFT FLOATING)	PRE_CTL = HIGH
VOD_CTL = LOW	V_{OD} = 300 mV_{PP}; 2.5 dB pre-emphasis (lowest power consumption)	V_{OD} = 300 mV_{PP}; 6 dB pre-emphasis	V_{OD} = 300 mV_{PP}; 8.5 dB pre-emphasis
VOD_CTL = VCC/2 (input left floating)	V_{OD} = 400 mV_{PP}; no pre-emphasis	V_{OD} = 400 mV_{PP}; 3.5 dB pre-emphasis	V_{OD} = 400 mV_{PP}; 5.5 dB pre-emphasis
VOD_CTL = HIGH	V_{OD} = 600 mV_{PP}; no pre-emphasis	V_{OD} = 600 mV_{PP}; 2.5 dB pre-emphasis	V_{OD} = 800 mV_{PP}, no pre-emphasis

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN75DP119RGYR	DP119	14-pin QFN Reel
SN75DP119RHHR	DP119	36-pin QFN Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE / UNIT
Supply Voltage Range(2)	V_{CC}		–0.3 V to 4 V
Voltage Range	Main Link I/O (OUTx, INx) Differential Voltage		–0.3 V to VCC+0.3 V
	Control Inputs		–0.3 V to 5.5 V
Electrostatic discharge	Human body model(3)	OUTx, AUX_SNK, HPD_IN, CAD_IN	±12 kV
		All other pins	±12 kV
	Charged-device model(4)		±1000 V
	Machine model(5)		±200 V
Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
14-pin QFN (RGY)	Low-K	800 mW	8 mW/°C	310 mW
	High-K	1800 mW	18 mW/°C	750 mW
36-pin QFN (RHH)	Low-K	1000 mW	10 mW/°C	400 mW
	High-K	2700 mW	27 mW/°C	1080 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{\theta JB}$	Junction-to-board thermal resitance	4×4 Thermal vias under powerpad	RGY		18		°C/W
			RHH		12		
$R_{\theta JC}$	Junction-to-pad (thermal pad) thermal resitance		RGY		5		°C/W
			RHH		5		
P_N	Device power under normal operation	EN = VCC, OUTx: V_{OD} = 800 mVpp, 3.5 dB pre-emphasis; 2.7 Gbps PRBS; VCC = 3.6 V				150	mW
P_{SD}	Device power dissipation under low power	No Activity on INx; EN=GND				360	µW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	0		85	°C
3-LEVEL CONTROL PINS (EN, VOD_CTL, PRE_CTL, EQ_CTL)					
V_{IH}	High-level input voltage	V_{CC}–0.5			V
V_{IM}	Mid-level input voltage	V_{CC}/2–0.3		V_{CC}/2+0.3	V
V_{IL}	Low-level input voltage			0.5	V

DEVICE POWER

SN75DP119 is designed to run from a single supply voltage of 3.3V.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CCDP1max}$	Supply current 1 DP lane selected	WorstCase: EN = V_{CC}/2 (1-lane) or V_{CC} (2-lane selected); 2.7Gbps PRBS; V_{ID} = 400 mV_{PP}; V_{OD} = 300 mVpp, 8.5 dB pre-emp (PRE_CTL=V_{CC}; V_OD_CTL=GND); EQ_CTL = V_{CC} (6 dB); V_{CC} = 3.3 V (for typ) and V_{CC} = 3.6 V (for max), (1)		16.2	21.3	mA
$I_{CCDP2max}$	Supply current 2 DP lanes selected			31.7	41.4	mA
$I_{CCDP3max}$	Supply current 1 DP lane selected	EN = V_{CC}/2 (1-lane) or VCC (2-lane selected); 2.7Gbps PRBS; V_{ID} = 400 mV_{PP}; V_{OD} = 300 mV_{PP}, 0 dB pre-emp (PRE_CTL = GND); VOD_CTL = VCC/2); EQ_CTL=GND (0 dB); V_{CC} = 3.3 V (for typ) and V_{CC} = 3.6 V (for max),		12.9	17.6	mA
$I_{CCDP4max}$	Supply current 2 DP lanes selected			24.9	34.1	mA
$I_{CCDP1typ}$	Supply current 1 DP lane selected	EN = V_{CC}/2 (1-lane) or V_{CC} (2-lane selected); 2.7Gbps PRBS; IN/OUT; V_{ID} = 600 mV_{PP}; (PRE_CTL=GND); VOD_CTL = V_{CC}); V_{CC} = 3.3 V, EQ_CTL = GND (no EQ) (2)		14.5		mA
$I_{CCDP2typ}$	Supply current 2 DP lanes selected			28.2		mA
$I_{CCDP3typ}$	Supply current 1 DP lane selected	EN = V_{CC}/2 (1-lane) or V_{CC} (2-lane selected); 2.7Gbps PRBS; no pre-emp; IN/OUT; V_{ID} = 800 mV_{PP}; (PRE_CTL= VOD_CTL = V_{CC}); V_{CC} = 3.3 V, EQ_CT L = GND (no EQ) (3)		14.5		mA
$I_{CCDP4typ}$	Supply current 2 DP lanes selected			28.2		mA
IPWRDN	Shutdown current (PWRDN mode)	EN = GND;		25	100	µA
3-LEVEL CONTROL PINS (EN, VOD_CTL, PRE_CTL, EQ_CTL)						
I_L	Low-level input current	V_I = 0.5 V; V_{CC} = 3.6 V	–30		30	µA
I_H	High-level input current	V_I = V_{CC} – 0.5 V; Vcc = 3.6V	–30		30	µA
I_M	Mid-level input current	V_I = V_{CC} /2 – 0.3V and V_I = V_{CC} /2 + 0.3 V; V_{CC} = 3.6 V	–30		30	µA
R_{bias}	Input bias resistance	See Figure 8	105	125	145	kΩ
R_{ESD}	input series resistance to biasing network	See Figure 8		2	2.4	kΩ

(1) This current consumption also applies to VOD=400mV with 5.5 dB pre-emphasis or VOD=600mV output swing and 2dB pre-emphasis
(2) This current consumption also applies to VOD=300mV with 2 dB pre-emphasis
(3) This current consumption also applies to VOD=300mV with 6dB pre-emphasis or VOD=400mV output swing and 3.5dB pre-emphasis

MAIN LINK IO

The SN75DP119 is designed to support the DisplayPort high speed differential main link with three levels of output voltage swing and three levels of pre-emphasis. The main link I/Os of the SN75DP119 are designed to be compliant with the DisplayPort 1.1a specification.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
MAIN LINK DIFFERENTIAL INPUT AND OUTPUT PINS IN[4:1] AND OUT[4:1]					
V_{ID}	Peak-to-peak input differential voltage – HBR (high bit rate)	0.15		1.4	V_{PP}
V_{ID}	Peak-to-peak input differential voltage – LBR (low bit rate)	0.15		1.4	V_{PP}
d_R	Data rate			2.7	Gbps
C_{AC}	AC coupling capacitance (each input and each output line)	1×75		2×200	nF
R_{tdiff}	Differential output termination resistance	80	100	120	Ω
V_{Oterm}	Output termination voltage (AC coupled)	0		2	V
$t_{SK(in\ HBR)}$	Intra-pair skew at the input package pins using 2.7 Gbps input data rate			100	ps
$t_{SK(in\ LBR)}$	Intra-pair skew at the input package pins using 1.62 Gbps input data rate			300	ps
$t_{R/F}$	Input rise and fall time			160	ps

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN[1:0], OUT[1:0]						
[$V_{OD(0.3)}$]	Output differential voltage swing	V_{PRE} = $V_{PRE(0.0)}$; 675 Mbps D10.2 test pattern; V_{ID} = 300 mVpp; EQ = 3 dB	300mV setting only used with pre-emphasis [300]			mV_{pp}
$V_{OD(0.4)}$				400		mV_{pp}
$V_{OD(0.6)}$				600		mV_{pp}
$V_{OD(0.75)}$				800		mV_{pp}
$V_{Eyemask}$	Eyemask compliance	V_{OD} = 800 mVpp test pattern measured in compliance with PHY CTS1.1 section 3.1 at test point TP2; V_{ID}= 300mV_{PP} ; EQ=3dB	pass			
$V_{PRE(0.0)}$	Driver output pre-emphasis	V_{OD} = $V_{OD(0.4)}$, $V_{OD(0.6)}$, or $V_{OD(0.8)}$ at 2.7Gbps only		0		dB
$V_{PRE(2.5)}$		V_{OD} = $V_{OD(0.3)}$ or $V_{OD(0.6)}$ at 2.7Gbps only		2.7		dB
$V_{PRE(3.5)}$		V_{OD} = $V_{OD(0.4)}$ at 2.7Gbps only; EQ=3dB	0.9	3.5		dB
$V_{PRE(6.0)}$		V_{OD} = $V_{OD(0.3)}$ or $V_{OD(0.4)}$ at 2.7Gbps only; EQ=3dB	3.3	6.0		dB
$V_{PRE(8.5)}$		V_{OD} = $V_{OD(0.3)}$ at 2.7Gbps only; EQ=3dB	7	8.5		dB
R_{OUT}	Driver output impedance (single ended)			100		Ω
R_{IN}	Differential input termination impedance		80	100	120	Ω
V_{Item}	Input termination voltage (AC coupled)	Self-biased	0	1.7	2	V
V_{OCM}	Output common mode voltage		0	1.55	2	V
V_{TXACCM}	Output AC common mode voltage	Verified through statistical measurements only using 1.62Gbps and 2.7Gbps PRBS7 data pattern measured at TP2; EQ = 3dB			20	mVrms
$I_{TXSHORT}$	Output short circuit current limit	OUT[1:0] shorted to GND; single-ended current			50	mA
$I_{RXSHORT}$	Input short circuit current limit	IN[1:0] shorted to GND (single ended)			50	mA

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R/F(DP)}$	Differential output edge rate (20%–80%)	All VOD options, Measured at TP1, PRBS7; V_{ID} = 300 mV_{PP}; EQ = 3dB; C_{LOAD} = 1 pF	50		155	ps
t_{PD}	Propagation delay time			325	550	ps
t_{skpp}	Part-to-Part skew	With identical voltage and temperature		0	160	ps
$t_{SK(1)}$	Intra-pair output skew	Signal input skew = 0ps; d_R = 2.7Gbps, No Pre-emphasis, 800 mVp-p , D10.2 pattern			20	ps
$t_{SK(2)}$	Inter-pair output skew				100	ps
$\Delta t_{DPJIT(PP)}$	Peak-to-peak output residual jitter at package pins	$V_{OD(0.4)}$; $V_{PRE(0.0)}$; Δt_{jit} = t_{jit}(output) – t_{jit}(input); verified through design simulation and statistical measurements only using 1.62Gbps and 2.7Gbps PRBS7 data pattern.			15	ps

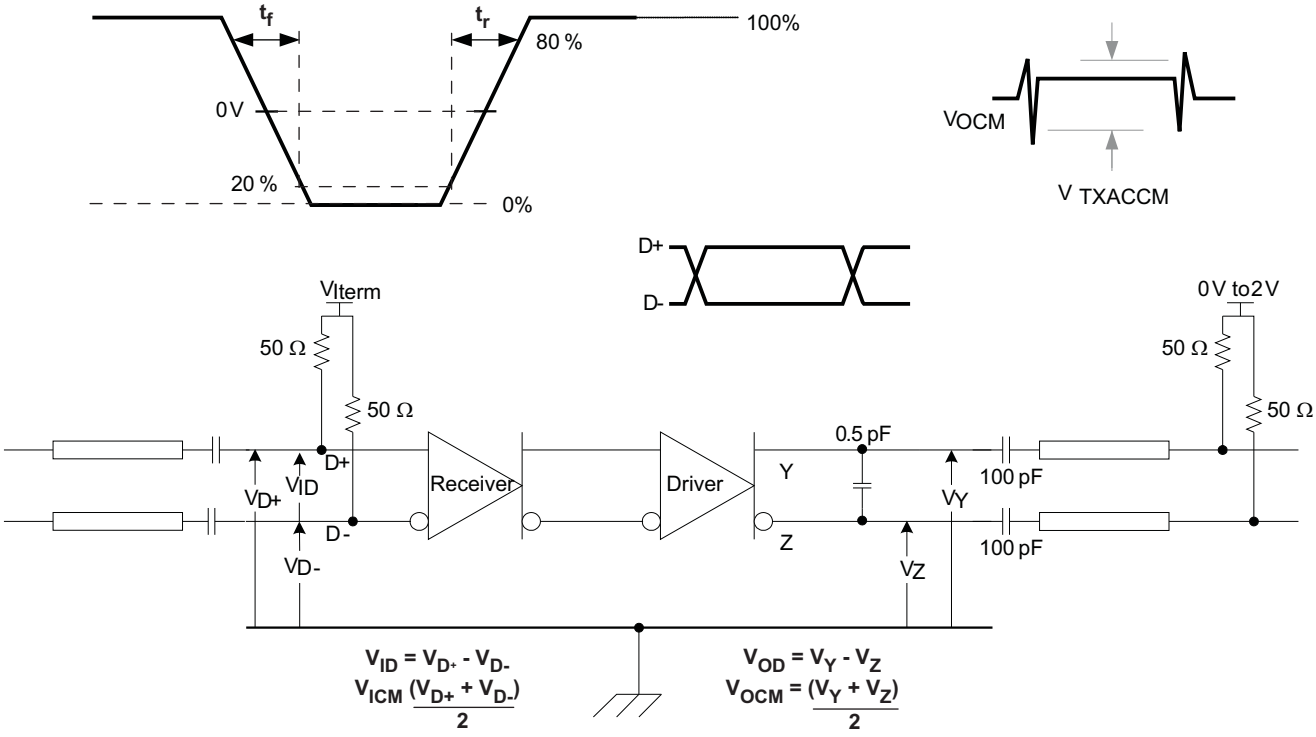


Figure 4. Main Link Test Circuit

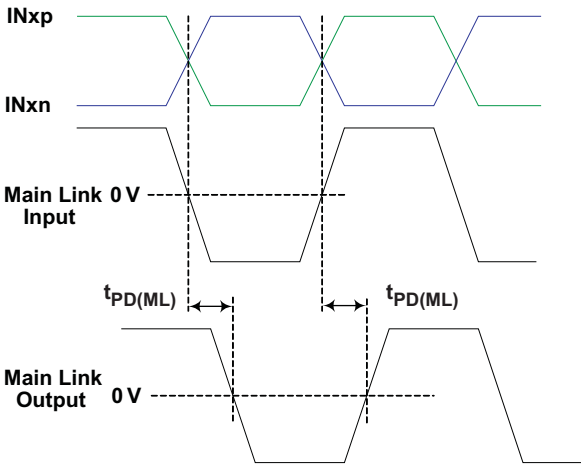


Figure 5. Main Link Delay Measurments

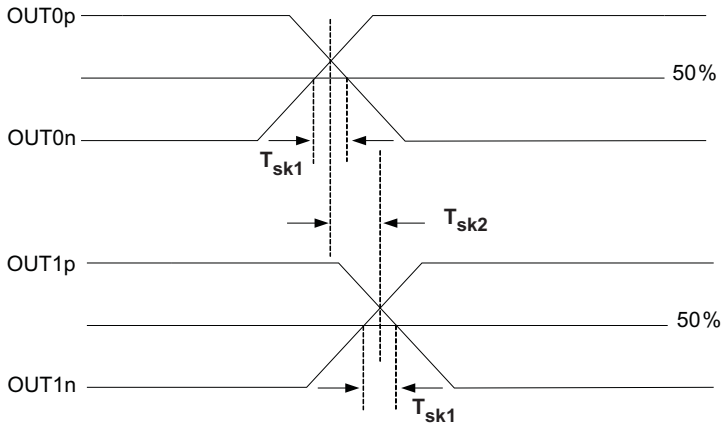


Figure 6. Main Link Skew Measurements

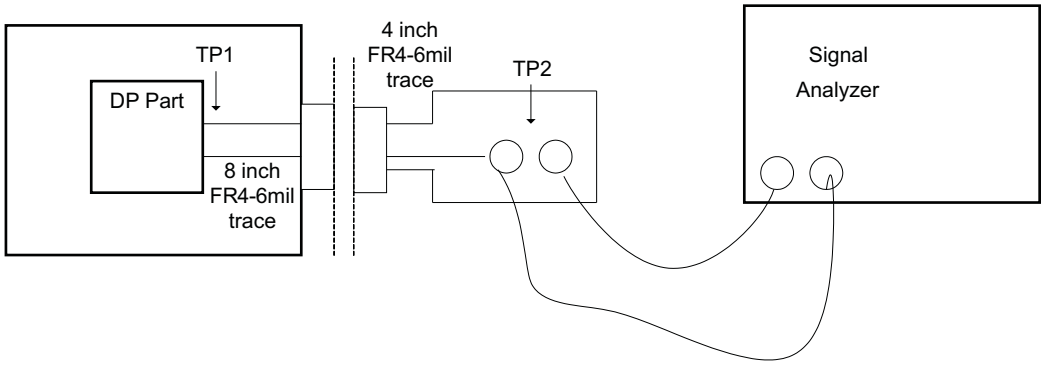


Figure 7. Display Port Compliance Setup

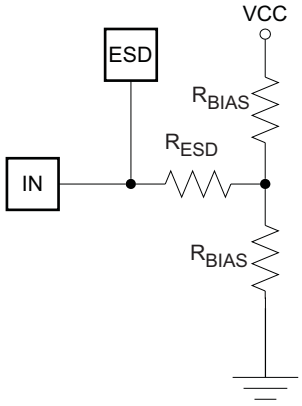


Figure 8. 3-Level Input Biasing Network

TYPICAL CHARACTERISTICS

DETERMINISTIC OUTPUT JITTER vs INPUT TRACE LENGTH

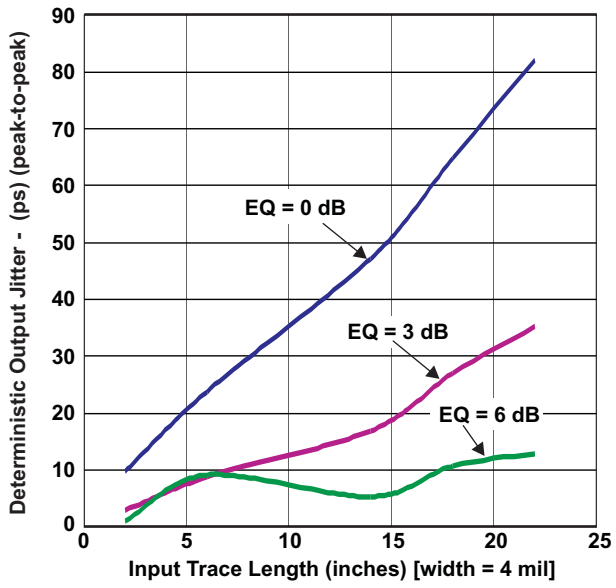
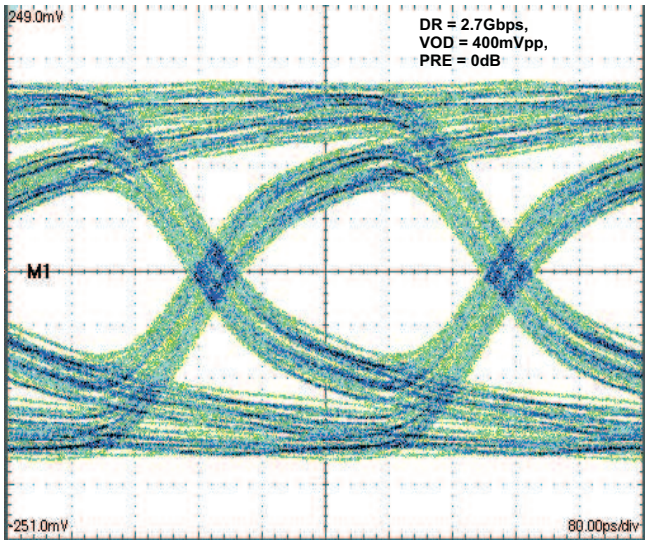


Figure 9.

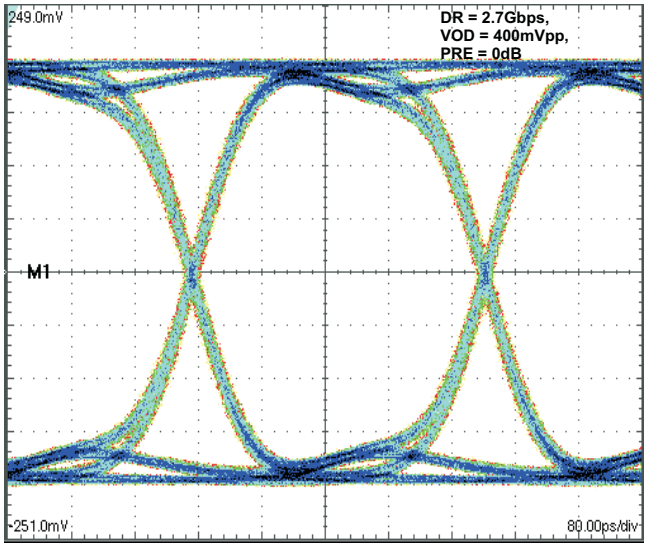
EYE PATTERN INPUT TO DP119



Trace Length = 16 (inches) [width = 4 mil]

Figure 10.

EYE PATTERN OUTPUT OF DP119



Trace Length = 16 (inches) [width = 4 mil]

Figure 11.

APPLICATION INFORMATION

Device Schematic

Figure 12 provides a simple schematic reference for the 14-pin package. In addition to this schematic sufficient VCC decoupling for the 3.3V power supply is necessary.

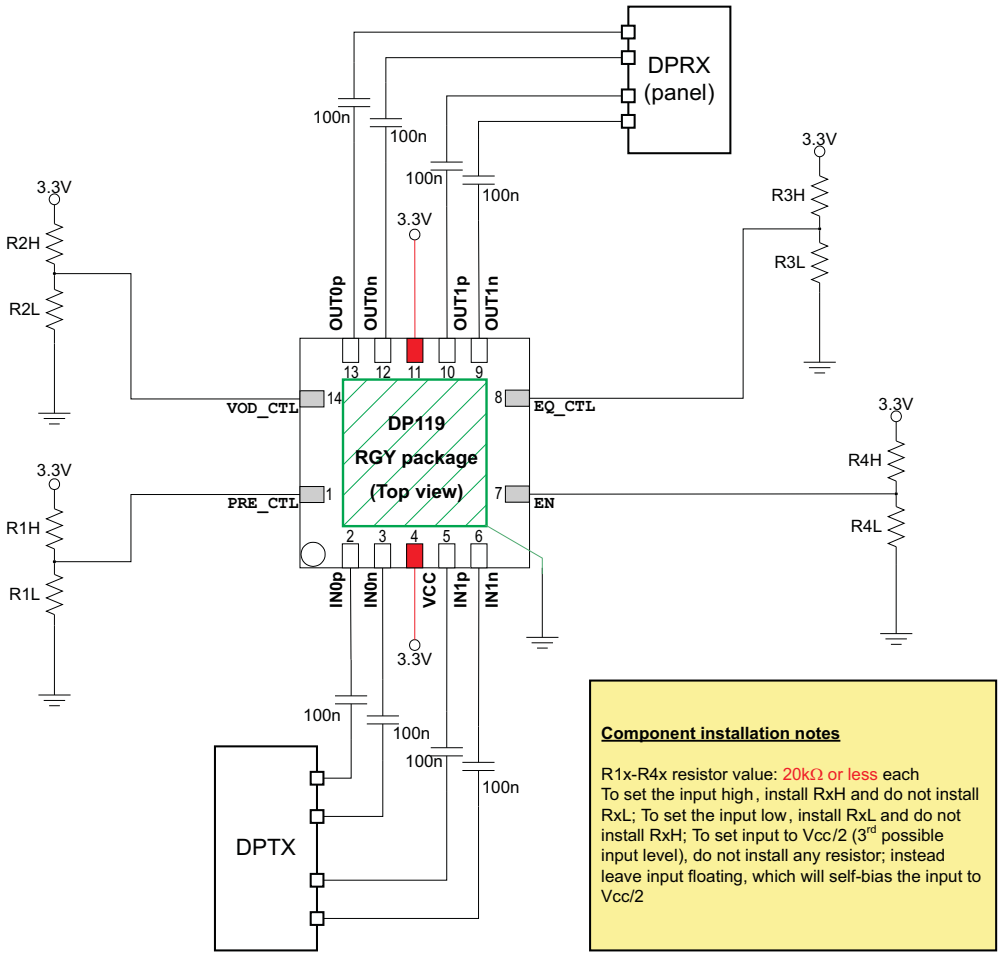


Figure 12. Simplified Schematic drawing

Layout Recommendation

Data rates of 2.7Gbps require fast edge rate, which can cause EMI radiation if the pcb is not designed carefully. Decoupling with small current loops is recommended. It is recommended to place the de-coupling cap as close as possible to the device and on the same side of the pcb (see Figure 13). Choose the capacitor such that the resonant frequency of the capacitor does not align closely with 2.7GHz. Also provide several GND vias to the thermal pad to minimize the area of current loops.

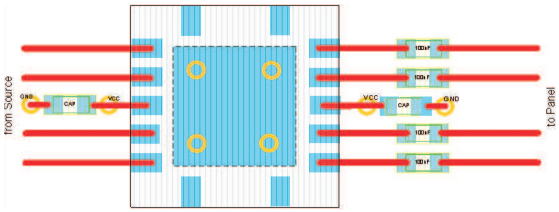


Figure 13. De-Coupling Layout Recommendation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75DP119RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75DP119RGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75DP119RHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN75DP119RHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

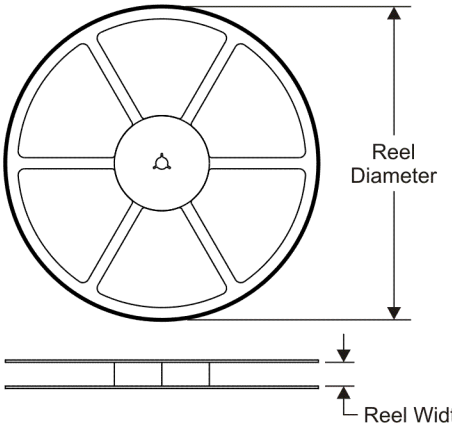
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

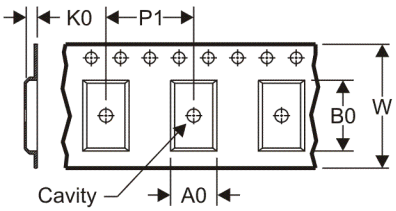
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

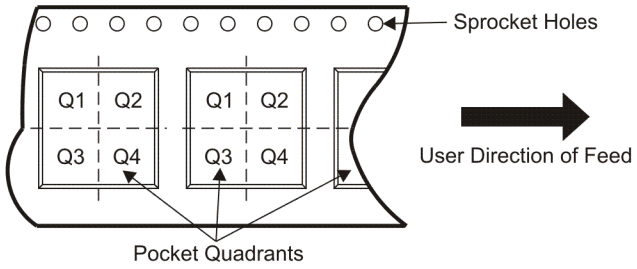


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

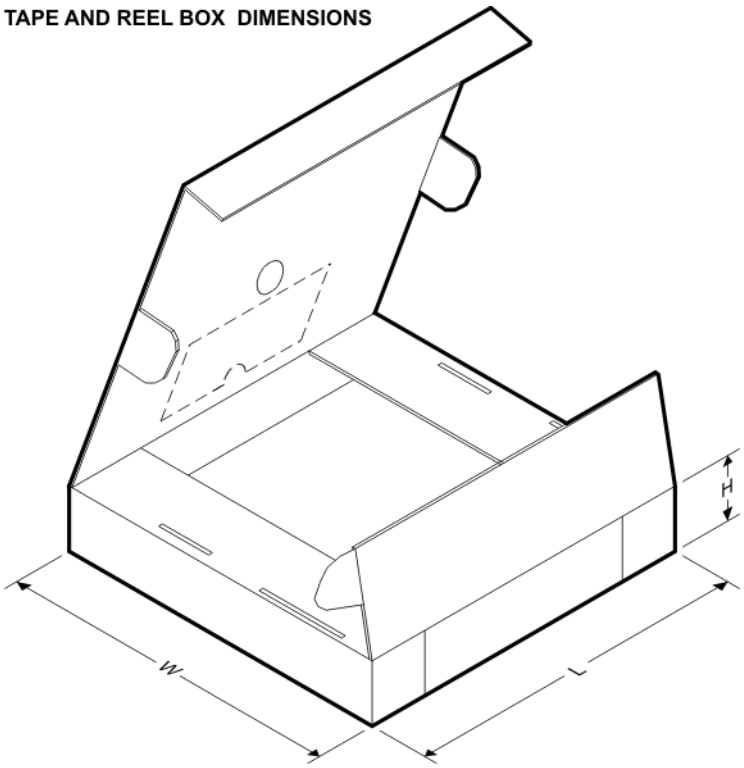
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP119RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN75DP119RGYT	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN75DP119RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
SN75DP119RHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

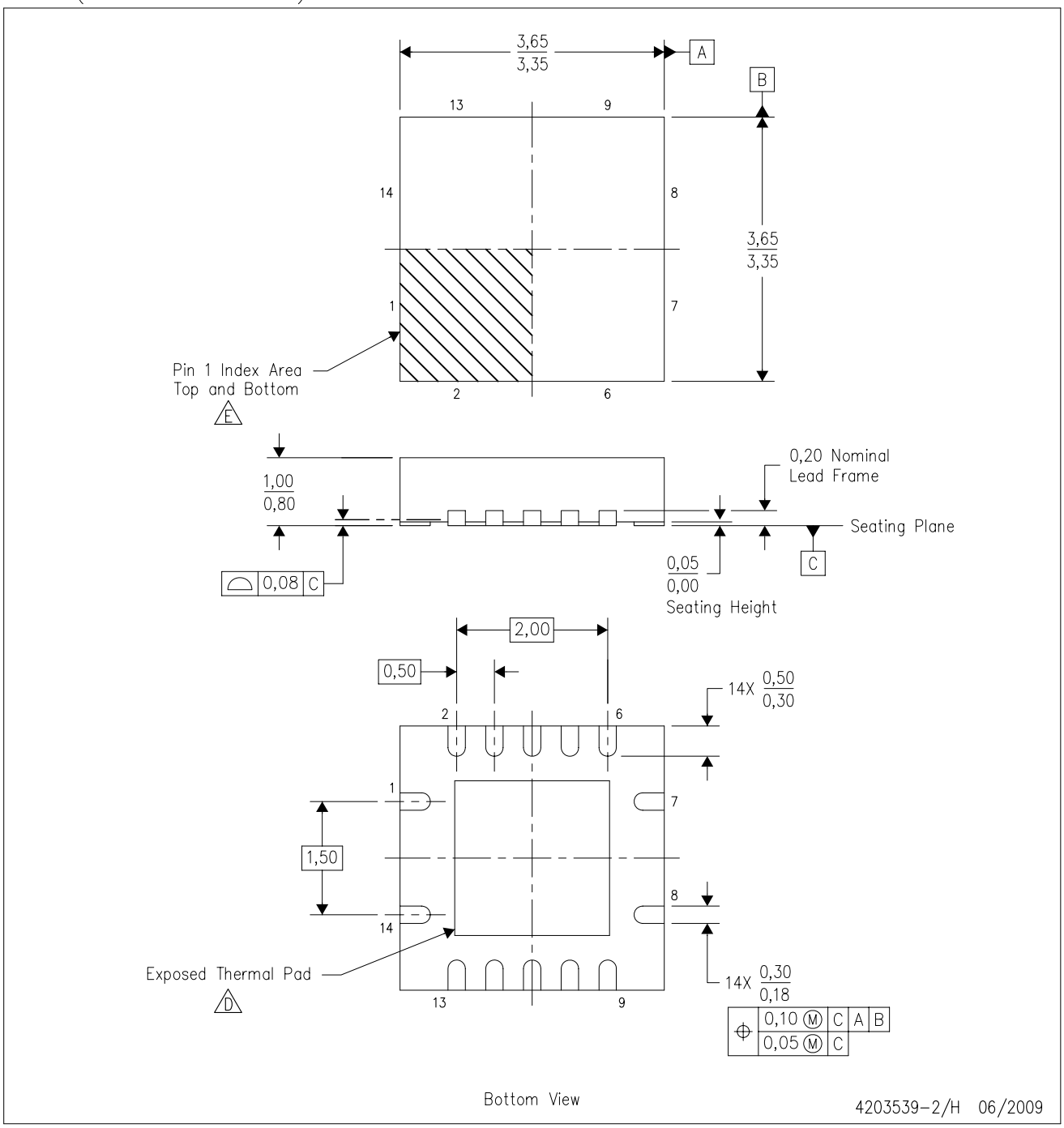
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP119RGYR	VQFN	RGY	14	3000	346.0	346.0	29.0
SN75DP119RGYT	VQFN	RGY	14	250	190.5	212.7	31.8
SN75DP119RHHR	VQFN	RHH	36	2500	346.0	346.0	33.0
SN75DP119RHHT	VQFN	RHH	36	250	190.5	212.7	31.8

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BA.

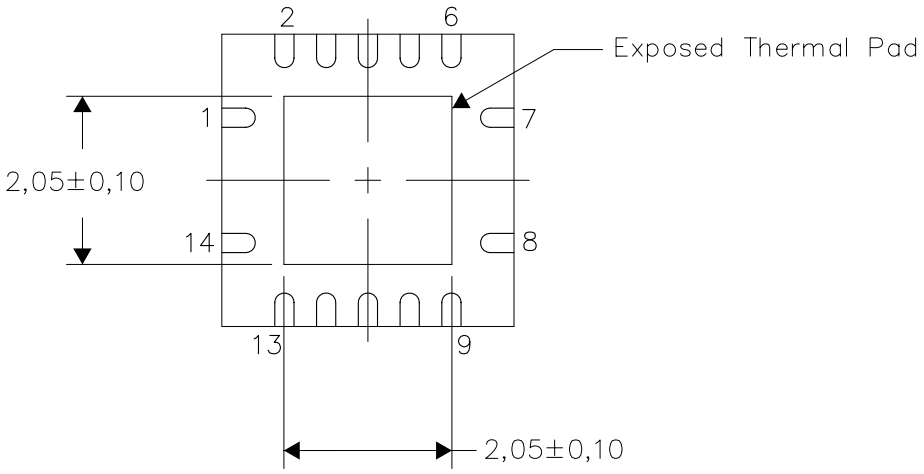
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

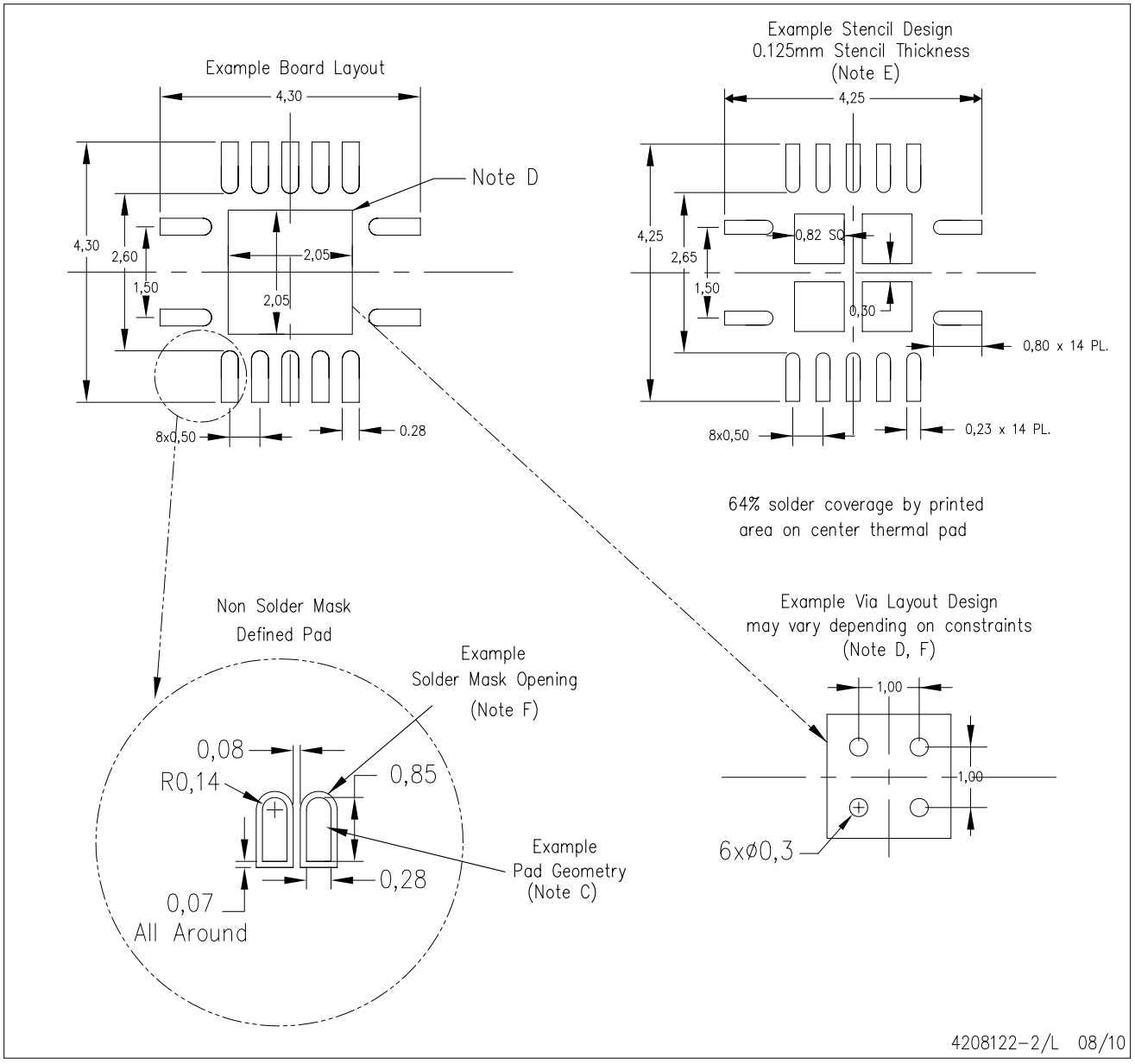


Bottom View

NOTES: All linear dimensions are in millimeters

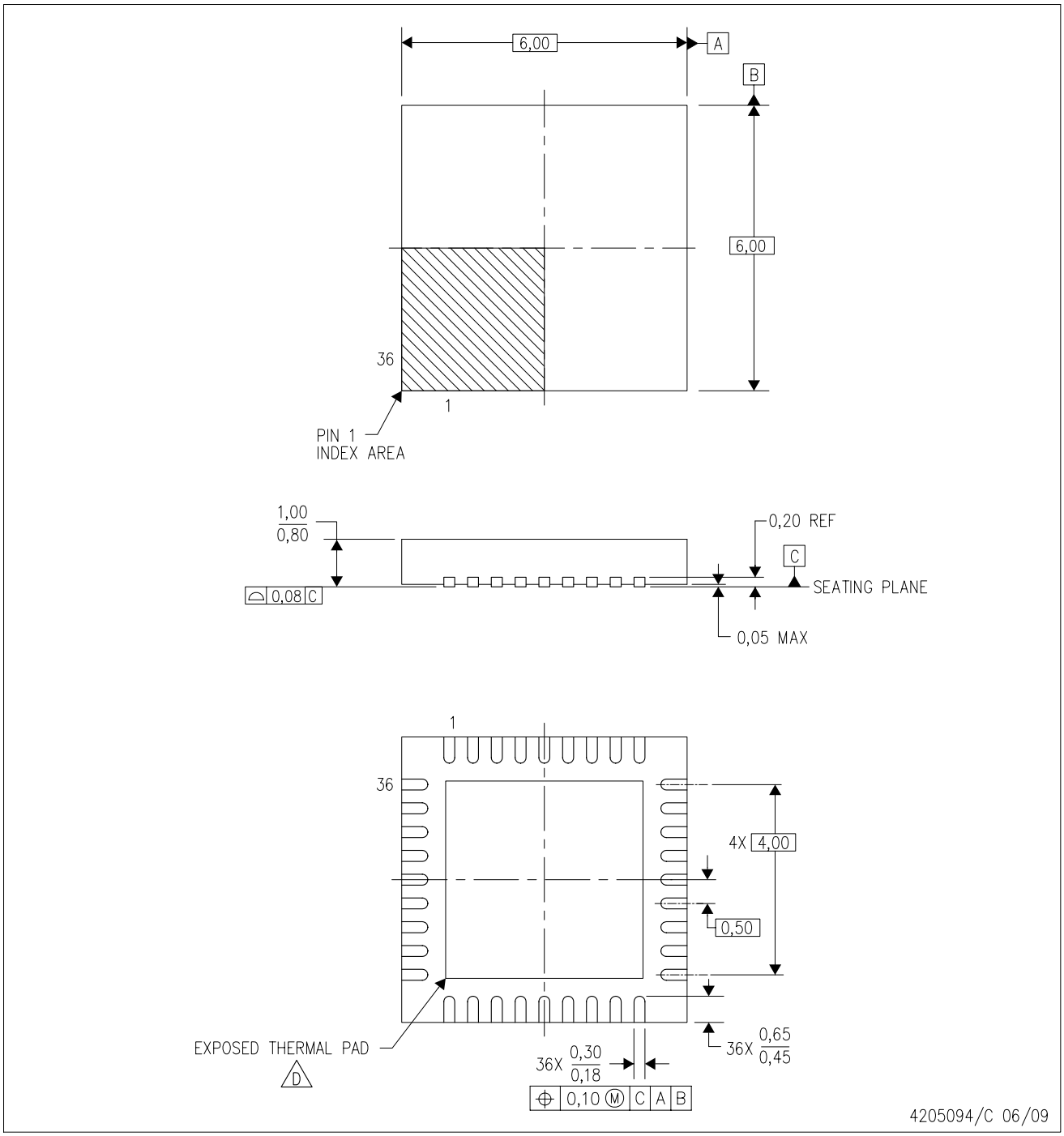
Exposed Thermal Pad Dimensions

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

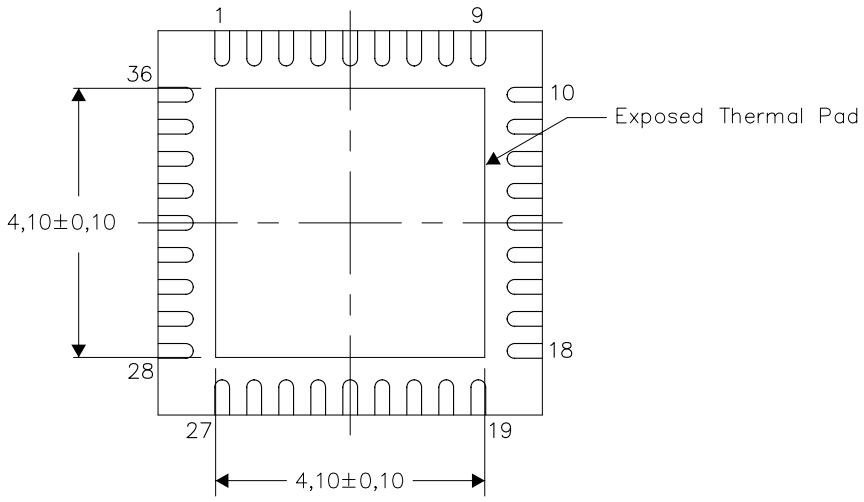
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



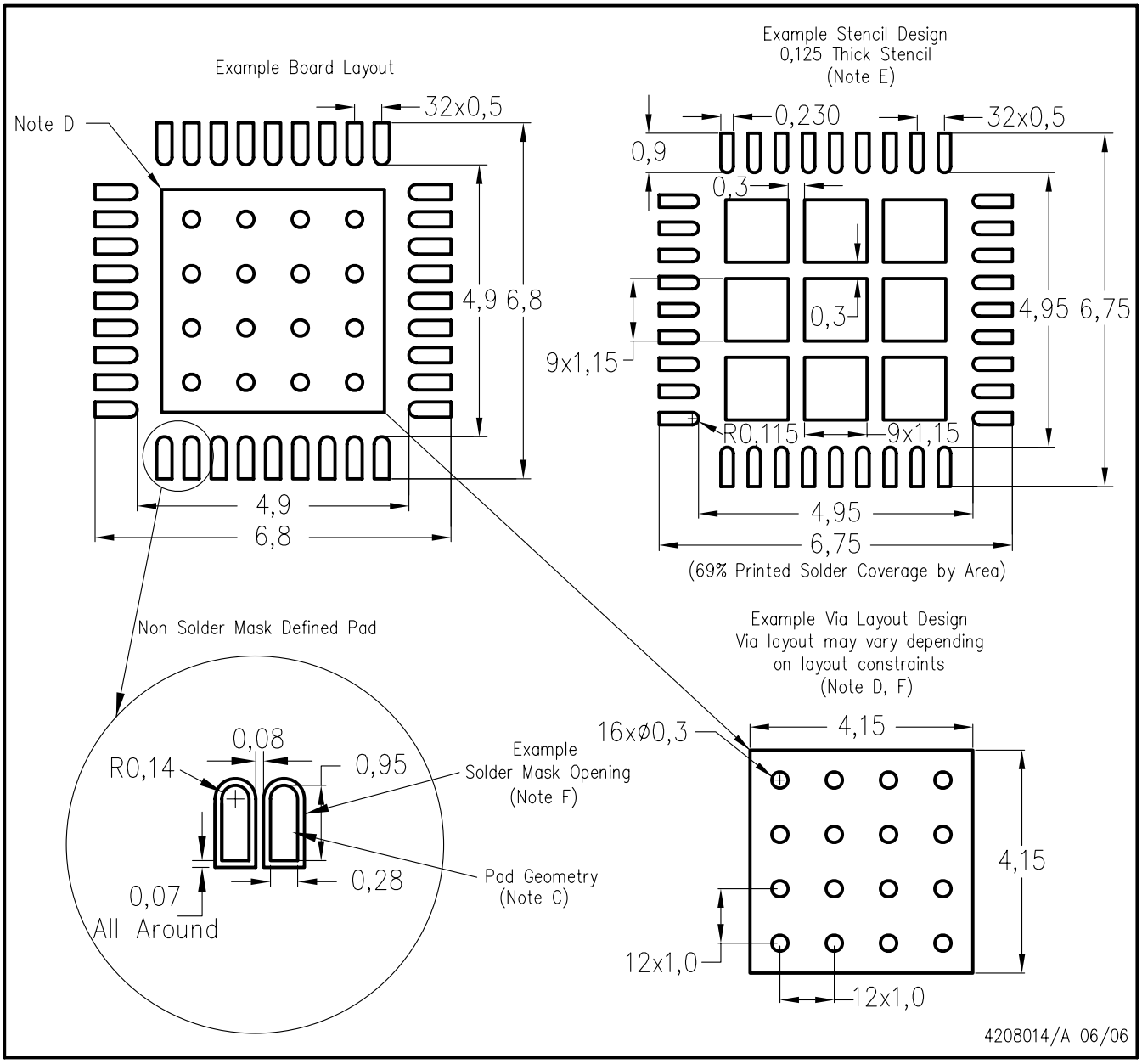
Bottom View

Exposed Thermal Pad Dimensions

4206362–3/H 09/10

NOTE: A. All linear dimensions are in millimeters

RHH (S–PQFP–N36)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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