

SN54ALVTH16244, SN74ALVTH16244 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCES070G – JUNE 1996 – REVISED MAY 1999

查询"74ALVTH16244VRE4"供应商

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- 5-V I/O Compatible
- High Drive Capability (–32 mA/64 mA)
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Auto3-State Eliminates Bus Current Loading When Voltage at the Output Exceeds V_{CC}
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package

NOTE: For tape and reel order entry:
The DGG package is abbreviated to GR, and
the DGV package is abbreviated to VR.

description

The 'ALVTH16244 devices are 16-bit buffers/line drivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

SN54ALVTH16244 . . . WD PACKAGE
SN74ALVTH16244 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1OE	1	48	2OE
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE



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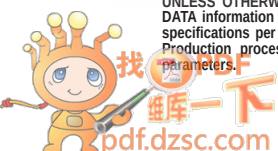
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**TEXAS
INSTRUMENTS**

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SN54ALVTH16244, SN74ALVTH16244
2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCES099C JUNE 1996 (REVISED) 16-BIT 3-STATE BUFFERS/DRIVERS 供应商

description (continued)

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

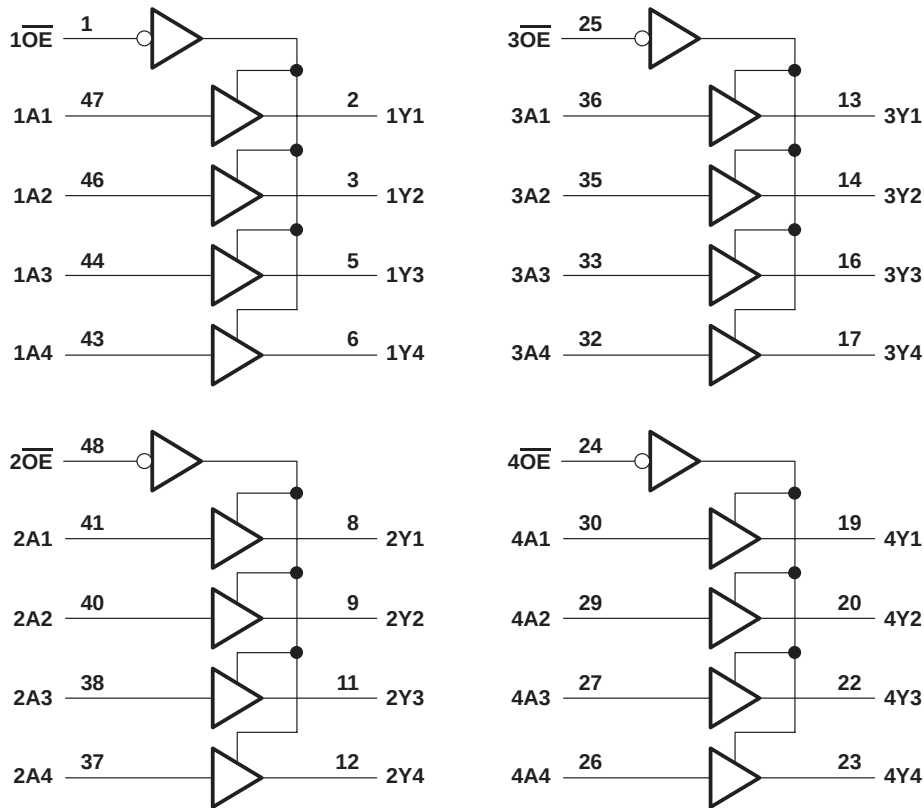
These devices are fully specified for hot-insertion applications using I_{OFF} and power-up 3-state. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54ALVTH16244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALVTH16244 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



SN54ALVTH16244, SN74ALVTH16244

2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCES099, JUNE 1998 (REVISED MARCH 1999)
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recommended operating conditions, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Note 3)

			SN54ALVTH16244		SN74ALVTH16244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		3	3.6	3	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	5.5	0	5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$			48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		$\mu\text{s/V}$
T_A	Operating free-air temperature		−55	125	−40	85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALVTH16244			SN74ALVTH16244			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}		$V_{CC} = 2.3 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.3 \text{ V}$, $I_{OH} = -6 \text{ mA}$	1.8						
		$V_{CC} = 2.3 \text{ V}$, $I_{OH} = -8 \text{ mA}$				1.8			
V_{OL}		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $I_{OL} = 100 \mu\text{A}$			0.2			0.2	V
		$V_{CC} = 2.3 \text{ V}$			0.4				
								0.4	
					0.5				
								0.5	
I_I	Control inputs	$V_{CC} = 2.7 \text{ V}$, $V_I = V_{CC} \text{ or GND}$			± 1			± 1	μA
		$V_{CC} = 0 \text{ or } 2.7 \text{ V}$, $V_I = 5.5 \text{ V}$			10			10	
	Data inputs	$V_{CC} = 2.7 \text{ V}$, $V_I = V_{CC}$			1			1	
		$V_{CC} = 2.7 \text{ V}$, $V_I = 0$			-5			-5	
I_{off}		$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_{I(hold)}$	Data inputs	$V_{CC} = 2.3 \text{ V}$, $V_I = 0.7 \text{ V}$			115			115	μA
		$V_{CC} = 2.3 \text{ V}$, $V_I = 1.7 \text{ V}$			-10			-10	
		$V_{CC} = 2.7 \text{ V}^\ddagger$, $V_I = 0 \text{ to } 2.7 \text{ V}$			± 300			± 300	
$I_{EX}^\S$		$V_{CC} = 2.3 \text{ V}$, $V_O = 5.5 \text{ V}$			125			125	μA
$I_{OZ(PU/PD)}^\P$		$V_{CC} \leq 1.2 \text{ V}$, $V_O = 0.5 \text{ V to } V_{CC}$, $V_I = \text{GND or } V_{CC}$, $\overline{OE} = \text{don't care}$			± 100			± 100	μA
I_{OZH}		$V_{CC} = 2.7 \text{ V}$, $V_O = 2.3 \text{ V}$, $V_I = 0.7 \text{ V or } 1.7 \text{ V}$			5			5	μA
I_{OZL}		$V_{CC} = 2.7 \text{ V}$, $V_O = 0.5 \text{ V}$, $V_I = 0.7 \text{ V or } 1.7 \text{ V}$			-5			-5	μA
I_{CC}		$V_{CC} = 2.7 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$			0.04	0.1		0.04	mA
					2.3	4.5		2.3	
					0.04	0.1		0.04	
C_i		$V_{CC} = 2.5 \text{ V}$, $V_I = 2.5 \text{ V or } 0$			3			3	pF
C_o		$V_{CC} = 2.5 \text{ V}$, $V_O = 2.5 \text{ V or } 0$			6			6	pF

[†] All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] Current into an output in the high state when $V_O > V_{CC}$

[¶] High-impedance state during power up/power down

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2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16244			SN74ALVTH16244			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}		V _{CC} = 3 V, I _I = −18 mA		−1.2			−1.2			V	
V _{OH}		V _{CC} = 3 V to 3.6 V, I _{OH} = −100 μA		V _{CC} −0.2			V _{CC} −0.2			V	
		V _{CC} = 3 V	I _{OH} = −24 mA	2							
			I _{OH} = −32 mA				2				
V _{OL}		V _{CC} = 3 V to 3.6 V, I _{OL} = 100 μA		0.2			0.2			V	
		V _{CC} = 3 V	I _{OL} = 16 mA				0.4				
			I _{OL} = 24 mA	0.5							
			I _{OL} = 32 mA				0.5				
			I _{OL} = 48 mA	0.55							
			I _{OL} = 64 mA				0.55				
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1			±1			μA	
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10			10				
	Data inputs	V _{CC} = 3.6 V	V _I = 5.5 V		20			20			
			V _I = V _{CC}		1			1			
			V _I = 0		−5			−5			
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100			μA	
I _I (hold)	Data inputs	V _{CC} = 3 V	V _I = 0.8 V		75			75			μA
			V _I = 2 V		−75			−75			
		V _{CC} = 3.6 V‡, V _I = 0 to 3.6 V		±500			±500				
I _{EX} §		V _{CC} = 3 V, V _O = 5.5 V		125			125			μA	
I _{OZ} (PU/PD)¶		V _{CC} ≤ 1.2 V, V _O = 0.5 V to V _{CC} , V _I = GND or V _{CC} , $\overline{OE}$ = don't care		±100			±100			μA	
I _{OZH}		V _{CC} = 3.6 V	V _O = 3 V, V _I = 0.8 V or 2 V	5			5			μA	
I _{OZL}		V _{CC} = 3.6 V	V _O = 0.5 V, V _I = 0.8 V or 2 V	−5			−5			μA	
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		0.07	0.1	0.07		0.1	mA	
			Outputs low		3.2	5	3.2		5		
			Outputs disabled		0.07	0.1	0.07		0.1		
ΔI _{CC} #		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.4			0.4			mA	
C _i		V _{CC} = 3.3 V, V _I = 3.3 V or 0		3			3			pF	
C _O		V _{CC} = 3.3 V, V _O = 3.3 V or 0		6			6			pF	

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] Current into an output in the high state when $V_O > V_{CC}$

[¶] High-impedance state during power up/power down

[#] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16244		SN74ALVTH16244		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3.1	1	3	ns
t_{PHL}			1	3.6	1	3.5	
t_{PZH}	$\overline{OE}$	Y	1.1	6	1.1	5.9	ns
t_{PZL}			1.1	4.8	1.1	4.7	
t_{PHZ}	$\overline{OE}$	Y	1.5	4.5	1.5	4.4	ns
t_{PLZ}			1	3.5	1	3.4	

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16244		SN74ALVTH16244		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.6	1	2.4	ns
t_{PHL}			1	2.6	1	2.5	
t_{PZH}	$\overline{OE}$	Y	1	3.9	1	3.8	ns
t_{PZL}			1	3	1	2.9	
t_{PHZ}	$\overline{OE}$	Y	1.5	4.3	1.5	4.2	ns
t_{PLZ}			1.5	3.7	1.5	3.6	

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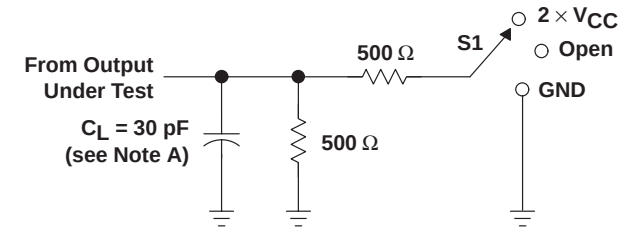
2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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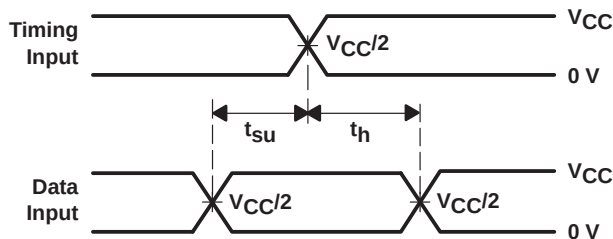
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

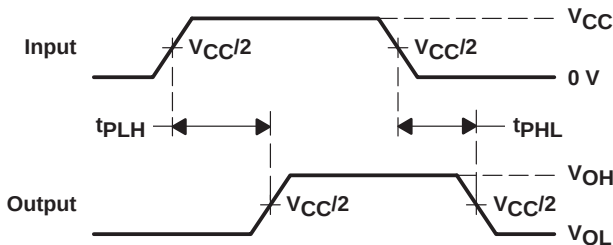


LOAD CIRCUIT

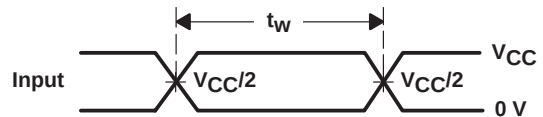
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



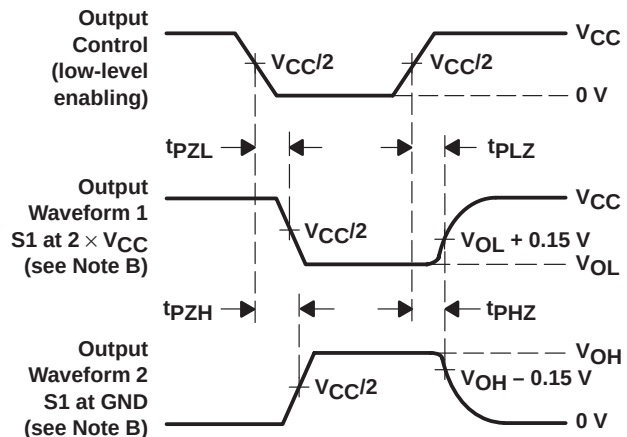
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



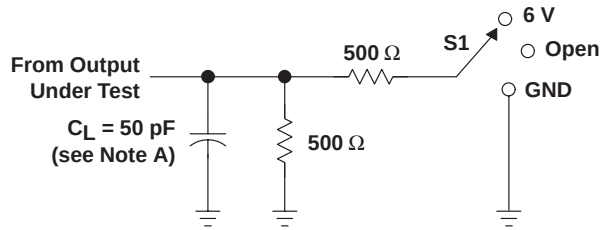
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

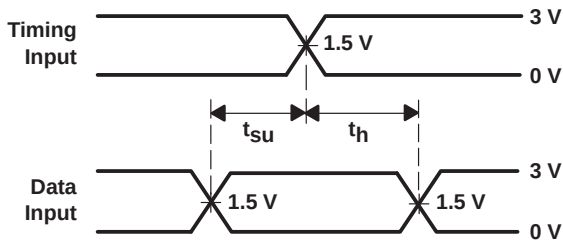
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$

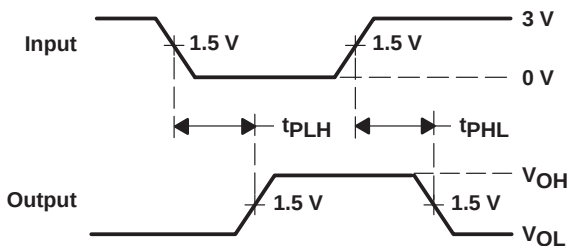


LOAD CIRCUIT

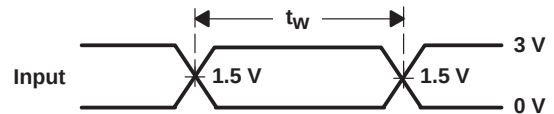
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



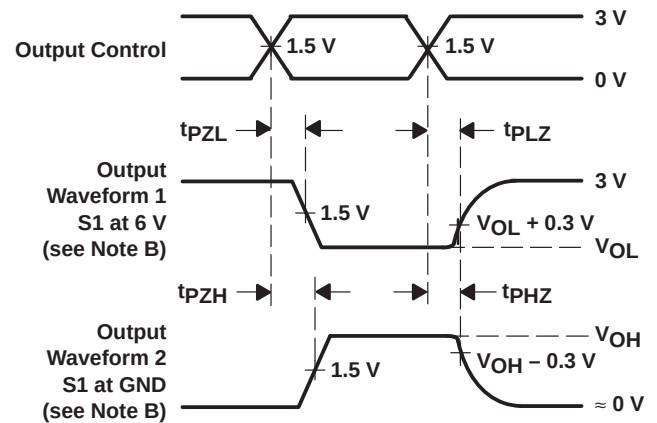
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVTH16244DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16244DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16244GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16244GRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16244VRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16244VRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16244ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74ALVTH16244DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16244DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16244GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16244KR	NRND	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74ALVTH16244VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

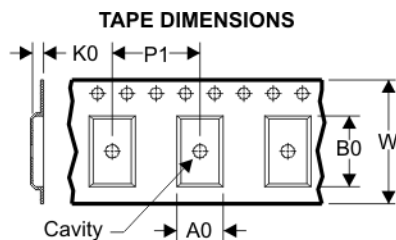
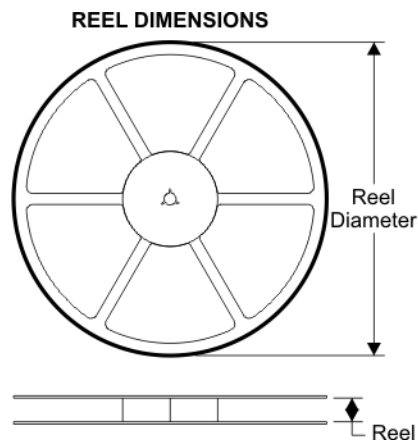
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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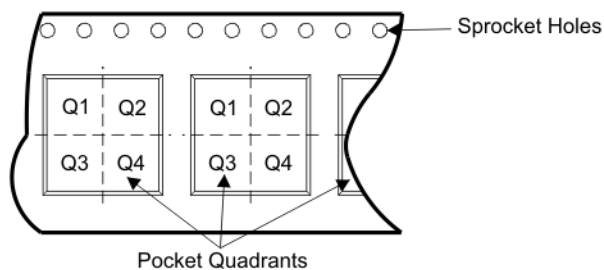
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TAPE AND REEL BOX INFORMATION



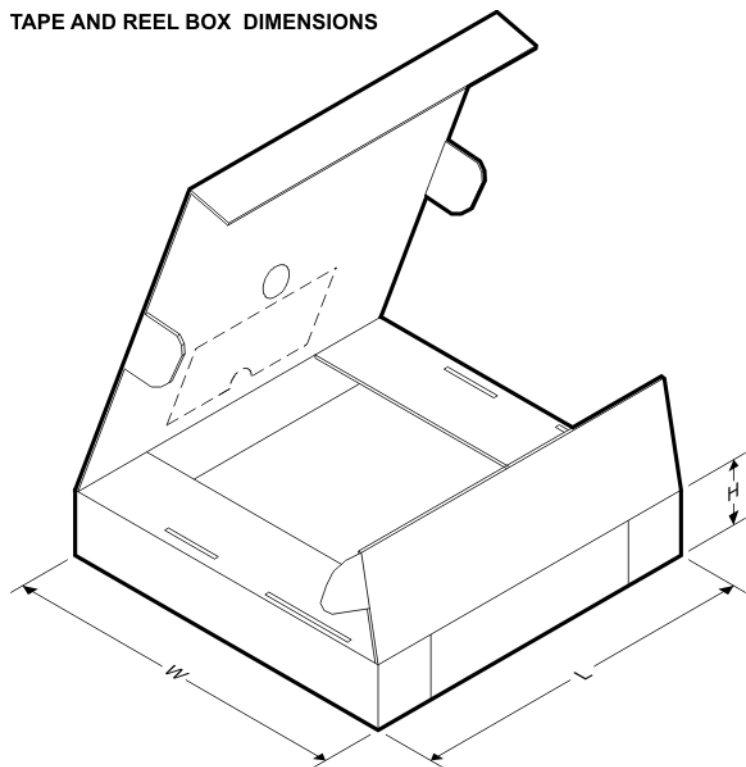
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ALVTH16244ZQLR	ZQL	56	SITE 32	330	16	4.8	7.3	1.45	8	16	Q1
SN74ALVTH16244DLR	DL	48	SITE 41	330	32	11.35	16.2	3.1	16	32	Q1
SN74ALVTH16244GR	DGG	48	SITE 41	330	24	8.6	15.8	1.8	12	24	Q1
SN74ALVTH16244KR	GQL	56	SITE 32	330	16	4.8	7.3	1.45	8	16	Q1
SN74ALVTH16244VR	DGV	48	SITE 41	330	24	6.8	10.1	1.6	12	24	Q1

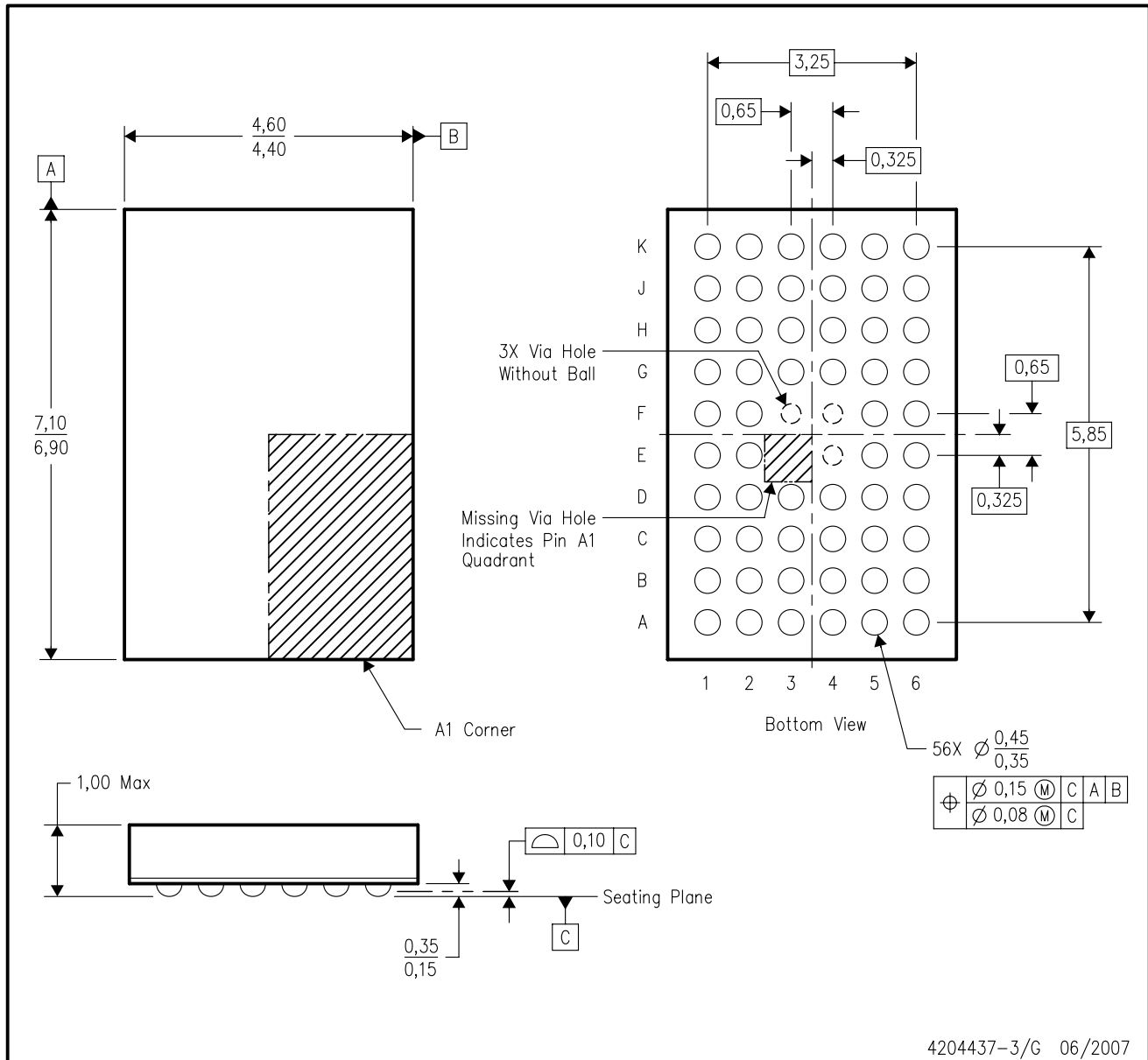
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
74ALVTH16244ZQLR	ZQL	56	SITE 32	346.0	346.0	0.0
SN74ALVTH16244DLR	DL	48	SITE 41	346.0	346.0	0.0
SN74ALVTH16244GR	DGG	48	SITE 41	346.0	346.0	0.0
SN74ALVTH16244KR	GQL	56	SITE 32	346.0	346.0	0.0
SN74ALVTH16244VR	DGV	48	SITE 41	346.0	346.0	0.0

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

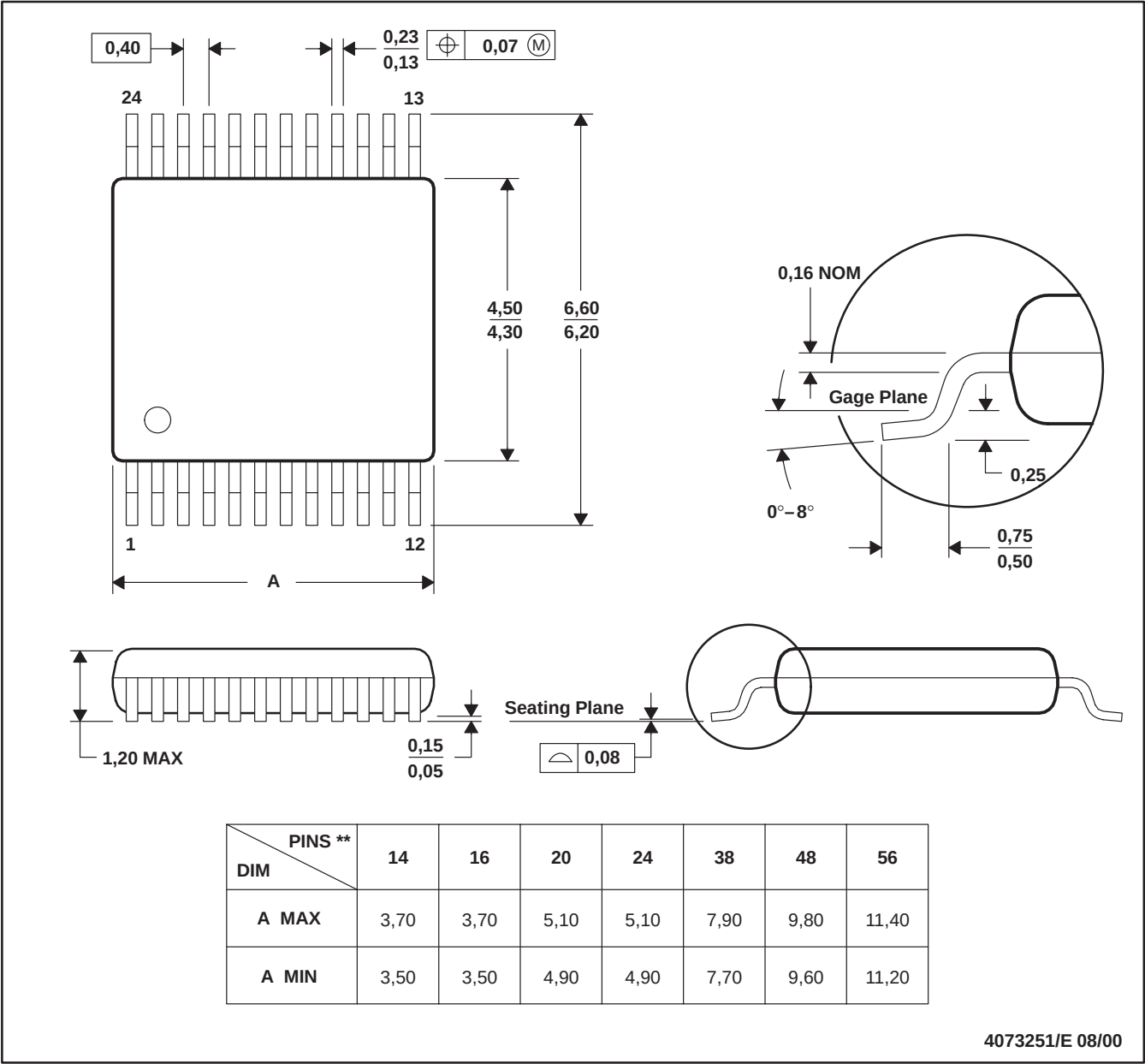


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

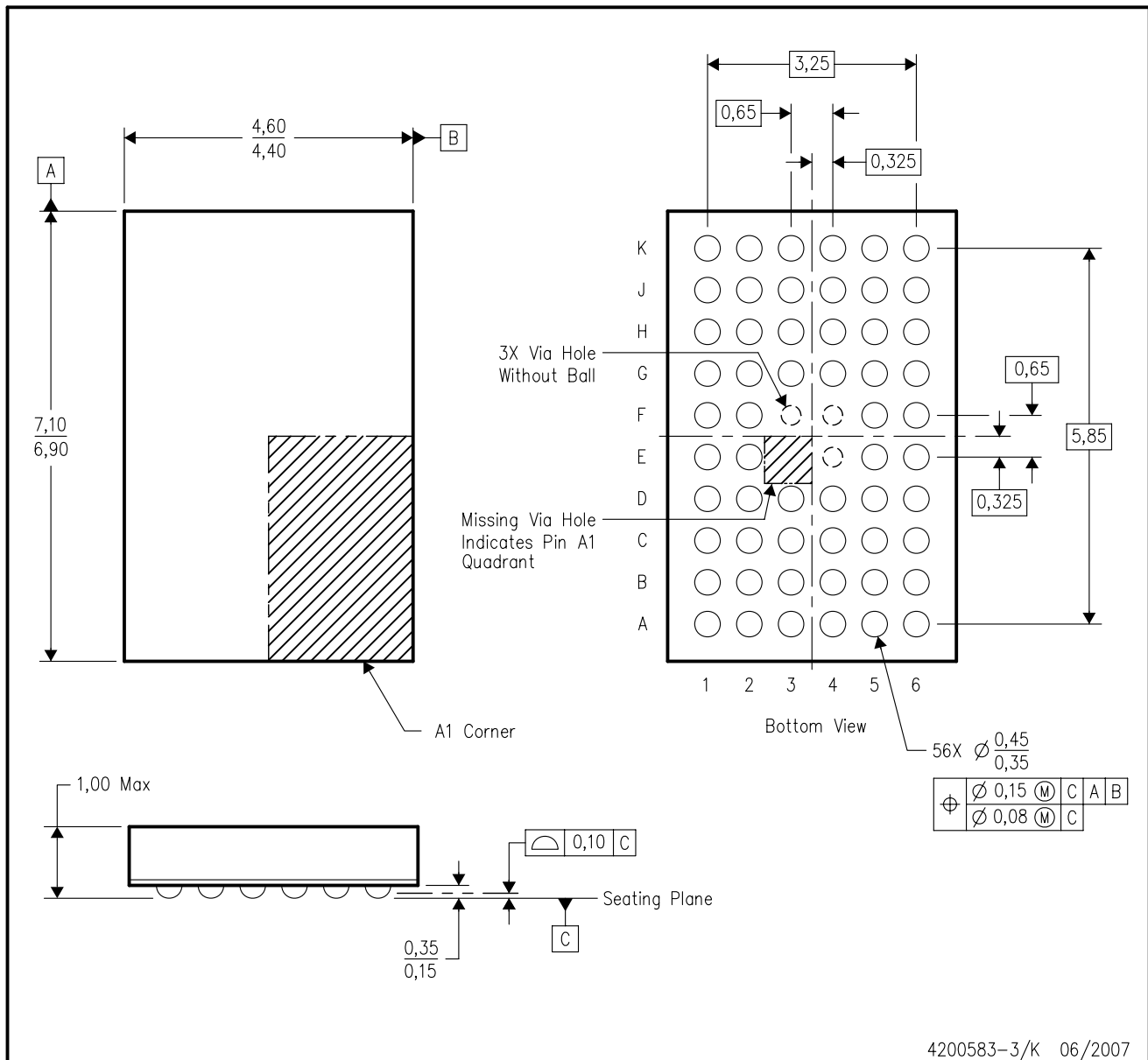
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

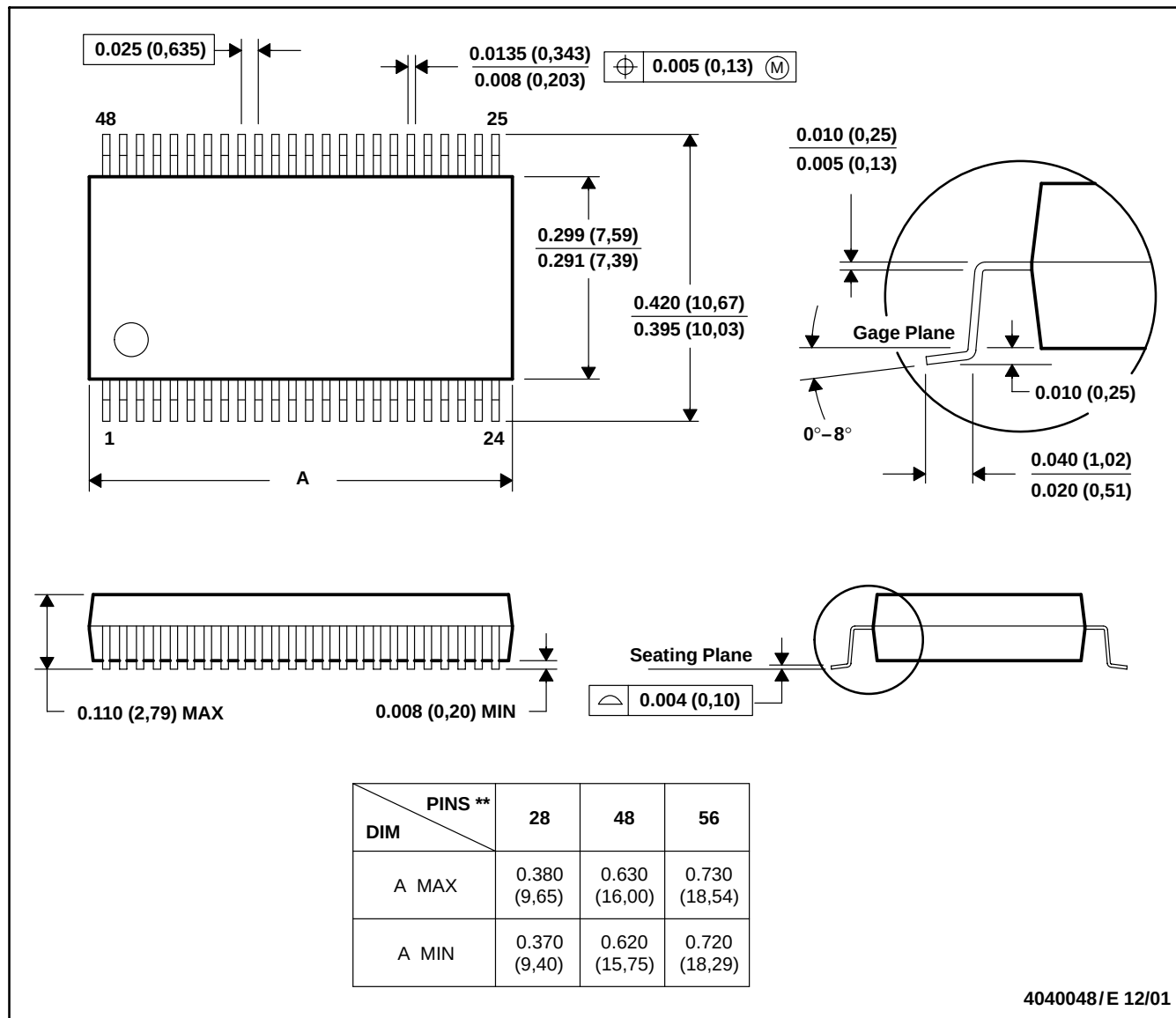


- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-285 variation BA-2.
 - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

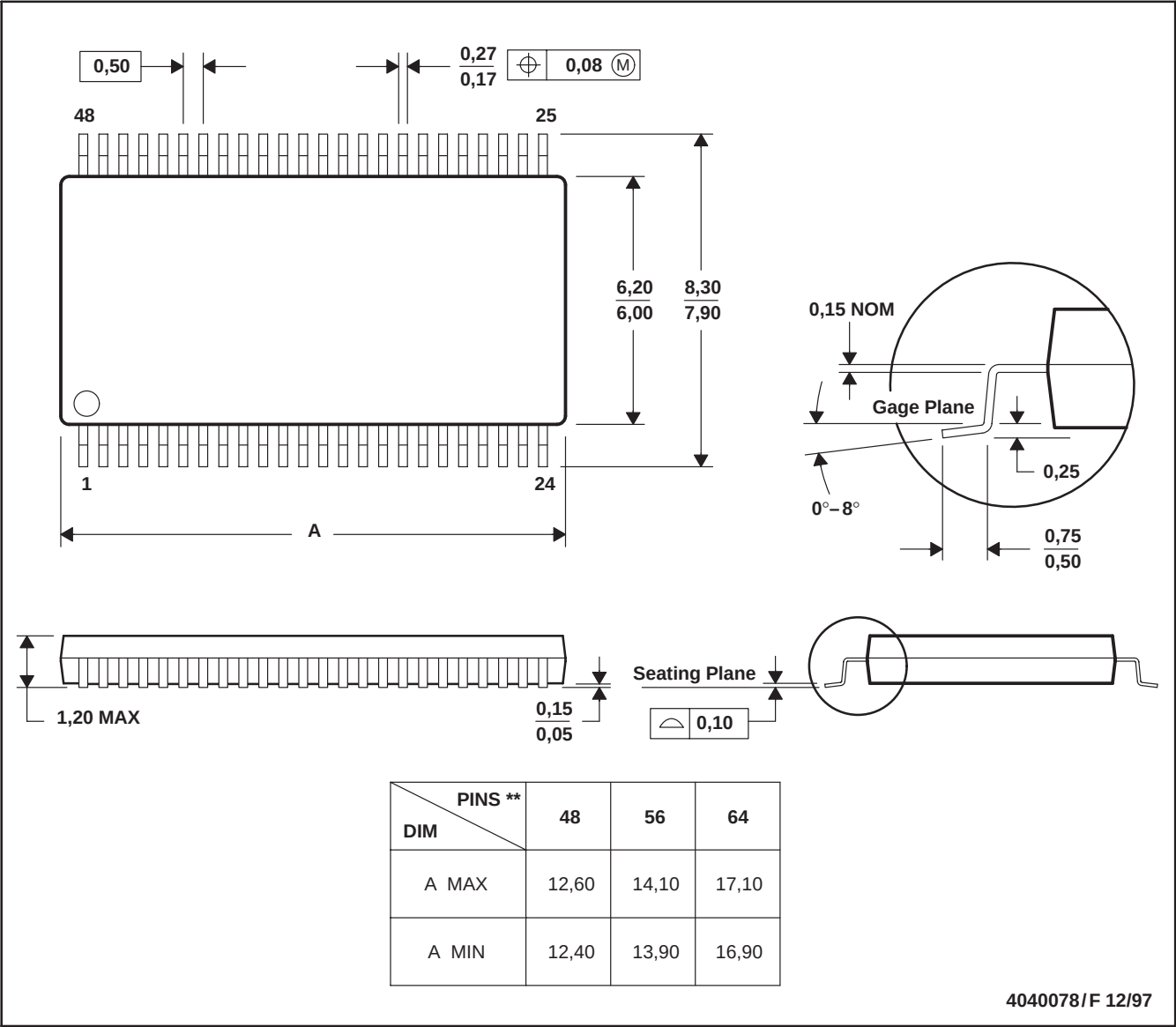
查询"74ALVTH16244VRE4"供应商

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DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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