

# 30 V, 2 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's e<sup>2</sup>PowerEdge family of low  $V_{CE(sat)}$  transistors are miniature surface mount devices featuring ultra low saturation voltage ( $V_{CE(sat)}$ ) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical application are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e<sup>2</sup>PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

## MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	-30	Vdc
Collector-Base Voltage	$V_{CBO}$	-50	Vdc
Emitter-Base Voltage	$V_{EBO}$	-5.0	Vdc
Collector Current - Continuous	$I_C$	-1.0	A
Collector Current - Peak	$I_{CM}$	-2.0	A

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$ (Note 1)	310	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (Note 1)	403	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$ (Note 2)	710	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (Note 2)	176	$^\circ\text{C}/\text{W}$
Total Device Dissipation (Single Pulse < 10 sec.)	$P_{D\text{single}}$ (Note 3)	575	mW
Junction and Storage Temperature Range	$T_J, T_{\text{stg}}$	-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

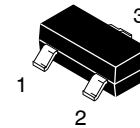
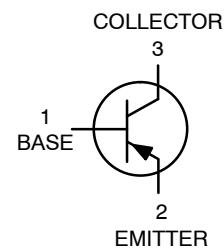
1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0 X 1.0 inch Pad.
3. Refer to Figure 8.



**ON Semiconductor**<sup>®</sup>

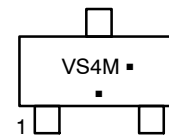
<http://onsemi.com>

**30 VOLTS**  
**2.0 AMPS**  
**PNP LOW  $V_{CE(sat)}$  TRANSISTOR**  
**EQUIVALENT  $R_{DS(on)}$  200 m $\Omega$**



**SOT-23 (TO-236)**  
**CASE 318**  
**STYLE 6**

## MARKING DIAGRAM



VS4 = Specific Device Code

M = Date Code\*

▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or overbar may vary depending upon manufacturing location.

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NSS30100LT1G	SOT-23 (Pb-Free)	3000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

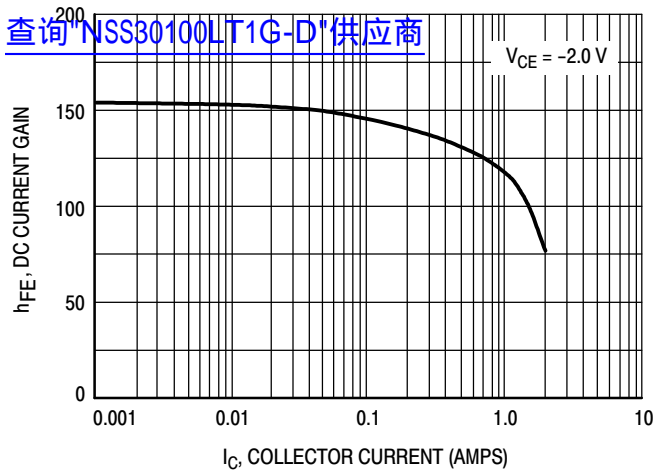
# NSS30100LT1G

## ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted)

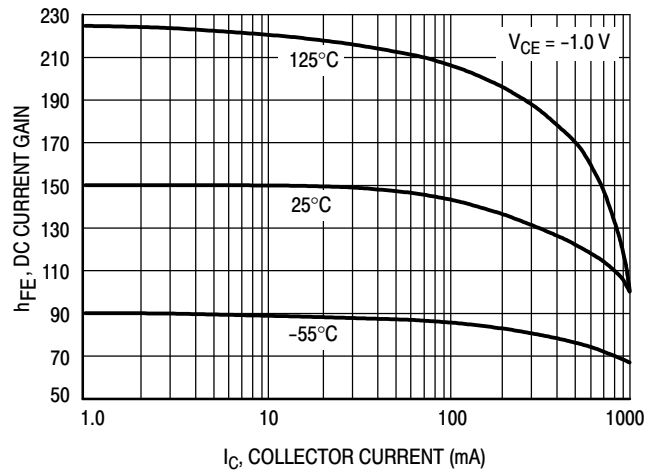
Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Breakdown Voltage ( $I_C = -10 \text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	-30	-	Vdc
Collector–Base Breakdown Voltage ( $I_C = -0.1 \text{ mA}$ , $I_E = 0$ )	$V_{(BR)CBO}$	-50	-	Vdc
Emitter–Base Breakdown Voltage ( $I_E = -0.1 \text{ mA}$ , $I_C = 0$ )	$V_{(BR)EBO}$	-5.0	-	Vdc
Collector Cutoff Current ( $V_{CB} = -30 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	-	-0.1	$\mu\text{A}$ dc
Collector–Emitter Cutoff Current ( $V_{CES} = -30 \text{ Vdc}$ )	$I_{CES}$	-	-0.1	$\mu\text{A}$ dc
Emitter Cutoff Current ( $V_{EB} = -4.0 \text{ Vdc}$ )	$I_{EBO}$	-	-0.1	$\mu\text{A}$ dc
<b>ON CHARACTERISTICS</b>				
DC Current Gain (Note 4) (Figure 1) ( $I_C = -1.0 \text{ mA}$ , $V_{CE} = -2.0 \text{ V}$ ) ( $I_C = -500 \text{ mA}$ , $V_{CE} = -2.0 \text{ V}$ ) ( $I_C = -1.0 \text{ A}$ , $V_{CE} = -2.0 \text{ V}$ ) ( $I_C = 2.0 \text{ A}$ , $V_{CE} = -2.0 \text{ V}$ )	$h_{FE}$	100 100 80 40	- 300 - -	
Collector–Emitter Saturation Voltage (Note 4) (Figure 3) ( $I_C = -0.5 \text{ A}$ , $I_B = -0.05 \text{ A}$ ) ( $I_C = -1.0 \text{ A}$ , $I_B = 0.1 \text{ A}$ ) ( $I_C = -2.0 \text{ A}$ , $I_B = -0.2 \text{ A}$ )	$V_{CE(sat)}$	- - -	-0.25 -0.30 -0.65	V
Base–Emitter Saturation Voltage (Note 4) (Figure 2) ( $I_C = -1.0 \text{ A}$ , $I_B = -0.1 \text{ A}$ )	$V_{BE(sat)}$	-	-1.2	V
Base–Emitter Turn–on Voltage (Note 4) ( $I_C = -1.0 \text{ A}$ , $V_{CE} = -2.0 \text{ V}$ )	$V_{BE(on)}$	-	-1.1	V
Cutoff Frequency ( $I_C = -100 \text{ mA}$ , $V_{CE} = -5.0 \text{ V}$ , $f = 100 \text{ MHz}$ )	$f_T$	100	-	MHz
Output Capacitance ( $f = 1.0 \text{ MHz}$ )	Cobo	-	15	pF

4. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle  $\leq$  2%.

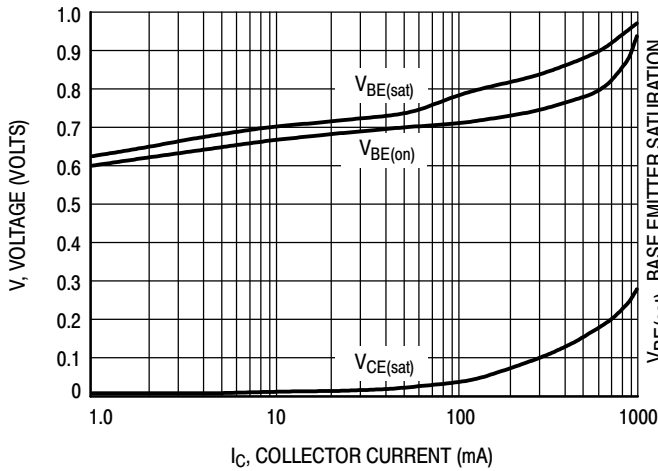
# NSS30100LT1G



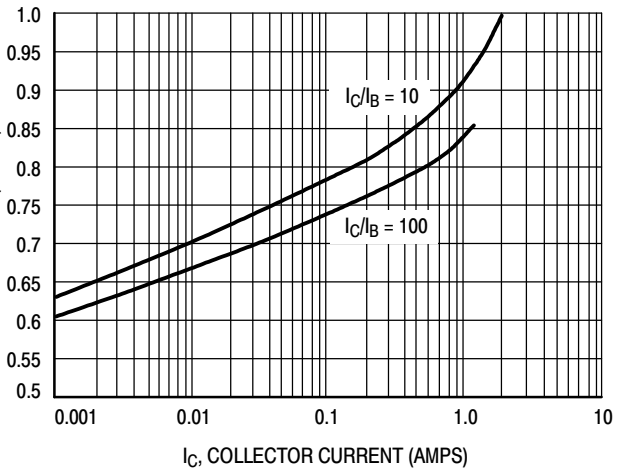
**Figure 1. DC Current Gain versus Collector Current**



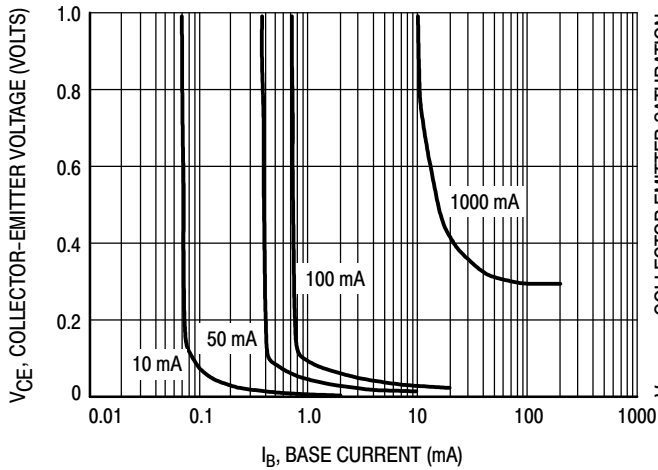
**Figure 2. DC Current Gain versus Collector Current**



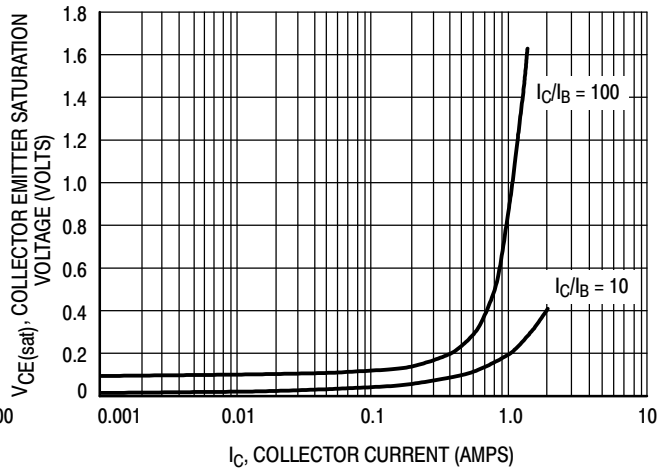
**Figure 3. "On" Voltages**



**Figure 4. Base Emitter Saturation Voltage versus Collector Current**



**Figure 5. Collector Emitter Saturation Voltage versus Collector Current**



**Figure 6. Collector Emitter Saturation Voltage versus Collector Current**

# NSS30100LT1G

[查询"NSS30100LT1G-D"供应商](#)

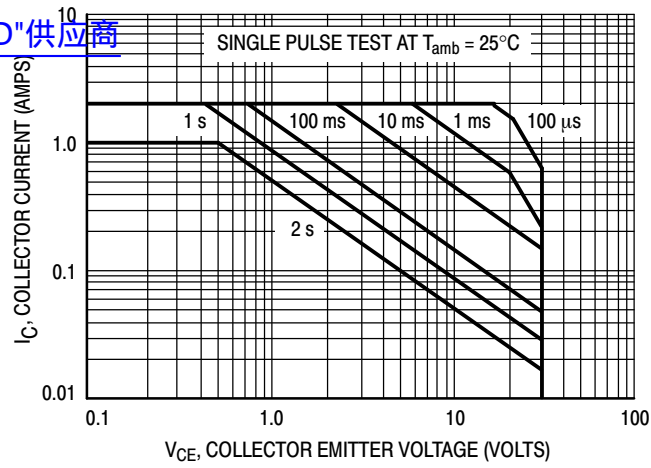


Figure 7. Safe Operating Area

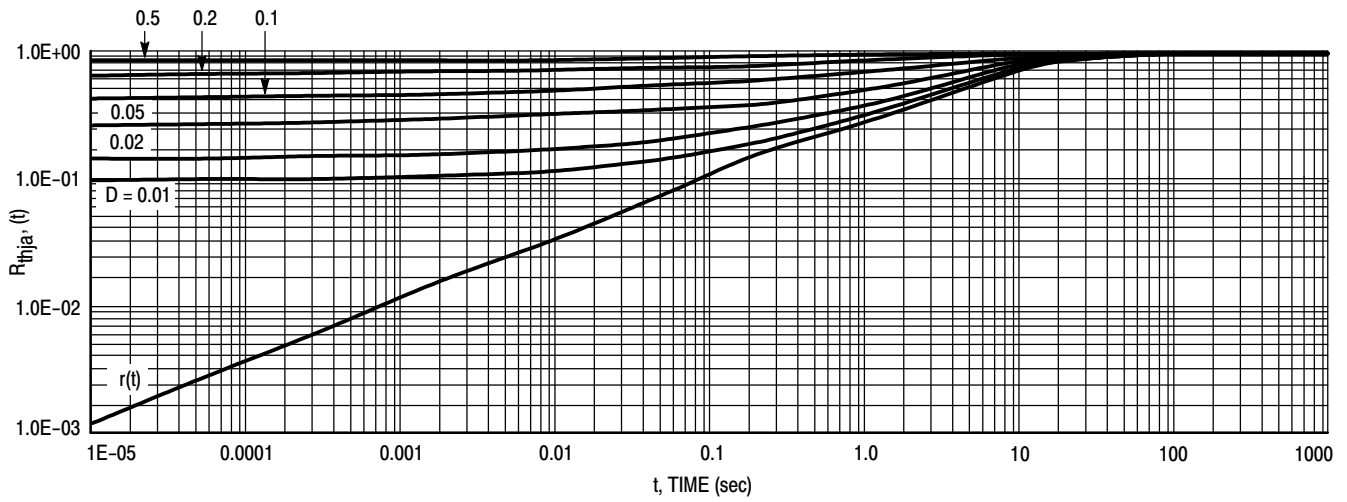


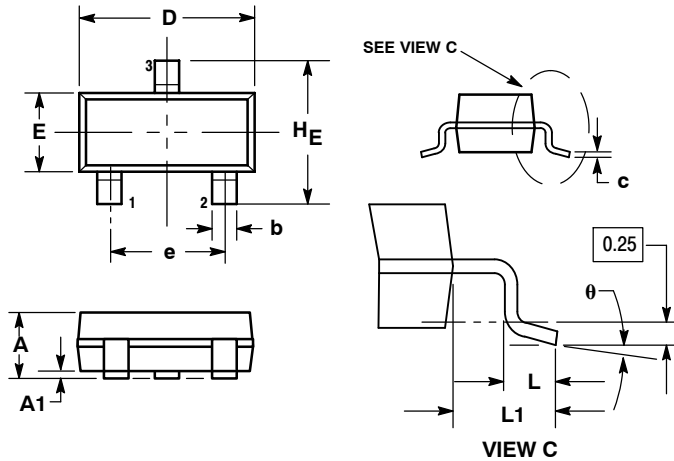
Figure 8. Normalized Thermal Response

# NSS30100LT1G

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## PACKAGE DIMENSIONS

SOT-23 (TO-236)  
CASE 318-08  
ISSUE AN

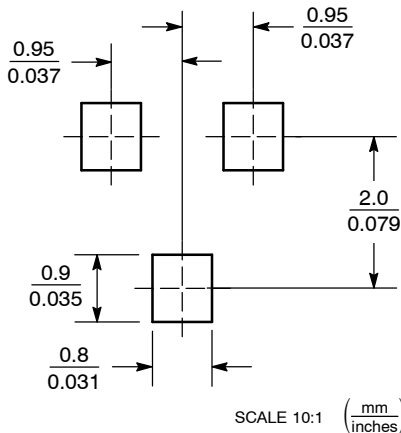


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
  4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:  
PIN 1: BASE  
2: EMITTER  
3: COLLECTOR

## SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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