December 2001

National Semiconductor

LM2722
High Speed Synchronous/Asynchronous MOSFET Driver

General Description

The LM2722, part of the LM2726 family, is designed to be used with multi-phase controllers. This part differs from the LM2726 by changing the functionality of the SYNC_EN pin from a whole chip enable to a low side MOSFET enable. As a result, the SYNC_EN pin now provides control between Synchronous and Asynchronous operations. Having this control can be advantageous in portable systems since Asynchronous operations can be more efficient at very light loads.

The LM2722 drives both top and bottom MOSFETs in a push-pull structure simultaneously. It takes a logic level PWM input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in cross-conduction protection circuitry prevents the top and bottom FETs from turning on simultaneously. The cross-conduction protection circuitry detects both the driver outputs and will not turn on a driver until the other driver output is low. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the LM2722 is typically 3A. In an SO-8 package, each driver is able to handle 50mA average current. Input UVLO (Under-Voltage-Lock-Out) forces both driver outputs low to ensure proper power-up and power-down operation. The gate drive bias voltage needed by the high side MOSFET is obtained through an external bootstrap. Minimum pulse width is as low as 55ns.

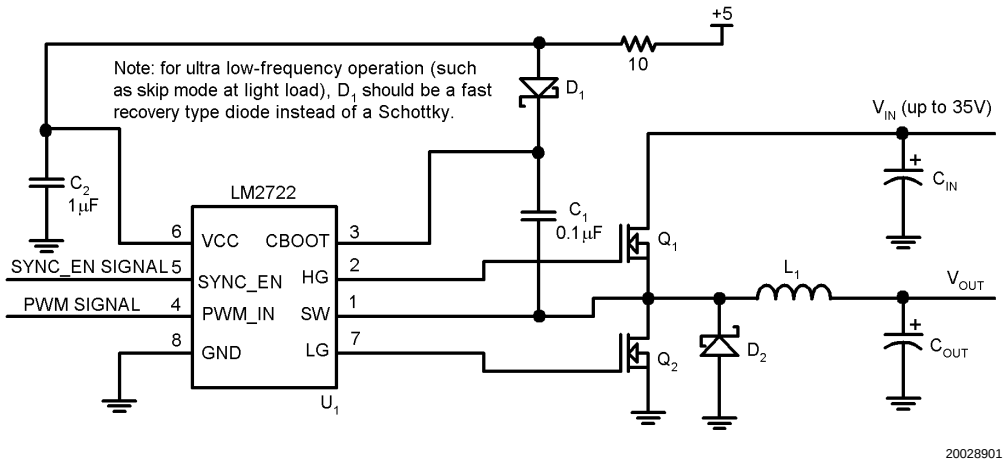
Features

- Synchronous or Asynchronous Operation
- Adaptive shoot-through protection
- Input Under-Voltage-Lock-Out
- Typical 20ns internal delay
- Plastic 8-pin SO package

Applications

- Driver for LM2723 Intel Mobile Northwood CPU core power supply.
- High Current DC/DC Power Supplies
- High Input Voltage Switching Regulators
- Fast Transient Microprocessors

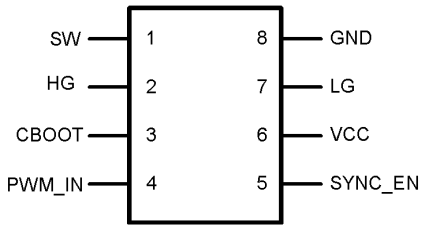
Typical Application



Note: National is an Intel Mobile Voltage Positioning (IMVP) licensee.

Connection Diagram

8-Lead Small Outline Package



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Top View

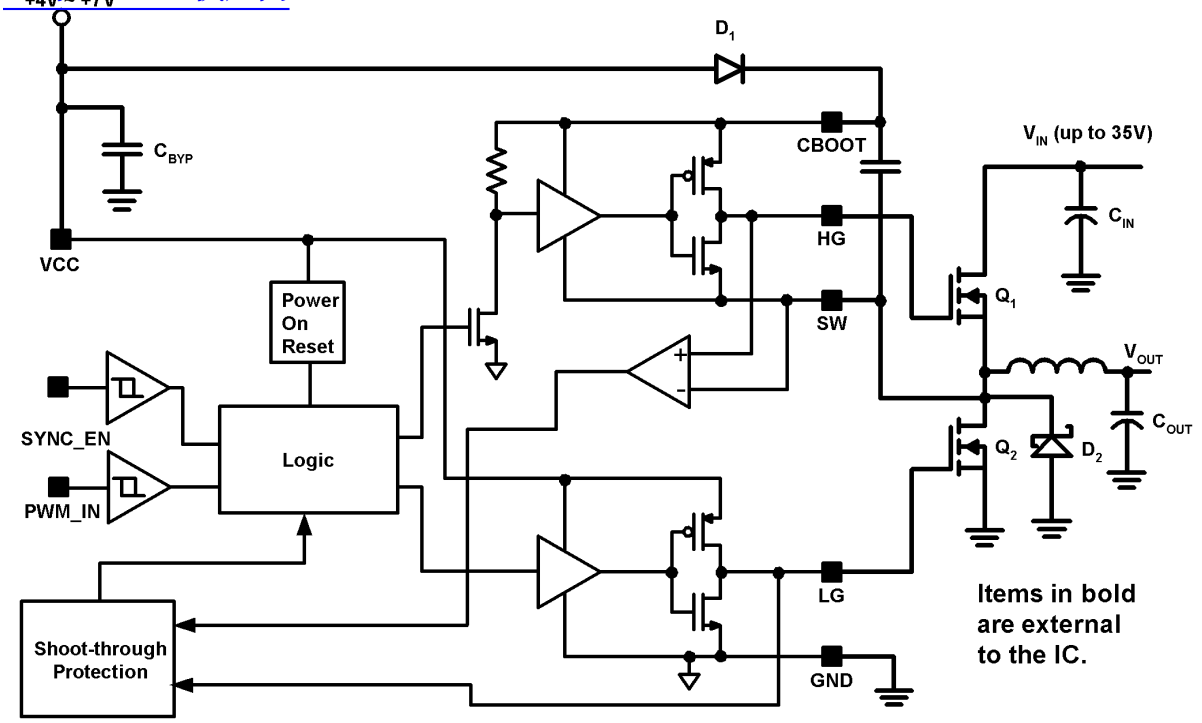
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2722	LM2722M	M08A	95 Units/Rail
	LM2722MX		2500 Units/Reel

Pin Description

Pin	Name	Function
1	SW	Top driver return. Should be connected to the common node of top and bottom FETs
2	HG	Top gate drive output
3	CBOOT	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver
4	PWM_IN	Accepts a 5V-logic control signal
5	SYNC_EN	Low gate Enable
6	VCC	Connect to +5V supply
7	LG	Bottom gate drive output
8	GND	Ground

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VCC	7.5V
CBOOT	42V
CBOOT to SW	8V
SW to PGND	36V
Junction Temperature	+150˚C
Power Dissipation (Note 2)	720mW
Storage Temperature	−65˚ to 150˚C
ESD Susceptibility	
Human Body Model (Note 3)	1kV
Soldering Time, Temperature	10sec., 300˚C

Operating Ratings (Note 1)

VCC	4V to 7V
Junction Temperature Range	−40˚ to 125˚C

Electrical Characteristics

VCC = CBOOT = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for T_A = T_J = +25˚C. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
POWER SUPPLY						
I_{q_op}	Operating Quiescent Current	PWM_IN = 0V		190	**300**	µA
TOP DRIVER						
	Peak Pull-Up Current	Test Circuit 1, V_{bias} = 5V, R = 0.1Ω		3.0		A
	Pull-Up Rds_on	I_{CBOOT} = I_{HG} = 0.7A		1.0		Ω
	Peak Pull-down Current	Test Circuit 2, V_{bias} = 5V, R = 0.1Ω		−3.2		A
	Pull-down Rds_on	I_{SW} = I_{HG} = 0.7A		0.5		Ω
t_4	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_6	Fall Time			12		ns
t_3	Pull-Up Dead Time	Timing Diagram		23		ns
t_5	Pull-Down Delay	Timing Diagram, from PWM_IN Falling Edge		27		ns
BOTTOM DRIVER						
	Peak Pull-Up Current	Test Circuit 3, V_{bias} = 5V, R = 0.1Ω		3.2		A
	Pull-up Rds_on	I_{VCC} = I_{LG} = 0.7A		1.0		Ω
	Peak Pull-down Current	Test Circuit 4, V_{bias} = 5V, R = 0.1Ω		3.2		A
	Pull-down Rds_on	I_{GND} = I_{LG} = 0.7A		0.5		Ω
t_8	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_2	Fall Time			14		ns
t_7	Pull-up Dead Time	Timing Diagram		28		ns
t_1	Pull-down Delay	Timing Diagram, from PWM_IN Rising Edge		13		ns
LOGIC						
V_{uvlo_up}	Power On Threshold	VCC rises from 0V toward 5V	**4**	3.7		V
V_{uvlo_dn}	Under-Voltage-Lock-Out Threshold			3.0	**2.5**	V
V_{uvlo_hys}	Under-Voltage-Lock-Out Hysteresis			0.7		V
V_{IH_EN}	SYNC_EN Pin High Input		**2.4**			V
V_{IL_EN}	SYNC_EN Pin Low Input				**0.8**	V

Electrical Characteristics (Continued)

VCC = EN = 5V, SYNC_EN = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for T_A = T_J = +25˚C. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{leak_EN}	SYNC_EN Pin Leakage Current	EN = 5V	**−2**		**2**	µA
		EN = 0V	**−2**		**2**	
t_{on_min}	Minimum Positive Input Pulse Width (Note 4)			55		ns
t_{off_min}	Minimum Negative Input Pulse Width (Note 5)			55		
V_{IH_PWM}	PWM_IN High Level Input Voltage	When PWM_IN pin goes high from 0V	**2.4**			V
V_{IL_PWM}	PWM_IN Low Level Input Voltage	When PWM_IN pin goes low from 5V			**0.8**	

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. Operating Ratings do not imply guaranteed performance limits.

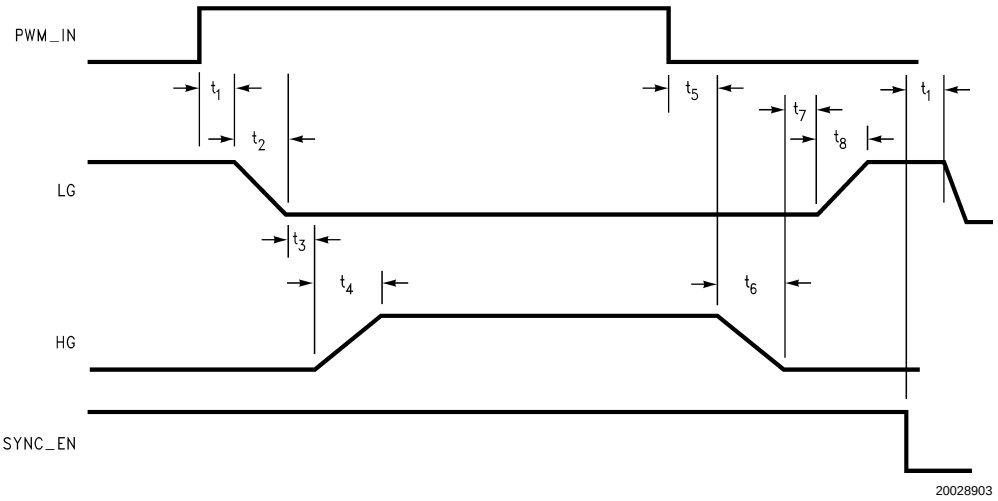
Note 2: Maximum allowable power dissipation is a function of the maximum junction temperature, T_{JMAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{MAX} = (T_{JMAX}-T_A) / \theta_{JA}$. The junction-to-ambient thermal resistance, θ_{JA}, for the LM2722, it is 172˚C/W. For a T_{JMAX} of 150˚C and T_A of 25˚C, the maximum allowable power dissipation is 0.7W.

Note 3: ESD machine model susceptibility is 100V.

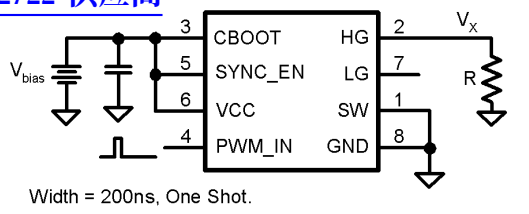
Note 4: If after a rising edge, a falling edge occurs sooner than the specified value, the IC may intermittently fail to turn on the bottom gate when the top gate is off. As the falling edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.

Note 5: If after a falling edge, a rising edge occurs sooner than the specified value, the IC may intermittently fail to turn on the top gate when the bottom gate is off. As the rising edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.

Timing Diagram



Test Circuits



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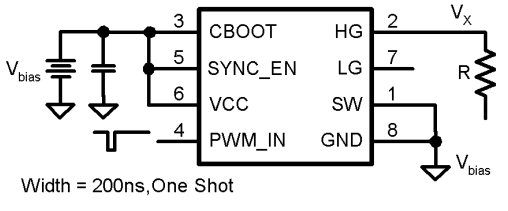
Test Circuit 1



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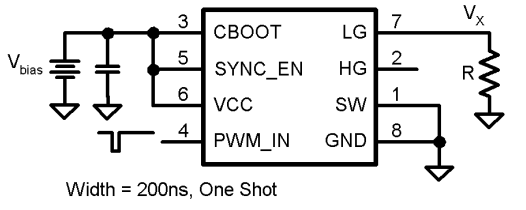
Test Circuit 2



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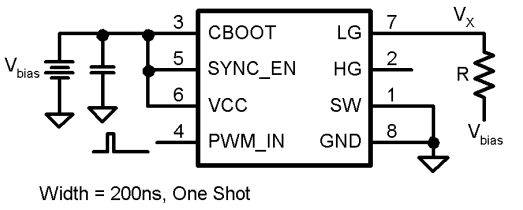
Test Circuit 3



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Test Circuit 4

$$I_{pull\_up} = \frac{V_x}{R}$$

$$I_{pull\_down} = \frac{V_{bias} - V_x}{R}$$

$$R_{ds\_pull\_up} = \frac{V_{bias} - V_x}{V_x} \cdot R$$

$$R_{ds\_pull\_down} = \frac{V_{bias} - V_x}{V_x} \cdot R$$

Typical Waveforms

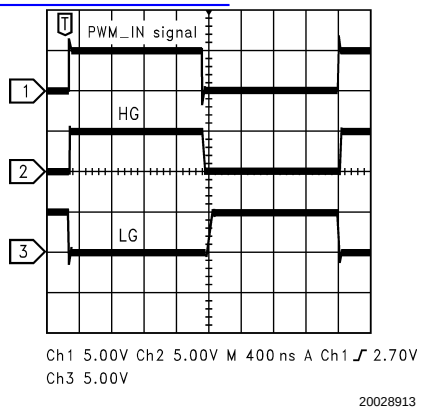


FIGURE 1. Switching Waveforms of Test Circuit

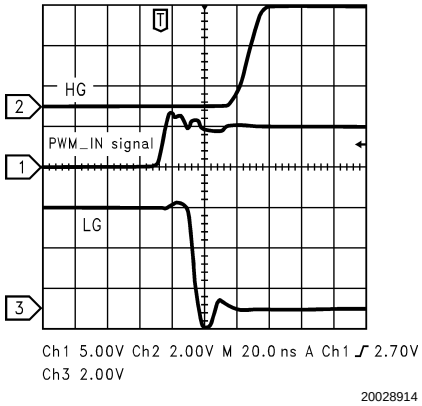


FIGURE 2. When Input Goes High

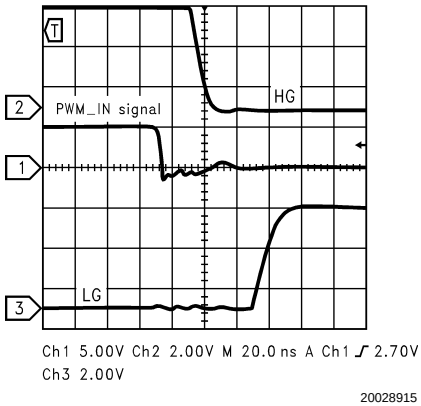


FIGURE 3. When Input Goes Low

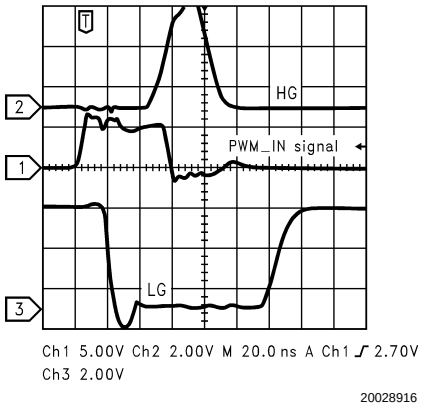


FIGURE 4. Minimum Positive Pulse

Application Information

Minimum Pulse Width

In order for the shoot-through prevention circuitry in the LM2722 to work properly, the pulses into the PWM_IN pin must be longer than 55ns. The internal logic waits until the first FET is off plus 20ns before turning on the opposite FET. If, after a falling edge, a rising edge occurs sooner than the specified time, t_{off_min}, the IC may intermittently fail to turn on the top gate when the bottom gate is off. As the rising edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output. This condition results in the PWM_IN pin in a high state and neither FET turned on. To get out of this state, the PWM_IN pin must see a low signal for greater than 55ns, before the rising edge.

This will also assure that the gate drive bias voltage has been restored by forcing the top FET source and C_{boot} to ground first. Then the internal circuitry is reset and normal operation will resume.

Conversely, if, after a rising edge, a falling edge occurs sooner than the specified miniumum pulse width, t_{on_min}, the IC may intermittently fail to turn on the bottom FET. As the falling edge occurs sooner and sooner, the driver will start to ignore the pulse and produce no output. This will result in the t_{off} inductor current taking a path through a diode provided for non-synchronous operation. The circuit will resume synchronous operation when the rising PWM pulses exceed 55ns in duration.

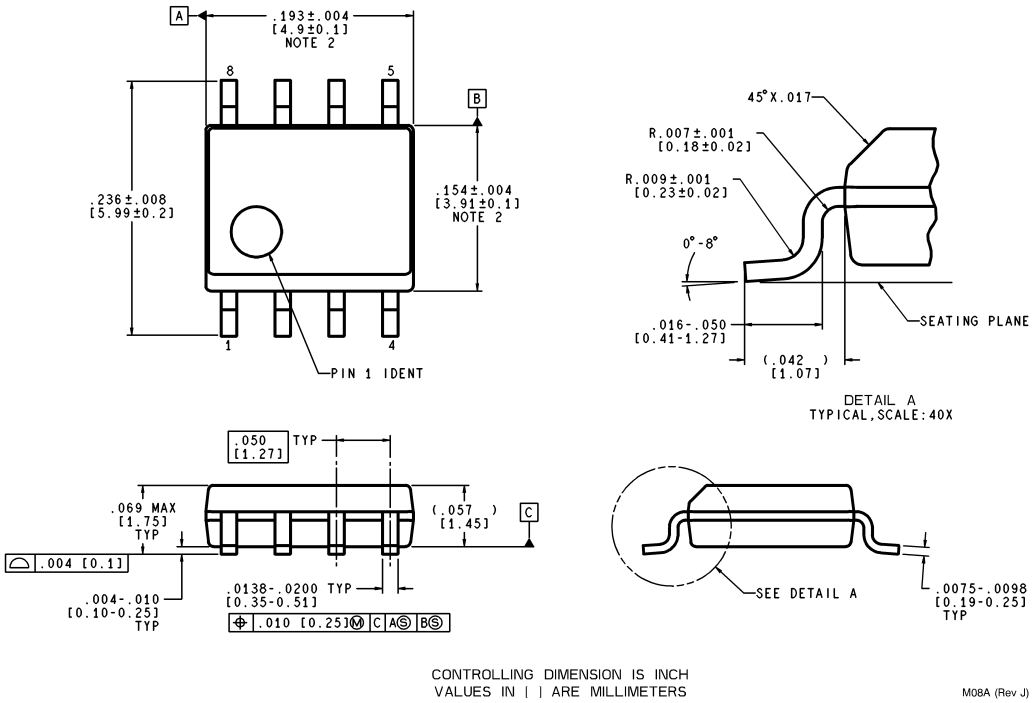
High Input Voltages or High Output Currents

At input voltages above twice the output voltage and at higher power levels, the designer may find snubber networks and gate drive limiting useful in reducing EMI and preventing injurious transients. A small resistor, 1Ω to 5Ω, between the driver outputs and the MOSFET gates will slightly increase the rise time and fall time of the output stage and reduce switching noise. The trade-off is 1% to 2% in efficiency.

A series R-C snubber across in parallel with the bottom FET can also be used to reduce ringing. Values of 10nF and 10Ω to 100Ω are a good starting point.

Physical Dimensions inches (millimeters)

Unless otherwise noted



8-Lead Small Outline Package
NS Package Number M08A

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