5V Automotive Regulator with Windowed Watchdog

Description

The EM6152 offers a high level of integration by combining voltage regulation, voltage monitoring and software monitoring using a windowed watchdog.

A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal voltage reference V_{REF}. The power-on reset function is initialized after V_{IN} reaches V_{REF} and takes the reset output inactive after a delay T_{POR} depending on external resistance R_{OSC}. The reset output goes active low when the V_{IN} voltage is less than V_{REF}. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a regulated output voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution.

If software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. For enhanced security, the watchdog must be serviced within an "open" time window. During the remaining time, the watchdog time window is "closed" and a reset will occur should a $\overline{TCL}$ pulse be received by the watchdog during this "closed" time window. The ratio of the open/closed window is either 33%/67% or 67%/33%.

The system ENABLE output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

When the microcontroller goes in stand-by mode or stops working, no signal is received on the $\overline{TCL}$ input of the EM6152 (version 55) and it goes into a stand-by mode in order to save power (CAN-bus sleep detector).

In EM6152, the voltage regulator has a low dropout voltage and a low quiescent current of 135 µA. The quiescent current increases only slightly in dropout prolonging battery life. Built-in protection includes a positive transient absorber for up to 45 V (load dump) and the ability to survive an unregulated input voltage of -42 V (reverse battery). The input may be connected to ground or to a reverse voltage without reverse current flowing from the output to the input.

Features

- ❑ Low quiescent current 135 µA
- ❑ -40°C to +125°C temperature range
- ❑ Highly accurate 5 V, 400 mA guaranteed output (actual maximum current depends on power dissipation)
- ❑ Low dropout voltage, typically 250 mV at 250 mA
- ❑ Unregulated DC input can withstand -42 V reverse battery and +45 V power transients
- ❑ Fully operational for unregulated DC input voltage up to 40 V and regulated output voltage down to 3.0 V
- ❑ No reverse output current
- ❑ Very low temperature coefficient for the regulated output
- ❑ Current limiting
- ❑ Windowed watchdog with an adjustable time windows, guaranteeing a minimum time and a maximum time between software clearing of the watchdog
- ❑ Time base accuracy ±8% (at 100ms)
- ❑ Sleep mode function (V55)
- ❑ Adjustable threshold voltage using external resistors
- ❑ Adjustable power on reset (POR) delay using one external resistor
- ❑ Open-drain active-low RESET output
- ❑ Reset output guaranteed for regulated output voltage down to 1.2 V
- ❑ System ENABLE output offers added security
- ❑ Qualified according to AEC-Q100
- ❑ Green SO-8 and PSOP2-16 packages (RoHS compliant)

Applications

- ❑ Automotive systems
- ❑ Industrial
- ❑ Home security systems
- ❑ Telecom / Networking
- ❑ Computers
- ❑ Set top boxes

Typical Operating Configuration

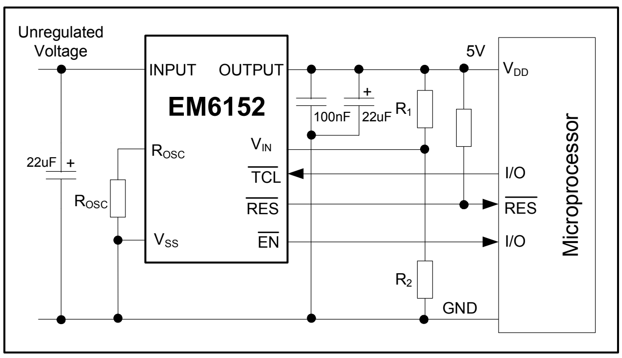


Fig. 1

Selection Table

Part Number	V_{REF}	Closed Window	Open Window	CAN-bus sleep detector
EM6152**V30**	1.17 V	67%	33%	No
EM6152**V50**	1.52 V	67%	33%	No
EM6152**V53**	1.52 V	33%	67%	No
EM6152**V55**	1.275 V	67%	33%	Yes

Please refer to Fig. 4 for more information about the open/closed window of the watchdog.

Ordering Information

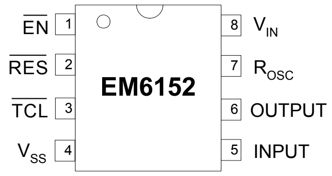
Part Number	Version	V_{REF}	Package	Delivery Form	Package Marking
EM6152V30SO8A+	V30	1.17 V	SO-8	Stick, 97 pcs	6152030
EM6152V30SO8B+				Tape & Reel, 2500 pcs	
EM6152V30PS16B+			PSOP2-16	Tape & Reel, 2500pcs	EM6152 030
EM6152V50SO8A+	V50	1.52 V	SO-8	Stick, 97 pcs	6152050
EM6152V50SO8B+				Tape & Reel, 2500 pcs	
EM6152V50PS16B+			PSOP2-16	Tape & Reel, 2500pcs	EM6152 050
EM6152V53SO8A+	V53	1.52V	SO-8	Stick, 97 pcs	6152053
EM6152V53SO8B+				Tape & Reel, 2500 pcs	
EM6152V53PS16B+			PSOP2-16	Tape & Reel, 2500pcs	EM6152 053
EM6152V55SO8A+	V55	1.275 V	SO-8	Stick, 97 pcs	6152055
EM6152V55SO8B+				Tape & Reel, 2500 pcs	

Note: the "+" symbol at the end of the part number means that this product is RoHS compliant (green).

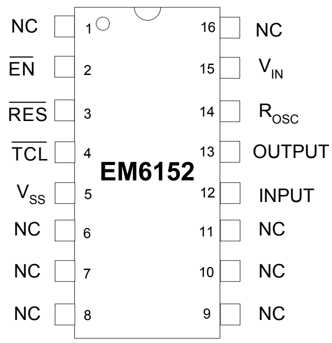
Pin Assignment and Description

SO8	PSOP2-16	Name	Function
1	2	$\overline{EN}$	Push-pull active low enable output
2	3	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{OUTPUT} even if unused
3	4	$\overline{TCL}$	Watchdog timer clear input signal
4	5	V_{SS}	GND terminal
5	12	INPUT	Voltage regulator input
6	13	OUTPUT	Voltage regulator output
7	14	R_{OSC}	R_{OSC} input for RC oscillator tuning
8	15	V_{IN}	Voltage comparator input
-	1, 6 to 11, 16	NC	No connect
-	Heat Sink Contact		Can be connected to Vss or left floating

SO8



PSOP2-16



Block Diagram EM6152

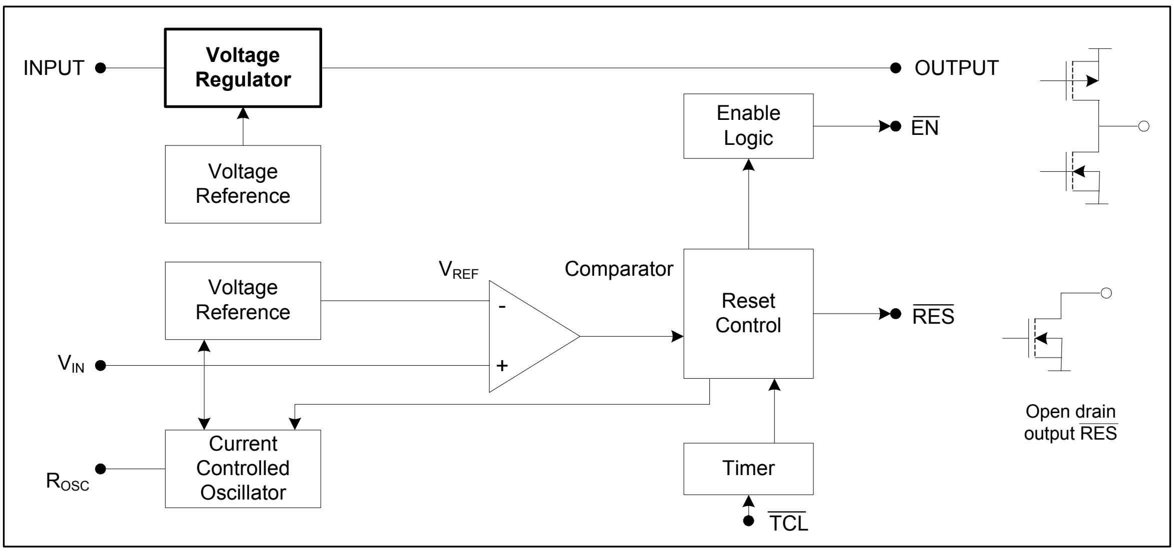


Fig. 3

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Continuous voltage at INPUT to V_{SS}	V_{INPUT}	-0.3 to +40V
Transients on INPUT for t < 100 ms and duty cycle 1%	V_{TRANS}	Up to +45V
Max. voltage at any signal pin	V_{MAX}	V_{OUTPUT} + 0.3V
Min. voltage at any signal pin	V_{MIN}	V_{SS} – 0.3V
Reverse supply voltage on INPUT	V_{REV}	-42V
Storage temperature	T_{STO}	-65 to +150 °C
ESD According to MIL-STD-883C method 3015.7	V_{Smax}	2000V

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Decoupling Methods

The input capacitor is necessary to compensate the line influences. A resistor of approx. 1 Ω connected in series with the input capacitor may be used to damp the oscillation of the input capacitor and input inductance. The ESR value of the capacitor plays a major role regarding the efficiency of the decoupling. It is recommended also to connect a ceramic capacitor (100 nF) directly at the IC's pins. In general the user must assure that pulses on the input line have slew rates lower than 1 V/µs. On the output side, the capacitor is necessary for the stability of the regulation circuit. The stability is guaranteed for values of 22 µF or greater. It is especially important to choose a capacitor with a low ESR value. Tantalum capacitors are recommended. See the notes related to Table 2. Special care must be taken in disturbed environments (automotive, proximity of motors and relays, etc.).

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, it is advised that normal precautions be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. At any time, all inputs must be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Operating junction temperature	T_j	-40	+125	°C
INPUT voltage (note 1)	V_{INPUT}	2.3	40	V
OUTPUT voltage (note 1, 2)	V_{OUTPUT}	1.2	5.5	V
$\overline{RES}$ and $\overline{EN}$ guaranteed (note 3)	V_{OUTPUT}	1.2		V
OUTPUT current (note 4)	I_{OUTPUT}		400	mA
Comparator input voltage	V_{IN}	0	V_{OUTPUT}	V
RC-oscillator programming	R_{OSC}	10	1000	kΩ
Package thermal resistance from junction to ambient : SO-8 PSOP2-16 150 MILS (note 5)	$R_{th(j-a)}$	 30	160 90	°C/W

Table 2

Note 1: full operation guaranteed. To achieve the load regulation specified in Table 3 a 22 µF capacitor or greater is required on the INPUT, see Fig. 1b. The 22 µF must have an effective resistance ≤ 5 Ω and a resonant frequency above 500 kHz.

Note 2: a 22 µF load capacitor and a 100 nF decoupling capacitor are required on the regulator OUTPUT for stability. The 22 µF must have an effective series resistance of ≤ 5 Ω and a resonant frequency above 500 kHz.

Note 3: $\overline{RES}$ must be pulled up externally to V_{OUTPUT} even if it is unused. ($\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test)

Note 4: the OUTPUT current will not apply to the full range of input voltage. Power dissipation that would require the EM6152 to work above the maximum junction temperature (+125°C) must be avoided.

Note 5: the thermal resistance specified assumes the package is soldered to a PCB. A typical value of 51°C/W has been obtained with a dual layer board, with the slug soldered to the heat-sink area of the PCB.

Electrical Characteristics

V_{INPUT} = 13.5 V, C_L = 22 µF + 100 nF, C_{INPUT} = 22 µF, T_j = -40 to +125°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode and sleep mode for V55	I_{SS}	R_{OSC} = don't care, TCL = V_{OUTPUT}, V_{IN} = 0 V, I_L = 1 mA		135	270	µA
Supply current (note1)	I_{SS}	R_{OSC} = 100 kΩ, I/P_S at V_{OUTPUT}, O/P_S 1 MΩ to V_{OUTPUT}, I_L = 1 mA		145	280	µA
Supply current (note 1)	I_{SS}	R_{OSC} = 100 kΩ, I/P_S at V_{OUTPUT}, O/P_S 1 MΩ to V_{OUTPUT}, I_L = 250 mA		7	14	mA
Output voltage	V_{OUTPUT}	5 mA ≤ I_L ≤ 250 mA	4.8	5	5.2	V
Line regulation (note 2)	V_{LINE}	12 V ≤ V_{INPUT} ≤ 32 V, I_L = 5 mA		10	25	mV
Load regulation (note 2)	V_L	5 mA ≤ I_L ≤ 250 mA, V_{INPUT}=6V		35	80	mV
Dropout voltage (note 3)	$V_{DROPOUT}$	I_L = 250 mA		250	500	mV
Output voltage temperature coefficient (note 4)	$V_{th(coeff)}$			0.5		mV/°C
Current limit	I_{Lmax}	OUTPUT tied to V_{SS}, V_{INPUT}=6V	400	600		mA
$\overline{\text{RES}}$ & $\overline{\text{EN}}$ Output Low Voltage	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 8 mA		0.25	0.45	V
		V_{OUTPUT} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
		V_{OUTPUT} = 1.2 V, I_{OL} = 0.5 mA		0.04	0.2	V
$\overline{\text{EN}}$ Output High Voltage	V_{OH}	V_{OUTPUT} = 4.5 V, I_{OH}= -1 mA	3.5	4.1		V
		V_{OUTPUT} = 2.0 V, I_{OH}= -100 µA	1.8	1.9		V
		V_{OUTPUT} = 1.2 V, I_{OH}= -20 µA	0.9	1.05		V
$\overline{\text{TCL}}$ Input Low Level	V_{IL}		V_{SS}		0.5	V
$\overline{\text{TCL}}$ Input High Level	V_{IH}		2.5		V_{OUTPUT}	V
Leakage current	I_{LI}	V_{SS} ≤ V_{TCL} ≤ V_{OUTPUT}		0.05		µA
Comparator reference (note 5, 6)	V_{REF}	Version V30 (replaces A6130)	1.135	1.170	1.205	V
		Version V50 (replaces A6150 and A6250)	1.475	1.520	1.565	V
		Version V53	1.475	1.520	1.565	V
		Version V55 (replaces A6155)	1.235	1.275	1.315	V
Comparator hysteresis (note 6)	V_{HY}			2		mV
V_{IN} input resistance	R_{VIN}			100		MΩ

Table 3

Note 1: if INPUT is connected to V_{SS}, no reverse current will flow from the OUTPUT to the INPUT, however the supply current specified will be sank by the OUTPUT to supply the EM6152.
Note 2: regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in OUTPUT voltage due to heating effects are covered in the specification for thermal regulation.
Note 3: the dropout voltage is defined as the INPUT to OUTPUT differential, measured with the input voltage equal to 5.0 V.
Note 4: output voltage temperature coefficient is defined as the change in OUTPUT voltage after a change in power dissipation is applied, excluding load or line regulation effects.
Note 5: the comparator and the voltage regulator have separate voltage references (see "Block Diagram" Fig. 3).
Note 6: the comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 5).

Timing Characteristics

V_{INPUT} = 13.5 V, I_L = 100 µA, C_L = 22 µF + 100 nF, C_{INPUT} = 22 µF, T_j = -40 to + 125 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delay $\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
V_{IN} sensitivity	T_{SEN}	V_{INhigh}=1.1xV_{REF}, V_{INlow}=0.9xV_{REF}	0.5	3	15	µs
Watchdog Reset Pulse Period	T_{WDRP}	$\overline{TCL}$ inactive	T_{CW} + T_{OW}+ T_{WDR}			ms
Version V30						
Power-on Reset delay	T_{POR}	R_{OSC}= 116.9 kΩ ±1%	91.6	100	108.3	
Closed Window Time	T_{CW}		74	80	85.76	
Open Window Time	T_{OW}		37	40	42.88	ms
Watchdog Time	T_{WD}		92.5	100	107.2	
Watchdog Reset Pulse Width if no $\overline{TCL}$	T_{WDR}		2.25	2.5	2.75	
Version V50						
Power-on Reset delay	T_{POR}	R_{OSC}= 121.6 kΩ ±1%	91.6	100	108.3	
Closed Window Time	T_{CW}		74	80	85.76	
Open Window Time	T_{OW}		37	40	42.88	ms
Watchdog Time	T_{WD}		92.5	100	107.2	
Watchdog Reset Pulse Width if no $\overline{TCL}$	T_{WDR}		2.25	2.5	2.75	
Version V53						
Power-on Reset delay	T_{POR}	R_{OSC} = 23.2 kΩ ±1%	4.57	5.0	5.44	
Closed Window Time	T_{CW}		9.24	10	10.77	
Open Window Time	T_{OW}		18.48	20	21.54	ms
Watchdog Time	T_{WD}		18.48	20	21.54	
Watchdog Reset Pulse Width if no $\overline{TCL}$	T_{WDR}		0.56	0.625	0.69	
Version V55						
Power-on Reset delay	T_{POR}	R_{OSC} = 107.5 kΩ ±1%	91.6	100	108.3	
Closed Window Time	T_{CW}		74	80	85.76	
Open Window Time	T_{OW}		37	40	42.88	
Watchdog Time	T_{WD}		92.5	100	107.2	ms
Watchdog Reset Pulse Width if no $\overline{TCL}$	T_{WDR}		2.25	2.5	2.75	
Watchdog Reset Pulse Width in Sleep Mode	T_{WDRS}	R_{OSC} off; R_{INT}=1MΩ	2.8	3.2	3.6	
Watchdog Reset Pulse Period in Sleep Mode	T_{WDRPS}	$\overline{TCL}$ inactive	750	1100	1450	

Table 4

For different values of T_{WD} and R_{OSC}, see figures 9 to 12.

Timing Waveforms

Watchdog Timeout Period

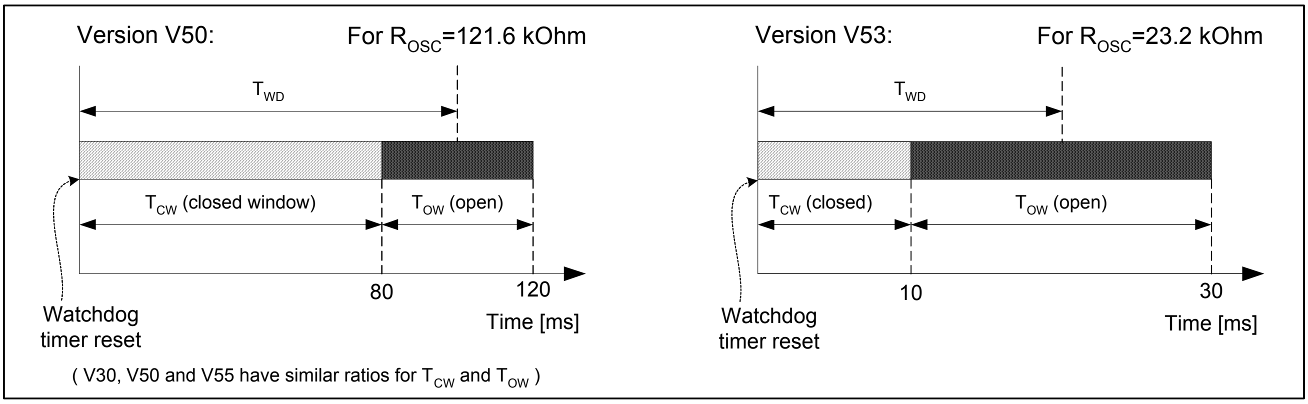


Fig. 4

Voltage Monitoring

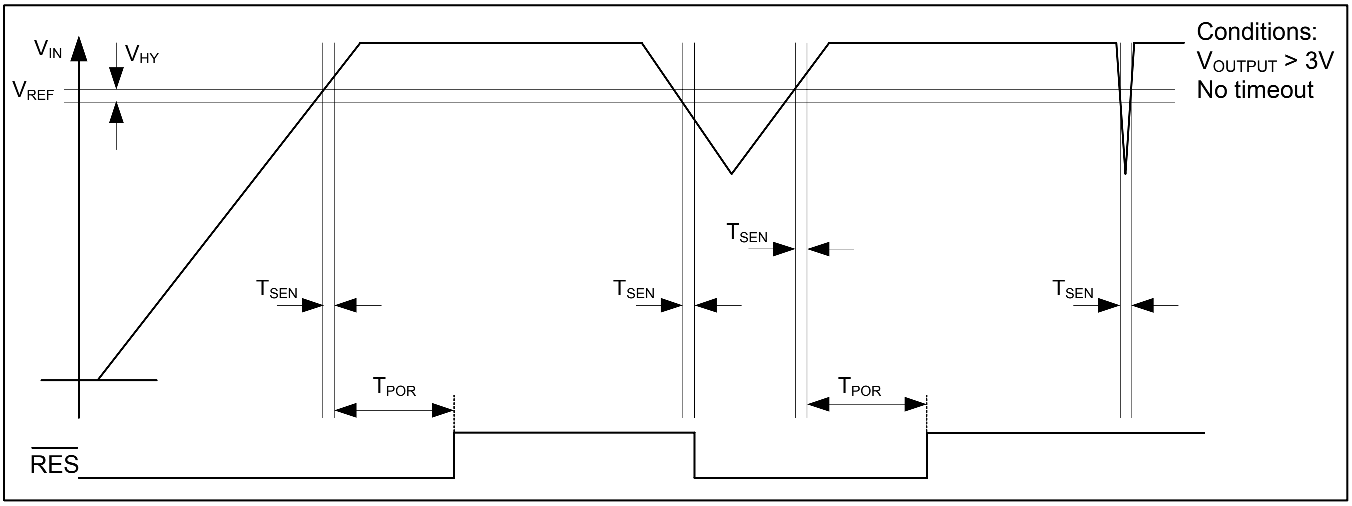


Fig. 5

Timer Reaction

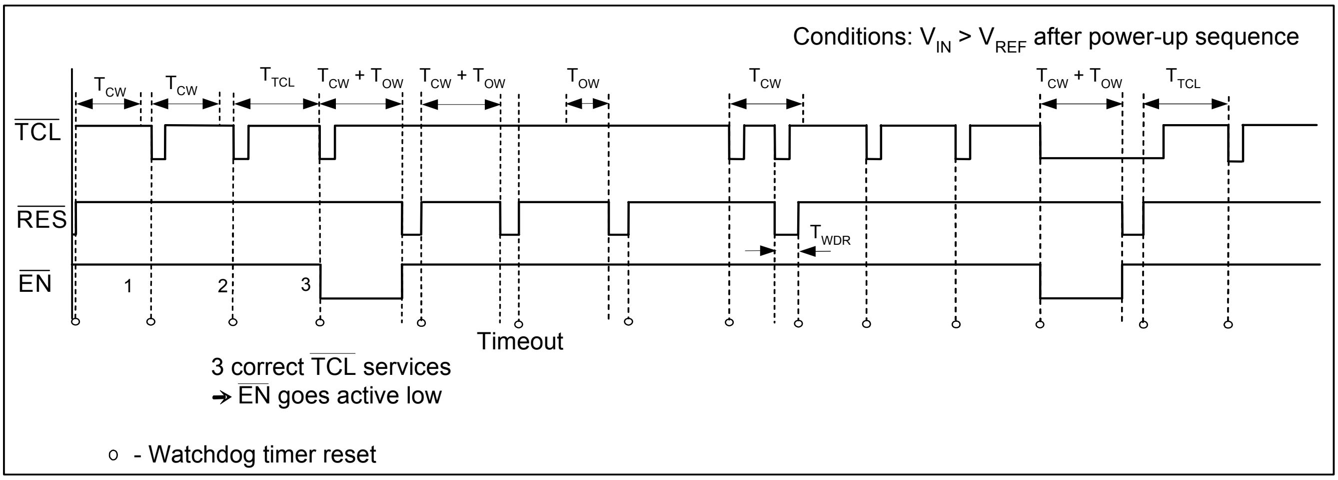


Fig. 6

Combined Voltage and Timer Reaction

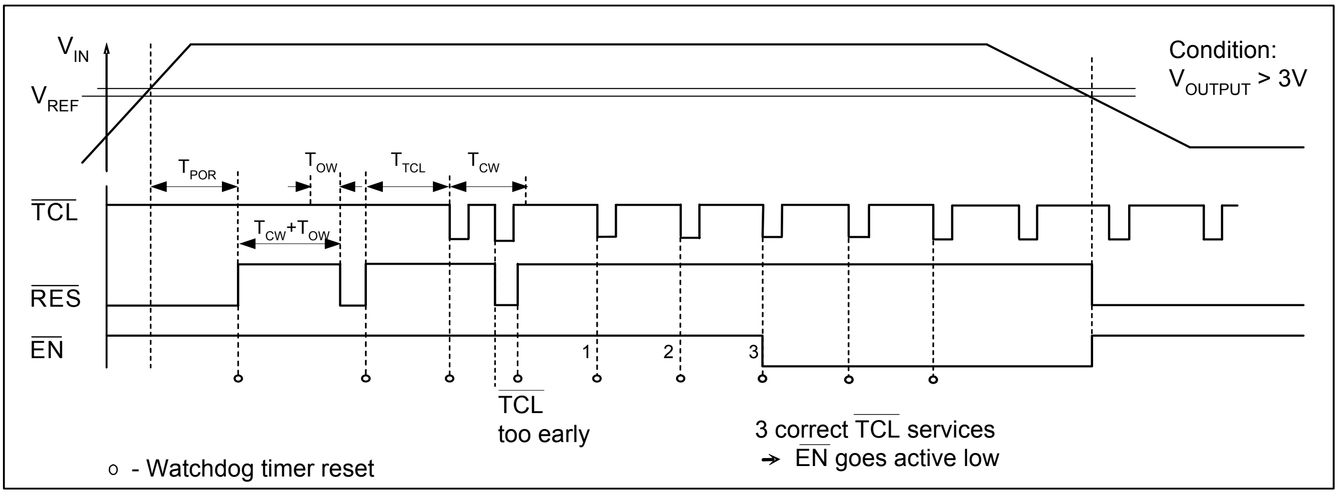


Fig. 7

Functional Description

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level applied on the V_{IN} input. The threshold voltage at which reset is asserted or released (V_{RESET}) is determined by the external voltage divider between V_{DD} and V_{SS}, as shown on Fig. 8. A part of V_{DD} is compared to the internal voltage reference. To determine the values of the divider, the leakage current at V_{IN} must be taken into account as well as the current consumption of the divider itself. Low resistor values will need more current, but high resistor values will make the reset threshold less accurate at high temperature, due to a possible leakage current at the V_{IN} input. The sum of the two resistors ($R_1 + R_2$) should stay below 500 kΩ. The formula is:

$$V_{RESET} = V_{REF} \times (1 + R_1/R_2).$$

Example: choosing R_1 = 200 kΩ and R_2 = 100 kΩ gives V_{RESET} =4.56 V (typical) for version V50 and V53.

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 5).

When V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on-reset (POR) delay T_{POR} (defined with the external resistor connected at R_{OSC} pin). The T_{POR} delay prevents repeated toggling of $\overline{RES}$ even if V_{DD} voltage drops out and recovers. The T_{POR} delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 3 µs.

Timer Programming

The on-chip oscillator allows the user to adjust the power-on reset (POR) delay T_{POR} and the watchdog time T_{WD} by changing the resistor value of the external resistor R_{OSC} connected between the pin R_{OSC} and V_{SS} (see Fig. 8). The closed and open window times (T_{CW} and T_{OW}) as well as the watchdog reset pulse width (T_{WDR}), which are T_{TCL} dependent, will vary accordingly. The watchdog time T_{WD} can be obtained with figures 9 to 12 or with the Excel application EM6151ResCalc.xls available on EM website. T_{POR} is equal to T_{WD} with the minimum and maximum tolerances increased by 1% (For Version 53, T_{POR} is one fourth of T_{WD}).

Note that the current consumption increases as the frequency increases.

Voltage Regulator

The EM6152 has a 5 V, 400 mA, low dropout voltage regulator. The low supply current makes the EM6152 particularly suitable for automotive systems which remain continuously powered. The input voltage range is 2.3 V to 40 V for operation and the input protection includes both reverse battery (42 V below ground) and load dump (positive transients up to 45 V). There is no reverse current flow from the OUTPUT to the INPUT when the INPUT equals V_{SS}. This feature is important for systems which need to implement (with capacitance) a minimum power supply hold-up time in the event of power failure. To achieve good load regulation a 22 µF capacitor (or greater) is needed on the INPUT (see Fig. 8). Tantalum or aluminium electrolytic are adequate for the 22 µF capacitor; film types will work but are relatively expensive. Many aluminium electrolytic have electrolytes that freeze at about –30°C, so tantalums are recommended for operation below –25°C. The important parameters of the 22 µF capacitor are an effective series resistance of lower than 3 Ω and a resonant frequency above 500 kHz.

A 22 µF capacitor (or greater) and a 100 nF capacitor are required on the OUTPUT to prevent oscillations due to instability. The specification of the 22 µF capacitor is as per the 22 µF capacitor on the INPUT (see previous paragraph).

The EM6152 will remain stable and in regulation with no external load and the dropout voltage is typically constant as the input voltage fall below its minimum level (see Table 2). These features are especially important in CMOS RAM keep-alive applications.

Power Dissipation

Care must be taken not to exceed the maximum junction temperature (+125°C). The power dissipation within the EM6152 is given by the formula:

$$P_{TOTAL} = (V_{INPUT} - V_{OUTPUT}) \times I_{OUTPUT} + (V_{INPUT}) \times I_{SS}$$

The maximum continuous power dissipation at a given temperature can be calculated using the formula:

$$P_{MAX} = (125°C - T_A) / R_{th(j-a)}$$

where $R_{th(j-a)}$ is the thermal resistance from the junction to the ambient and is specified in Table 2. Note that $R_{th(j-a)}$ given in Table 2 assumes that the package is soldered to a PCB (see figure 16). The above formula for maximum power dissipation assumes a constant load (i.e. >100 s). The transient thermal resistance for a single pulse is much lower than the continuous value.

CAN-Bus Sleep Mode Detector (version 55)

When the microcontroller goes into a standby mode, it implies that it does not send any pulses on the $\overline{TCL}$ input of the EM6152. After three reset pulse periods (T_{CW} + T_{OW} + T_{WDR}) on the $\overline{RES}$ output, the circuit switches on an internal resistor of 1 MΩ, and it will have a reset pulse of typically 3 ms every 1 second on the $\overline{RES}$ output. When a $\overline{TCL}$ edge (rising or falling) appears on the $\overline{TCL}$ input or the power supply goes down and up, the circuit switches to the R_{OSC}.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two periods, a closed window period (T_{CW}) and an open window period (T_{OW}), see Fig. 4. If no pulse is applied on the $\overline{TCL}$ input during the open window period T_{OW}, the $\overline{RES}$ output goes low for a time T_{WDR}. When a pulse is applied on the $\overline{TCL}$ input, the cycle is restarted with a close window period.

For example if T_{WD} = T_{POR} = 100ms, T_{CW} = 80 ms, T_{OW} = 40ms and T_{WDR} = 2.5ms.

When V_{IN} recovers after a drop below V_{REF}, the pad $\overline{RES}$ is set low for the time T_{POR} during which any $\overline{TCL}$ activation is disabled.

Timer Clearing and RES Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the TCL input within the programmed open window timeout period a short watchdog RES pulse is generated which is equal to T_{WDR} (see Fig. 6).
With the open window constraint, new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. If software is stuck in a loop which includes the routine to clear the watchdog then a conventional watchdog would not make a system reset even though the software is malfunctioning; the circuit would make a system reset because the watchdog would be cleared too quickly.
If no TCL signal is applied before the closed and open windows expire, RES will start to generate square waves of period $T_{WDRP} = T_{CW} + T_{OW} + T_{WDR}$. The watchdog will remain in this state until the next TCL falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, EN, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable-EN Output").
The RES output must be pulled up to V_{OUTPUT} even if the output is not used by the system (see Fig 8).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 6. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds RES active for the time of the POR delay. A TCL pulse will have no effect until this power-on-reset delay is completed. When the risk exists that TCL temporarily floats, e.g. during T_{POR}, a pull-up to V_{OUTPUT} is required on that pin. After the POR delay has elapsed, RES goes inactive and the watchdog timer starts acting. If no TCL pulse occurs, RES goes active low for a short time T_{WDR} after each closed and open window period. A TCL pulse coming during the open window clears the watchdog timer. When the TCL pulse occurs too early (during the closed window), RES goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 3µs overrides the timer and immediately forces RES active and EN inactive. Any further TCL pulse has no effect until the next power-up sequence has completed.

Enable - EN Output

The system enable output, EN, is inactive always when RES is active and remains inactive after a RES pulse until the watchdog is serviced correctly 3 consecutive times (i.e. the TCL pulse must come in the open window). After three consecutive services of the watchdog with TCL during the open window, the EN goes active low.

A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The circuit prevents the above failure mode by using the EN output to disable the motor controls until software has successfully cleared the watchdog three times (i.e. the system has correctly re-started after a reset condition).

Typical Application

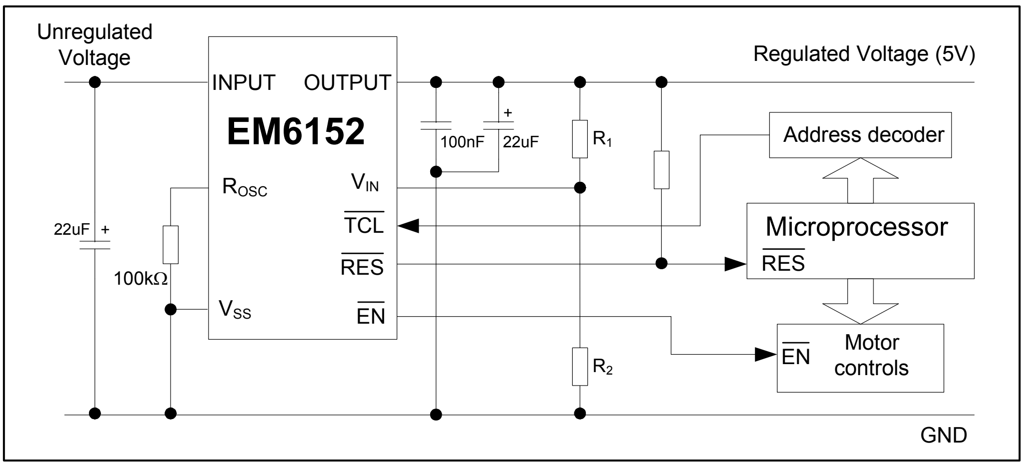


Fig. 8

The important parameters of the 22 µF input capacitor are an effective series resistance lower than 3 Ω and a resonant frequency above 500 kHz.

V30 R_{OSC} Coefficient versus T_{WD} at V_{DD}= 5.0V and T_j=-40 to +125°C

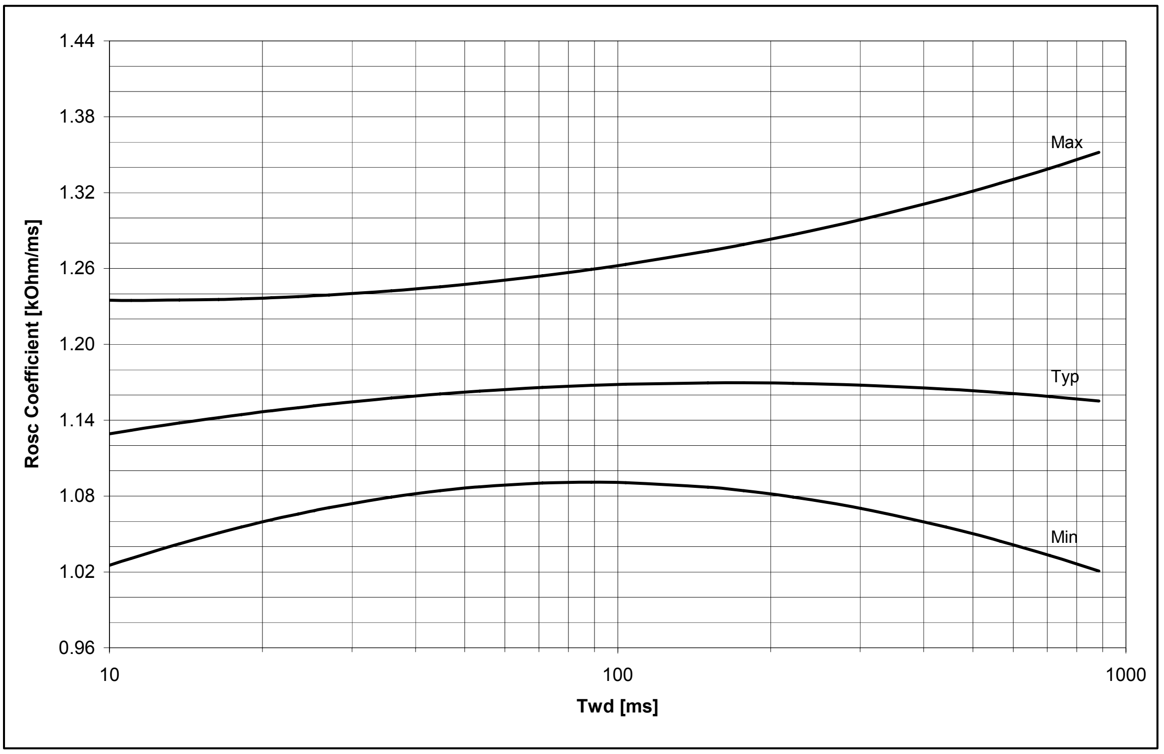


Fig. 9

V50 R_{OSC} Coefficient versus T_{WD} at V_{DD}= 5.0V and T_j=-40 to +125°C

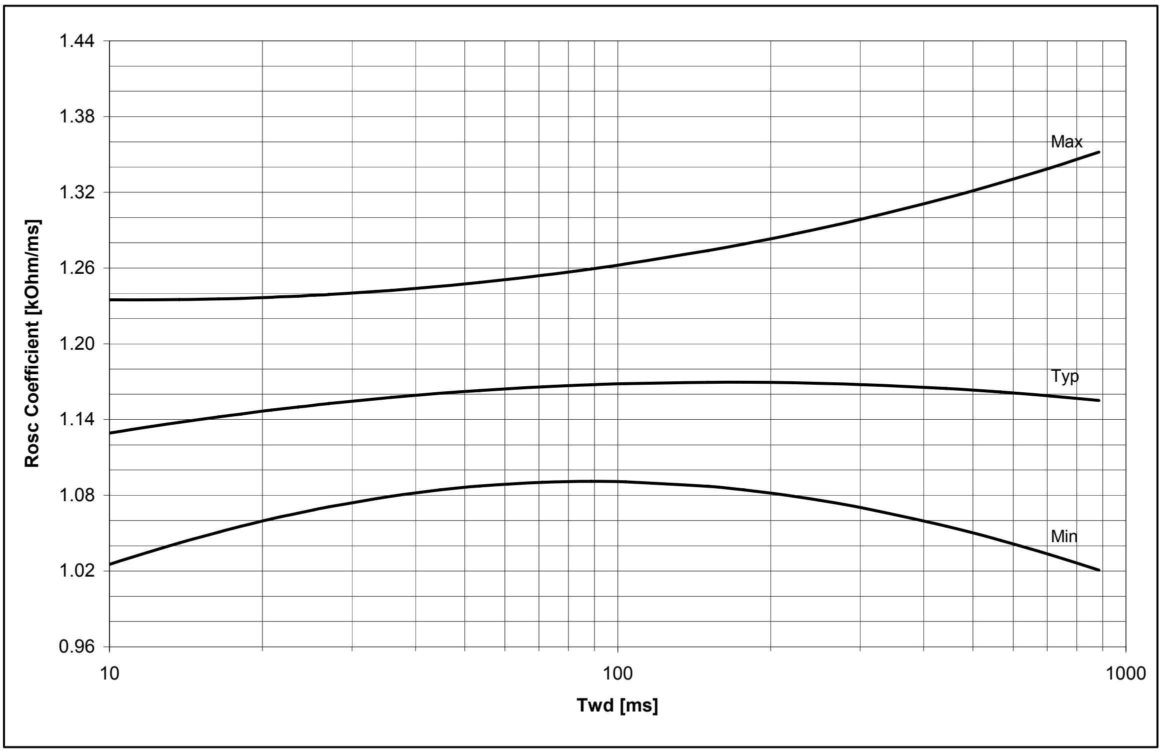


Fig. 10

V53 R_{OSC} Coefficient versus T_{WD} at V_{DD}= 5.0V and T_j=-40 to +125°C

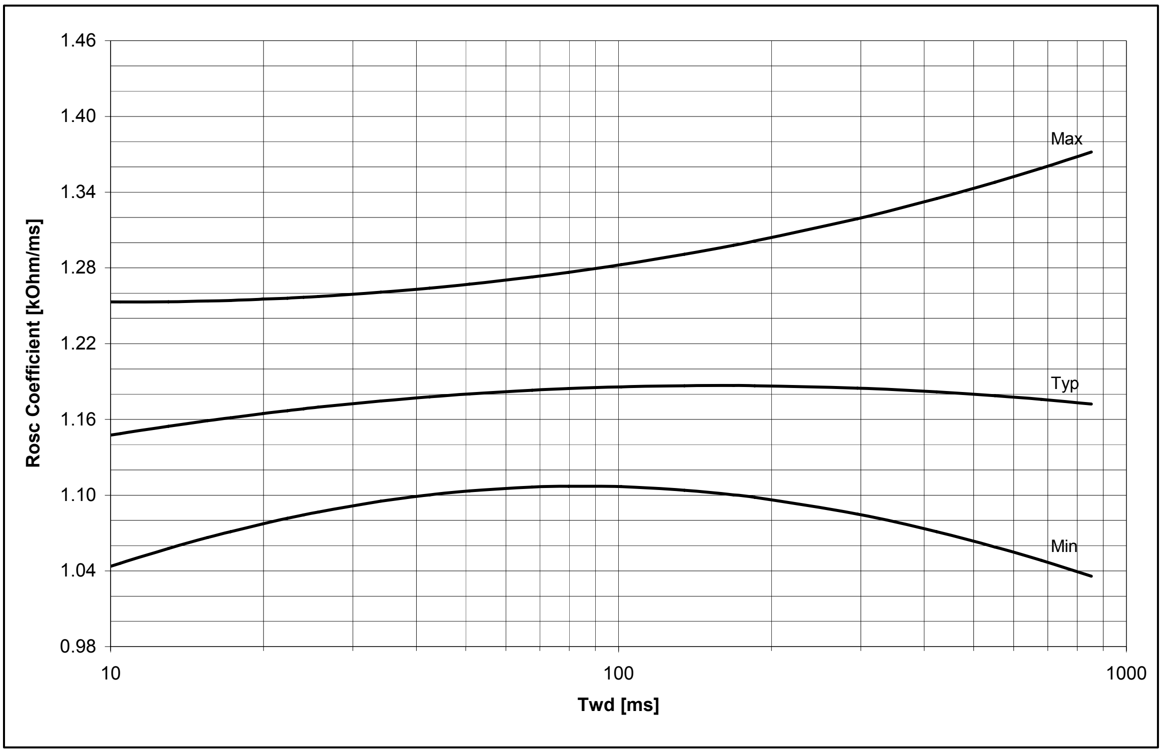


Fig. 11

V55 R_{OSC} Coefficient versus T_{WD} at V_{DD}= 5.0V and T_j=-40 to +125°C

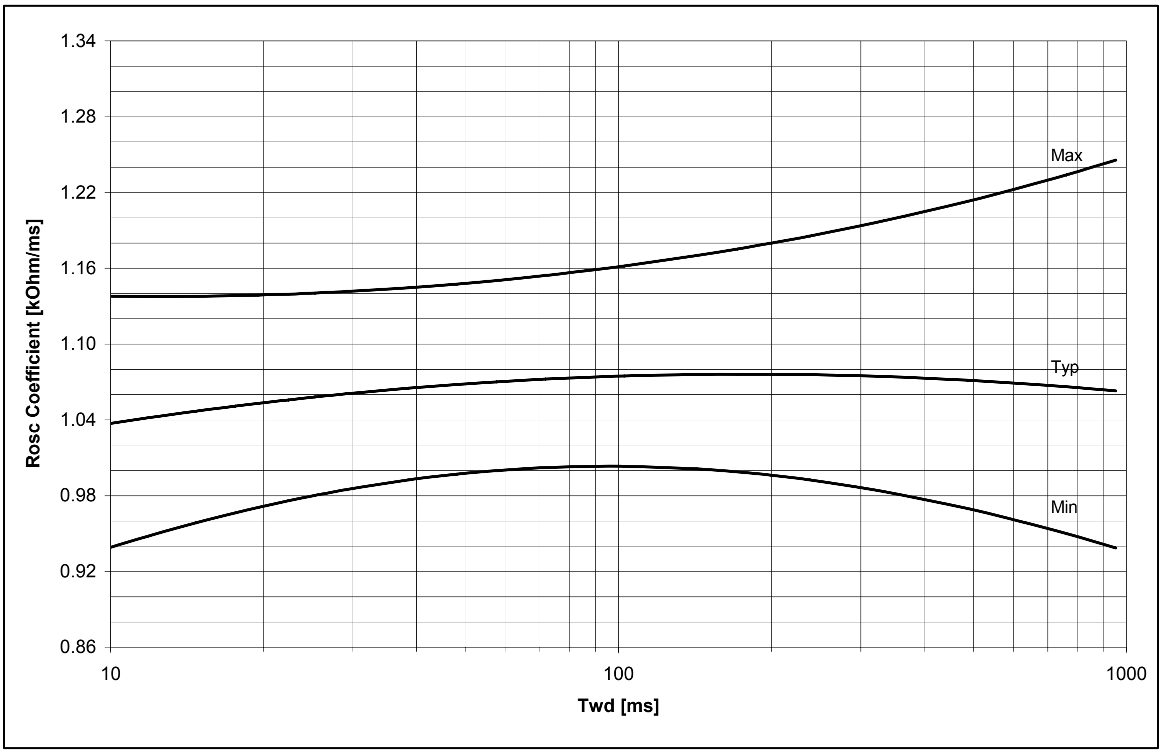


Fig. 12

Typical maximum OUTPUT current versus INPUT voltage

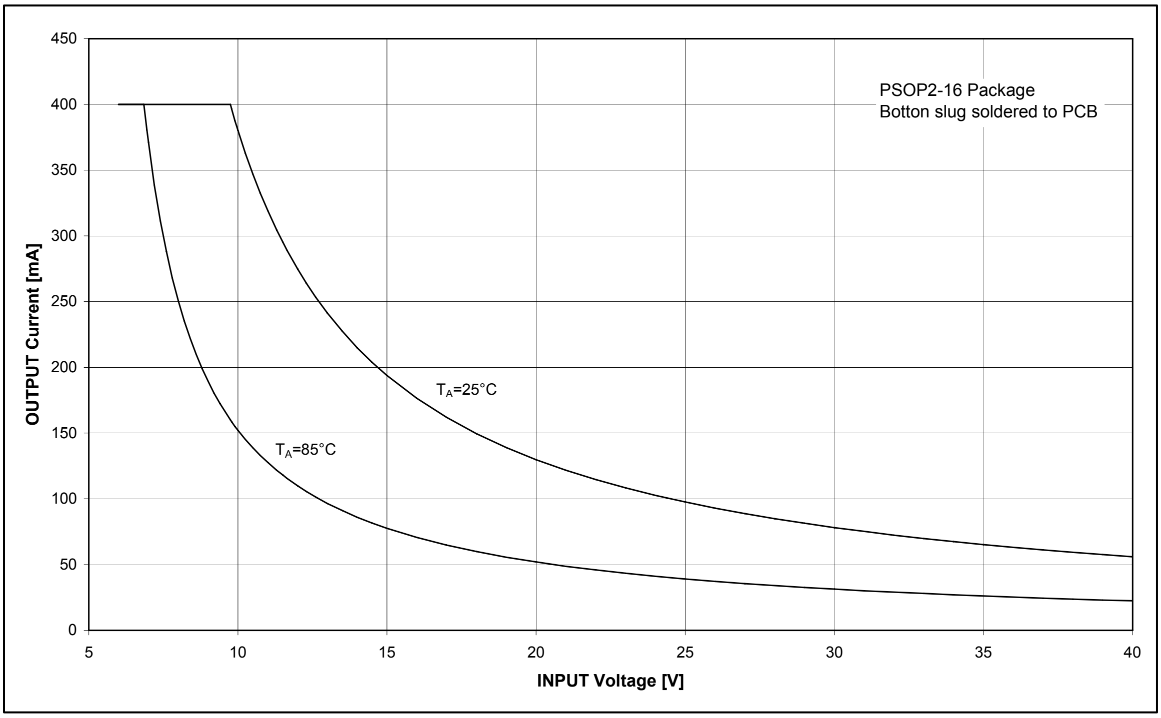
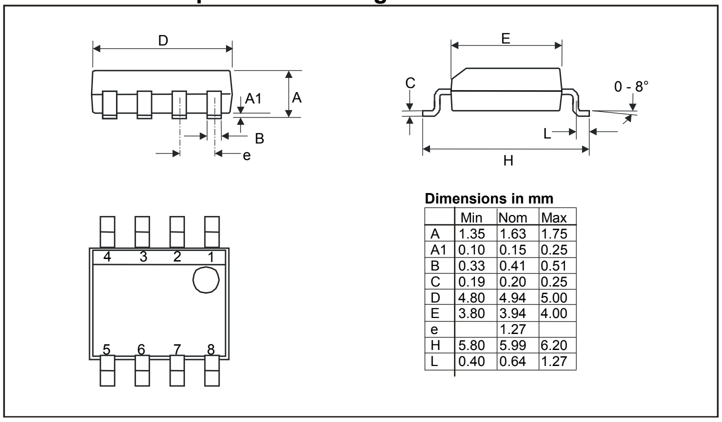


Fig. 13

Package Information

Dimensions of 8-pin SOIC Package



Dimensions in mm

	Min	Nom	Max
A	1.35	1.63	1.75
A1	0.10	0.15	0.25
B	0.33	0.41	0.51
C	0.19	0.20	0.25
D	4.80	4.94	5.00
E	3.80	3.94	4.00
e		1.27	
H	5.80	5.99	6.20
L	0.40	0.64	1.27

Fig. 14

Dimensions of PSOP2-16 Package

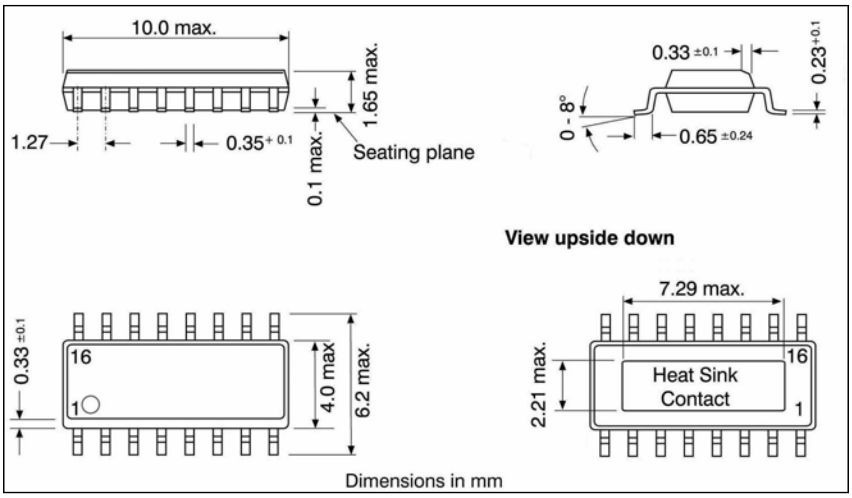


Fig. 15

Dual Layer PCB

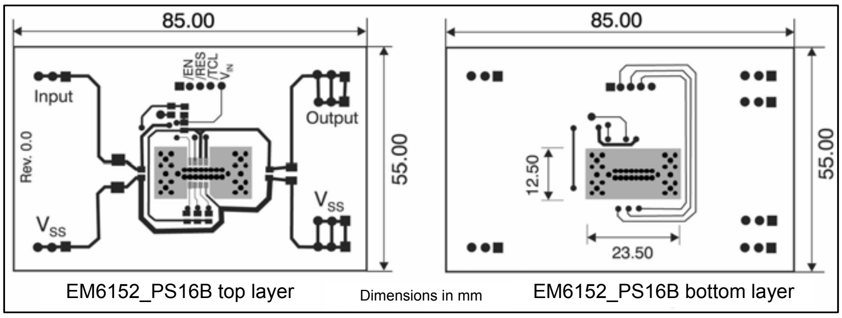


Fig. 16

SUBJECT TO CHANGE WITHOUT NOTICE