19-3798; Rev 0; 09/06

Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

General Description

The MAX4670 is an integrated T1/E1/J1 analog protection switch for 1+1 and N+1 line-card redundancy applications. It protects two T1/E1/J1 ports by combining eight SPDT switches in a single package. The switch is optimized for high-return loss and pulse-template performance in T1/E1/J1 long-haul and short-haul applications. The part offers built-in chip-side surge protection capability for short-haul intrabuilding applications.

The MAX4670 replaces two diode arrays or two transient voltage suppressors (TVSs) and four dual-SPDT relays, significantly reducing board space and simplifying PC board routing. The MAX4670 pinout is targeted for T1/E1/J1 applications, resulting in a simplified layout when interfacing with standard line transformers and line interface units (LIUs).

The MAX4670 has four 1.0Ω (max) on-resistance switches with 60pF/40pF on-/off-capacitances for interfacing to the LIU transmitter outputs. The MAX4670 also includes four 10Ω (max) on-resistance switches with low 24pF/12pF on-/off-capacitances for interfacing to the LIU receiver inputs. Four logic inputs control the receive/transmit pairs, in addition to a $\overline{\text{SWITCH}}$ input that connects all switches to the system's protection bus.

The MAX4670 operates from a single +2.7V to +3.6V supply and is available in 32-pin thermally enhanced TQFN package. The MAX4670 is specified over the -40°C to +85°C operating temperature range.

Applications

Optical Multiplexers (ADMs, M13s, etc.)

Edge Routers

Multiservice Switches

Base Station Controllers (Wireless Infrastructure Equipment)

Media Gateways (VoIP)

Functional Diagram/Truth Table appears at end of data sheet.

Features

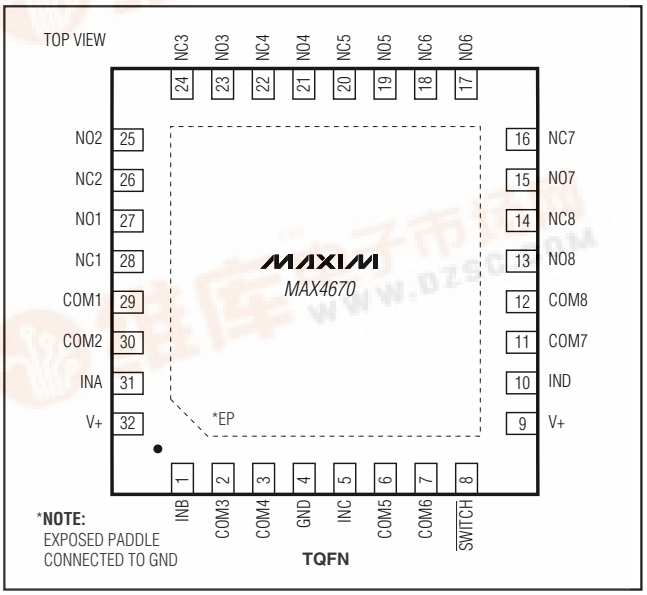
- ♦ **Single +3.3V Supply Voltage**
- ♦ **Quad-DPDT/Octal-SPDT Switches Support Two T1/E1/J1 Ports**
- ♦ **Low R_{ON}**
- ♦ **0.7Ω (typ) in Transmit Path; 5Ω (typ) in Receive Path**
- ♦ **Low C_{ON}/C_{OFF}**
  60pF/40pF (typ) in Transmit Path
  24pF/12pF (typ) in Receive Path
- ♦ **Chip Surge Protection**
  IEC 61000-4-5 (8µs to 20µs Surge)
  Class 2 (±1kV)
- ♦ **-70dB (typ) Crosstalk/Off-Isolation (3MHz)**
- ♦ **Small, 32-Pin TQFN Package**

Ordering Information

PART*	PIN-PACKAGE	SURGE PROTECTION	PKG CODE
MAX4670ETJ	32 TQFN (5mm x 5mm)	YES	T3255-4

**This part operates at a -40°C to +85°C temperature range.*

Pin Configuration



Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V+, IN_, SWITCH .....-0.3V to +4V
COM_, NO_, NC_ (Note 1) .....-0.3V to (V+ + 0.3V)
Continuous Current
NO_, NC_, COM_ (Tx interface).....±150mA
NO_, NC_, COM_ (Rx interface) .....±100mA
Peak Currents
NO_, NC_, COM_ (Tx interface)
(pulsed at 1ms, 10% duty cycle) .....±300mA
NO_, NC_, COM_ (Rx interface)
(pulsed at 1ms, 10% duty cycle) .....±200mA
Peak Surge Currents
Poised at 8µs 21.4A
Poised at 20µs 11.9A
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 21.3mW/°C above +70°C) 1702mW
38-Pin TSSOP (derate 13.7mW/°C above +70°C) 1096mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on NO_, NC_, COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Rx INTERFACE							
On-Resistance	R_{ON}	V+ = 3V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	T_A = +25°C		5	9	Ω
			T_A = T_{MIN} to T_{MAX}			10	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 3V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	T_A = +25°C			1.0	Ω
			T_A = T_{MIN} to T_{MAX}			1.3	
On-Resistance Flatness (Note 4)	$R_{FLAT(ON)}$	V+ = 3V; $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 1.5V, 2.0V	T_A = +25°C		2.0	3.0	Ω
			T_A = T_{MIN} to T_{MAX}			3.4	
NO_ or NC_ Off-Leakage Current	$I_{NO(OFF)}$ / $I_{NC(OFF)}$	V+ = 3.6V; $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3.3V, 0.3V		-1		+1	µA
COM_ On-Leakage Current	$I_{COM(ON)}$	V+ = 3.6V; $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3.3V, 0.3V or floating		-1		+1	µA
Tx INTERFACE							
On-Resistance (Note 5)	R_{ON}	V+ = 3V, $I_{COM\_}$ = 100mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	T_A = +25°C		0.7	0.9	Ω
			T_A = T_{MIN} to T_{MAX}			1.0	
On-Resistance Match Between Channels (Notes 3, 5)	ΔR_{ON}	V+ = 3V, $I_{COM\_}$ = 100mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	T_A = +25°C		0.03	0.150	Ω
			T_A = T_{MIN} to T_{MAX}			0.175	
On-Resistance Flatness (Notes 5, 6)	$R_{FLAT(ON)}$	V+ = 3V; $I_{COM\_}$ = 100mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 1.5V, 2.0V	T_A = +25°C		0.1	0.18	Ω
			T_A = T_{MIN} to T_{MAX}			0.2	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +3.6V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
NO_ or NC_ Off-Leakage Current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V+ = 3.6V; $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V		-1		+1	µA
COM_ On-Leakage Current	$I_{COM(ON)}$	V+ = 3.6V; $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V or floating		-1		+1	µA
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF, Figure 2	T_A = +25°C			400	ns
			$T_A = T_{MIN}$ to T_{MAX}			750	
Turn-Off Time	t_{OFF}	V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, Figure 2	T_A = +25°C			200	ns
			$T_A = T_{MIN}$ to T_{MAX}			750	
Break-Before-Make Delay	t_D	R_L = 50Ω, C_L = 35pF, Figure 3			80		ns
Charge Injection	Q	V_{GEN} = 1.5V, R_{GEN} = 0Ω, C_L = 1nF, Figure 4	Rx interface		8		pC
			Tx interface		20		
On-Channel 3dB Bandwidth	BW		Rx interface		300		MHz
			Tx interface		300		
Off-Isolation (Note 7)	V_{ISO1}	Rx interface	R_L = 50Ω, C_L = 35pF, f < 3MHz		-65		dB
	V_{ISO2}		R_L = 50Ω, C_L = 35pF, 3MHz < f < 30MHz		-58		
	V_{ISO1}	Tx interface	R_L = 50Ω, C_L = 35pF, f < 3MHz		-60		
	V_{ISO2}		R_L = 50Ω, C_L = 35pF, 3MHz < f < 30MHz		-40		
Crosstalk (Note 8)	V_{CT1}	Rx interface, Figure 5	R_L = 50Ω, C_L = 35pF, f < 3MHz		-65		dB
	V_{CT2}		R_L = 50Ω, C_L = 35pF, 3MHz < f < 30MHz		-50		
	V_{CT1}	Tx interface, Figure 5	R_L = 50Ω, C_L = 35pF, f < 3MHz		-78		
	V_{CT2}		R_L = 50Ω, C_L = 35pF, 3MHz < f < 30MHz		-30		
NC_ or NO_ Off-Capacitance	C_{OFFRX}	Rx interface f = 1MHz, Figure 6			12		pF
	C_{OFFTX}	Tx interface f = 1MHz, Figure 6			40		
COM_ On-Capacitance	$C_{COM(ON)TX}$	f = 1MHz	Rx interface		24		pF
	$C_{COM(ON)RX}$		Tx interface		60		

Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +3.6V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

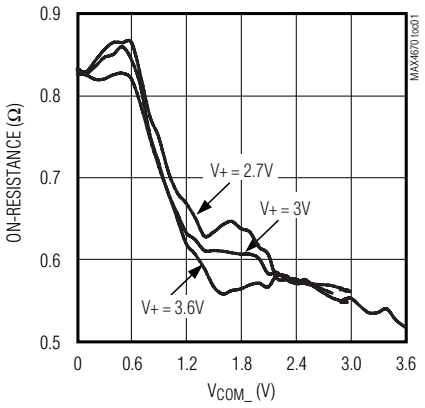
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O (IN_, $\overline{SWITCH}$)						
Input-Low Voltage	V_{IL}	V+ = 2.7V			0.5	V
Input-High Voltage	V_{IH}	V+ = 3.6V	1.4			V
Input Leakage Current	I_{IL}	$V_{IN\_}$ = 0 or V+, $V_{\overline{SWITCH}}$ = 0 or V+	-1		+1	µA
SUPPLY						
Operating Voltage Range	V+		2.7		3.6	V
Supply Current	I+	V+ = 3.6V, $V_{IN\_} = V_{\overline{SWITCH}}$ = 0 or V+			10	µA

Note 2: The algebraic convention is used in this data sheet. The most negative value is shown in the minimum column.
Note 3: Devices are 100% tested at hot and room and guaranteed by design at cold.
Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 5: Guaranteed by design.
Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
Note 7: Off-isolation = $20\log_{10} [V_{COM\_} / (V_{NO\_}$ or $V_{NC\_})]$, $V_{COM\_}$ = output, $V_{NO\_}$ or $V_{NC\_}$ = input to off switch.
Note 8: Crosstalk between any two switches.

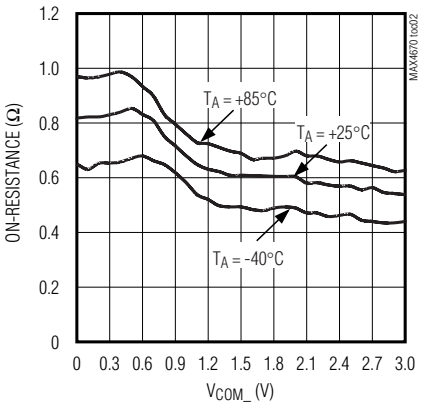
Typical Operating Characteristics

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)

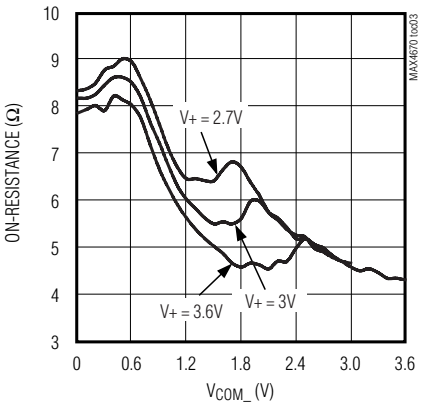
ON-RESISTANCE vs. COM_VOLTAGE (Tx INTERFACE)



ON-RESISTANCE vs. COM_ VOLTAGE OVER TEMPERATURE (Tx INTERFACE)



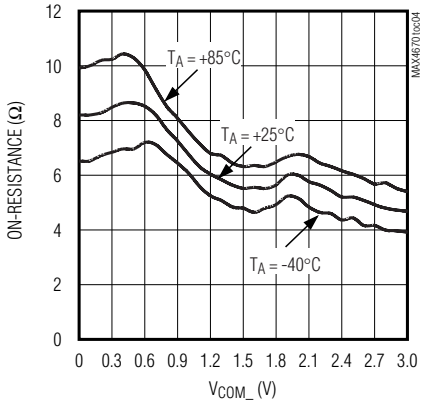
ON-RESISTANCE vs. COM_VOLTAGE (Rx INTERFACE)



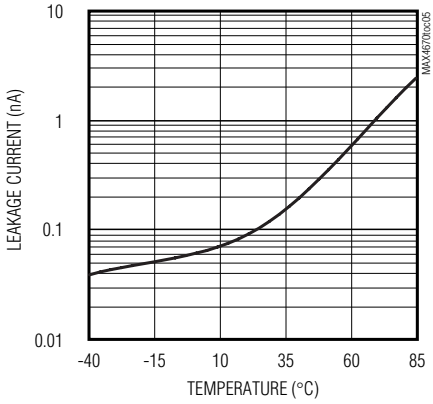
Typical Operating Characteristics (continued)

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)

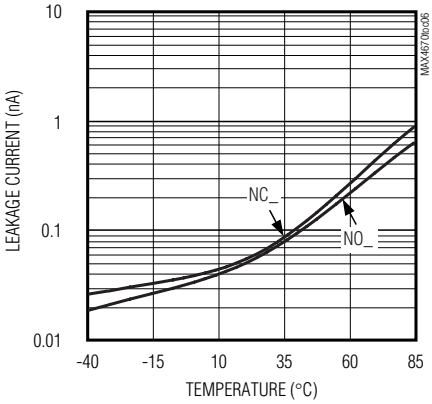
ON-RESISTANCE vs. COM_ VOLTAGE OVER TEMPERATURE (Rx INTERFACE)



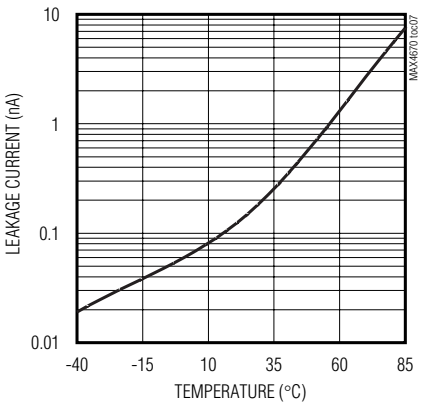
COM_ LEAKAGE CURRENT vs. TEMPERATURE (Tx INTERFACE)



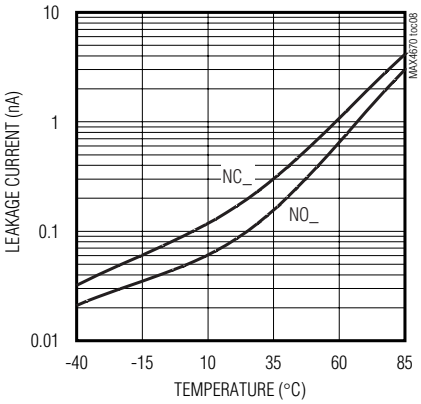
NC_/NO_ LEAKAGE CURRENT vs. TEMPERATURE (Tx INTERFACE)



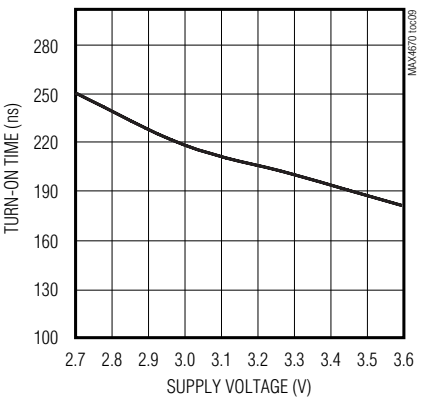
COM_ LEAKAGE CURRENT vs. TEMPERATURE (Rx INTERFACE)



NC_/NO_ LEAKAGE CURRENT vs. TEMPERATURE (Rx INTERFACE)



TURN-ON TIME vs. SUPPLY VOLTAGE (Tx INTERFACE)

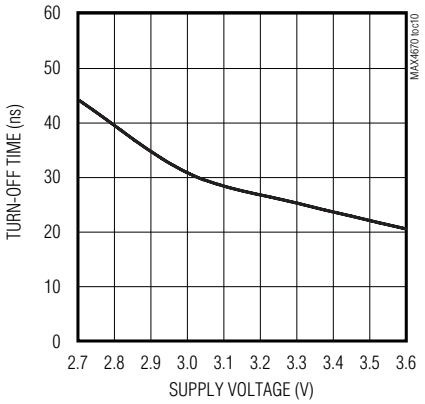


Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

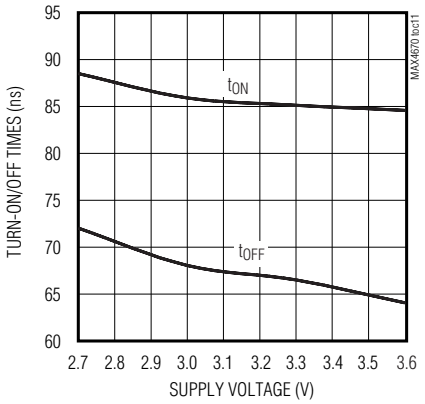
Typical Operating Characteristics (continued)

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)

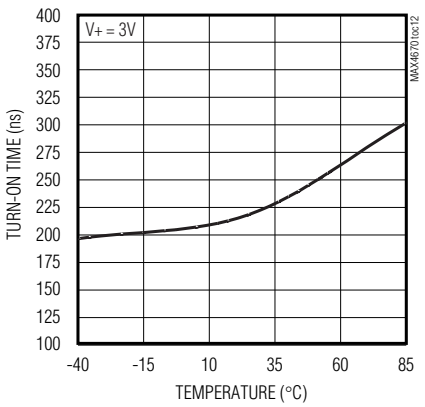
TURN-OFF TIME vs. SUPPLY VOLTAGE (Tx INTERFACE)



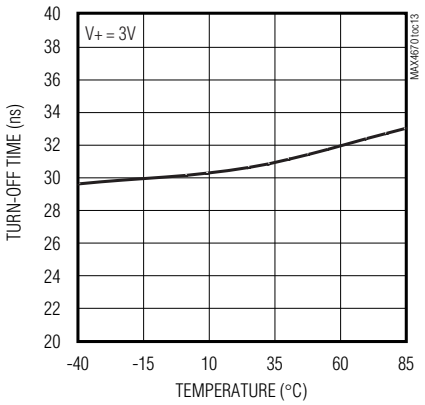
TURN-ON/OFF TIMES vs. SUPPLY VOLTAGE (Rx INTERFACE)



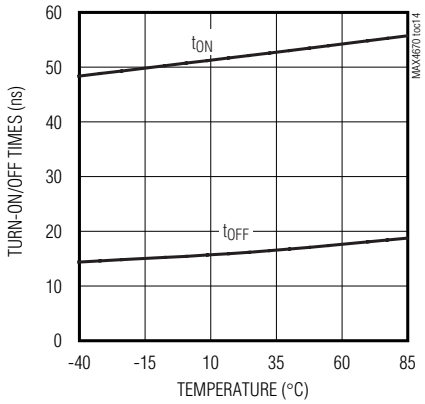
TURN-ON TIME vs. TEMPERATURE (Tx INTERFACE)



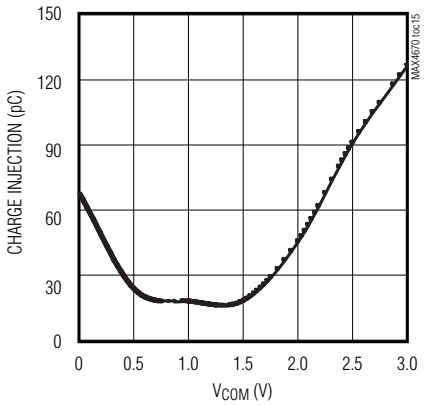
TURN-OFF TIME vs. TEMPERATURE (Tx INTERFACE)



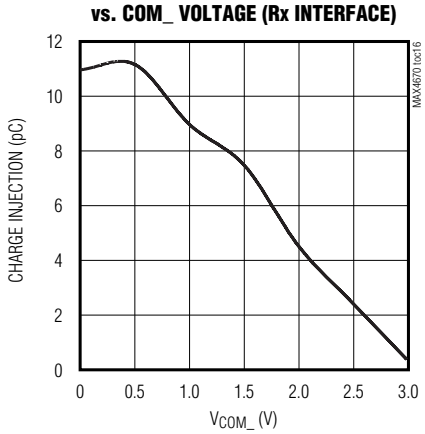
TURN-ON/OFF TIMES vs. TEMPERATURE (Rx INTERFACE)



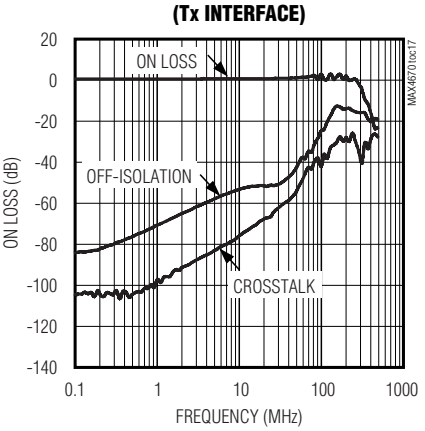
CHARGE INJECTION vs. COM_ VOLTAGE (Tx INTERFACE)



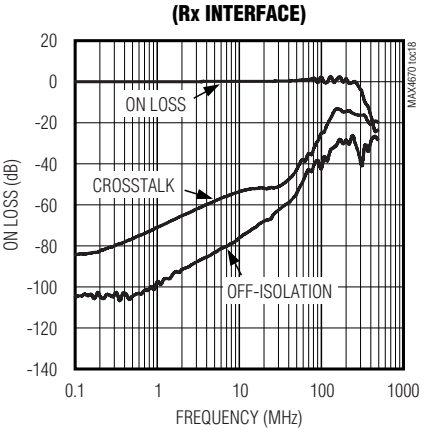
CHARGE INJECTION vs. COM_ VOLTAGE (Rx INTERFACE)



FREQUENCY RESPONSE (Tx INTERFACE)



FREQUENCY RESPONSE (Rx INTERFACE)



Pin Description

PIN	NAME	FUNCTION
—	N.C.	No Connection. Not internally connected.
1	INB	Transmitter 1 Logic Control. Drive INB high to connect NC3 and NC4. INB logic is ignored when $\overline{SWITCH}$ asserts low.
2	COM3	Common Terminal 3. Transmitter 1 positive differential terminal. Connect COM3 to the transmit interface transformer.
3	COM4	Common Terminal 4. Transmitter 1 negative differential terminal. Connect COM4 to the transmit interface transformer.
4	GND	Ground
5	INC	Transmitter 2 Logic Control. Drive INC high to connect NC5 and NC6. INC logic is ignored when $\overline{SWITCH}$ asserts low.
6	COM5	Common Terminal 5. Transmitter 2 positive differential terminal. Connect COM5 to the transmit interface transformer.
7	COM6	Common Terminal 6. Transmitter 2 negative differential terminal. Connect COM6 to the transmit interface transformer.
8	$\overline{SWITCH}$	Protection Switch Control. Assert $\overline{SWITCH}$ low to connect all switches to protection bus. When $\overline{SWITCH}$ asserts low, $\overline{SWITCH}$ overrides all IN_ inputs. Assert $\overline{SWITCH}$ high to enable all switches and let the respective IN control the switches.
9, 32	V+	Positive Supply Voltage. Bypass V+ to ground with a 0.1µF ceramic capacitor.
10	IND	Receiver 2 Logic Control. Drive IND high to connect NC7 and NC8. IND logic is ignored when $\overline{SWITCH}$ asserts low.
11	COM7	Common Terminal 7. Receiver 2 positive differential terminal. Connect COM7 to the receive interface transformer.
12	COM8	Common Terminal 8. Receiver 2 negative differential terminal. Connect COM8 to the receive interface transformer.
13	NO8	Normally Open Terminal 8. Receiver 2 differential protection terminal. Connect NO8 to the protection bus.
14	NC8	Normally Closed Terminal 8. Receiver 2 differential terminal. Connect NC8 to LIU receiver.
15	NO7	Normally Open Terminal 7. Receiver 2 differential protection terminal. Connect NO7 to the protection bus.
16	NC7	Normally Closed Terminal 7. Receiver 2 differential terminal. Connect NC7 to LIU receiver.
17	NO6	Normally Open Terminal 6. Transmitter 2 differential protection terminal. Connect NO6 to the protection bus.
18	NC6	Normally Closed Terminal 6. Transmitter 2 differential terminal. Connect NC6 to LIU receiver.
19	NO5	Normally Open Terminal 5. Transmitter 2 differential protection terminal. Connect NO5 to the protection bus.
20	NC5	Normally Closed Terminal 5. Transmitter 2 differential terminal. Connect NC5 to LIU receiver.
21	NO4	Normally Open Terminal 4. Transmitter 1 differential protection terminal. Connect NO4 to the protection bus.

Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

Pin Description (continued)

PIN	NAME	FUNCTION
22	NC4	Normally Closed Terminal 4. Transmitter 1 differential terminal. Connect NC4 to LIU receiver.
23	NO3	Normally Open Terminal 3. Transmitter 1 differential protection terminal. Connect NO3 to the protection bus.
24	NC3	Normally Closed Terminal 3. Transmitter 1 differential terminal. Connect NC3 to LIU receiver.
25	NO2	Normally Open Terminal 2. Receiver 2 differential protection terminal. Connect NO2 to the protection bus.
26	NC2	Normally Closed Terminal 2. Receiver 1 differential terminal. Connect NC2 to LIU receiver.
27	NO1	Normally Open Terminal 1. Receiver 1 differential protection terminal. Connect NO1 to the protection bus.
28	NC1	Normally Closed Terminal 1. Receiver 1 differential terminal. Connect NC1 to LIU receiver.
29	COM1	Common Terminal 1. Receiver 1 positive differential terminal. Connect COM1 to the receive interface transformer.
30	COM2	Common Terminal 2. Receiver 1 negative differential terminal. Connect COM2 to the receive interface transformer.
31	INA	Receiver 1 Logic Control. Drive INA low to connect receiver 1 to the LIU. INA logic is ignored when $\overline{SWITCH}$ asserts low.
EP	EP	Exposed Paddle. Connect EP to GND or leave unconnected.

Detailed Description

The MAX4670 is a quad-DPDT/octal-SPDT analog switch optimized for T1/E1/J1 line-card redundancy protection applications. This analog switch is configurable as two differential transmitter and receiver pairs utilized in T1/E1/J1 redundancy architecture.

The MAX4670 has four low 0.7Ω on-resistance switches with 60pF and 40pF on- and off-capacitances, respectively, for interfacing to the LIU transmitter inputs. The MAX4670 also includes four 5Ω on-resistance switches with low 24pF and 12pF on- and off-capacitances, respectively, for interfacing to the LIU receiver inputs.

The MAX4670 replaces two diode arrays or two transient voltage suppressors and four dual-SPDT relays, significantly reducing board space and simplifying PC board routing. The MAX4670 pinouts are targeted for T1/E1/J1 applications, resulting in a simplified layout when interfacing with standard line transformers and LIUs. Figure 1 is the functional diagram.

Logic Inputs (IN_, $\overline{SWITCH}$)

The MAX4670 four logic inputs (IN_) control the switches in pairs and contain a global logic input ($\overline{SWITCH}$) that connects all COMs to their respective NO_ inputs. $\overline{SWITCH}$ overrides all IN_ inputs when asserted low, thus connecting all NO_ to COM_ outputs (transmitter/receiver pairs to the protection bus). When $\overline{SWITCH}$ asserts high, IN_ controls the switch pairs. See Table 1.

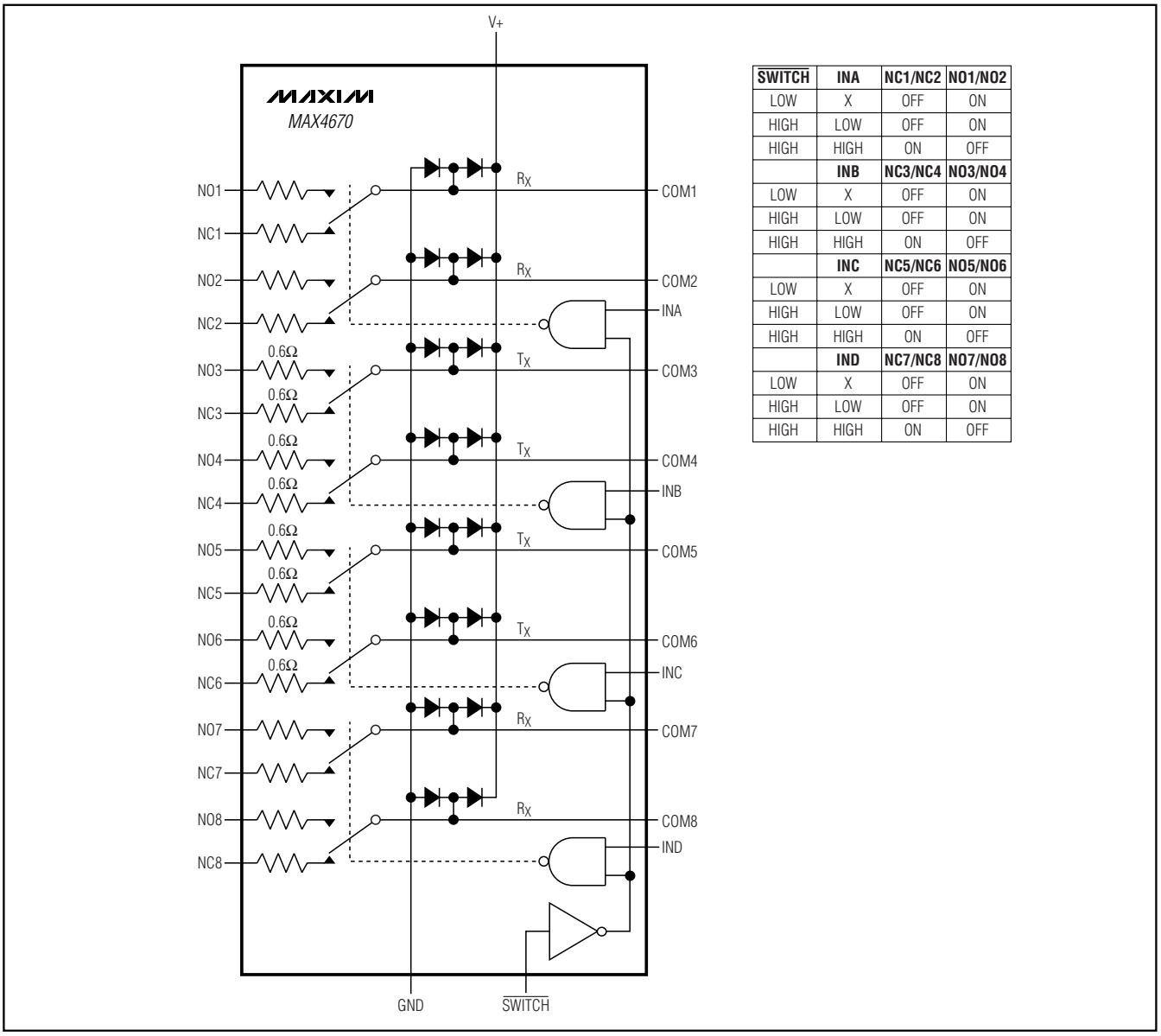
Surge Protection

The MAX4670 includes chip-side, surge-protection capability for short-haul intrabuilding applications. The low-capacitance diodes suppress surge residuals from the primary, line-side protection devices. It is assumed that adequate primary protection is included on the line die of the transformer, as represented in Figures 7–10. Table 2 lists the applicable surge protection setups for E1 interfaces. The MAX4670 surge test was performed per IEC 61000-4-5 Class 2 specifications and passed at ±1kV with only an in-line transformer and primary surge suppressor. The transformer was a Halo TG83-1505NX transformer and the surge suppressor was a Teccor P0640SC.

Applications Information

Redundancy Architecture

Figures 7 through 10 illustrate the MAX4670 used in two different redundancy architectures. There is one backup card for up to N line cards in the system (in this example, N = 3). In the event one of the line cards fails (memory failure, power supply went down, etc.), a system supervisory card issues a command to the switches to reroute the traffic to and from the problem line card to the backup line card.



SWITCH	INA	NC1/NC2	NO1/NO2
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF
	INB	**NC3/NC4**	**NO3/NO4**
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF
	INC	**NC5/NC6**	**NO5/NO6**
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF
	IND	**NC7/NC8**	**NO7/NO8**
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF

Figure 1. Functional Diagram

In a switching-card architecture, a common switching card contains all the protection switches for the T1/E1/J1 lines entering the system (see Figures 7 and 8).

With an adjacent card architecture, the switches protecting any given line card reside physically in the adjacent line card (see Figures 9 and 10).

Receive and transmit interfaces reside in the same board for each T1/E1/J1 port. The diagrams represent the typical interface transformers and resistors recommended for Dallas/Maxim LIUs, such as the DS21Q55.

The protection switches are placed in the low-voltage side of the transformer to meet the isolation requirements. Note that there is also a TVS in the line side of the transformers. The receive and transmit resistors provide impedance matching to the T1/E1/J1 transmission cable characteristic impedance. Refer to Application Note 2857 for more information on T1/E1/J1 applications.

Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

Table 1. MAX4670 Truth Table

$\overline{SWITCH}$	INA	NC1/NC2	NO1/NO2
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF
—	**INB**	**NC3/NC4**	**NO3/NO4**
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF
—	**INC**	**NC5/NC6**	**NO5/NC6**
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF
—	**IND**	**NC7/NC8**	**NO7/NO8**
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF

Table 2. IEC 61000-4-5 Test Conditions

TEST CONFIGURATION	TEST CONDITIONS
Differential Surge (Line to Line)	500V peak, 12A min current, 8µs/20µs surge
Common-Mode Surge (Line to GND)	1000V peak, 24A min current, 8µs/20µs surge

LIU Interface Recommendations

The MAX4670 low 0.7Ω (typ) on-resistance is adequate, even in applications where the LIUs require no external series transmit resistors (Rt = 0 in Figures 8 and 10). However, in some instances, increase the LIU output amplitude to compensate for R_{ON} if the LIU supports programmable output amplitude. With LIUs requiring external transmit resistors, it is recommended to reduce Rt by the amount of the typical R_{ON} with LIUs requiring external transmit resistors.

For example, if the LIU vendor recommends Rt = 9.1Ω, the actual value in the application should be:

$$Rt = Rt - R_{ON} = 9.1\Omega - 0.7 = 8.4\Omega$$

The receive interface series resistance is small enough to support LIUs with internal line termination, provided the external 120Ω parallel resistor combination (Rr) is connected, as shown in Figures 7 and 9.

While in normal operation, the MAX4670 requires the input and output signals to be within the V+ and GND supply rails.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 11 shows the Human Body Model. Figure 12 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to ICs. The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstands voltage measured to IEC 61000-4-2, and is generally lower than that measured using the Human Body Model. Figure 13 shows the IEC 61000-4-2 model, and Figure 14 shows the current waveform for the ±8kV IEC, 61000-4-2 Level 4, ESD Contact Discharge test. The Air-Gap test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing.

Test Circuits/Timing Diagrams

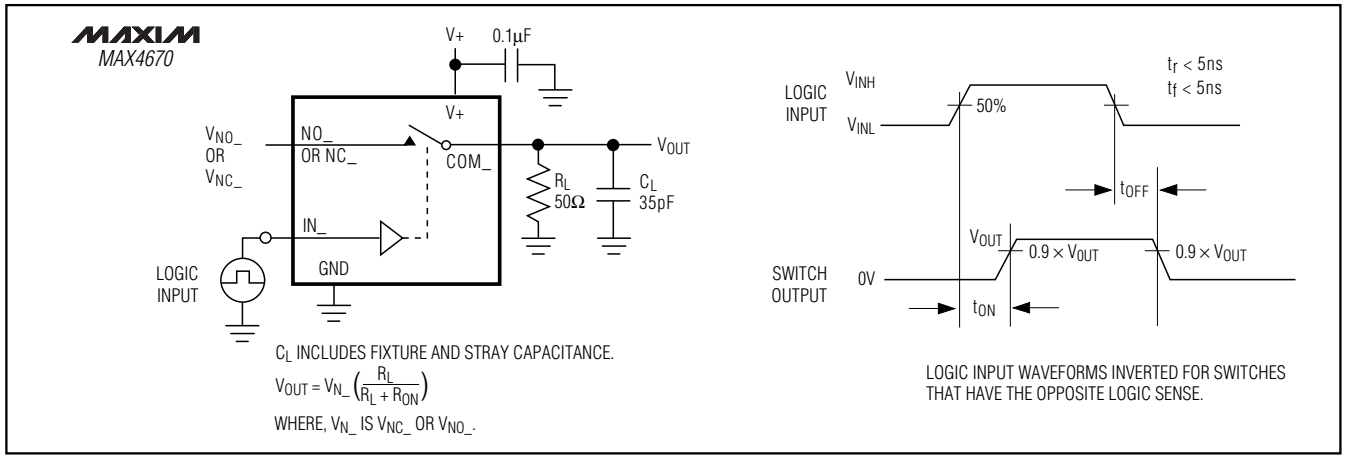


Figure 2. Switching Time

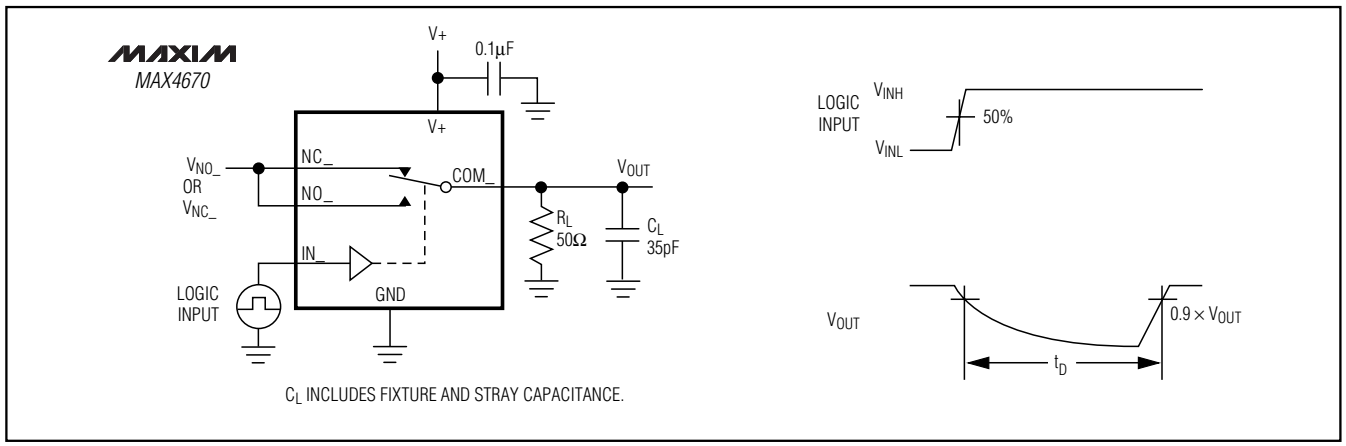


Figure 3. Break-Before-Make Intervals

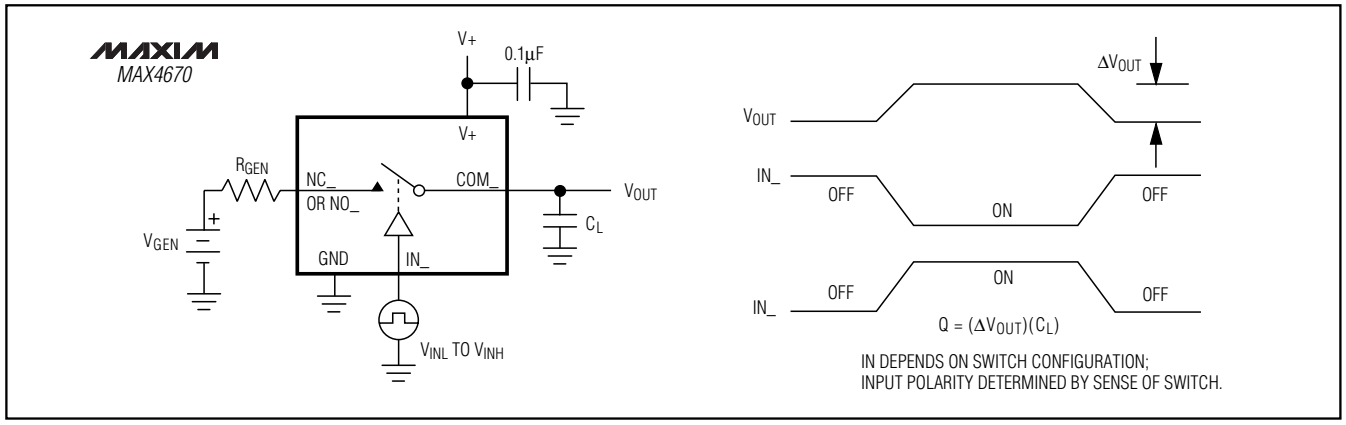


Figure 4. Charge Injection

Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

Test Circuits/Timing Diagrams (continued)

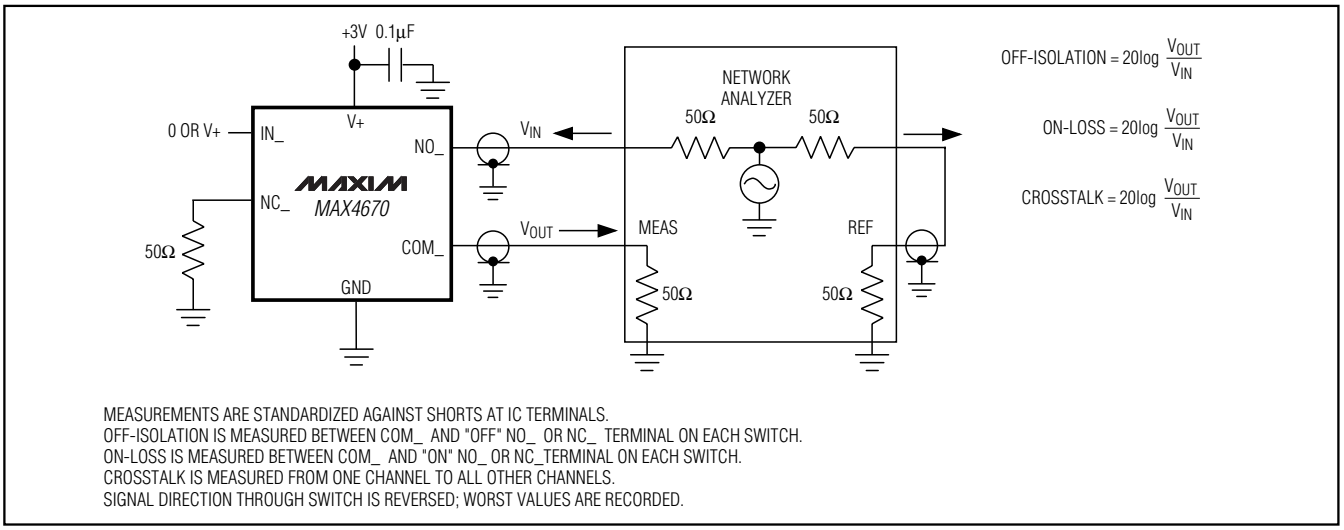


Figure 5. On-Loss, Off-Isolation, and Crosstalk

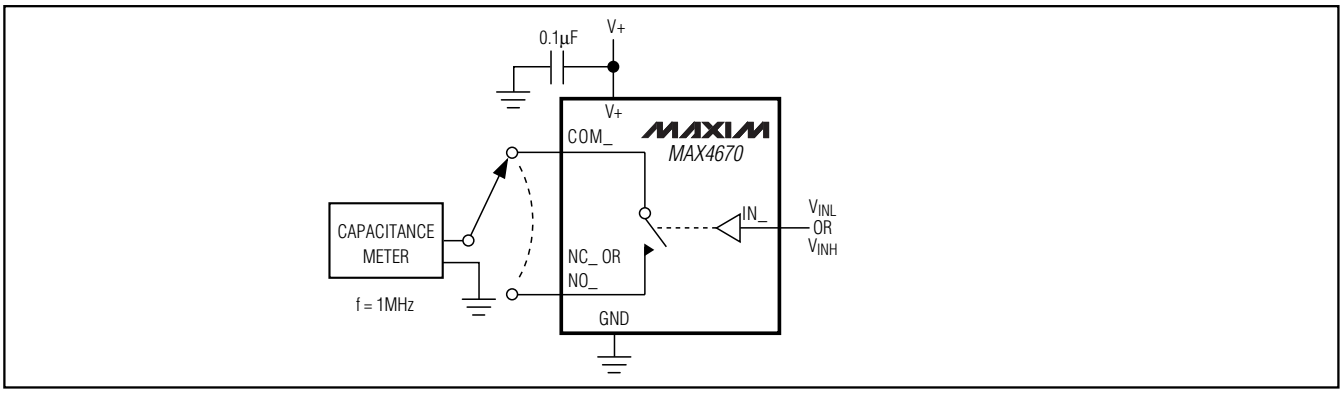


Figure 6. Channel Off-/On-Capacitance

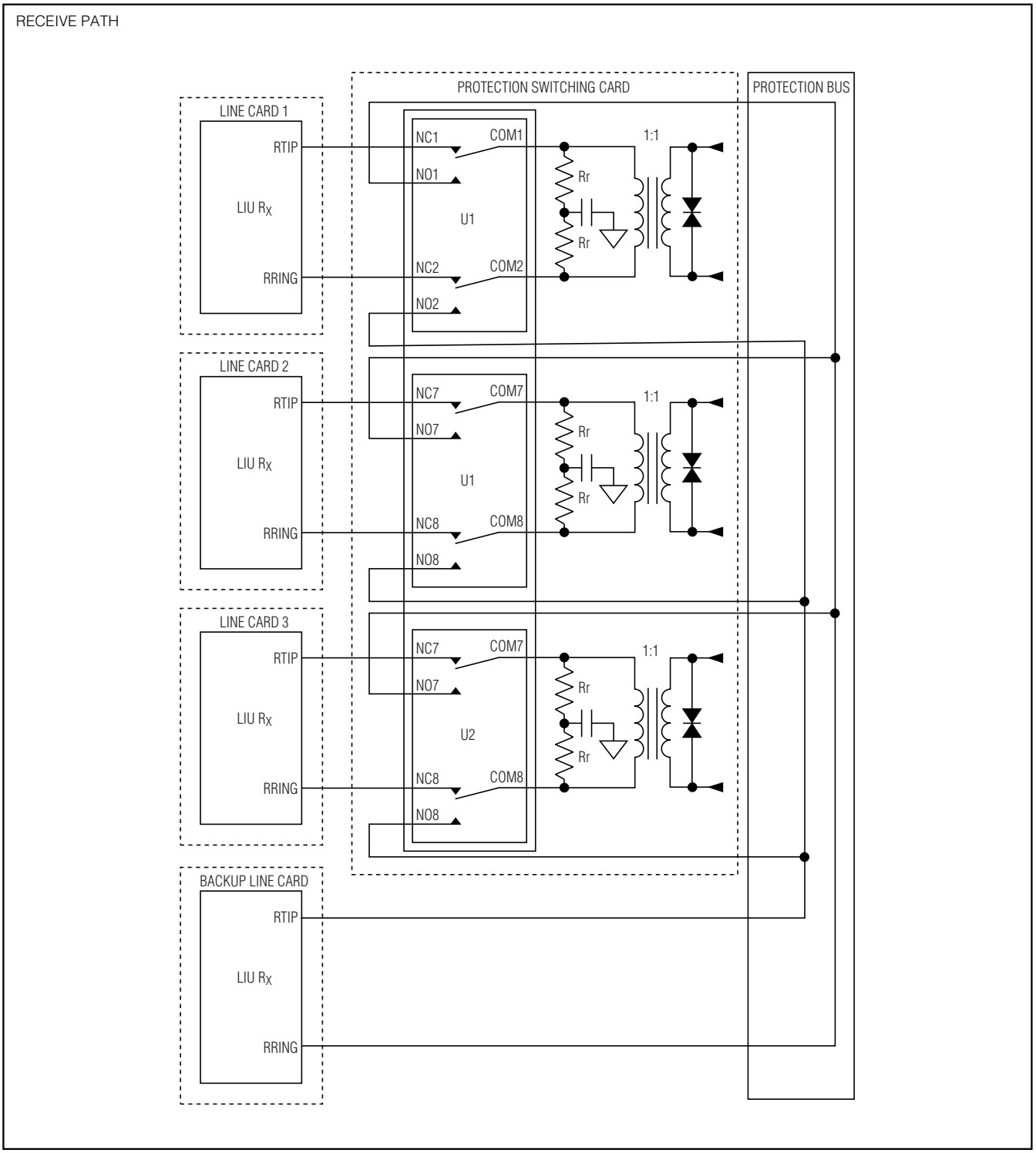


Figure 7. Switching-Card-Architecture Receive Path

Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

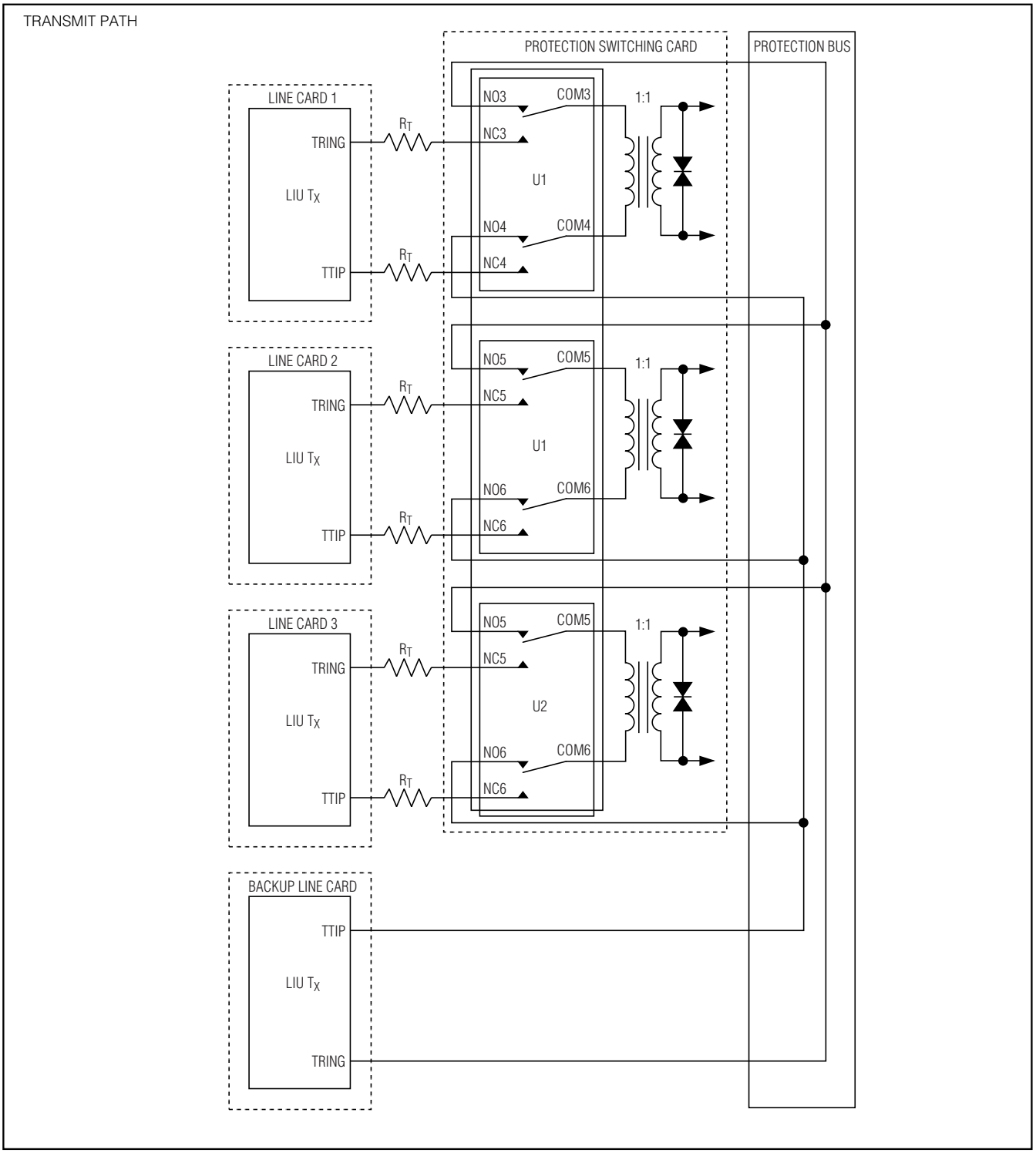


Figure 8. Switching-Card-Architecture Transmit Path

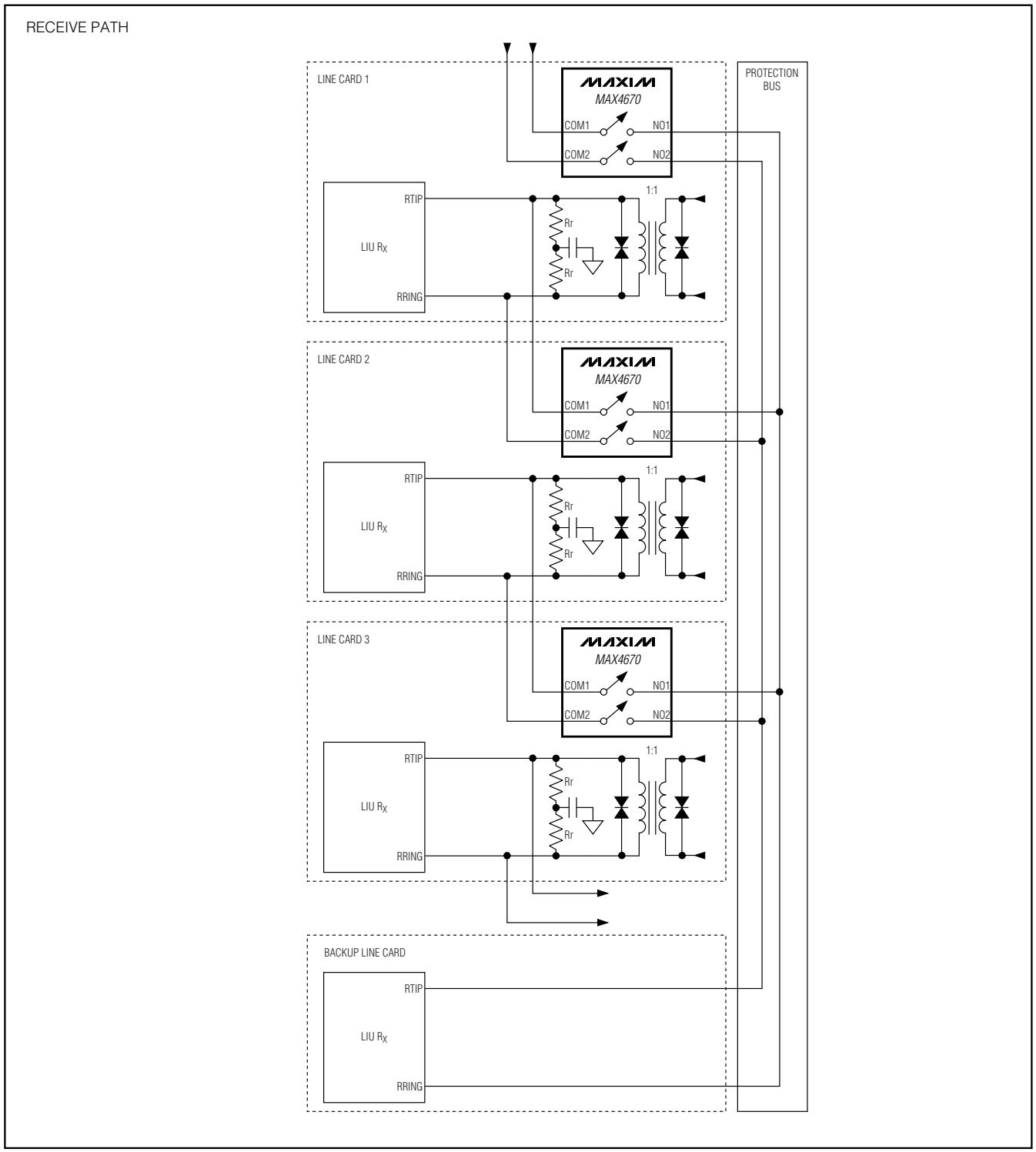


Figure 9. Adjacent-Card-Architecture Receive Path

Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

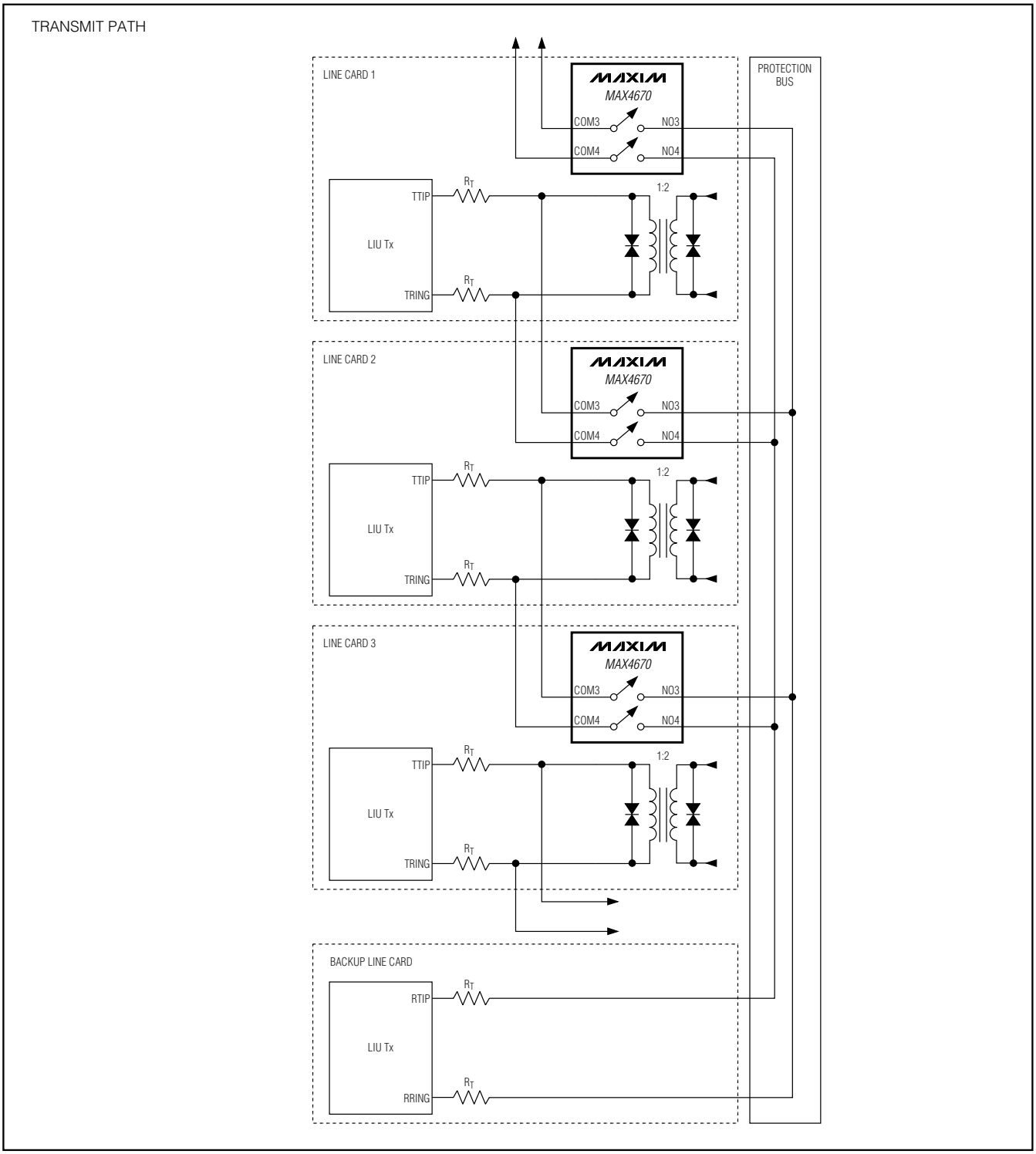


Figure 10. Adjacent-Card-Architecture Transmit Path

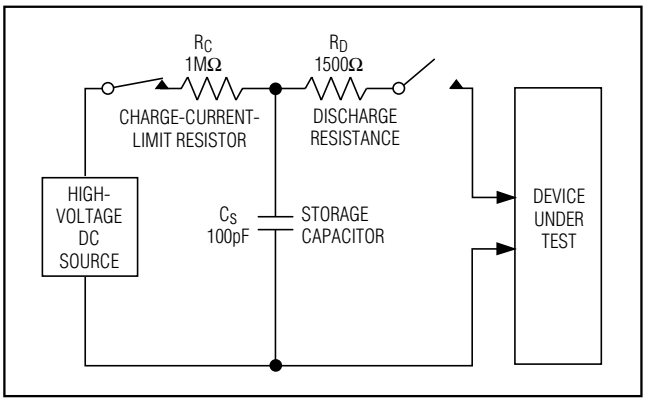


Figure 11. Human Body ESD Test Model

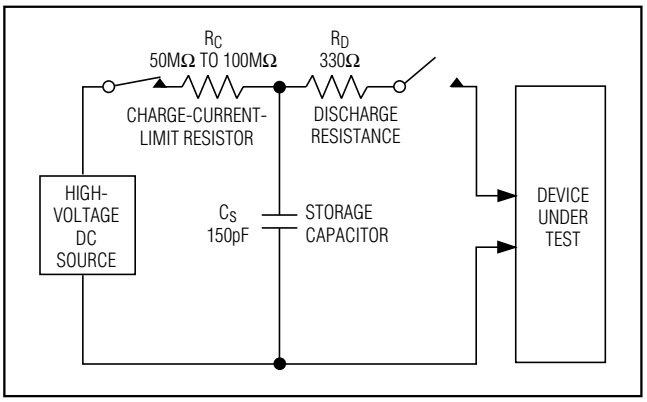


Figure 13. IEC 1000-4-2 ESD Test Model

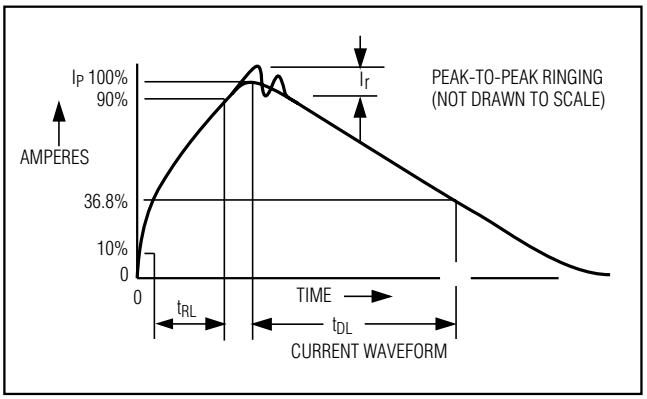


Figure 12. Human Body Model Current Waveform

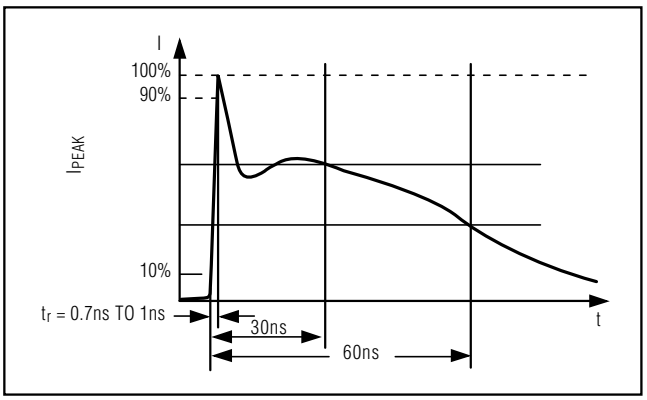
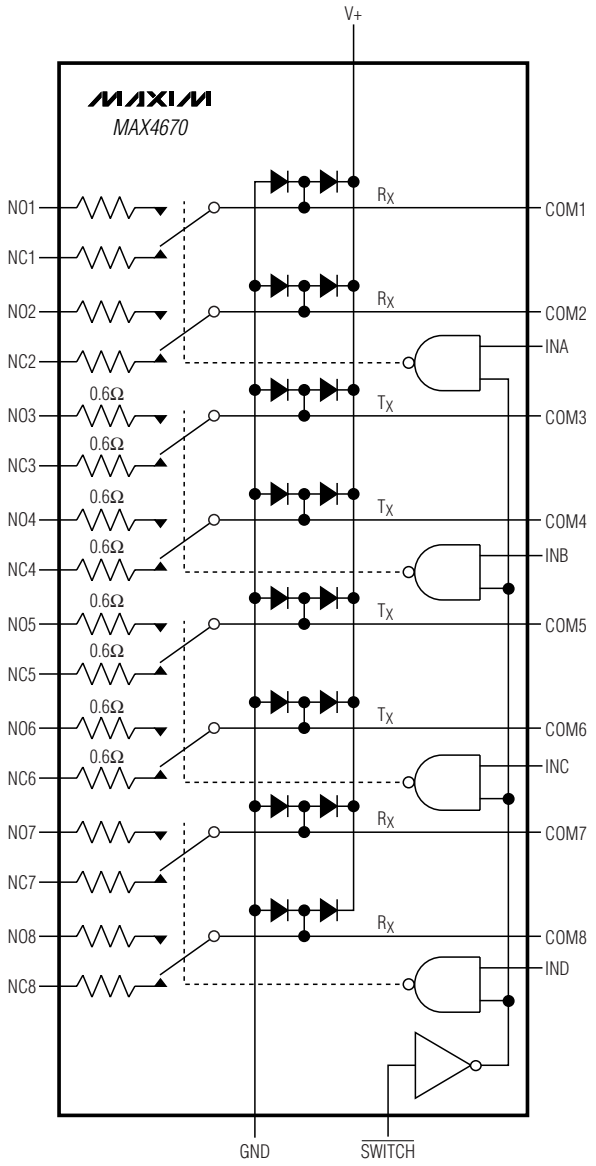


Figure 14. IED 1000-4-2 ESD Generator Current Waveform

Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

Functional Diagram/Truth Table



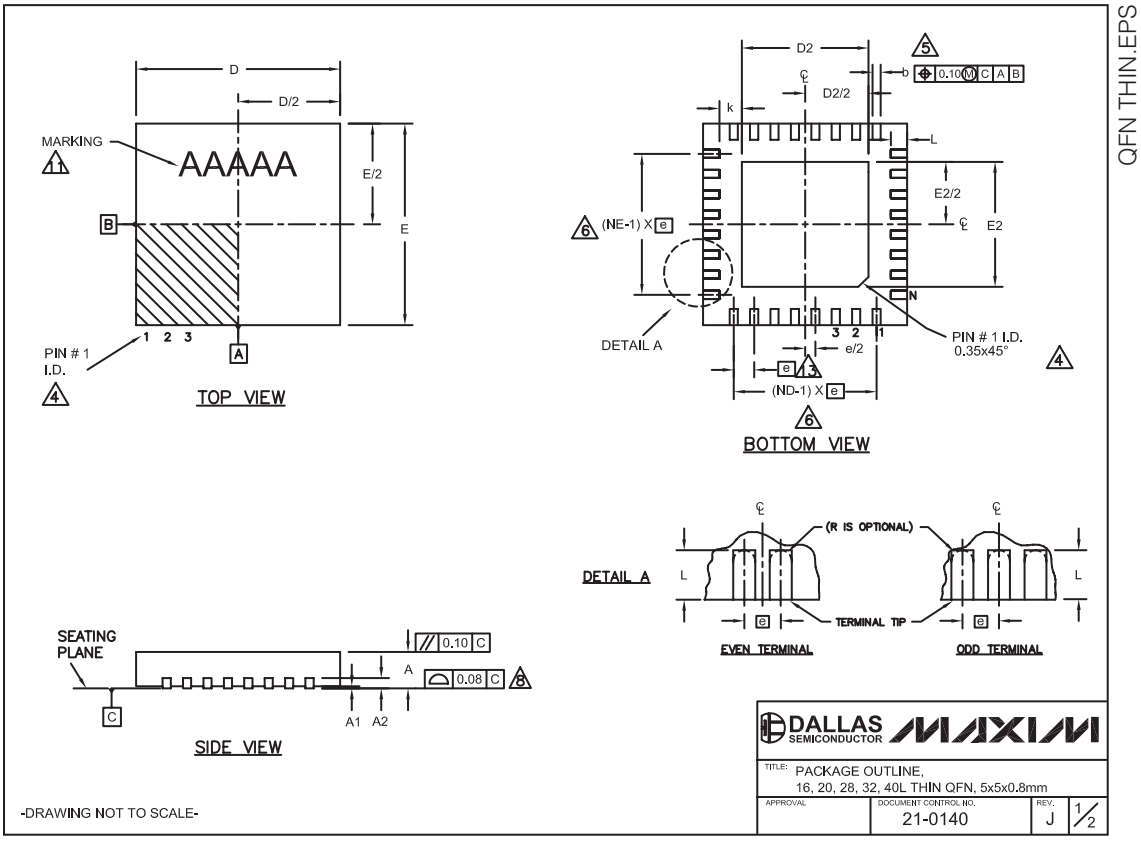
SWITCH	INA	NC1/NC2	NO1/NO2
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF
	INB	**NC3/NC4**	**NO3/NO4**
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF
	INC	**NC5/NC6**	**NO5/NO6**
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF
	IND	**NC7/NC8**	**NO7/NO8**
LOW	X	OFF	ON
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF

Chip Information

PROCESS: CMOS

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Integrated T1/E1/J1 Short-Haul and Long-Haul Protection Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			---			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	J	2/2