SN74GTL2107 12-BIT GTL-/GTL/GTL+ TO LVTTL TRANSLATOR

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SCLS699-JULY 2006

FEATURES

- Operates as a GTL-/GTL/GTL+ to LVTTL or LVTTL to GTL-/GTL/GTL+ Translator
- Series Termination on TTL Output of 30 Ω
- Latch-Up Testing Done to JEDEC Standard JESD 78
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

The SN74GTL2107 is a 12-bit translator that interfaces between the 3.3-V LVTTL chip set I/O and the Xeon™ processor GTL-/GTL/GTL+ I/O. The device is designed for platform health management in dual-processor applications.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V _{REF}	GTL reference voltage
2–6, 8, 10–13, 15, 23	ENn nAn	Data and enable inputs/outputs (LVTTL) on all inputs and pin 15 output. Remaining outputs are open drain.
7, 9, 16, 17–22, 24–27	nBn	Data inputs/outputs (GTL-/GTL/GTL+)
14	GND	Ground (0 V)
28	V _{CC}	Positive supply voltage

ORDERING INFORMATION

T _A	PACKAG	6E ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
40°C to 95°C	TCCOD DW	Tube	SN74GTL2107PW	CK2407	
-40°C to 85°C	TSSOP – PW Tape and reel		SN74GTL2107PWR	GK2107	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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FUNCTION TABLES(1)

INPU	TS	OUTPUT
EN1	1BI/2BI	1AO/2AO (OPEN DRAIN)
Н	L	L
Н	Н	Н
L	X	Н

(1) H = High voltage level, L = Low voltage level

INP	UTS	OUTPUT
EN2	3BI/4BI	3AO/4AO (OPEN DRAIN)
Н	L	L
Н	Н	Н
L	Χ	Н

INPUT 9BI	OUTPUT 9AO
L	L
Н	Н

INPU'	INPUTS OUTP			
10AI1/10AI2	9BI	10BO1/10BO2		
L	L	L		
L	Н	L		
Н	L	L		
Н	Н	Н		

INF	PUTS	INPUT/OUTPUT	OUTPUT		
EN2	5BI/6BI	5A/6A (OPEN DRAIN)	7BO1/7BO2		
Н	L	L	H ⁽¹⁾		
Н	Н	L ⁽²⁾	L		
Н	Н	Н	Н		
L	Н	L ⁽²⁾	L		
L	Н	Н	Н		
L	L	Н	Н		
L	L	L ⁽²⁾	Н		

- (1) The enable on 7BO1/7BO2 includes a delay that prevents a transient condition (where 5BI/6BI goes from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.
- (2) Open-drain input/output terminal is driven to a logic-low state by an external driver.

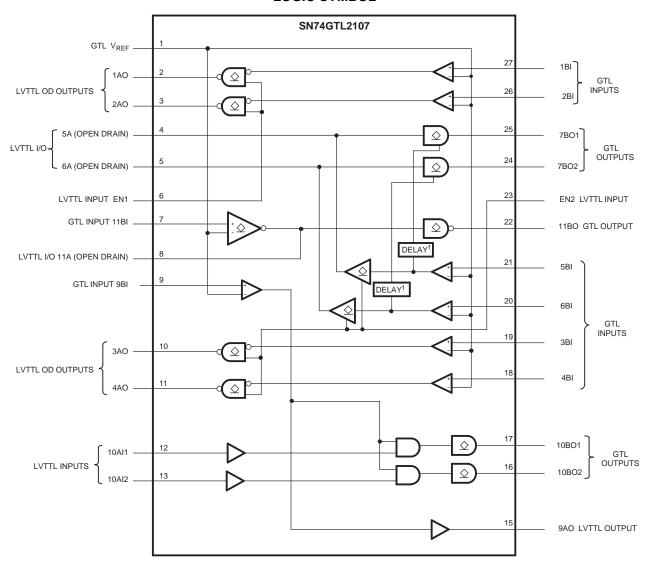
INPUT 11BI	INPUT/OUTPUT 11A (OPEN DRAIN)	OUTPUT 11BO
L	Н	L
L	L(1)	Н
Н	L	Н

 Open-drain input/output terminal is driven to a logic-low state by an external driver.



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LOGIC SYMBOL



(1) The enable on 7BO1/7BO2 includes a delay that prevents a transient condition (where 5BI/6BI go from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

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Absolute Maximum Ratings (1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V_{CC}	Supply voltage range		-0.5	4.6	V	
V	Input voltage range (3)	A port (LVTTL)	-0.5	4.6	V	
VI	input voitage range (*)	B port (GTL)	-0.5	4.6	V	
V	Output voltage range (output in OFF or HIGH state) ⁽³⁾	A port	-0.5	4.6	V	
Vo	Output voltage range (output in OFF of Fight State)	B port	-0.5	4.6	V	
I _{IK}	Input diode current	V _I < 0		-50	mA	
I _{OK}	Output diode current	V _O < 0		-50	mA	
	Current into any output in the LOW state	A port		32	mA	
	Current into any output in the LOW state	B port		30	IIIA	
	Current into any output in the HIGH state	A port		-32	mA	
θ_{JA}	Package thermal impedance (4)			62	°C/W	
T _{stg}	Storage temperature range		-60	150	°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltages are referenced to GND (ground = 0 V).

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
		GTL-	0.85	0.9	0.95	
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
		Overall	0.5	2/3 V _{TT}	1.8	
\ /	Defenses valtage	GTL-	0.5	0.6	0.63	.,
V_{REF}	Reference voltage	GTL	0.76	0.8	0.84	V
		GTL+	0.87	1	1.1	
.,	land altere	A port	0	3.3	3.6	.,
V _I	Input voltage	B port	0	V_{TT}	3.6	V
.,	I Pale Tarrel Conset codings	A port	2			.,
V_{IH}	High-level input voltage	B port	V _{REF} + 50 mV			V
.,	Landard Sandradtana	A port			0.8	
V_{IL}	Low-level input voltage	B port			V _{REF} – 50 mV	V
I _{OH}	High-level output current	A port			-16	mA
	Landard autout	A port			16	Δ
I _{OL}	Low-level output current	B port			3.3 3.6 0.9 0.95 1.2 1.26 1.5 1.65 V _{TT} 1.8 0.6 0.63 0.8 0.84 1 1.1 3.3 3.6 V _{TT} 3.6 V_{TT} 3.6 V_{TT} 0.8 $V_{REF} - 50 \text{ mV}$ -16	mA
T _A	Operating free-air temperature	<u>'</u>	-40		85	°C

⁽³⁾ The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

⁽⁴⁾ The performance capability of a high-performance integrated circuit, in conjunction with its thermal environment, can create junction temperatures that are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.

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Electrical Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	-40°C	to 85°C		UNIT	
	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNII	
V (2)	A nort	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}, I_{OH} = -100 \mu\text{A}$	V _{CC} - 0.2			V	
V _{OH} ⁽²⁾	A port	$V_{CC} = 3 \text{ V}, I_{OH} = -16 \text{ mA}$	2.1			V	
V (2)	A port	$V_{CC} = 3 \text{ V}, I_{OL} = 16 \text{ mA}$			8.0	V	
VOL(=)	B port	$V_{CC} = 3 \text{ V}, I_{OL} = 15 \text{ mA}$			0.4	V	
	A nort	$V_{CC} = 3.6 \text{ V}, V_{I} = V_{CC}$			±1		
I	A port	$V_{CC} = 3.6, V_I = 0 V$			±1	μΑ	
	B port	$V_{CC} = 3.6 \text{ V}, V_I = V_{TT} \text{ or GND}$			±1		
I _{CC}	A or B port	$V_{CC} = 3.6 \text{ V}, V_I = V_{CC} \text{ or GND}, I_O = 0$			12	mA	
$\Delta I_{CC}^{(3)}$	A port or control inputs	$V_{CC} = 3.6 \text{ V}, V_{I} = V_{CC} - 0.6 \text{ V}$			500	μΑ	
0	A port	V _O = 3 V or 0		5		~F	
C _{IO}	B port	V _O = V _{TT} or 0		4		pF	

- All typical values are at V_{CC} = 3.3 V, T_A = 25°C. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This is the increase in supply current for each input that is at the specified LVTTL voltage, rather than V_{CC} or GND.

Switching Characteristics

over recommended operating free-air temperature range

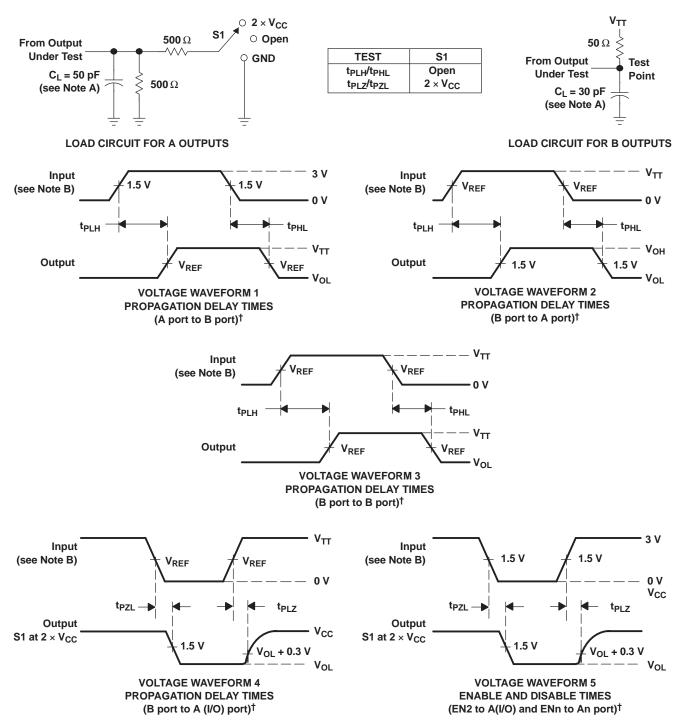
PARAMETER			GTL-		GTL			GTL+				
		WAVEFORM	V _{CC} = V _R	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{REF} = 0.6 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{REF} = 0.8 \text{ V}$			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V} $ $V_{REF} = 1 \text{ V}$			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
t _{PLH}	An to Bn	1	2	4	8	2	4	8	2	4	8	ns
t _{PHL}	All to Bil	ı	2	5.5	10	2	5.5	10	2	5.5	10	115
t _{PLH}	9BI to 9AO	2	2	5.5	10	2	5.5	10	2	5.5	10	ns
t_{PHL}	9BI 10 9AO	2	2	5.5	10	2	5.5	10	2	5.5	10	115
t _{PLH}	9BI to 10BOn	3	2	6	11	2	6	11	2	6	11	ns
t _{PHL}	961 to 106011	3	2	6	11	2	6	11	2	6	11	115
t _{PLH}	11BI to 11BO	3	2	8	13	2	8	13	2	8	13	ns
t _{PHL} ⁽²⁾	TIBITO TIBO	3	2	14	21	2	14	21	2	14	21	115
t _{PLH}	Bn to Bn	3	4	7	11	4	7	11	4	7	11	ns
t _{PHL}	BII to BII	3	120	205	350	120	205	350	120	205	350	115
t_{PLZ}	ENn to An	5	1	3	7	1	3	7	1	3	7	ns
t_{PZL}	LINII to All	3	1	3	7	1	3	7	1	3	7	113
t_{PLZ}	Bn to An (I/O)	4	2	5	10	2	5	10	2	5	10	ns
t_{PZL}	Bir to Air (I/O)	4	2	5	10	2	5	10	2	5	10	115
t_{PLZ}	Bn to An	4	2	5	10	2	5	10	2	5	10	ns
t_{PZL}	BIT to AII	7	2	5	10	2	5	10	2	5	10	115
t_{PLZ}	EN2 to An (I/O)	5	1	3	7	1	3	7	1	3	7	ns
t _{PZL}	EN2 to An (I/O)	ວ	1	3	7	1	3	7	1	3	7	115

⁽¹⁾ All typical values are measured at V_{CC} = 3.3 V and T_A = 25°C.

⁽²⁾ Includes –7.6-ns RC rise time of test-load pullup on 11 A, 1.5-kΩ pullup, and 21-pF load on 11 A has approximately 23-ns RC rise time.



PARAMETER MEASUREMENT INFORMATION V_{TT} = 1.2 V, V_{REF} = 0.8 V for GTL and V_{TT} = 1.5 V, V_{REF} = 1 V for GTL+



[†] All control inputs are LVTTL levels.

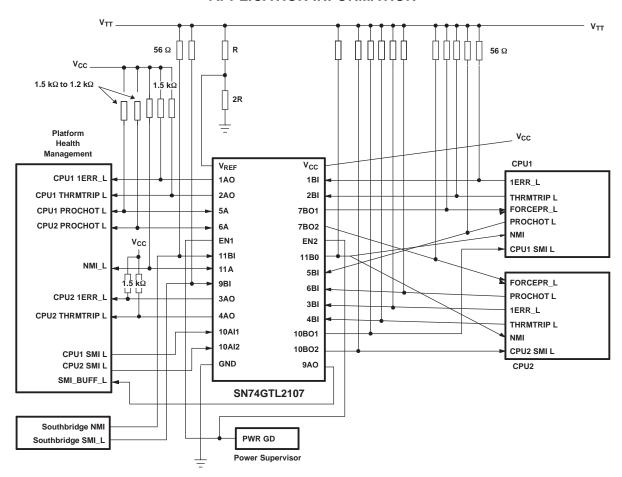
NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 $\Omega,\,t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns,
- C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



APPLICATION INFORMATION



Frequently Asked Questions

Question 1: On the SN74GTL2107 LVTTL input, specifically 10Al1 and 10Al2, when the SN74GTL2107 is powered down, these inputs may be pulled up to 3.3 V, and we want to ensure that there is no leakage path to the power rail under this condition. Are the LVTTL inputs high impedance when the device is powered down, and will there be any leakage?

Answer 1: When the device is powered down, the LVTTL inputs are in a high-impedance state and do not leak to V_{DD} if they are pulled high while the device is powered down.

Question 2: Do all the LVTTL inputs have the same powered-down characteristic?

Answer 2: Yes

Question 3: What is the condition of the other GTL I/O and LVTTL output pins when the device is powered down?

Answer 3: The open-drain outputs, both GTL and LVTTL, do not leak to the power supply if they are pulled high while the device is powered down. The GTL inputs also do not leak to the power supply under the same conditions. The LVTTL totem-pole outputs, however, are not open-drain type outputs, and there is current flow on these pins if they are pulled high when V_{DD} is at ground.



18-Jul-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74GTL2107PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2107PWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2107PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2107PWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

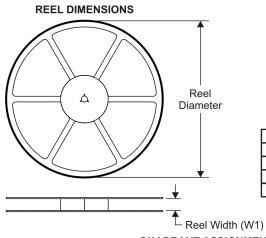
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

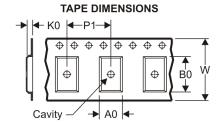
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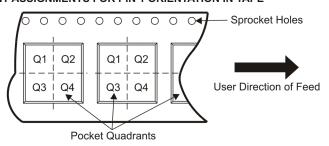
TAPE AND REEL INFORMATION





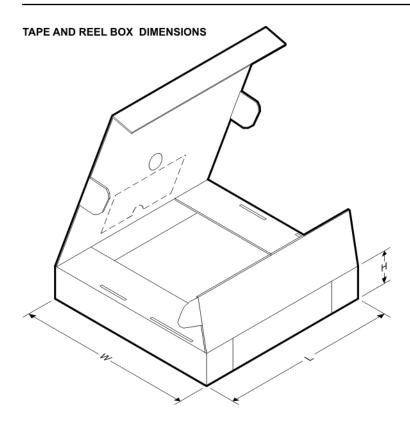
_		
	A0	Dimension designed to accommodate the component width
Γ	B0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
Γ	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL2107PWR	TSSOP	PW	28	2000	330.0	16.4	7.1	10.4	1.6	12.0	16.0	Q1



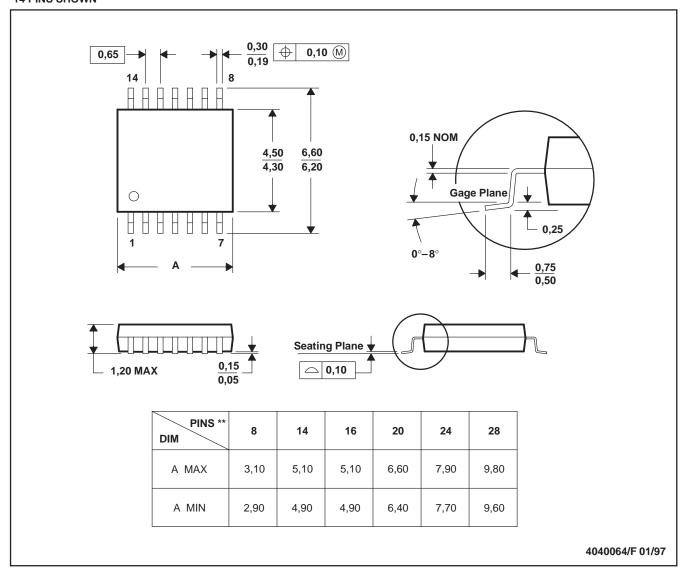
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL2107PWR	TSSOP	PW	28	2000	346.0	346.0	33.0

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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