4.5V to 18V Input, 3-A Synchronous Step-Down SWIFT™ Converter with Eco-Mode™

Check for Samples: TPS54326

FEATURES

- **D-CAP2™ Mode Enables Fast Transient Response**
- **Low Output Ripple and Allows Ceramic Output Capacitor**
- **Wide V_{CC} Input Voltage Range: 4.5 V to 18 V**
- **Wide V_{IN} Input Voltage Range: 2 V to 18 V**
- **Output Voltage Range: 0.76 V to 5.5 V**
- **Highly Efficient Integrated FET's Optimized for Lower Duty Cycle Applications - 120 mΩ (High Side) and 70 mΩ (Low Side)**
- **High Efficiency, less than 10 μA at Shutdown**
- **Auto-Skip Eco-Mode™ for High Efficiency at Light Load**
- **High Initial Bandgap Reference Accuracy**
- **Adjustable Soft Start**
- **Pre-Biased Soft Start**
- **700-kHz Switching Frequency (f_{SW})**
- **Cycle-By-Cycle Overcurrent Limit**
- **Power Good Output**

APPLICATIONS

- **Wide Range of Applications for Low Voltage System**
  - **Digital TV Power Supply**
  - **High Definition Blu-ray Disc™ Players**
  - **Networking Home Terminal**
  - **Digital Set Top Box (STB)**

DESCRIPTION

The TPS54326 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54326 enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54326 uses the D-CAP2™ mode control which provides a fast transient response with no external components. The adoptive on-time control supports seamless operation between PWM mode at heavy load condition and reduced frequency Eco-Mode™ operation at light load for high efficiency.

The TPS54326 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V V_{CC} input , and from 2-V to 18-V VIN input power supply voltage. The output voltage can be programmed between 0.76 V and 5.5 V. The device also features an adjustable slow start time and a power good function. The TPS54326 is available in the 14 pin HTSSOP or 16 pin QFN package, and designed to operate from −40°C to 85°C.
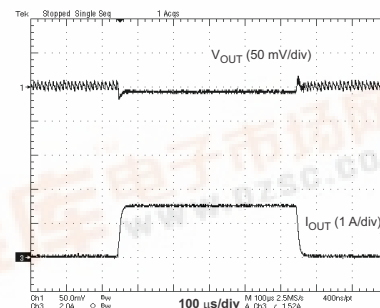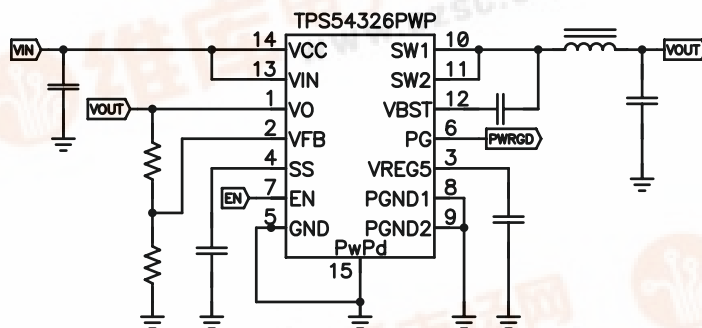
SWIFT, D-CAP2, Eco-Mode, PowerPAD are trademarks of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disc Association.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION[1]

T_A	PACKAGE[2] [3]	ORDERABLE PART NUMBER	PIN	TRANSPORT MEDIA, QUANTITY
−45°C to 85°C	PowerPAD™ (HTSSOP) – PWP	TPS54326PWP	14	Tube
		TPS54326PWPR		Tape and Reel, 2000
	Plastic Quad Flat Pack (QFN)	TPS54326RGTT	16	Tape and Reel, 250
		TPS54326RGTR		Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) All package options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

			VALUE	UNIT
V_I	Input voltage range	V_{IN}, V_{CC}, EN	−0.3 to 20	V
		V_{BST}	−0.3 to 26	V
		V_{BST} (vs SW1, SW2)	−0.3 to 6.5	V
		V_{FB}, V_O, SS, PG	−0.3 to 6.5	V
		SW1, SW2	−2 to 20	V
		SW1, SW2 (10 ns transient)	−3 to 20	V
V_O	Output voltage range	V_{REG5}	−0.3 to 6.5	V
		P_{GND1}, P_{GND2}	−0.3 to 0.3	V
V_{diff}	Voltage from GND to POWERPAD		−0.2 to 0.2	V
ESD rating	Electrostatic discharge	Human Body Model (HBM)	2	kV
		Charged Device Model (CDM)	500	V
T_J	Operating junction temperature		−40 to 150	°C
T_{stg}	Storage temperature		−55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS[1]

(2 oz. trace and copper pad with solder)

PACKAGE	θ_{JA}	T_A = 25°C POWER RATING	T_A = 85°C POWER RATING
PWP 14	44.5°C/W	2.25 W	0.9 W
RGT 16	47.4°C/W	2.10 W	0.84 W

(1) Rating based on JEDEC high thermal conductivity (High K) board with 2 x 2 arrays of thermal vias. See Texas Instruments application report (SLMA002) regarding thermal characteristic of the PowerPAD™ package.

Product Folder Link(s) :TPS54326

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply input voltage range		4.5	18	V
V_{IN}	Power input voltage range		2	18	V
V_I	Input voltage range	V_{BST}	−0.1	24	V
		V_{BST} (vs SW1, SW2)	−0.1	5.7	
		SS, PG	−0.1	5.7	
		EN	−0.1	18	
		V_O, V_{FB}	−0.1	5.5	
		SW1, SW2	−1.8	18	
		SW1, SW2 (10 ns transient)	−3	18	
		P_{GND1}, P_{GND2}	−0.1	0.1	
V_O	Output voltage range	V_{REG5}	−0.1	5.7	V
T_A	Operating free-air temperature		−40	85	°C
T_J	Operating junction temperature		−40	125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{CC}, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VCC}	Operating - non-switching supply current	V_{CC} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.8 V		850	1300	µA
I_{VCCSDN}	Shutdown supply current	V_{CC} current, T_A = 25°C, EN = 0 V		1.8	10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	2			V
V_{ENL}	EN low-level input voltage	EN			0.4	V
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FB}	Voltage light load mode	T_A = 25°C, V_O = 1.05 V, I_O = 10 mA		771		mV
V_{FB}	Threshold voltage, continuous mode	T_A = 25°C, V_O = 1.05 V	757	765	773	mV
		T_A = 0°C to 85°C, V_O = 1.05 V[1]	753		777	
		T_A = -40°C to 85°C, V_O = 1.05 V[1]	751		779	
I_{VFB}	Input current	V_{FB} = 0.8 V, T_A = 25°C		0	±0.1	µA
R_{Dischg}	V_O discharge resistance	EN = 0 V, V_O = 0.5 V, T_A = 25°C		50	100	Ω
V_{REG5} OUTPUT						
V_{VREG5}	Output voltage	T_A = 25°C, 6 V < V_{CC} < 18 V, 0 < I_{VREG5} < 5 mA	5.3	5.5	5.7	V
V_{LN5}	Line regulation	6 V < V_{CC} < 18 V, I_{VREG5} = 5 mA			20	mV
V_{LD5}	Load regulation	0 mA < I_{VREG5} < 5 mA			100	mV
I_{VREG5}	Output current	V_{CC} = 6 V, V_{REG5} = 4 V, T_A = 25°C		70		mA
MOSFET						
$R_{DS(on)h}$	High side switch resistance	25°C, V_{BST} - SW1, SW2 = 5.5 V		120		mΩ
$R_{DS(on)l}$	Low side switch resistance	25°C		70		mΩ
CURRENT LIMIT						
I_{ocl}	Current limit	L_{OUT} = 1.5µH [1]	3.5	4.1	5.5	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature [1]		150		°C
		Hysteresis [1]		25		
ON-TIME TIMER CONTROL						

(1) Specified by Design (not production tested).

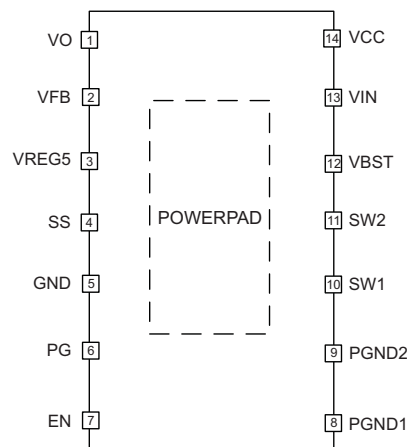## ELECTRICAL CHARACTERISTICS (continued)

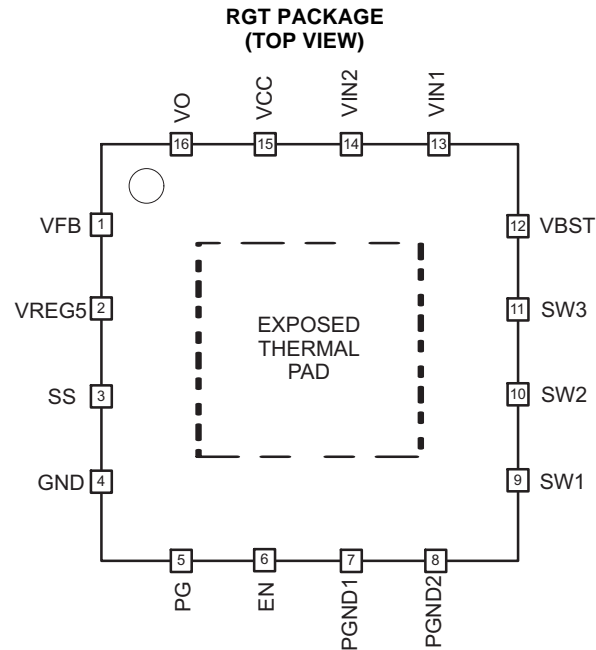over operating free-air temperature range, V_{CC}, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		145		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.7 V		260	310	ns
SOFT START						
I_{SSC}	SS charge current	V_{SS} = 0 V	1.4	2	2.6	µA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	0.1	0.2		mA
POWER GOOD						
V_{THPG}	Threshold	V_{FB} rising (good)	85	90	95	%
		V_{FB} falling (fault)		85		
I_{PG}	Sink current	PG = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	115	120	125	%
t_{OVPDEL}	Output OVP prop delay			5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65	70	75	%
		Hysteresis		10		
t_{UVPDEL}	Output UVP delay			0.25		ms
t_{UVPEN}	Output UVP enable delay	Relative to soft-start time		x 1.7		
UVLO						
UVLO	Threshold	Wake up V_{REG5} voltage	3.55	3.8	4.05	V
		Hysteresis V_{REG5} voltage	0.23	0.35	0.47	

DEVICE INFORMATION

PWP PACKAGE
(TOP VIEW)

PWP PACKAGE
(TOP VIEW)

```
        VO    [1]              [14]  VCC
        VFB   [2]              [13]  VIN
        VREG5 [3]              [12]  VBST
                  | POWERPAD |
        SS    [4]              [11]  SW2
        GND   [5]              [10]  SW1
        PG    [6]              [9]   PGND2
        EN    [7]              [8]   PGND1
```

**RGT PACKAGE
(TOP VIEW)**

PIN FUNCTIONS

| PIN			DESCRIPTION
NAME	PWP 14	RGT 16	
VO	1	16	Connect to output of converter. This pin is used for On-Time Adjustment.
VFB	2	1	Converter feedback input. Connect with feedback resistor divider.
VREG5	3	2	5.5 V power supply output. A capacitor (typical 1μF) should be connected to GND.
SS	4	3	Soft-start control. A external capacitor should be connected to GND.
GND	5	4	Signal ground pin
PG	6	5	Open drain power good output
EN	7	6	Enable control input
PGND1, PGND2	8, 9	7, 8	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2	10, 11	9, 10, 11	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparators.
VBST	12	12	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin.
VIN	13	13, 14	Power input and connected to high side NFET drain
VCC	14	15	Supply input for 5 V internal linear regulator for the control circuitry
Exposed Thermal Pad or PowerPAD ™	Back side	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND.

Functional Block Diagram
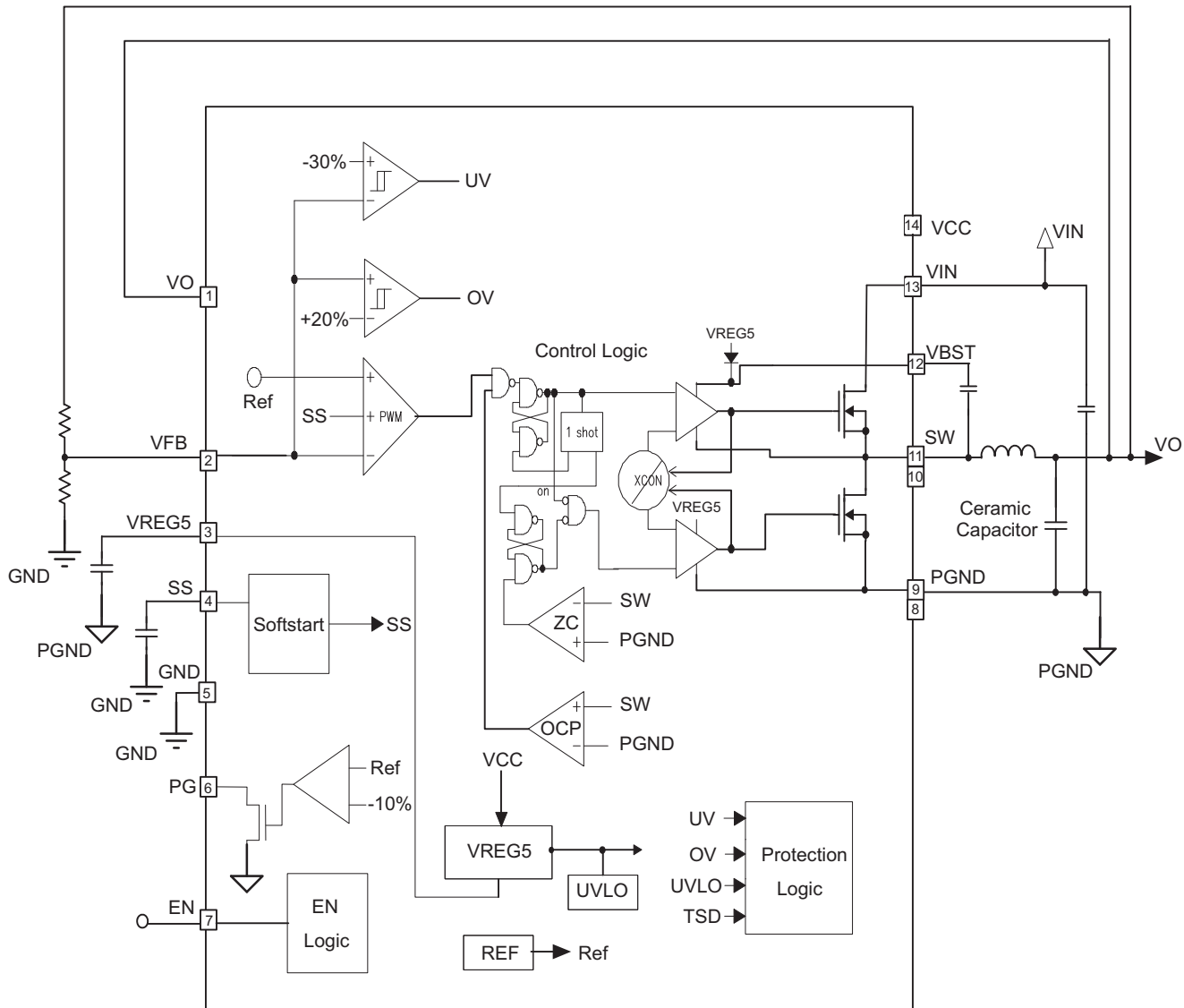
A.   Block diagram shown is for PWP 14 pin package. QFN 16 pin package block diagram is identical except for pin out.

OVERVIEW

The TPS54326 is a 3-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs and Auto-Skip Eco-Mode™ to improve light lode efficiency . It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS54326 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot timer is set by the converter input voltage ,V_{IN}, and the output voltage ,V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

PWM Frequency and Adaptive On-Time Control

TPS54326 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54326 runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. The actual frequency may vary from 700 kHz depending on the off time, which is ended when the fed back portion of the output voltage falls to the V_{FB} threshold voltage.

Light Load Eco-Mode™ Control

The TPS54326 is designed with Eco-Mode™ to increase light load efficiency . As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as is was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \bullet L \bullet fws} = \frac{(V_{IN} - V_{OUT}) \bullet V_{OUT}}{V_{IN}}$$

(1)

Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 2-μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 2. VFB voltage is 0.765 V and SS pin source current is 2 μA.

$$Tss(ms) = \frac{C6(nF) \bullet Vref}{Iss(\mu A)} = \frac{C6(nF) \bullet 0.765}{2}$$

(2)

A unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

Power Good

The power good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage is within -10% of the target value, internal comparators detect power good state and the power good signal becomes high. The power good output, PG, is an open drain output. If the feedback voltage goes under 15% of the target value, the power good signal becomes low after a 10 μs internal delay.

Output Discharge Control

TPS54326 discharges the output when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO and thermal shutdown). The output is discharged by an internal 50-Ω MOSFET which is connected from VO to PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

Current Protection

Output current is limited by cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller keeps the OFF state when the inductor current is larger than the over current trip level. To provide accuracy and a cost effective solution, the device supports temperature compensated internal MOSFET $R_{DS(on)}$ sensing.

The inductor current is monitored by the voltage between PGND pin and SW1/SW2 pin. In an overcurrent condition, the current to the load exceeds the current to the output capacitor; thus, the output voltage tends to fall off. Eventually the output voltage will fall below the undervoltage protection threshold and the device will shutdown.

Over/Undervoltage Protection

The TPS54326 detects over and undervoltage conditions by monitoring the feedback voltage (VFB). This function is enabled after approximately 1.7 times the soft-start time. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET turns on. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 μs, the device latches off both internal top and bottom MOSFET.

UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS54326 is shut off. This is protection is non-latching.

Thermal Shutdown

Thermal protection is self-activating. If the junction temperature exceeds the threshold value (typically 150°C), the TPS54326 shuts off. This protection is non-latching.
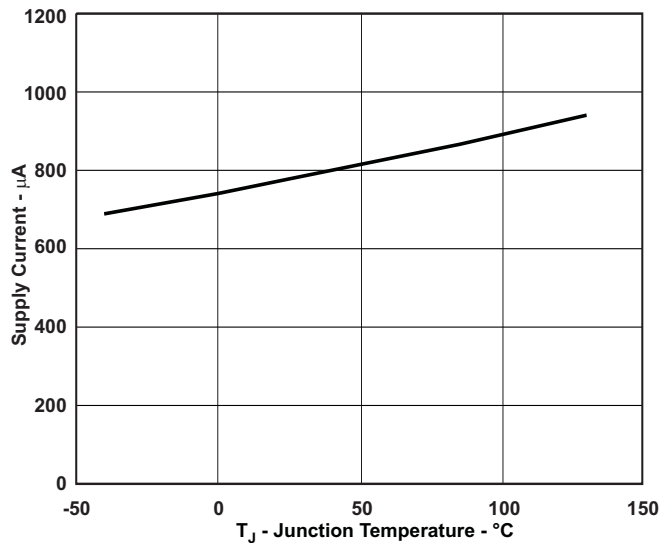
TYPICAL CHARACTERISTICS
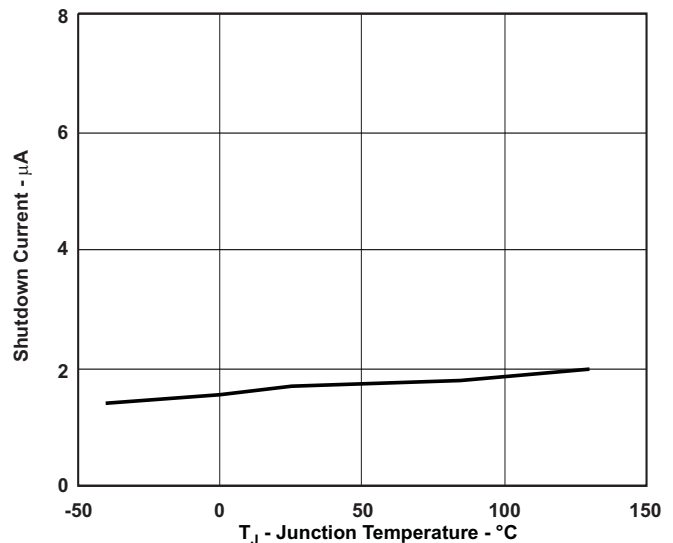

Figure 1. V$_{CC}$ SUPPLY CURRENT vs. JUNCTION TEMPERATURE

Figure 2. V$_{CC}$ SHUTDOWN CURRENT vs. JUNCTION TEMPERATURE

Product Folder Link(s) :*TPS54326*

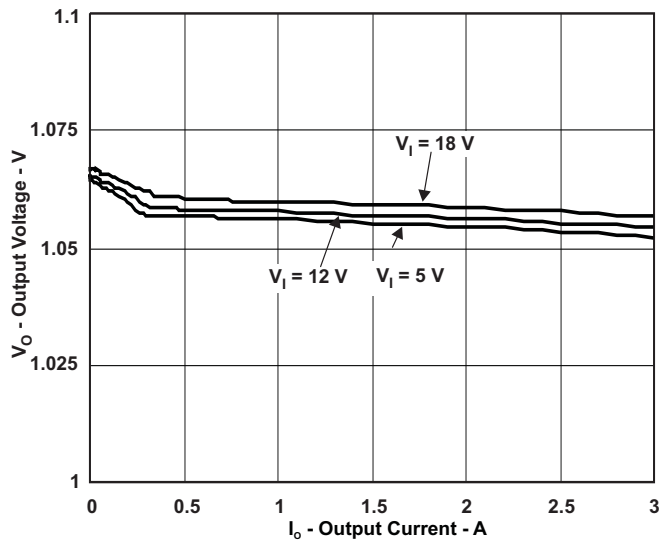
TPS54326

TYPICAL CHARACTERISTICS (continued)

Figure 3. 1.05-V OUTPUT VOLTAGE vs. OUTPUT CURRENT

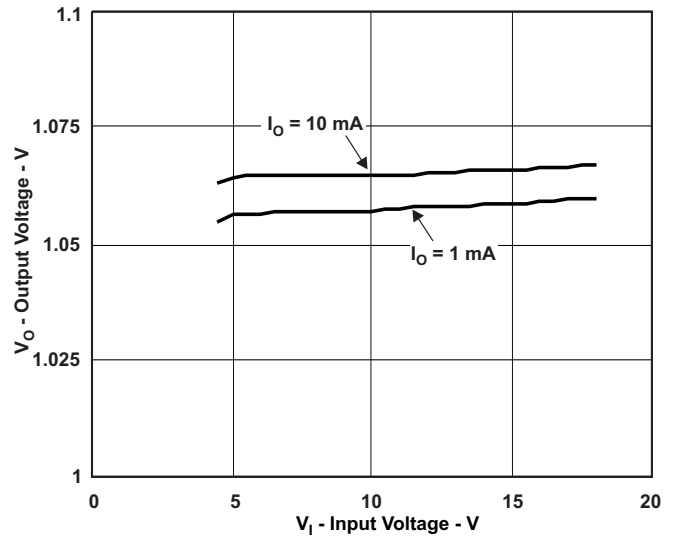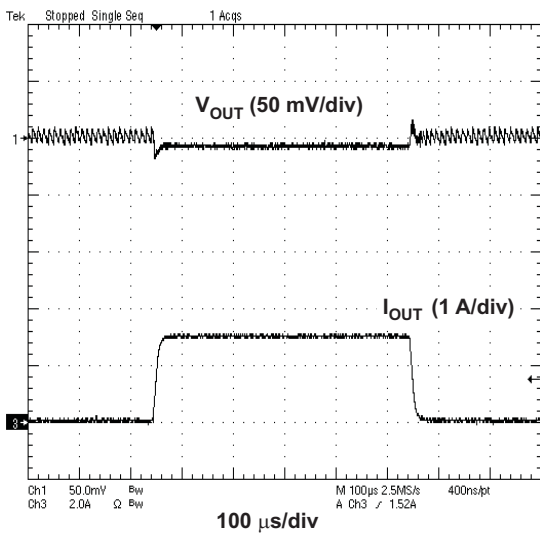
Figure 4. 1.05-V OUTPUT VOLTAGE vs. INPUT VOLTAGE

Figure 5. 1.05-V, 0-A TO 3-A LOAD TRANSIERESPONSE
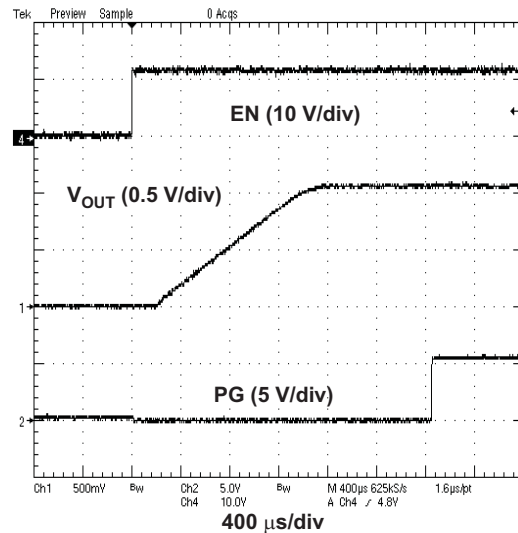

Figure 6. START-UP WAVE FORM

Product Folder Link(s) :TPS54326
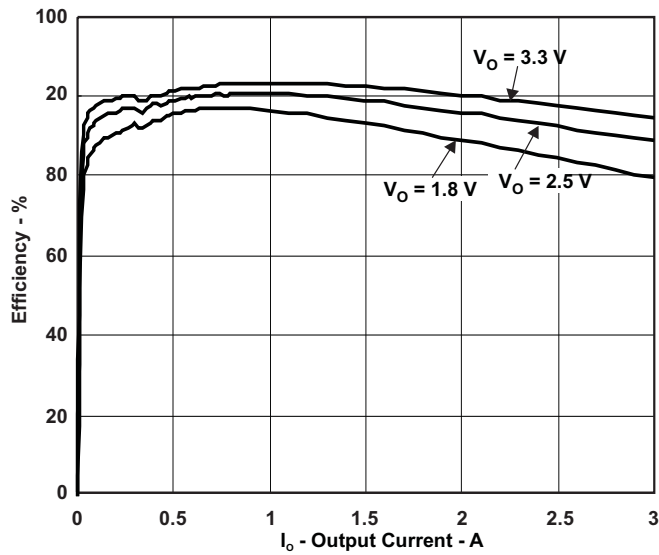
TYPICAL CHARACTERISTICS (continued)

Figure 7. EFFICIENCY vs. OUTPUT CURRENT
(V_{IN} = 12 V)

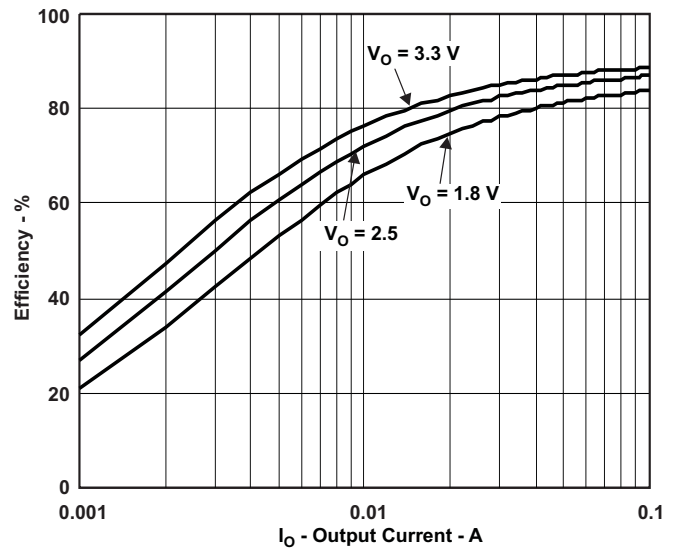Figure 8. LIGHT LOAD EFFICIENCY vs. OUTPUT
CURRENT

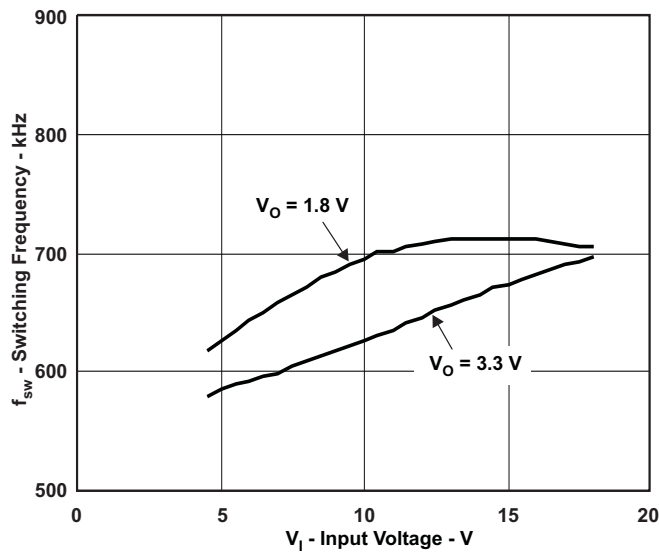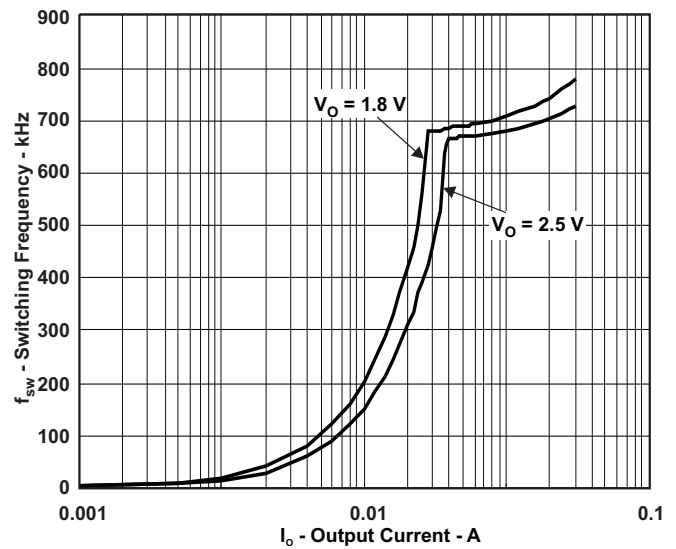Figure 9. SWITCHING FREQUENCY vs INPUT VOLTAGE

Figure 10. SWITCHING FREQUENCY vs OUTPUT
CURRENT

Product Folder Link(s) : TPS54326
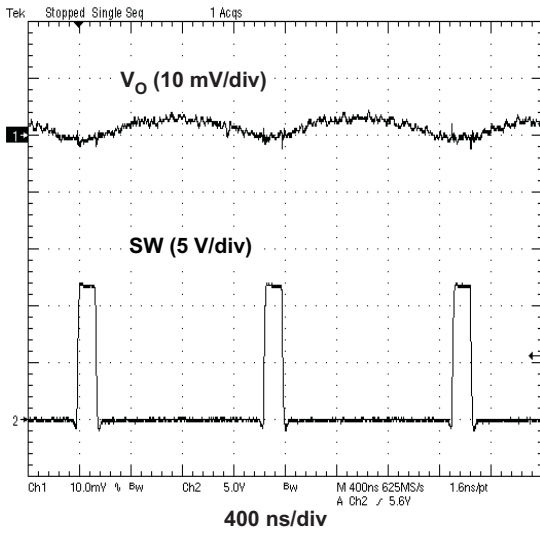
TYPICAL CHARACTERISTICS (continued)

Figure 11. VOLTAGE RIPPLE At OUTPUT
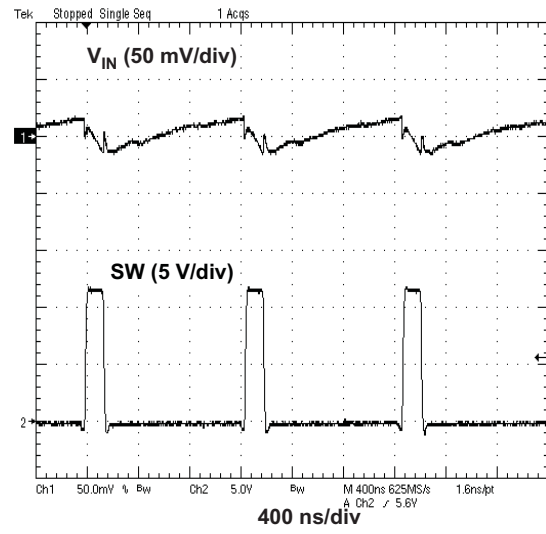
Figure 12. VOLTAGE RIPPLE At INPUT

TPS54326

DESIGN GUIDE

Step By Step Design Procedure

This example details the design of a switching regulator design using ceramic output capacitors.

This design is available as the HPA540 evaluation module (EVM). A few parameters must be known in order to start the design process. These parameters are typically determined on the system level. For this example, start with the following known parameters:

- Input voltage range = 4.5 - 18 V
- Output voltage = 1.05 V
- Output current = 3 A
- Output voltage ripple = 3% of output voltage, 31.5 mV

Figure 13 shows the schematic diagram for this design example.
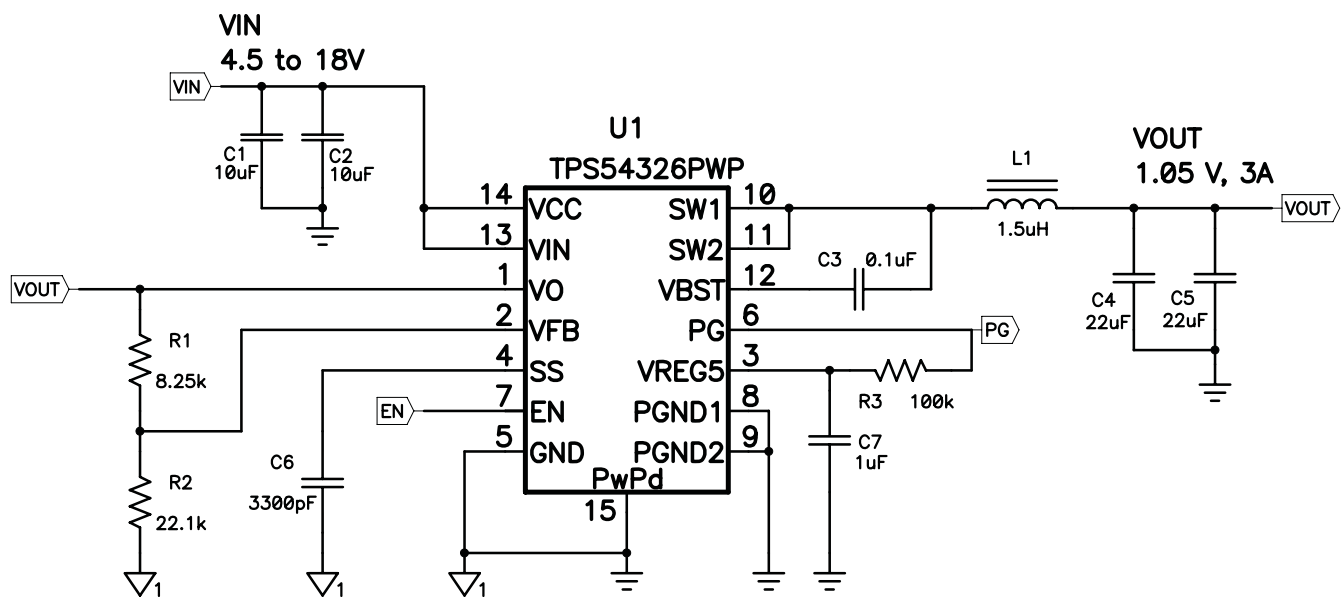
Figure 13. Schematic

Output Inductor Selection

The inductance value is selected to provide approximately 30% peak-to-peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improves S/N ratio and contributes to stable operation. Smaller ripple currents result in lower output voltage ripple. When using low ESR output capacitors output ripple voltage is usually low, so larger ripple currents are acceptable. The coefficient Kind represents the percentage of ripple current. The value of Kind must not be greater than 0.4. Use 0.3 when using low ESR output capacitors. Equation 3 can be used to calculate L1. Use 700 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$L_O = \frac{V_{OUT}}{V_{IN(max)}} \bullet \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \bullet f_{SW} \bullet Kind} \tag{3}$$

$$Ilp\text{-}p = \frac{V_{OUT}}{V_{IN(max)}} \bullet \frac{V_{IN(max)} - V_{OUT}}{L_O \bullet f_{SW}} \tag{4}$$

$$I_{lpeak} = I_O + \frac{Ilp\text{-}p}{2} \tag{5}$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} Ilp\text{-}p^2} \tag{6}$$

For this design example, use KIND = 0.3 and the inductor value is calculated to be 1.56 µH. For this design, a nearest standard value was chosen: 1.5 µH. For 1.5 µH, the calculated peak current is 3.47 A and the calculated RMS current is 3.012 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

Output Capacitor Selection

The capacitor value and ESR determines the amount of output voltage ripple. Recommended to use ceramic output capacitor. Using Equation 7 to Equation 9, an initial estimate for the capacitor value, ESR, and RMS current can be calculated. If the load transients are significant consider using the load step, instead of ripple current to calculate the maximum ESR.

$$C_O > \frac{1}{8 \bullet f_{SW}} \bullet \frac{1}{\left(\frac{V_{O(ripple)}}{I_{(ripple)}} - R_{ESR} \right)} \tag{7}$$

$$R_{ESR} < \frac{V_{O(ripple)}}{I_{l(ripple)}} \tag{8}$$

$$I_{CO(RMS)} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{\sqrt{12} \bullet V_{IN} \bullet L_O \bullet f_{SW}} \tag{9}$$

For this design, the minimum required capacitance is 8.45 µF and maximum ESR is 33 Ω. Two TDK C3216JB0J226M 22 µF output capacitors are used. The maximum ESR is 12 Ω each. The calculated RMS current is .271 A and each output capacitor is rated for 2 A.

Input Capacitor Selection

The device requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage. In case of separate V_{CC} and V_{IN}, then a ceramic capacitor over 10 µF is recommended for the V_{IN} and also placing ceramic capacitor over 0.1 µF for the V_{CC} is recommended.

Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

VREG5 Capacitor Selection

A 1-µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 10 and Equation 11 to calculate V_{OUT}.

To improve efficiency at light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

For output voltage from 0.76 V to 2.5 V:

$$V_{OUT} = 0.765 \bullet \left(1 + \frac{R1}{R2} \right) \tag{10}$$

For output voltage over 2.5 V:

$$V_{OUT} = (0.763 + 0.0017 \bullet V_{OUT}) \bullet \left(1 + \frac{R1}{R2} \right) \tag{11}$$

The required output voltage for this design is 1.05 V, so the equation of (add cross reference) is used to calculate the value of R1. With R2 = 22.1 kΩ, R1 is 8.25 kΩ.

THERMAL INFORMATION

The PWP 14 pin package incorporates an exposed PowerPAD™ and the QFN 16 pin package incorporates a similar exposed thermal pad. These exposed thermal pads are designed to be connected to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, see the Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for the PWP 14 pin and QFN 16 pin packages are shown in the Thermal Pad Mechanical Data section of this data sheet.

LAYOUT CONSIDERATIONS

The following layout guidelines are provided using the PWP 14 pin package as an example. The general guidelines and routing are also applicable to the QFN 16 pin package. Allowance should be made for the differences in the package pin configurations.

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. PCB pattern for VIN, SW, and PGND should be as broad as possible.
14. If VIN and VCC is shorted, VIN and VCC patterns need to be connected with broad pattern lines.
15. VIN Capacitor should be placed as near as possible to the device.
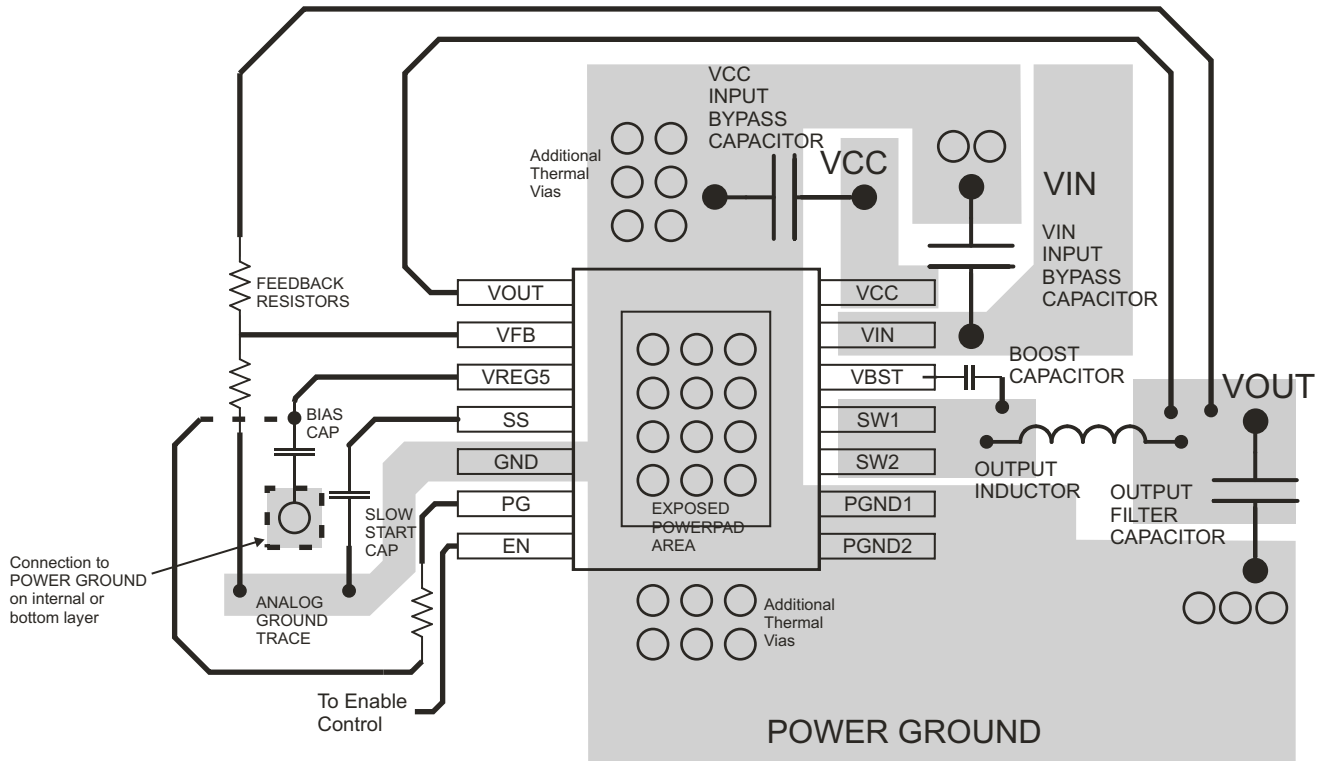
Figure 14. TPS54326 Layout

REVISION HISTORY

PACKAG

![Texas Instruments logo]

www.ti.com

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Pea
TPS54326PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
TPS54326PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
TPS54326RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
TPS54326RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

Reel Diameter

Reel Width (W1)

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1	Q2
Q3	Q4

Q1	Q2
Q3	Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54326PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS54326RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54326RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54326PWPR	HTSSOP	PWP	14	2000	346.0	346.0	29.0
TPS54326RGTR	QFN	RGT	16	3000	346.0	346.0	29.0
TPS54326RGTT	QFN	RGT	16	250	190.5	212.7	31.8

"TPS54326"

PWP (R−PDSO−G**)   PowerPAD™ PLASTIC SMALL−OUTLINE PACKAGE
20 PIN SHOWN

0,65

0,30
0,19   ⊕ 0,10Ⓜ

20   11

Thermal Pad
(See Note D)

4,50   6,60
4,30   6,20

0,15 NOM

Gage Plane

0,25

1   10

0°−8°

0,75
0,50

A

1,20 MAX

0,15
0,05

Seating Plane

0,25

⌒ 0,10

DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60
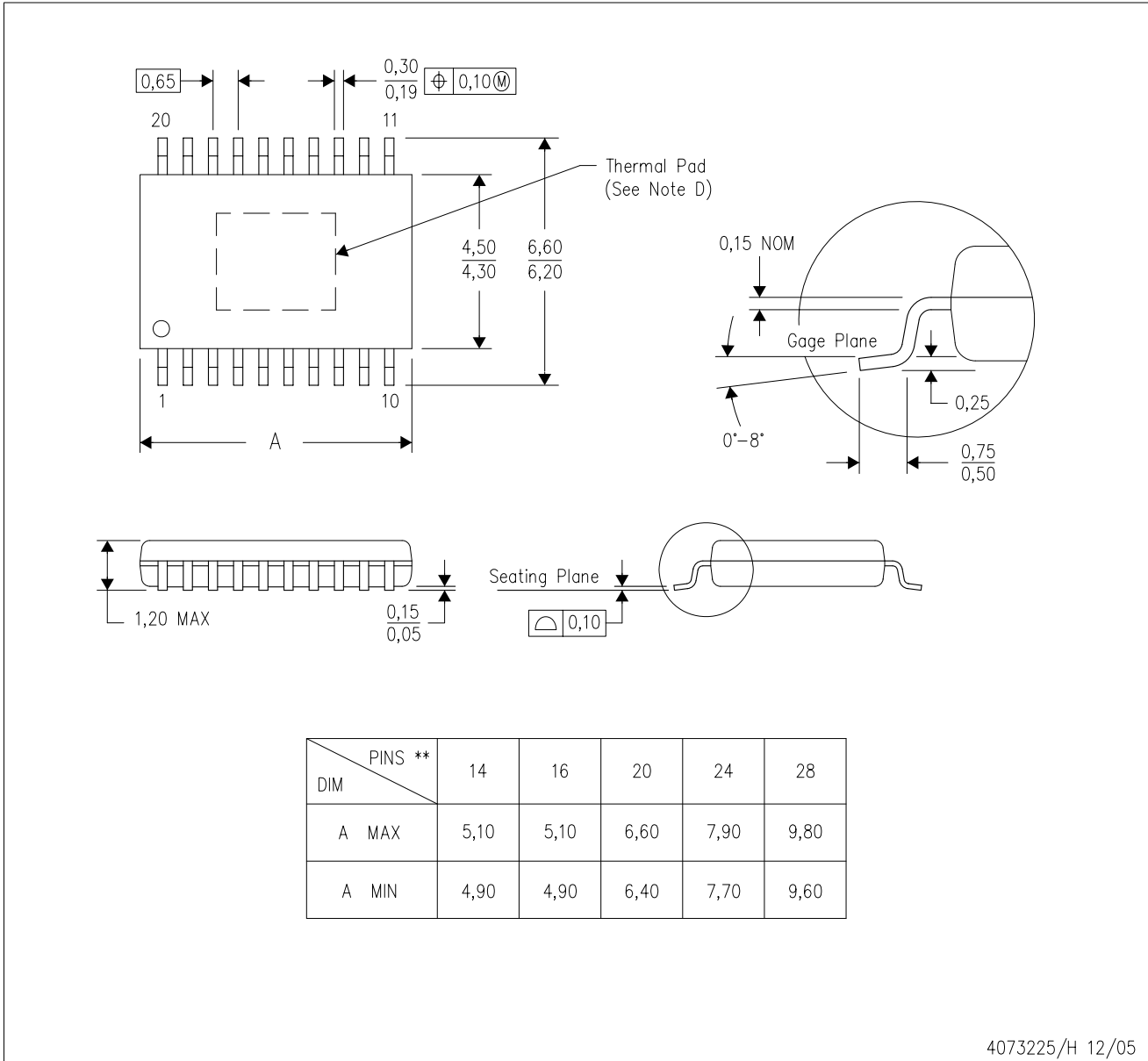
4073225/H 12/05

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
         E.   Falls within JEDEC MO−153

PowerPAD is a trademark of Texas Instruments.

PWP (R-PDSO-G14)   PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

14   8

Exposed Thermal Pad

$\frac{2,46}{1,65}$

1   7

$\frac{2,31}{1,35}$
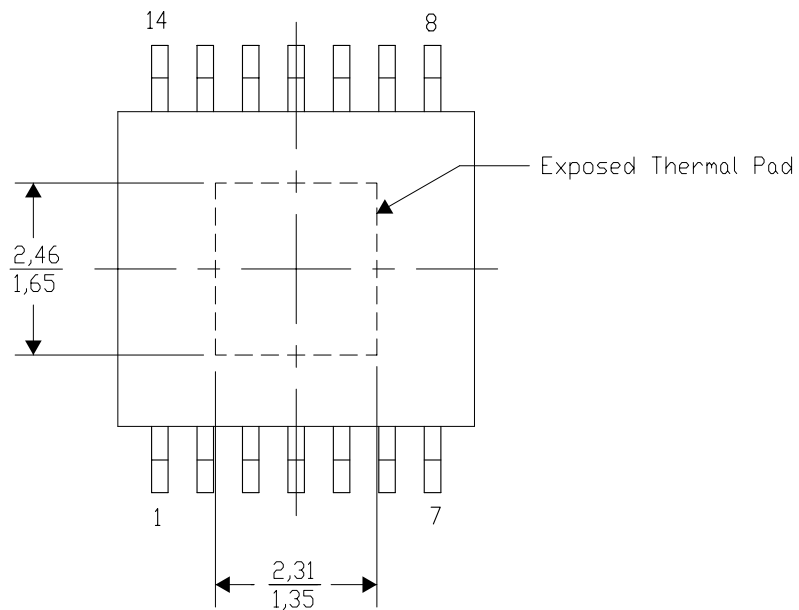
Top View

Exposed Thermal Pad Dimensions

4206332-2/S   11/10

NOTE: A. All linear dimensions are in millimeters

"TPS54326"

PWP (R−PDSO−G14)   PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses

Increasing copper area will
enhance thermal performance
(See Note D)

4x1,5   12x0,65

solder mask
over copper

14x0,25

14x1,55

2,46 3,4 5,6

5,6 2,46 Y

X

(See Note E)
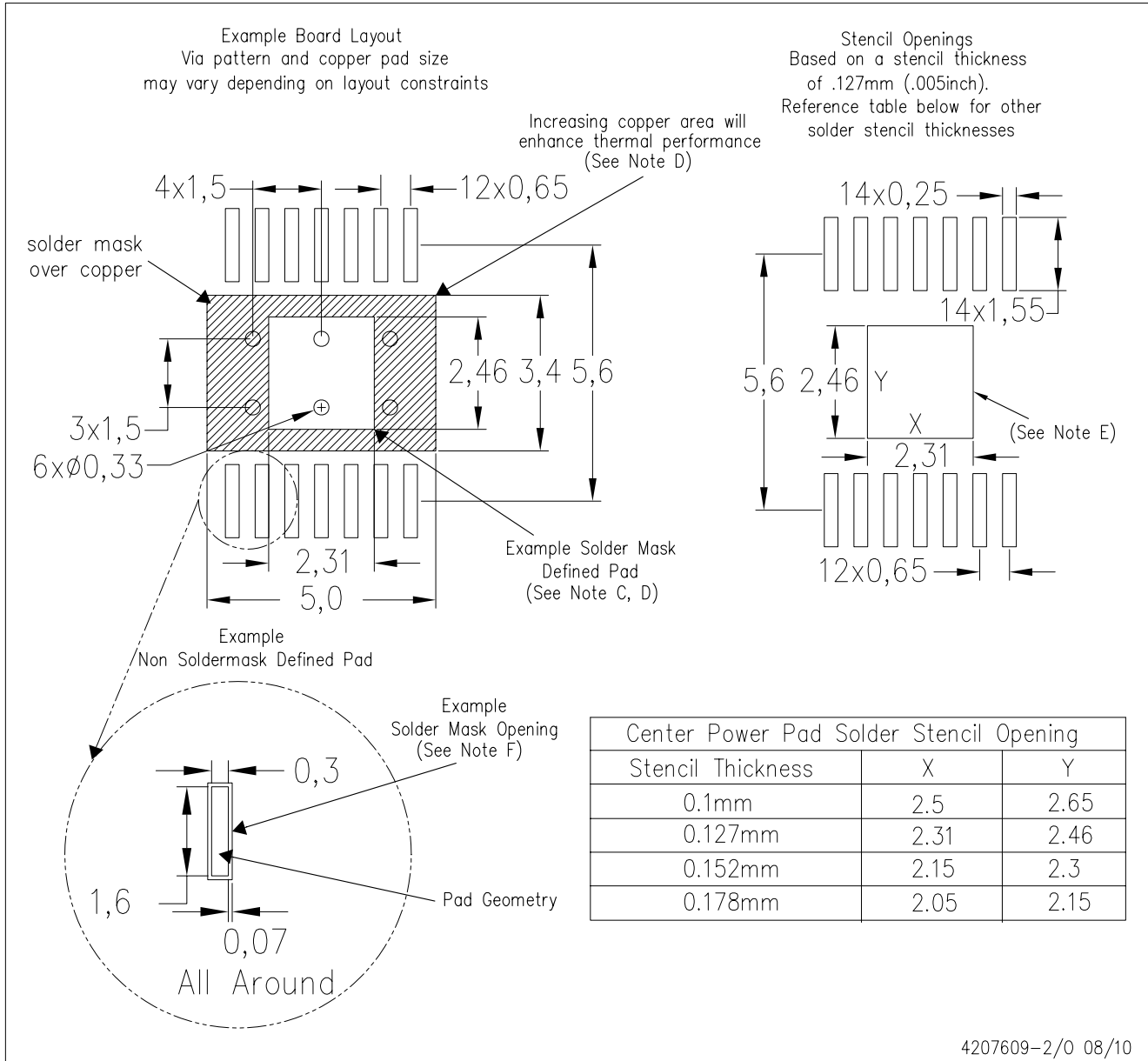
3x1,5

6xØ0,33

2,31

2,31

5,0

12x0,65

Example Solder Mask
Defined Pad
(See Note C, D)

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

0,07

All Around

Pad Geometry

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609−2/0 08/10
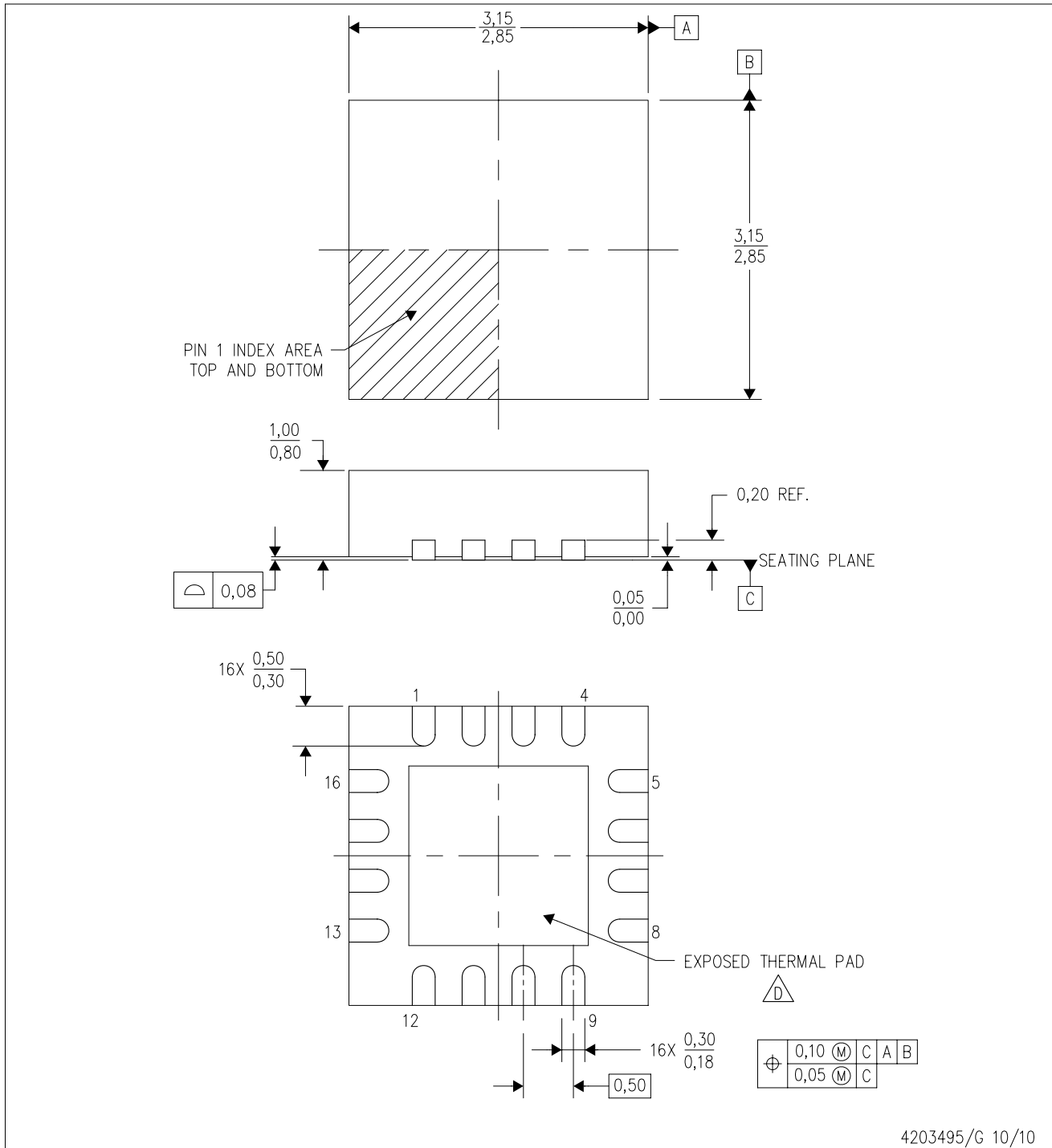
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
            Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout. These documents are available at
            www.ti.com <http://www.ti.com>. Publication IPC−7351 is recommended for alternate designs.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
            metal load solder paste. Refer to IPC−7525 for other stencil recommendations.
        F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
PowerPAD is a trademark of Texas Instruments.

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RGT (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

3,15 / 2,85   A

B

3,15 / 2,85

PIN 1 INDEX AREA
TOP AND BOTTOM

1,00 / 0,80

0,20 REF.

SEATING PLANE

0,08

0,05 / 0,00   C

16X 0,50 / 0,30

1   4

16   5

13   8

12   9

EXPOSED THERMAL PAD
D

16X 0,30 / 0,18

0,50

0,10 Ⓜ C A B
0,05 Ⓜ C

4203495/G 10/10

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         C. Quad Flatpack, No−leads (QFN) package configuration.
         D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
             See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
         E. Falls within JEDEC MO−220.
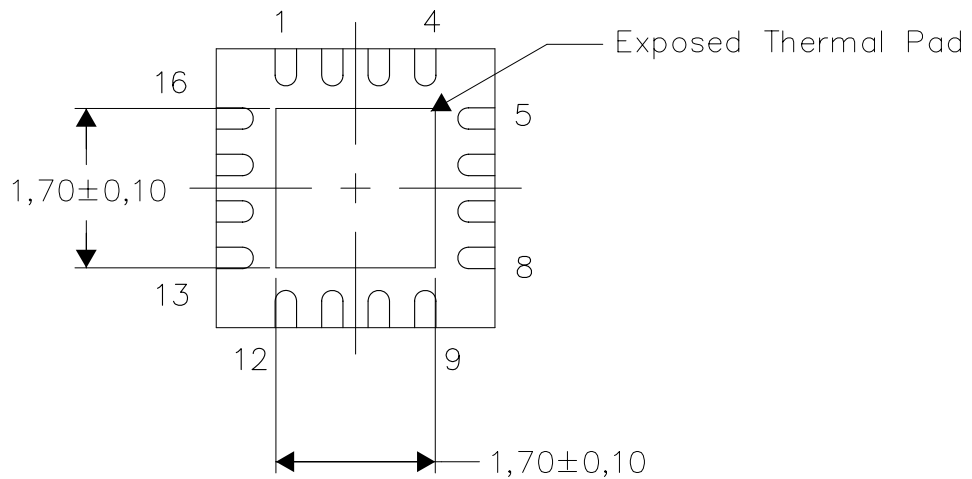
RGT (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

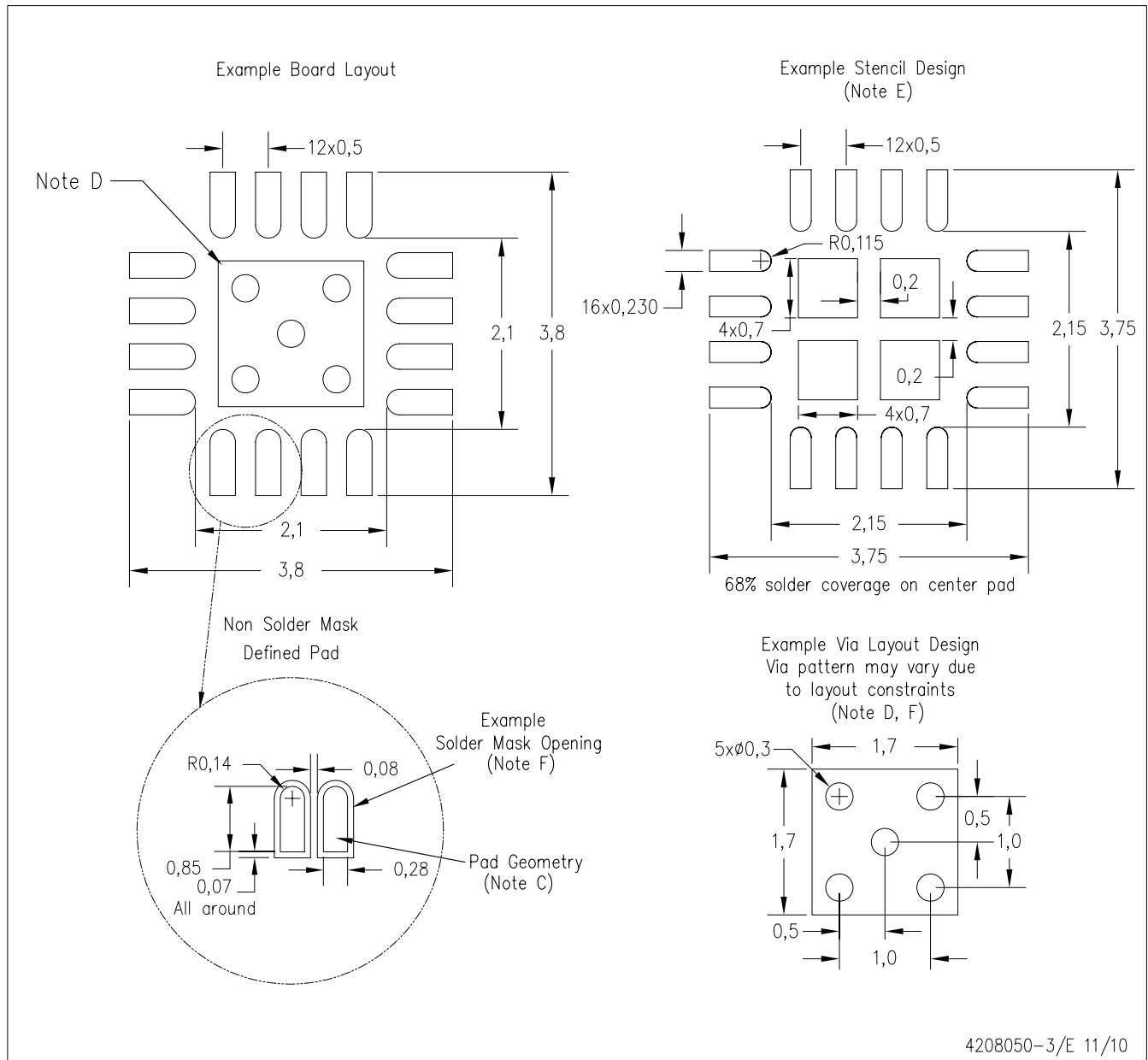The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad

1,70±0,10

1,70±0,10

Bottom View

Exposed Thermal Pad Dimensions

4206349−4/0 11/10

NOTE: A. All linear dimensions are in millimeters

"TPS54326"

RGT (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Note D

12x0,5

2,1 3,8

2,1

3,8

Non Solder Mask
Defined Pad

R0,14   0,08

0,85
0,07
All around

0,28

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

Example Stencil Design
(Note E)

12x0,5

R0,115

16x0,230

0,2

4x0,7

0,2

4x0,7

2,15 3,75

2,15

3,75

68% solder coverage on center pad

Example Via Layout Design
Via pattern may vary due
to layout constraints
(Note D, F)

5xØ0,3   1,7

1,7   0,5

1,0

0,5

1,0

4208050−3/E 11/10

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note,
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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"TPS54326"

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