MX29LV040C

4M-BIT [512K x 8] CMOS SINGLE VOLTAGE 3V ONLY EQUAL SECTOR FLASH MEMORY

FEATURES

- Extended single - supply voltage range 2.7V to 3.6V
- 524,288 x 8 only
- Single power supply operation
  - 3.0V only operation for read, erase and program operation
- **Fully compatible with MX29LV040 device**
- Fast access time: 55R/70/90ns
- Low power consumption
  - 30mA maximum active current
  - 0.2uA typical standby current
- Command register architecture
  - 8 equal sector of 64K-Byte each
  - Byte Programming (9us typical)
  - Sector Erase (Sector structure 64K-Byte x8)
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability
  - Automatically program and verify data at specified address
- Erase suspend/Erase Resume
  - Suspends sector erase operation to read data from, or program data to, any sector that is not being erased, then resumes the erase
- Status Reply
  - Data# Polling & Toggle bit for detection of program and erase operation completion
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Any combination of sectors can be erased with erase suspend/resume function
- CFI (Common Flash Interface) compliant
  - Flash device parameters stored on the device and provide the host system to access
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Package type:
  - 32-pin PLCC
  - 32-pin TSOP
  - **All Pb-free devices are RoHS Compliant**
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash
- 20 years data retention

GENERAL DESCRIPTION

The MX29LV040C is a 4-mega bit Flash memory organized as 512K bytes of 8 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV040C is packaged in 32-pin PLCC and TSOP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29LV040C offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV040C has separate chip enable (CE#) and output enable (OE#) controls.

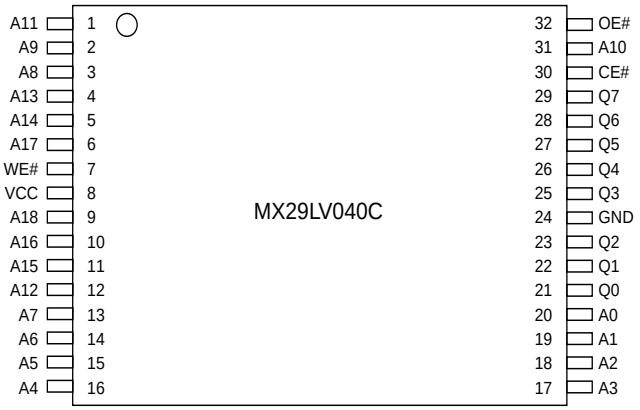
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LV040C uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX29LV040C uses a 2.7V~3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

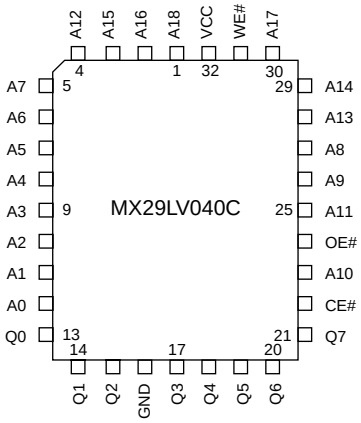
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamperes on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

32 TSOP (Standard Type) (8mm x 20mm)



32 PLCC



SECTOR STRUCTURE

Table 1. MX29LV040C SECTOR ADDRESS TABLE

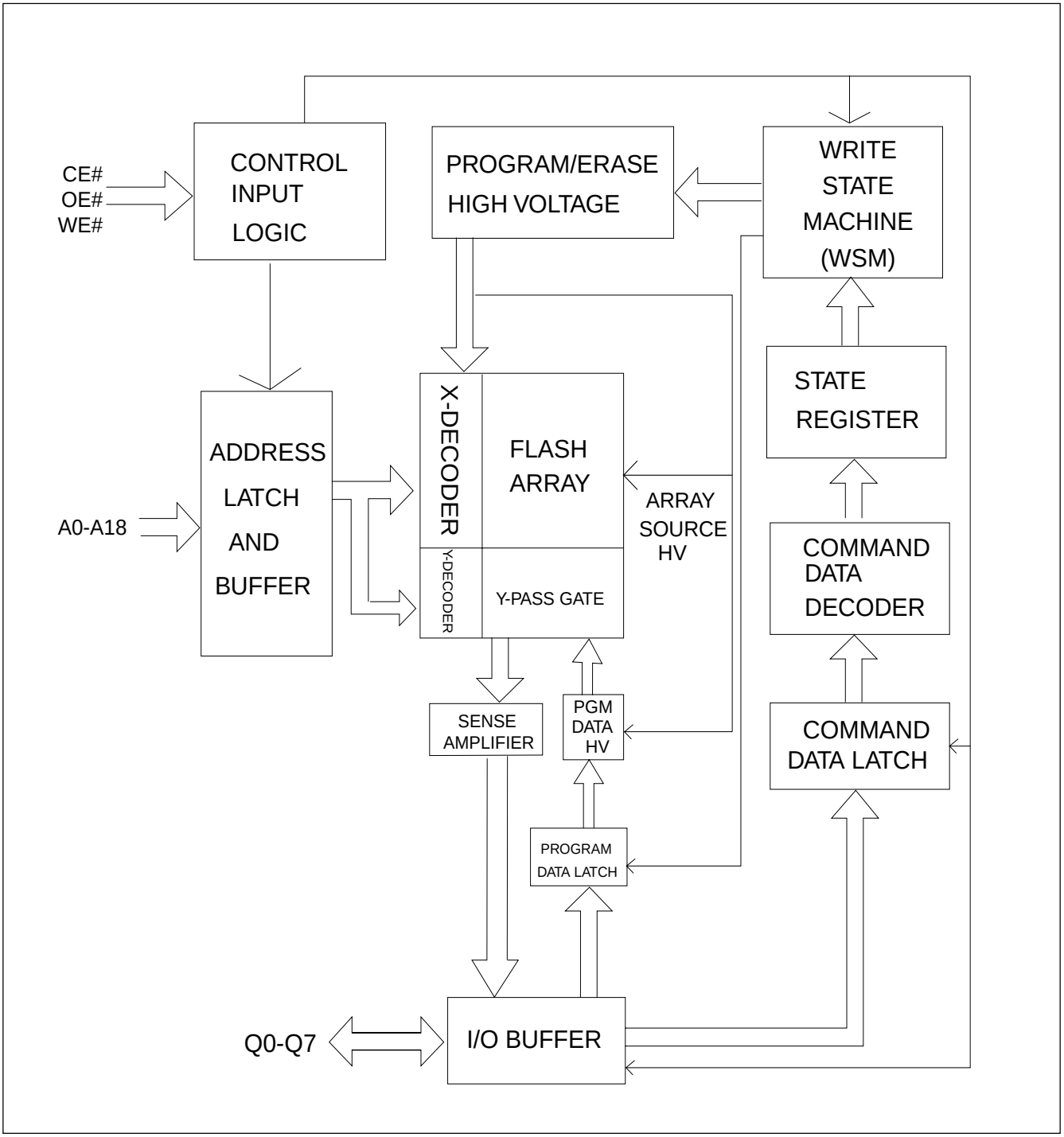
Sector	A18	A17	A16	Address Range
SA0	0	0	0	00000h-0FFFFh
SA1	0	0	1	10000h-1FFFFh
SA2	0	1	0	20000h-2FFFFh
SA3	0	1	1	30000h-3FFFFh
SA4	1	0	0	40000h-4FFFFh
SA5	1	0	1	50000h-5FFFFh
SA6	1	1	0	60000h-6FFFFh
SA7	1	1	1	70000h-7FFFFh

Note:All sectors are 64 Kbytes in size.

PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
GND	Ground Pin
VCC	+3.0V single power supply

BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX29LV040C is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX29LV040C is less than 10 seconds.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 4 second. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX29LV040C is sector(s) erasable using MXIC's Auto Sector Erase algorithm. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device. An erase operation can erase one sector, multiple sectors, or the entire device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to Data# Polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation. Refer to write operation status table 6, for more information on these status bits.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the erasing operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of WE# or CE#, whichever happens first.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29LV040C electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

AUTOMATIC SELECT

The automatic select mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on Q7~Q0. This mode is mainly adapted for programming equipment on the device to be programmed with its programming algorithm. When programming by high voltage method, automatic select mode requires VID (11.5V to 12.5V) on address pin A9 and other address pin A6, A1, and A0 as referring to Table 2. In addition, to access the automatic select codes in-system, the host can issue the automatic select command through the command register without requiring VID, as shown in table 3.

To verify whether or not sector being protected, the sector address must appear on the appropriate highest order address bit (see Table 1 and Table 2). The rest of address bits, as shown in table 3, are don't care. Once all necessary bits have been set as required, the programming equipment may read the corresponding identifier code on Q7~Q0.

TABLE 2. MX29LV040C AUTOMATIC SELECT MODE OPERATION

Description		CE#	OE#	WE#	A18 | A16	A15 | A10	A9	A8 | A7	A6	A5 | A2	A1	A0	Q7~Q0
Read	Manufacture Code	L	L	H	X	X	VID	X	L	X	L	L	C2H
Silicon ID	Device ID	L	L	H	X	X	VID	X	L	X	L	H	4FH
Sector Protection Verification		L	L	H	SA	X	VID	X	L	X	H	L	01H (protected)
													00H (unprotected)

NOTE:SA=Sector Address, X=Don't Care, L=Logic Low, H=Logic High

TABLE 3. MX29LV040C COMMAND DEFINITIONS

Command	Bus	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
	Cycle	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXXH	F0H										
Read	1	RA	RD										
Read Manufacture ID	4	555H	AAH	2AAH	55H	555H	90H	X00H	C2H				
Read Silicon ID	4	555H	AAH	2AAH	55H	555H	90H	X01H	4FH				
Sector Protect	4	555H	AAH	2AAH	55H	555H	90H	(SA)	00H				
Verify								x02H	01H				
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend	1	XXXH	B0H										
Sector Erase Resume	1	XXXH	30H										
CFI Query	1	AAH	98										

Note:
1. ADI = Address of Device identifier; A1=0, A0 = 0 for manufacturer code,A1=0, A0 = 1 for device code. A2-A18=do not care. (Refer to table 2)
   DDI = Data of Device identifier : C2H for manufacture code, 4FH for device code.
   X = X can be VIL or VIH
   RA=Address of memory location to be read.
   RD=Data to be read at location RA.
2. PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   SA = Address of the sector.
3. For Sector Protect Verify operation : If read out data is 01H, it means the sector has been protected. If read out data is 00H, it means the sector is still not being protected.
4. Any number of CFI data read cycle are permitted.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 3 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress.

TABLE 4. MX29LV040C BUS OPERATION

DESCRIPTION	CE#	OE#	WE#	ADDRESS								Q0~Q7
				A18 | A16	A15 | A10	A9	A8 | A7	A6	A5 | A2	A1	A0	
Read	L	L	H	AIN								Dout
Write	L	H	L	AIN								DIN(3)
Reset	X	X	X	X								High Z
Output Disable	L	H	H	X								High Z
Standby	Vcc±0.3V	X	X	X								High Z
Sector Protect	L	H	L	SA	X	X	X	L	X	H	L	X
Chip Unprotect	L	H	L	X	X	X	X	H	X	H	L	X
Sector Protection Verify	L	L	H	SA	X	VID	X	L	X	H	L	CODE(5)

NOTES:

1. Manufacture and device codes may also be accessed via a command register write sequence. Refer to Table 3.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 3 for valid Data-In during a write operation.
4. X can be VIL or VIH, L=Logic Low=VIL, H=Logic High=VIH.
5. Code=00H/XX00H means unprotected.
   Code=01H/XX01H means protected.
6. A18~A13=Sector address for sector protect.

REQUIREMENTS FOR READING ARRAY DATA

To read array data from the outputs, the system must drive the CE# and OE# pins to VIL. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at VIH.

The internal state machine is set for reading array data upon device power-up. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid address on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory , the system must drive WE# and CE# to VIL, and OE# to VIH.

An erase operation can erase one sector, multiple sectors , or the entire device. Table 1 indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Writing specific address and data commands or sequences into the command register initiates device operations. Table 3 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence section for more information.

ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

STANDBY MODE

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# pin is both held at VCC±0.3V. (Note that this is a more restricted voltage range than VIH.) If CE# is held at VIH, but not within VCC±0.3V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (tCE) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

ICC3 in the DC Characteristics table represents the standby current specification.

OUTPUT DISABLE

With the OE# input at a logic high level (VIH), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage (VID). However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29LV040C contains a Silicon-ID-Read operation to supple traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL, A0=VIL retrieves the manufacturer code of C2H. A read cycle with A1=VIL, A0=VIH returns the device code of 4FH for MX29LV040C.

SET-UP AUTOMATIC CHIP/SECTOR ERASE COMMANDS

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array(no erase verification command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 6), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last WE# or CE# pulse, whichever happens first in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

TABLE 5. EXPANDED SILICON ID CODE

Pins	A0	A1	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code (Hex)
Manufacture code	VIL	VIL	X	1	0	0	0	0	1	0	C2H
Device code	VIH	VIL	0	1	0	0	1	1	1	1	4FH
Sector Protection Verification	VIL	VIH	0	0	0	0	0	0	0	0	00H (Unprotected)

READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands" for more infor-mation on this mode. The system must issue the reset command to re-enable the device for reading array data if Q5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence be-fore programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data (also applies to SILICON ID READ during Erase Suspend).

If Q5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Sector Erase Set-up command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of WE# or CE#, whichever happens later, while the command(data) is latched on the rising edge of WE# or CE#, whichever happens first. Sector addresses selected are loaded into internal register on the sixth falling edge of WE# or CE#, whichever happens later. Each successive sector load cycle started by the falling edge of WE# or CE#, whichever happens later must begin within 50us from the rising edge of the preceding WE# or CE#, whichever happens first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase(30H) or Erase Suspend(B0H) during the time-out period resets the device to read mode.

Table 6. Write Operation Status

	Status		Q7 (Note1)	Q6	Q5 (Note2)	Q3	Q2
In Progress	Byte Program in Auto Program Algorithm		Q7#	Toggle	0	N/A	No Toggle
	Auto Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program	Q7#	Toggle	0	N/A	N/A
Exceeded Time Limits	Byte Program in Auto Program Algorithm		Q7#	Toggle	1	N/A	No Toggle
	Auto Erase Algorithm		0	Toggle	1	1	Toggle
	Erase Suspend Program		Q7#	Toggle	1	N/A	N/A

Note:
1. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. Q5 switches to '1' when an Auto Program or Auto Erase operation has exceeded the maximum timing limits. See "Q5:Exceeded Timing Limits " for more information.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 100us to suspend the erase operations. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and program commands.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended sectors.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing. The minimum time from Erase Resume to next Erase Suspend is 400us. Repeatedly suspending the device more often may have undetermined effects.

AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, A three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next WE# pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the WE# or CE#, whichever happens first. The rising edge of WE# or CE#, whichever happens first, also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

The device provides Q2, Q3, Q5, Q6, Q7 to determine the status of a write operation. If the program operation was unsuccessful, the data on Q5 is "1" (see Table 6), indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode(no program verify command is required).

WORD/BYTE PROGRAM COMMAND SEQUENCE

The device programs one byte of data for each program operation. The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 3 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using Q7, or Q6. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set Q5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6 and Q7. Table 6 and the following subsections describe the functions of these bits. Q7 and Q6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Q7: Data# Polling

The Data# Polling bit, Q7, indicates to the host sys-tem whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Automatic Program algorithm, the device outputs on Q7 the complement of the datum programmed to Q7. This Q7 status also applies to programming during Erase Suspend. When the Automatic Program algorithm is complete, the device outputs the datum programmed to Q7. The system must provide the program address to read valid status information on Q7. If a program address falls within a protected sector, Data# Polling on Q7 is active for approximately 1 us, then the device returns to reading array data.

During the Automatic Erase algorithm, Data# Polling produces a "0" on Q7. When the Automatic Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on Q7. This is analogous to the complement/true datum output described for the Automatic Program algorithm: the erase function changes all the bits in a sector to "1" prior to this, the device outputs the "complement," or "0". The system must provide an address within any of the sectors selected for erasure to read valid status information on Q7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on Q7 is active for approximately 100 us, then the device returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects Q7 has changed from the complement to true data, it can read valid data at Q7-Q0 on the following read cycles. This is because Q7 may change asynchronously with Q0-Q6 while Output Enable (OE#) is asserted low.

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# or CE#, whichever happens first, in the command sequence (prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2 us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 6 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# or CE#, whichever happens first, in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 6 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5
Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data# Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector maynot be reused, (other sectors are still functional and can be reused).

The time-out condition will not appear if a user tries to program a non blank location without erasing. Please note that this is not a device failure condition since the device was incorrectly used.

Q3
Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data# Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data# Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data# Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

DATA PROTECTION

The MX29LV040C is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

LOW VCC WRITE INHIBIT

When VCC is less than VLKO the device does not accept any write cycles. This protects data during VCC power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until VCC is greater than VLKO. The system must provide the proper signals to the control pins to prevent unintentional write when VCC is greater than VLKO.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on CE# or WE# will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of OE# = VIL, CE# = VIH or WE# = VIH. To initiate a write cycle CE# and WE# must be a logical zero while OE# is a logical one.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

POWER-UP SEQUENCE

The MX29LV040C powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

SECTOR PROTECTION

The MX29LV040C features hardware sector protection. This feature will disable both program and erase operations for these sectors protected. To activate this mode, the programming equipment must force VID on address pin A9 and OE# (suggest VID = 12V). Programming of the protection circuitry begins on the falling edge of the WE# pulse and is terminated on the rising edge. Please refer to sector protect algorithm and waveform.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with CE# and OE# at VIL and WE# at VIH). When A1=VIH, A0=VIL, A6=VIL, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses, except for A1, are don't care. Address locations with A1 = VIL are reserved to read manufacturer and device codes.(Read Silicon ID)

It is also possible to determine if the sector is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

CHIP UNPROTECT

The MX29LV040C also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin OE# and address pin A9. The CE# pins must be set at VIL. Pins A6 must be set to VIH. Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotected mechanism begins on the falling edge of the WE# pulse and is terminated on the rising edge.

It is also possible to determine if the chip is unprotected in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs(Q0-Q7) for an unprotected sector.

It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages . . . . -65°C to +150°C

Ambient Temperature

with Power Applied. . . . . -65°C to +125°C

Voltage with Respect to Ground

VCC (Note 1) . . . . . -0.5 V to +4.0 V

A9, OE#, and

All other pins (Note 1) . . . . . -0.5 V to VCC +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot VSS to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is VCC +0.5 V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods up to 20 ns.
2. Minimum DC input voltage on pins A9 and OE# is -0.5 V. During voltage transitions, A9 and OE# may overshoot VSS to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RATINGS

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . -40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for full voltage range. . . . . +2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Table 7. CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN1	Input Capacitance			8	pF	VIN = 0V
CIN2	Control Pin Capacitance			12	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

Table 8. DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 2.7V to 3.6V

Symbol	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS	
ILI	Input Leakage Current			± 1	uA	VIN = VSS to VCC	
ILIT	A9 Input Leakage Current			35	uA	VCC=VCC max; A9=12.5V	
ILO	Output Leakage Current			± 1	uA	VOUT = VSS to VCC, VCC=VCC max	
ICC1	VCC Active Read Current		7	12	mA	CE#=VIL, OE#=VIH	@5MHz
			2	4	mA		@1MHz
ICC2	VCC Active write Current		15	30	mA	CE#=VIL, OE#=VIH	
ICC3	VCC Standby Current		0.2	5	uA	CE#;VCC ± 0.3V	
ICC4	VCC Standby Current During Reset		0.2	5	uA	CE#; VCC ± 0.3V	
ICC5	Automatic sleep mode		0.2	5	uA	VIH=VCC ± 0.3V;VIL=VSS ± 0.3V	
VIL	Input Low Voltage(Note 1)	-0.5		0.8	V		
VIH	Input High Voltage	0.7xVCC		VCC+ 0.3	V		
VID	Voltage for Auto Select	11.5		12.5	V	VCC=3.3V	
VOL	Output Low Voltage			0.45	V	IOL = 4.0mA, VCC= VCC min	
VOH1	Output High Voltage(TTL)	0.85xVCC				IOH = -2mA, VCC=VCC min	
VOH2	Output High Voltage (CMOS)	VCC-0.4				IOH = -100uA, VCC min	
VLKO	Low VCC Lock-Out Voltage (Note 4)	1.4		2.1	V		

NOTES:
1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.
3. Automatic sleep mode enable the low power mode when addresses remain stable for tACC +30ns.
4. Not 100% tested.

AC CHARACTERISTICS TA = -40°C to 85°C, VCC = 2.7V~3.6V

Table 9. READ OPERATIONS

			29LV040C-55R		29LV040C-70		29LV040C-90			
SYMBOL	PARAMETER		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tRC	Read Cycle Time (Note 1)		55		70		90		ns	
tACC	Address to Output Delay			55		70		90	ns	CE#=OE#=VIL
tCE	CE# to Output Delay			55		70		90	ns	OE#=VIL
tOE	OE# to Output Delay			30		30		35	ns	CE#=VIL
tDF	OE# High to Output Float (Note1)		0	25	0	25	0	30	ns	CE#=VIL
tOEH	Output Enable	Read	0		0		0		ns	
	Hold Time	Toggle and Data# Polling	10		10		10		ns	
tOH	Address to Output hold		0		0		0		ns	CE#=OE#=VIL

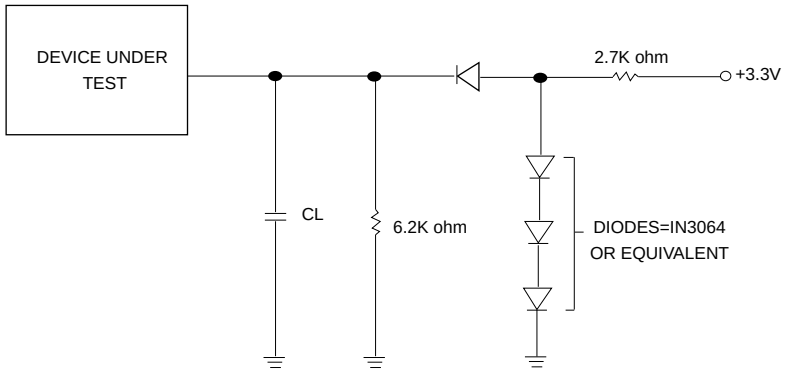
TEST CONDITIONS:

- Input pulse levels: 0V/3.0V.
- Input rise and fall times is equal to or less than 5ns.
- Output load: 1 TTL gate + 100pF (Including scope and jig), for 29LV040C-90. 1 TTL gate + 30pF (Including scope and jig) for 29LV040C-70.
- Reference levels for measuring timing: 1.5V.

NOTE:

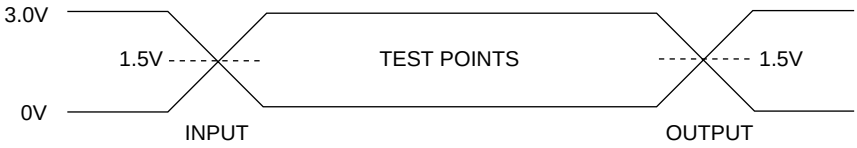
1. Not 100% tested.
2. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Figure 1. SWITCHING TEST CIRCUITS



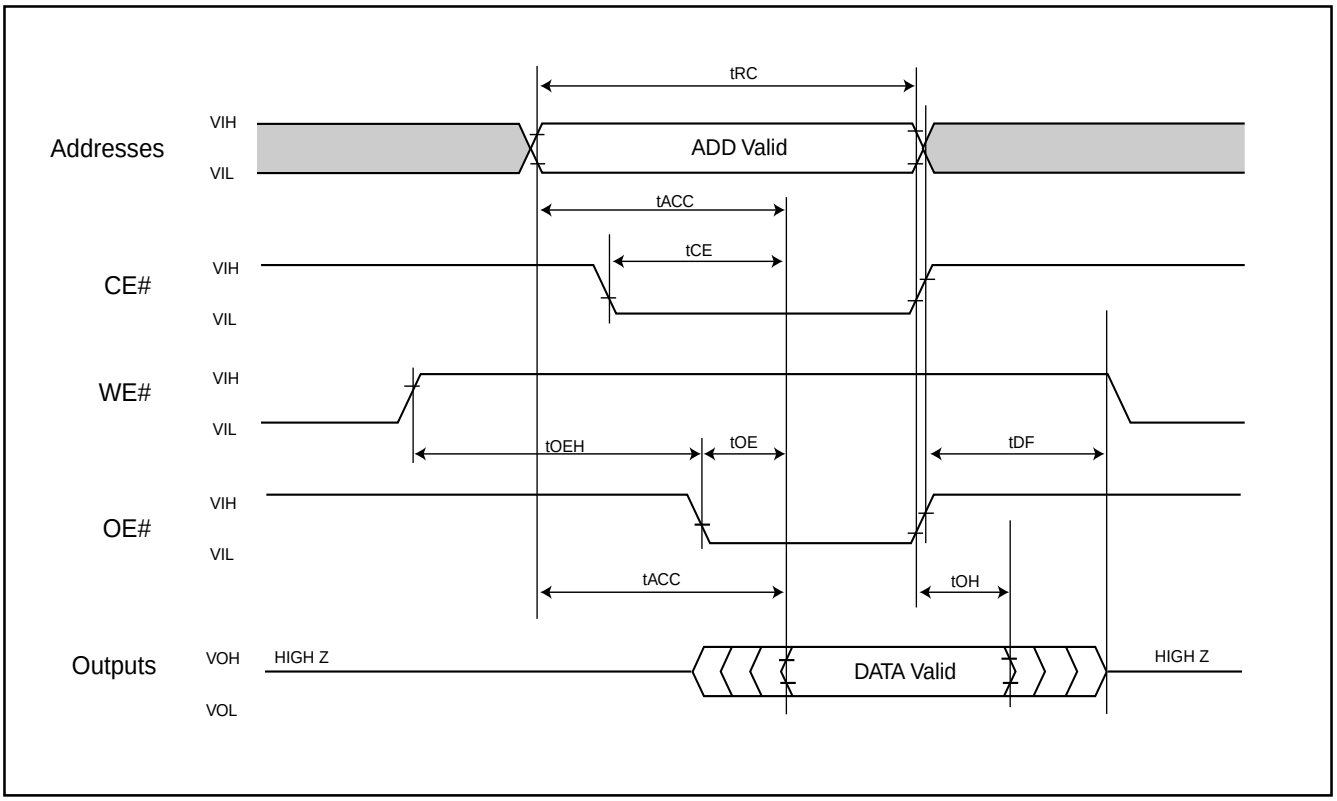
CL=100pF Including jig capacitance
CL=30pF for MX29LV040C-70

Figure 2. SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are < 5ns.

Figure 3. READ TIMING WAVEFORMS



AC CHARACTERISTICS TA = -40°C to 85°C, VCC = 2.7V~3.6V

Table 10. Erase/Program Operations

		29LV040C-55R		29LV040C-70		29LV040C-90		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	Unit
tWC	Write Cycle Time (Note 1)	55		70		90		ns
tAS	Address Setup Time	0		0		0		ns
tAH	Address Hold Time	45		45		45		ns
tDS	Data Setup Time	35		35		45		ns
tDH	Data Hold Time	0		0		0		ns
tOES	Output Enable Setup Time	0		0		0		ns
tGHWL	Read Recovery Time Before Write (OE# High to WE# Low)	0		0		0		ns
tCS	CE# Setup Time	0		0		0		ns
tCH	CE# Hold Time	0		0		0		ns
tWP	Write Pulse Width	35		35		35		ns
tWPH	Write Pulse Width High	30		30		30		ns
tWHWH1	Programming Operation (Note 2)	9(TYP.)		9(TYP.)		9(TYP.)		us
tWHWH2	Sector Erase Operation (Note 2)	0.7(TYP.)		0.7(TYP.)		0.7(TYP.)		sec
tVCS	VCC Setup Time (Note 1)	50		50		50		us
tBAL	Sector Address Load Time		50		50		50	us

NOTES:

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

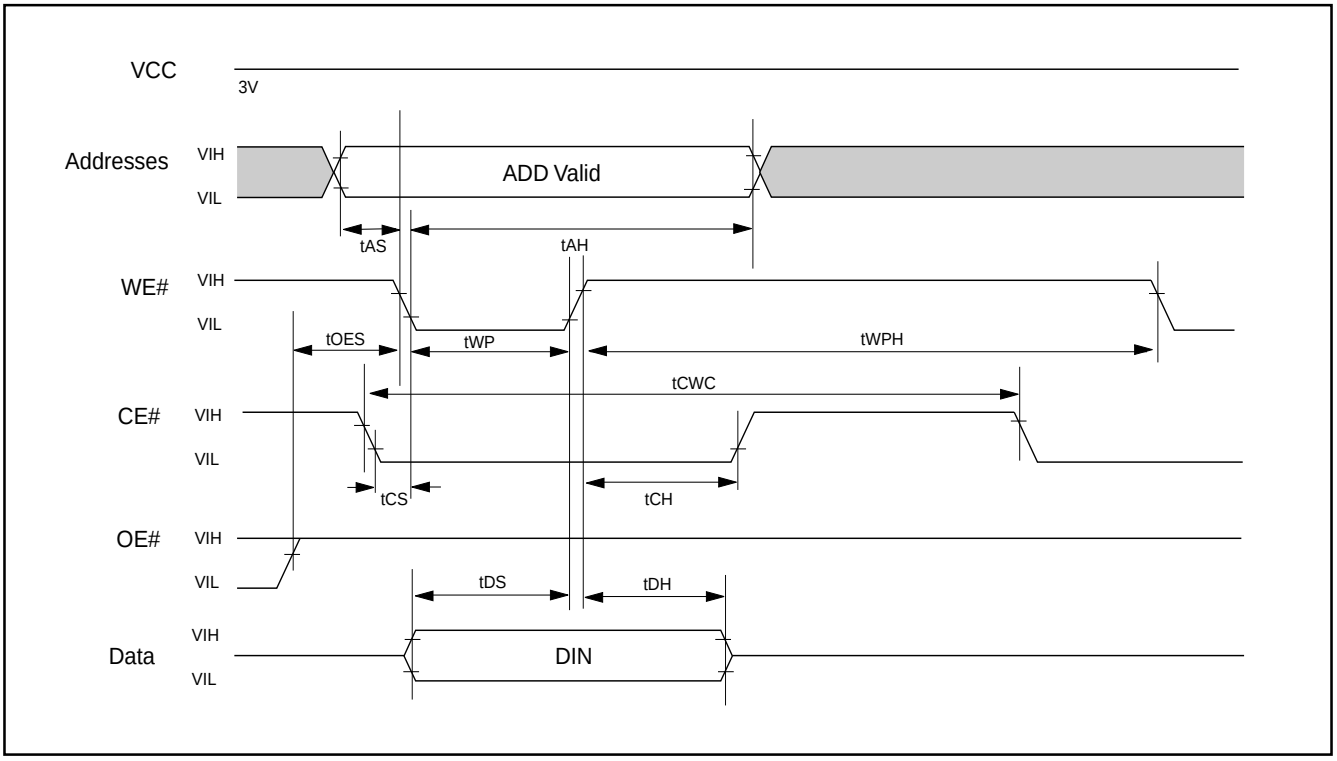
AC CHARACTERISTICS TA = -40°C to 85°C, VCC = 2.7V~3.6V

Table 11. Alternate CE# Controlled Erase/Program Operations

		29LV040C-55R		29LV040C-70		29LV040C-90		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
tWC	Write Cycle Time (Note 1)	55		70		90		ns
tAS	Address Setup Time	0		0		0		ns
tAH	Address Hold Time	45		45		45		ns
tDS	Data Setup Time	35		35		45		ns
tDH	Data Hold Time	0		0		0		ns
tOES	Output Enable Setup Time	0		0		0		ns
tGHEL	Read Recovery Time Before Write	0		0		0		ns
tWS	WE# Setup Time	0		0		0		ns
tWH	WE# Hold Time	0		0		0		ns
tCP	CE# Pulse Width	35		35		35		ns
tCPH	CE# Pulse Width High	30		30		30		ns
tWHWH1	Programming Operation(note2)	9(Typ.)		9(Typ.)		9(Typ.)		us
tWHWH2	Sector Erase Operation (note2)	0.7(Typ.)		0.7(Typ.)		0.7(Typ.)		sec

NOTE:
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

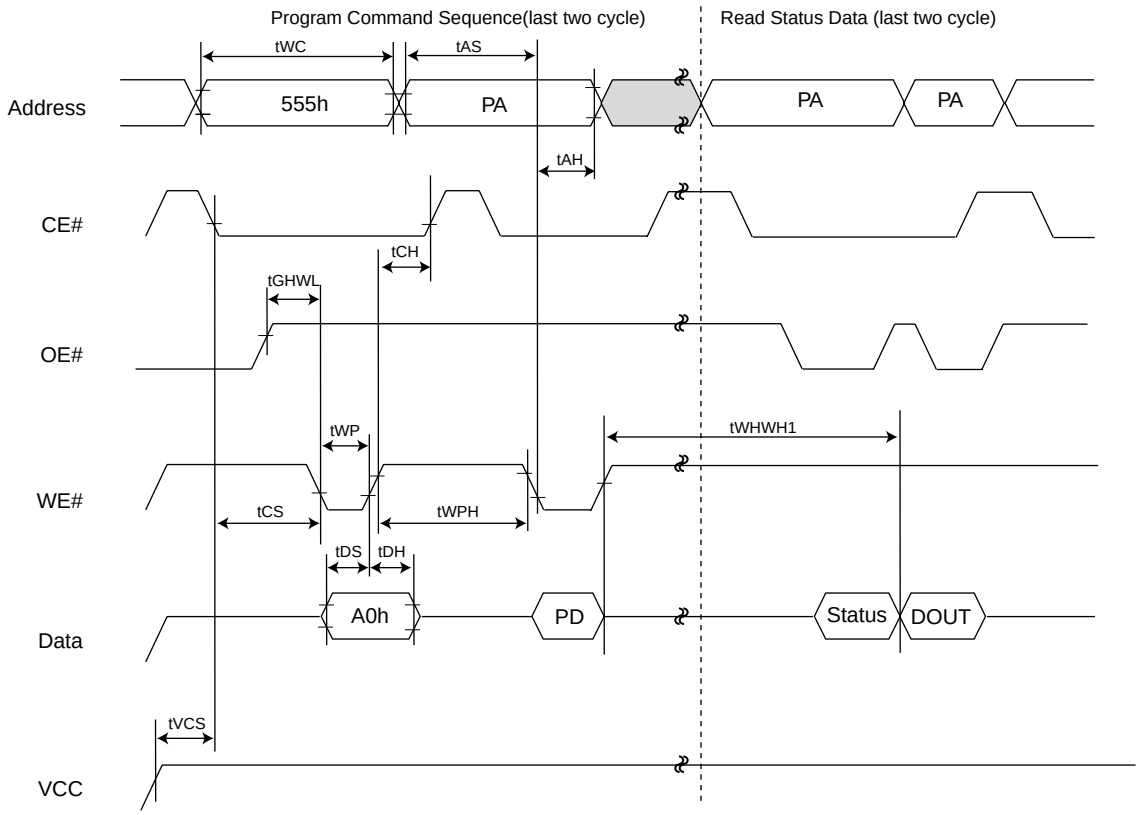
Figure 4. COMMAND WRITE TIMING WAVEFORM



AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional verification by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by Data# Polling and toggle bit checking after automatic programming starts. Device outputs DATA# during programming and DATA# after programming on Q7.(Q6 is for toggle bit; see toggle bit, Data# Polling, timing waveform)

Figure 5. AUTOMATIC PROGRAMMING TIMING WAVEFORM



NOTES:
1.PA=Program Address, PD=Program Data, DOUT is the true data the program address

Figure 6. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

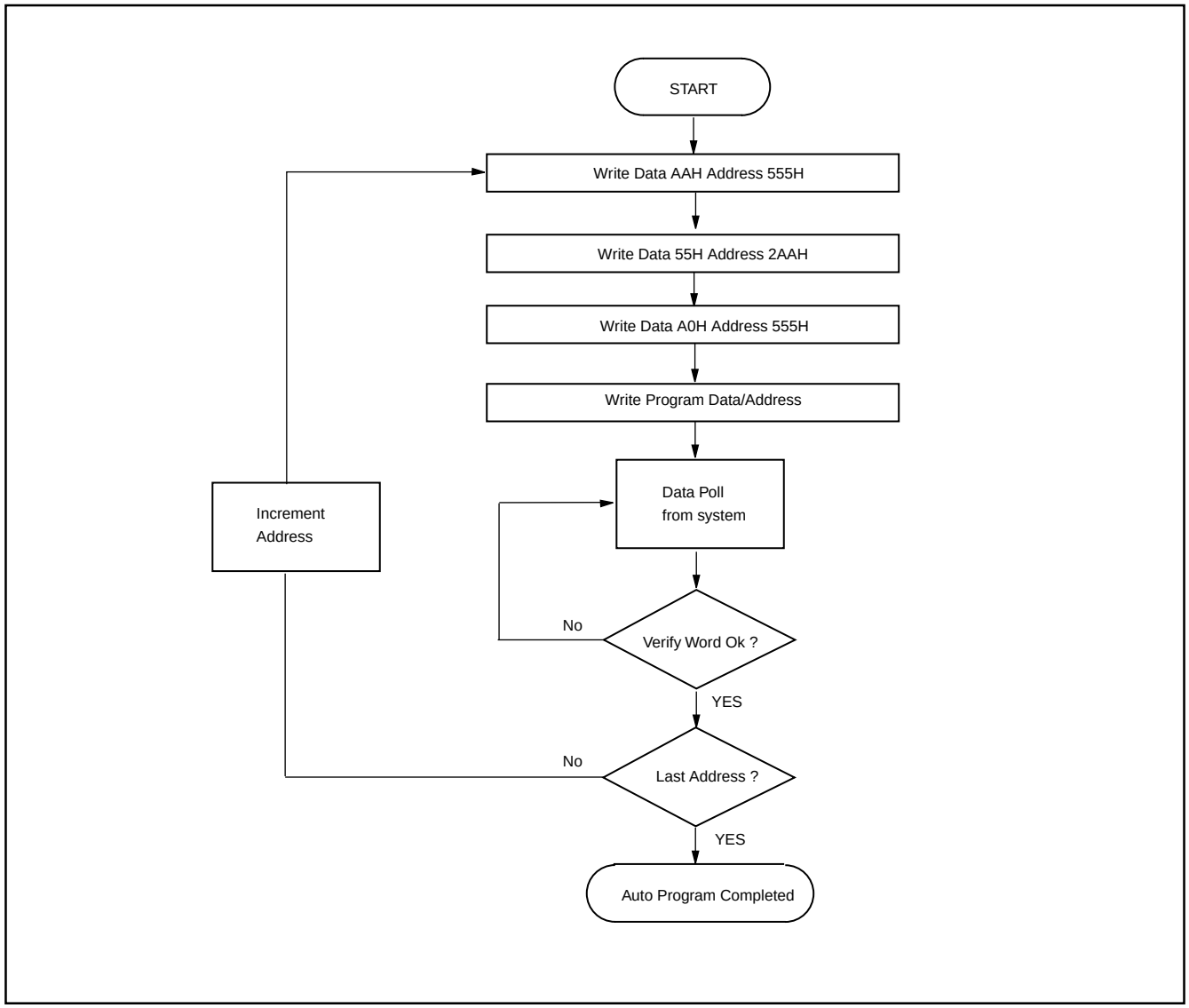
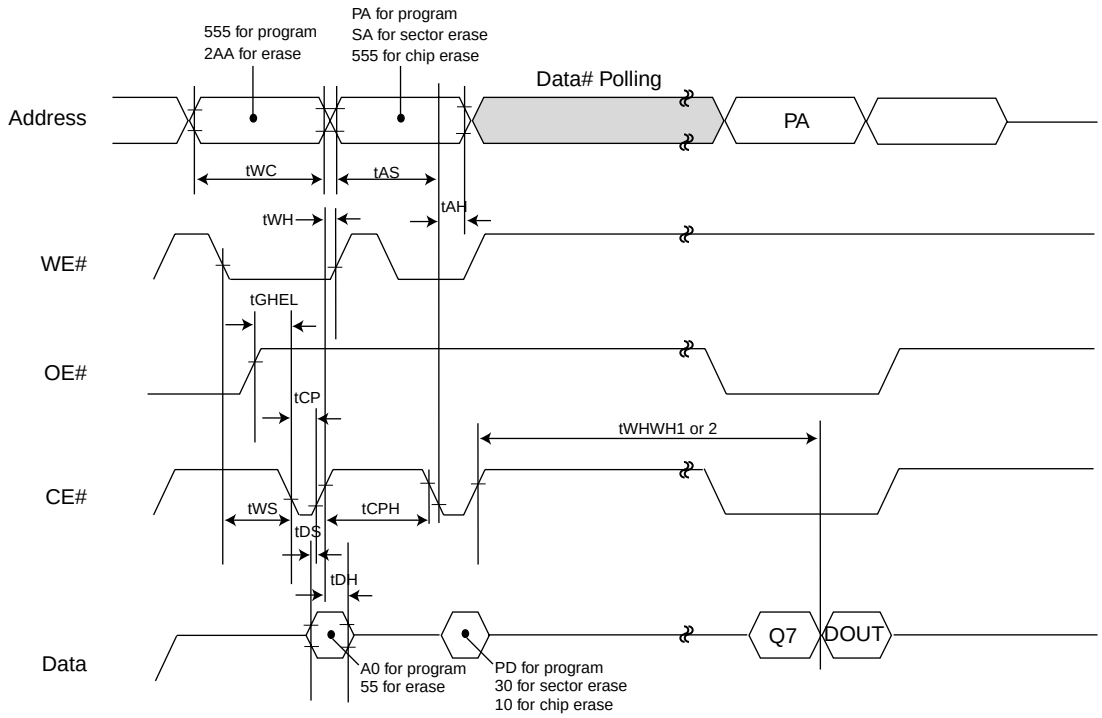


Figure 7. CE# CONTROLLED PROGRAM TIMING WAVEFORM



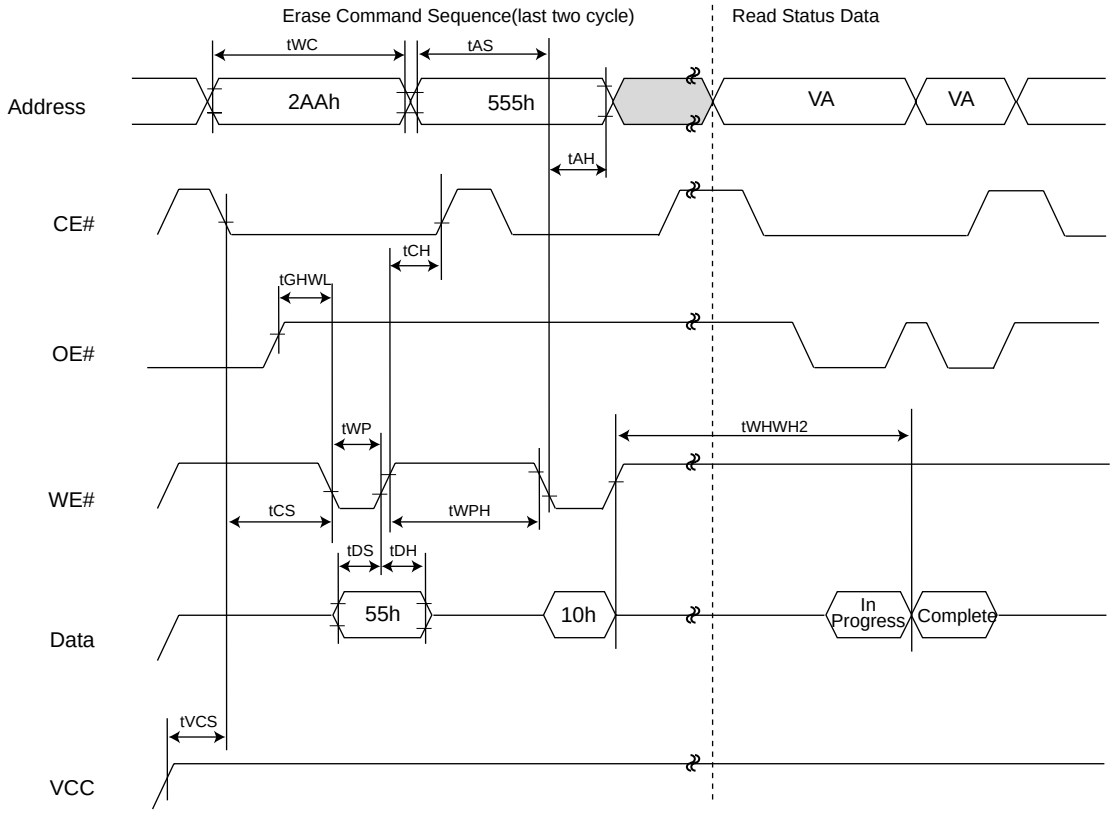
NOTES:

1.PA=Program Address, PD=Program Data, DOUT=Data Out, Q7=complement of data written to device.
2.Figure indicates the last two bus cycles of the command sequence.

AUTOMATIC CHIP ERASE TIMING WAVEFORM

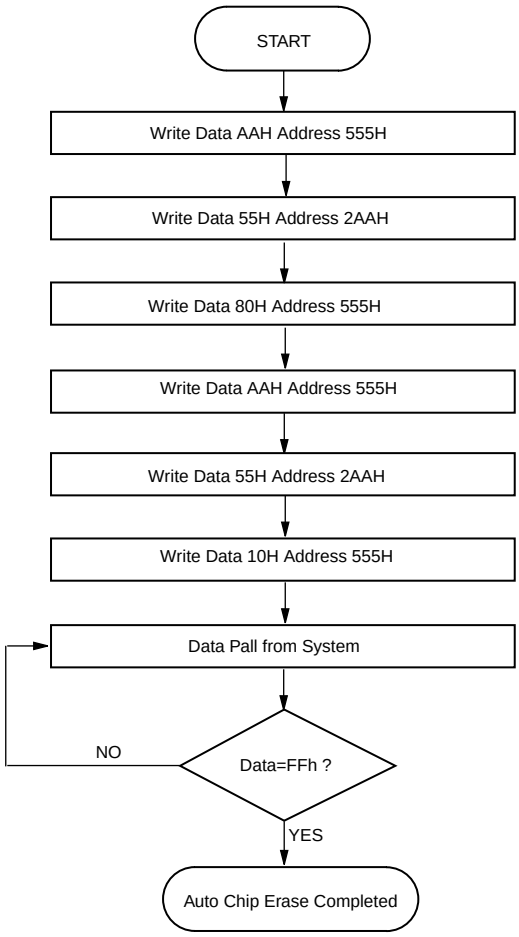
All data in chip are erased. External erase verification is not required because data is verified automatically by internal control circuit. Erasure completion can be verified by Data# Polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, Data# Polling, timing waveform)

Figure 8. AUTOMATIC CHIP ERASE TIMING WAVEFORM



NOTES:
SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

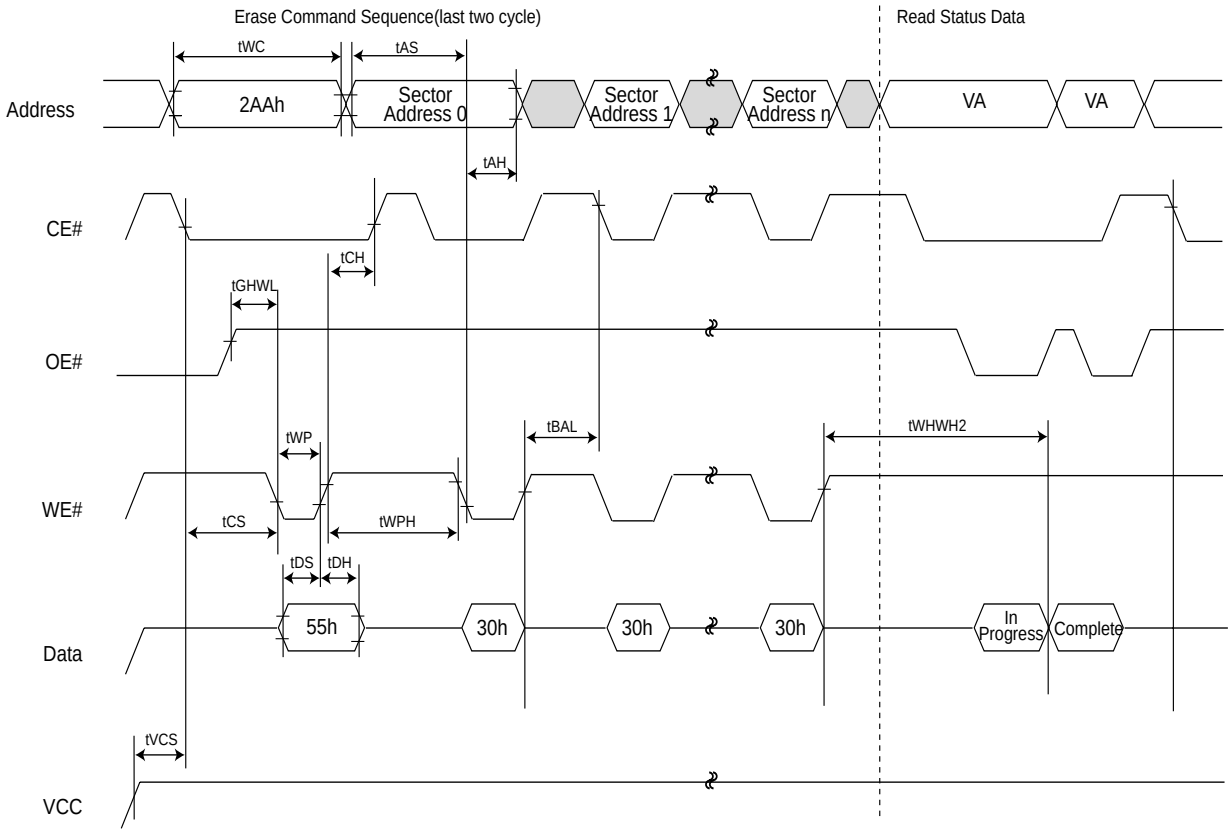
Figure 9. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART



AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Sector indicated by A13 to A18 are erased. External erase verify is not required because data are verified automatically by internal control circuit. Erasure completion can be verified by Data# Polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, Data# Polling, timing waveform)

Figure 10. AUTOMATIC SECTOR ERASE TIMING WAVEFORM



NOTES:
SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

Figure 11. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

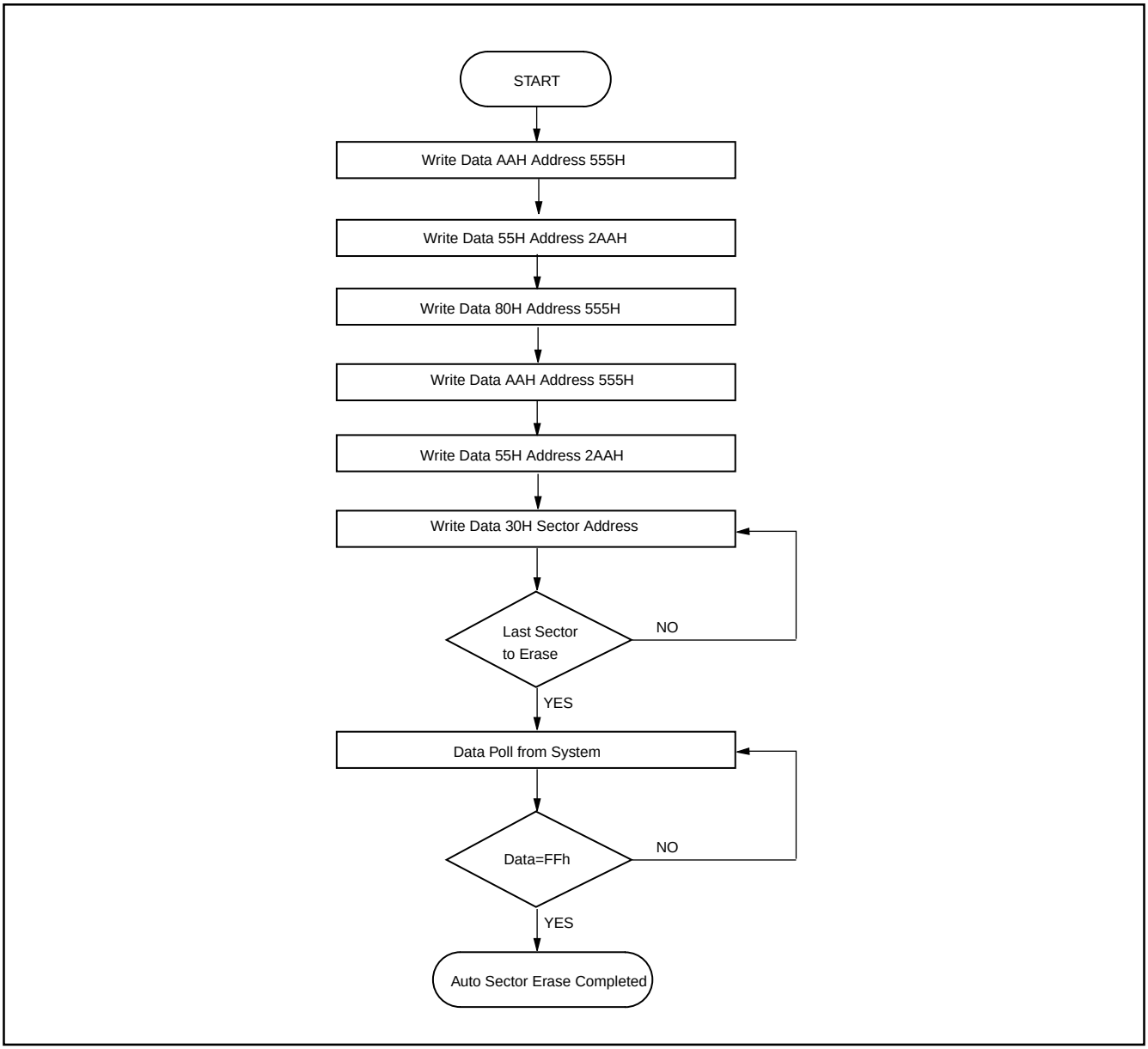
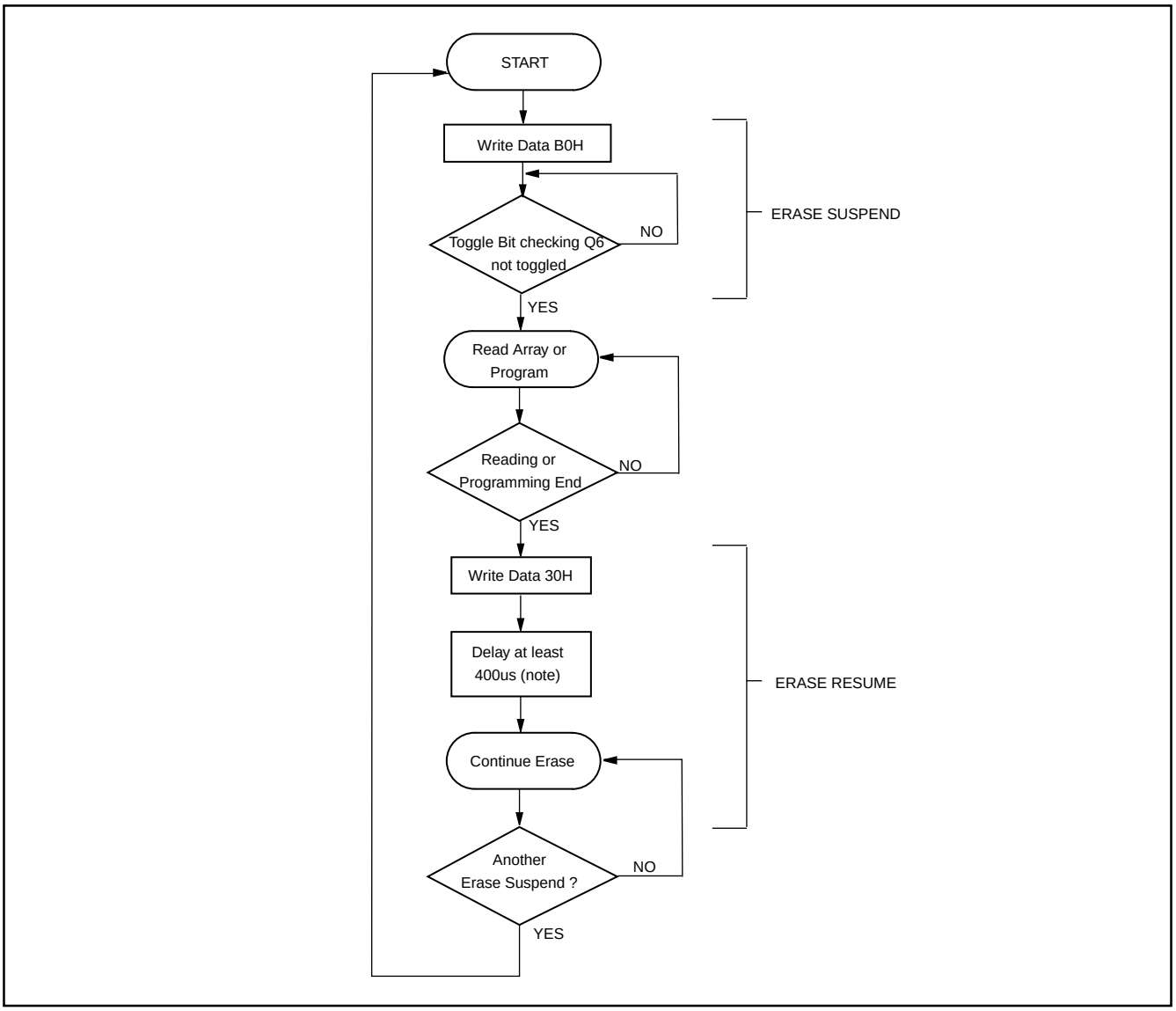


Figure 12. ERASE SUSPEND/ERASE RESUME FLOWCHART



Note: Repeatedly suspending the device more often may have undetermined effects.

Figure 13. TIMING WAVEFORM FOR SECTOR PROTECT

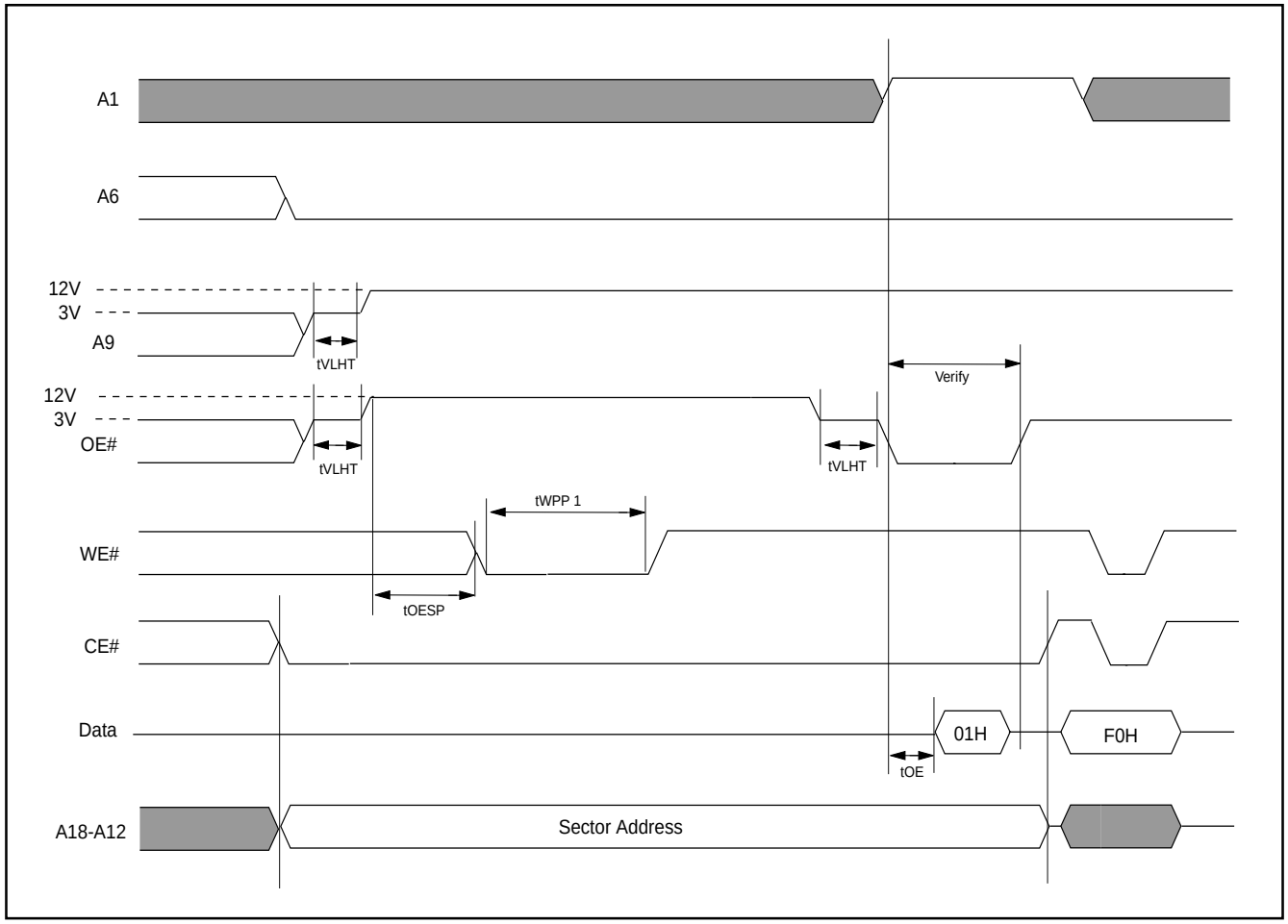


Figure 14. SECTOR PROTECTION ALGORITHM

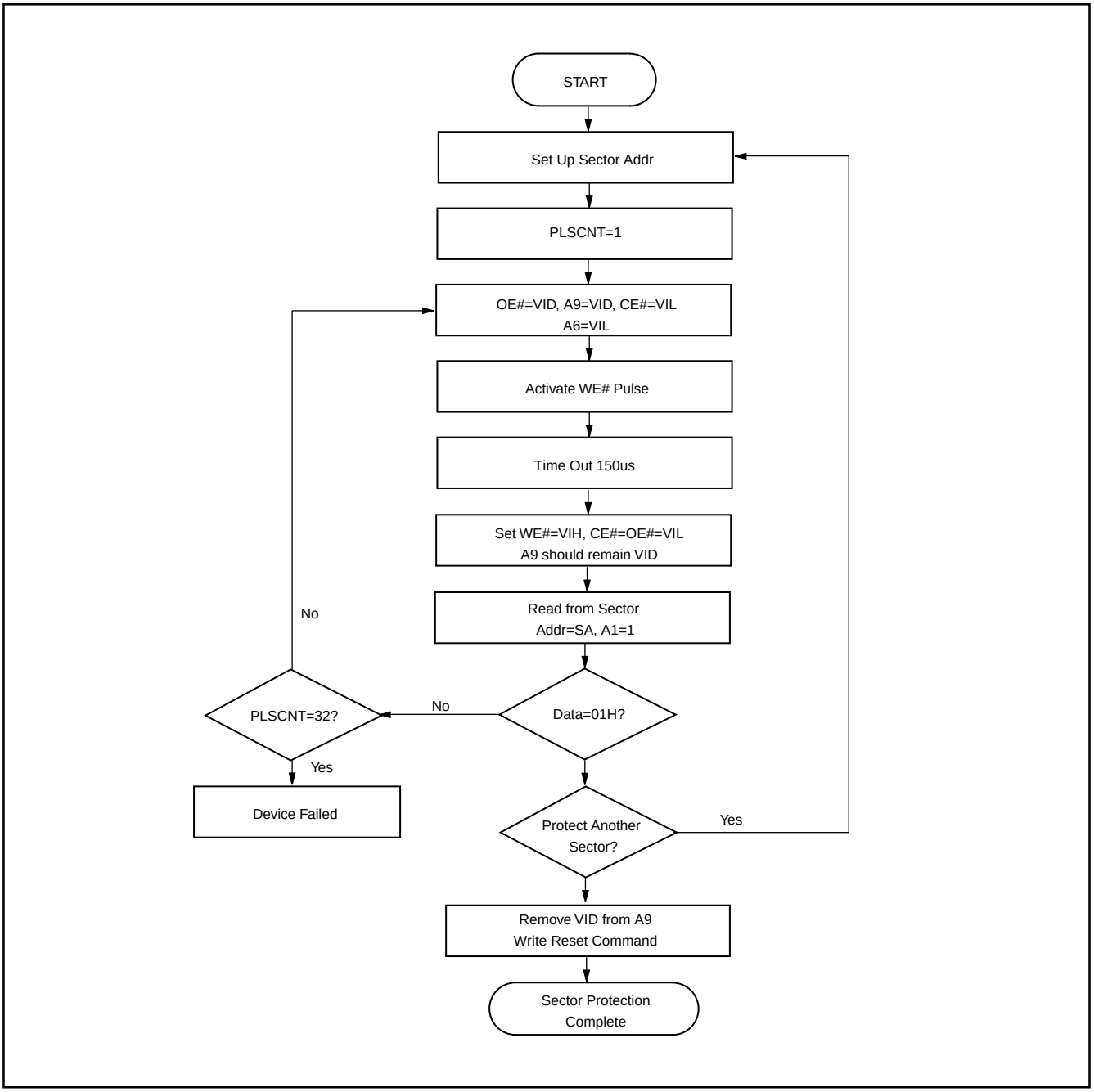
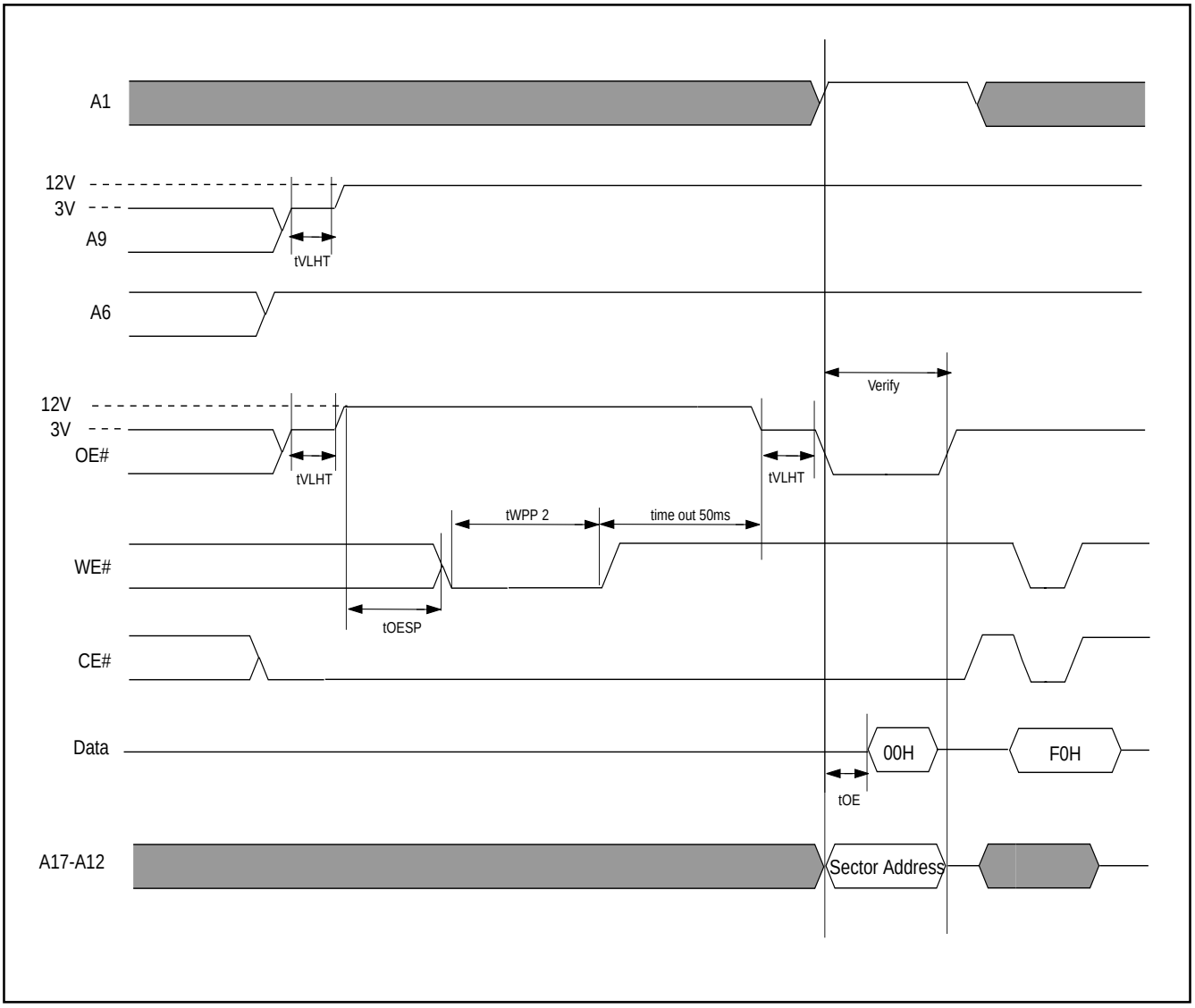
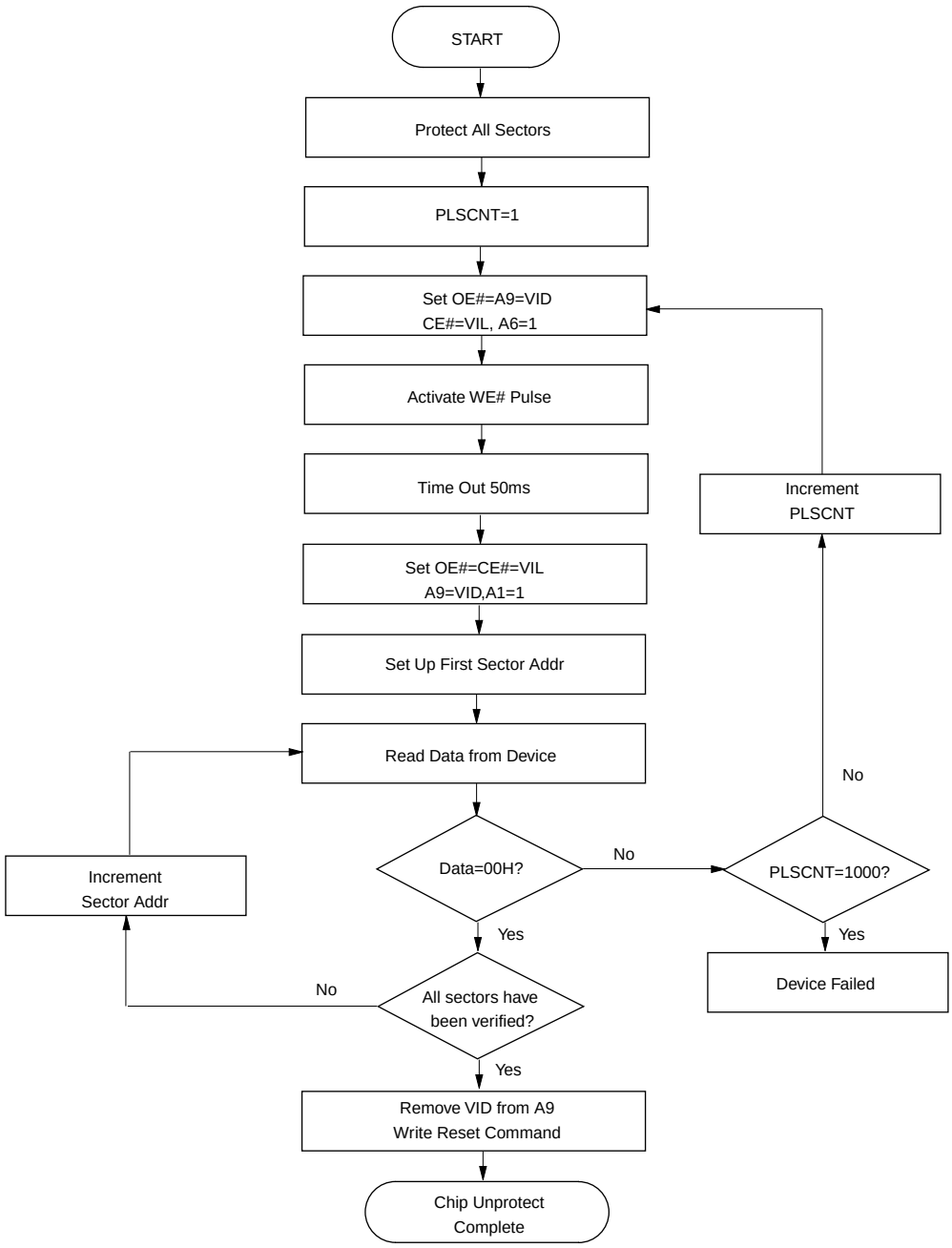


Figure 15. TIMING WAVEFORM FOR CHIP UNPROTECTED



Notes: tWPP1 (Write pulse width for sector protect)=100ns min.
tWPP2 (Write pulse width for sector unprotect)=100ns min.

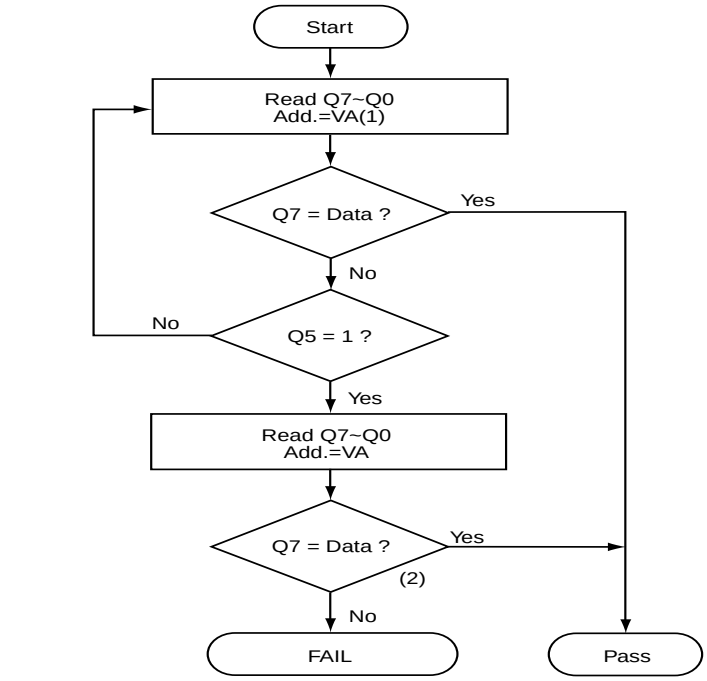
Figure 16. CHIP UNPROTECTED ALGORITHM



* It is recommended before unprotect whole chip, all sectors should be protected in advance.

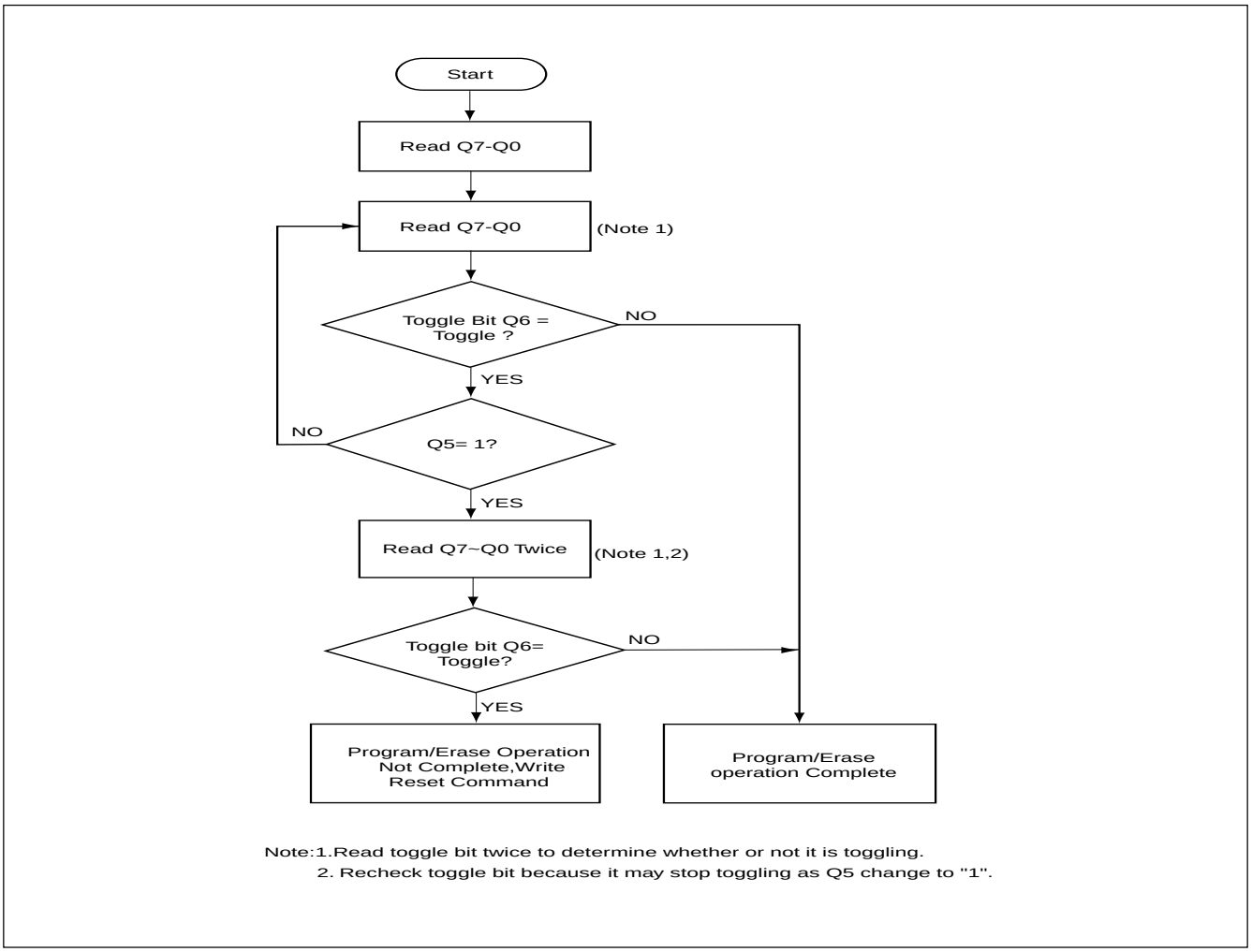
WRITE OPERATION STATUS

Figure 17. DATA# POLLING ALGORITHM



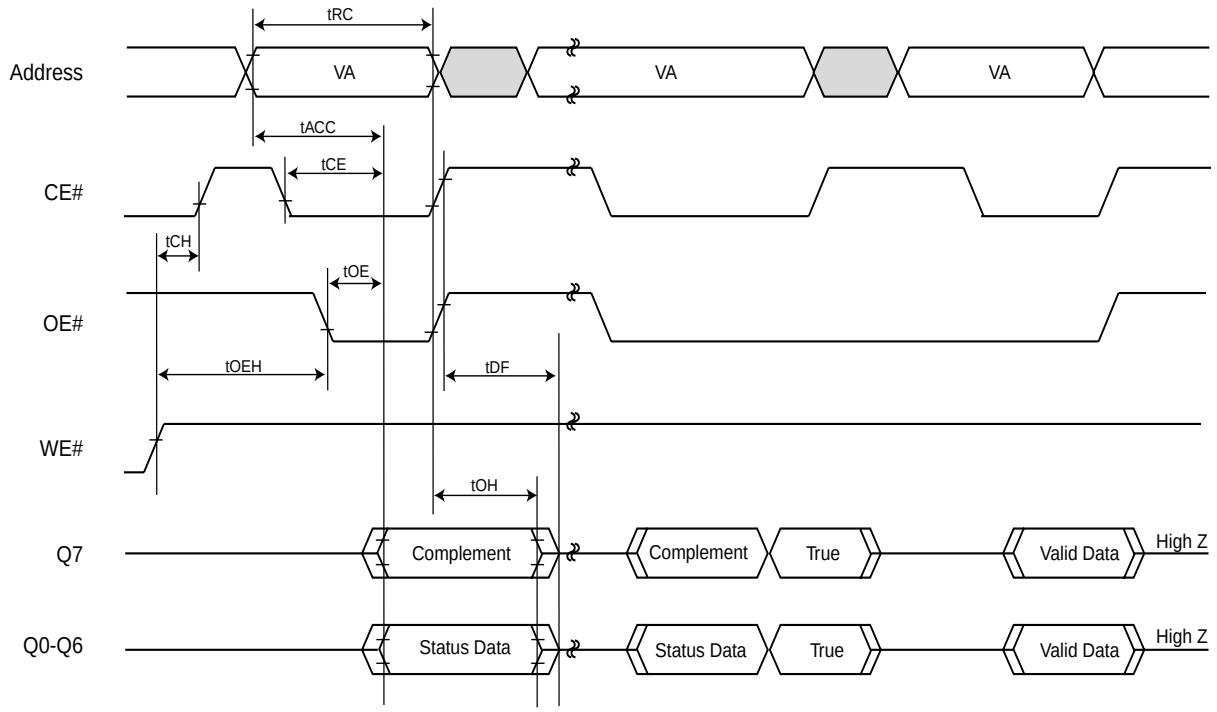
NOTE : 1.VA=Valid address for programming
2.Q7 should be re-checked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 18. TOGGLE BIT ALGORITHM



Note:1.Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 change to "1".

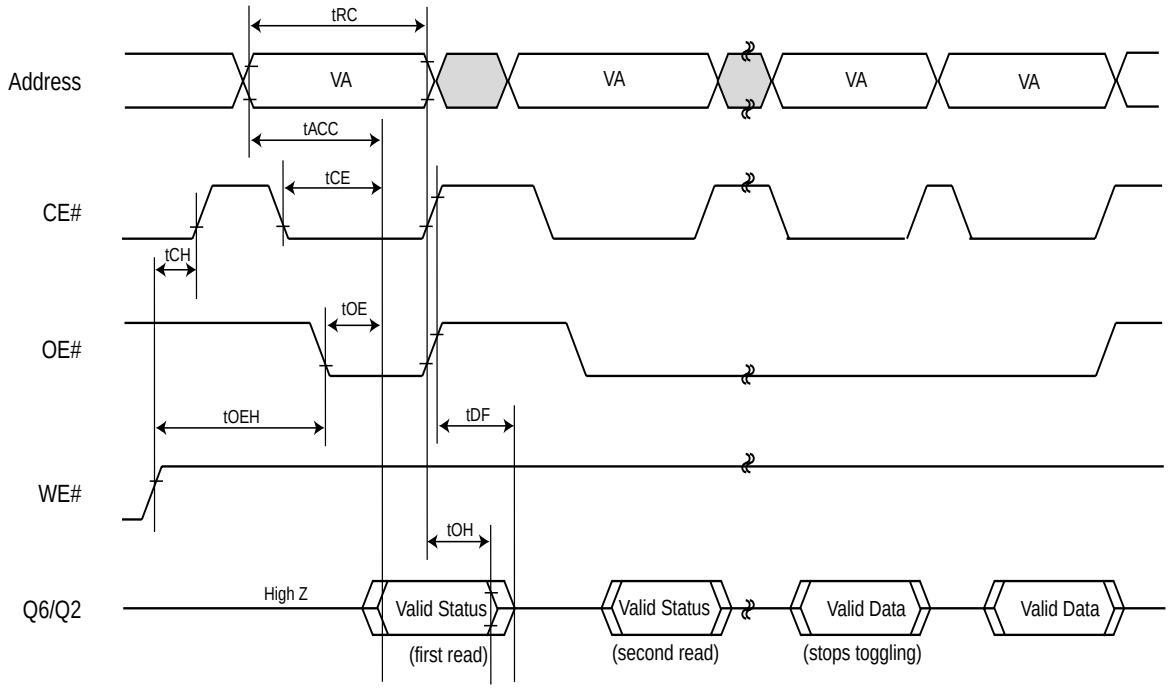
Figure 19. DATA# POLLING TIMINGS (DURING AUTOMATIC ALGORITHMS)



NOTES:

1. VA=Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data read cycle.
2. CE# must be toggled when DATA# polling.

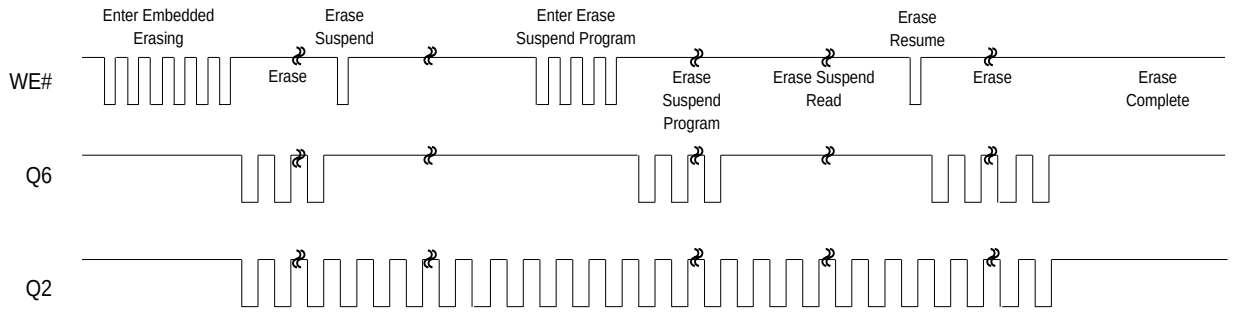
Figure 20. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



NOTES:

1. VA=Valid address; not required for Q6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.
2. CE# must be toggled when toggle bit toggling.

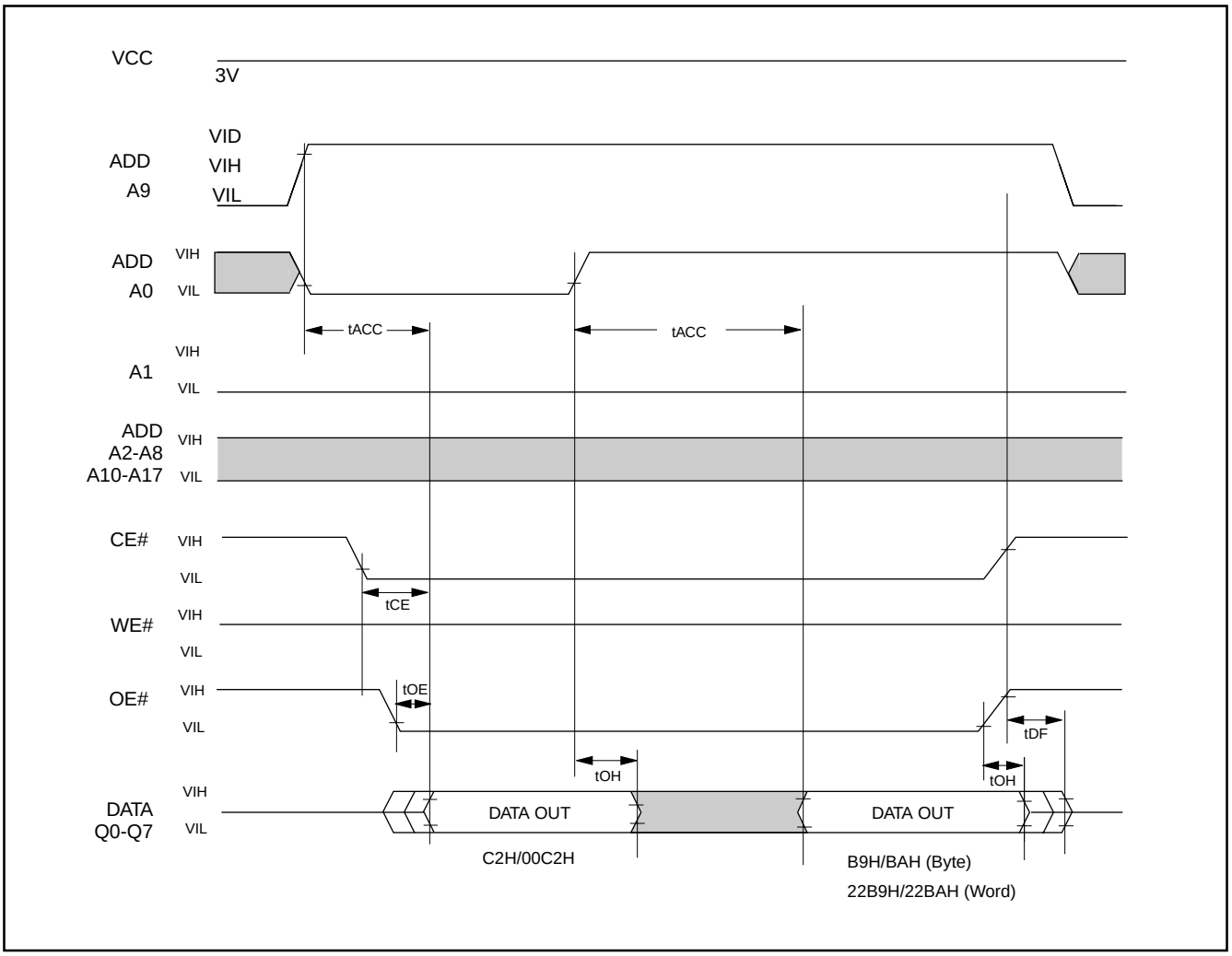
Figure 21. Q6 vs Q2 for Erase and Erase Suspend Operations



NOTES:

The system can use OE# or CE# to toggle Q2/Q6, Q2 toggles only when read at an address within an erase-suspended

Figure 22. ID CODE READ TIMING WAVEFORM



RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

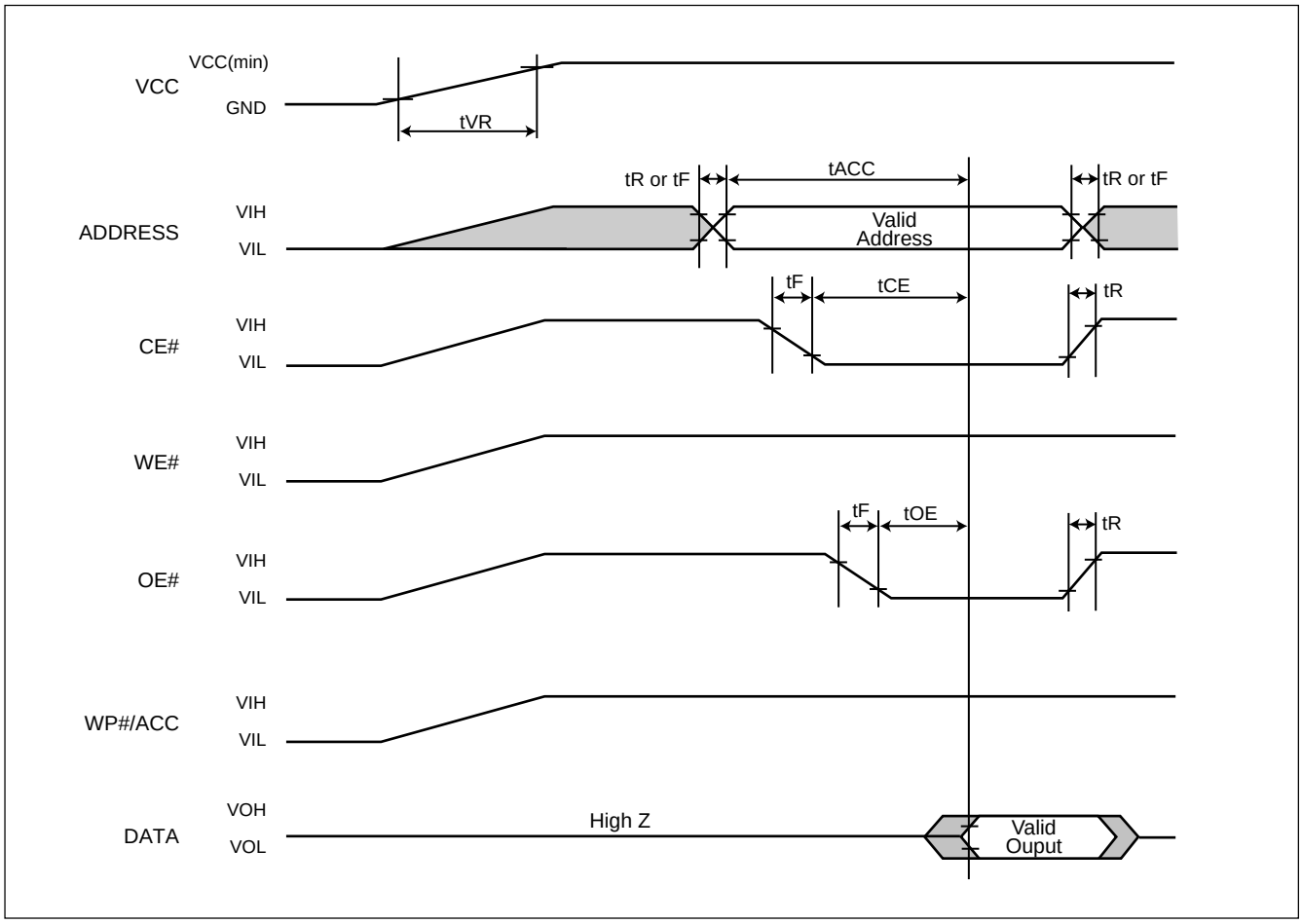


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V
tR	Input Signal Rise Time	1,2		20	us/V
tF	Input Signal Fall Time	1,2		20	us/V

Notes :
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

Table 12. ERASE AND PROGRAMMING PERFORMANCE (1)

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX.(3)	
Sector Erase Time		0.7	15	sec
Chip Erase Time		4	32	sec
Byte Programming Time		9	300	us
Chip Programming Time		4.5	13.5	sec
Erase/Program Cycles	100,000			Cycles

Note: 1.Not 100% Tested, Excludes external system level over head.
2.Typical values measured at 25°C, 3V.
3.Maximum values measured at 25°C, 2.7V.

Table 13. LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	12.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: VCC = 3.0V, one pin at a time.		

Table 14. DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Data Retention Time	150°C	10	Years
	125°C	20	Years

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE (for MX29LV040C)

MX29LV040C is capable of operating in the CFI mode. This mode all the host system to determine the manufacturer of the device such as operating parameters and configuration. Two commands are required in CFI mode. Query command of CFI mode is placed first, then the Reset command exits CFI mode. These are described in Table 15.

The single cycle Query command is valid only when the device is in the Read mode, including Erase Suspend, Standby mode, and Read ID mode; however, it is ignored otherwise.

The Reset command exits from the CFI mode to the Read mode, or Erase Suspend mode, or read ID mode. The command is valid only when the device is in the CFI mode.

TABLE 15-1. CFI mode: Identification Data Values

(All values in these tables are in hexadecimal)

Description	Address (Byte Mode)	Data
Query-unique ASCII string "QRY"	20	0051
	22	0052
	24	0059
Primary vendor command set and control interface ID code	26	0002
	28	0000
Address for primary algorithm extended query table	2A	0040
	2C	0000
Alternate vendor command set and control interface ID code (none)	2E	0000
	30	0000
Address for secondary algorithm extended query table (none)	32	0000
	34	0000

TABLE 15-2. CFI Mode: System Interface Data Values

(All values in these tables are in hexadecimal)

Description	Address (Byte Mode)	Data
VCC supply, minimum (2.7V)	36	0027
VCC supply, maximum (3.6V)	38	0036
VPP supply, minimum (none)	3A	0000
VPP supply, maximum (none)	3C	0000
Typical timeout for single word/byte write (2^N us)	3E	0004
Typical timeout for Minimum size buffer write (2^N us)	40	0000
Typical timeout for individual block erase (2^N ms)	42	000A
Typical timeout for full chip erase (2^N ms)	44	0000
Maximum timeout for single word/byte write times (2^N X Typ)	46	0005
Maximum timeout for buffer write times (2^N X Typ)	48	0000
Maximum timeout for individual block erase times (2^N X Typ)	4A	0004
Maximum timeout for full chip erase times (not supported)	4C	0000

TABLE 15-3. CFI Mode: Device Geometry Data Values
(All values in these tables are in hexadecimal)

Description	Address (Byte Mode)	Data
Device size (2^N bytes)	4E	0013
Flash device interface code (refer to the CFI publication 100)	50	0000
	52	0000
Maximum number of bytes in multi-byte write (not supported)	54	0000
	56	0000
Number of erase block regions	58	0001
Erase block region 1 information (refer to the CFI publication 100)	5A	0007
	5C	0000
	5E	0000
	60	0001
Erase block region 2 information	62	0000
	64	0000
	66	0000
	68	0000
Erase block region 3 information	6A	0000
	6C	0000
	6E	0000
	70	0000
Erase block region 4 information	72	0000
	74	0000
	76	0000
	78	0000

TABLE 15-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values
(All values in these tables are in hexadecimal)

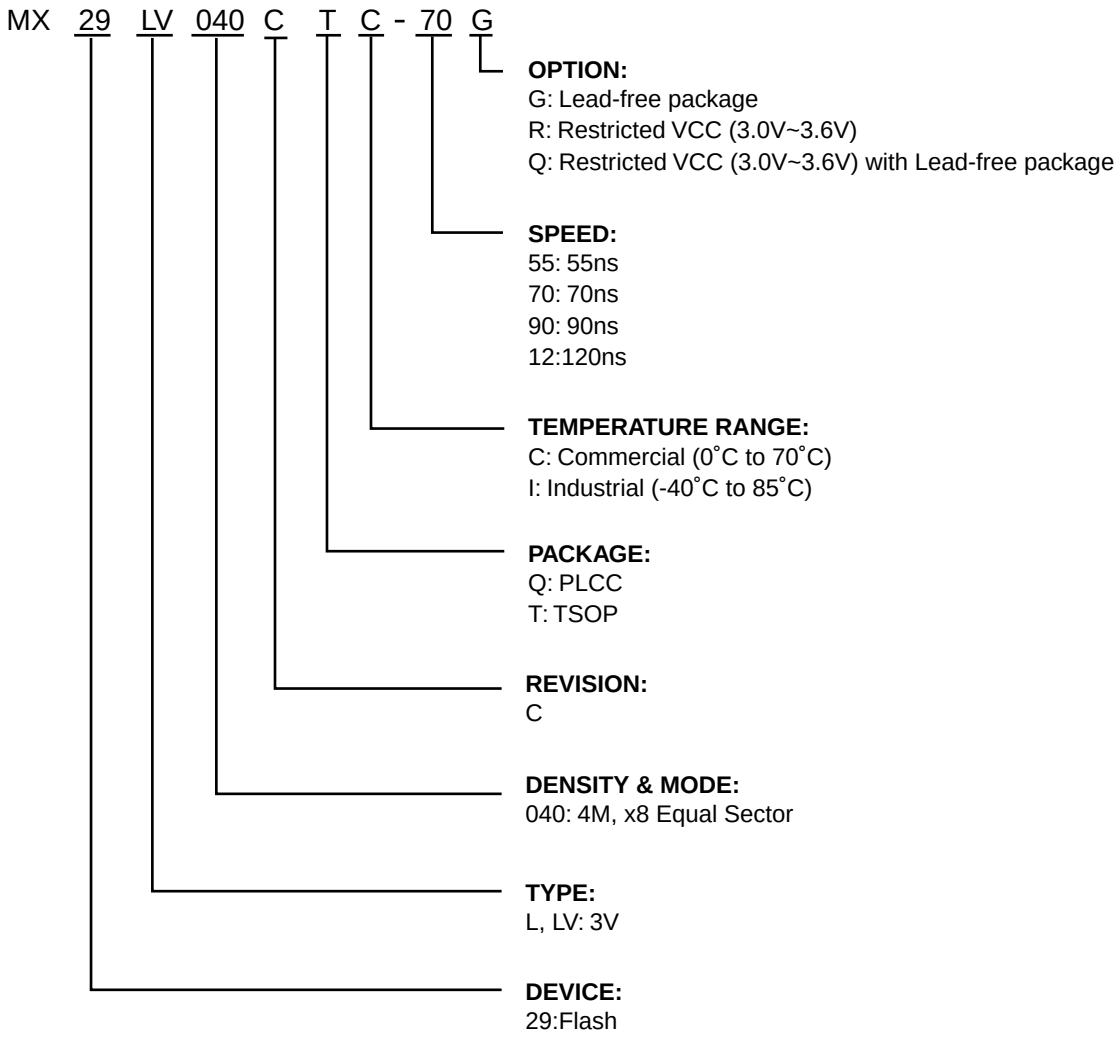
Description	Address (Byte Mode)	Data
Query-unique ASCII string "PRI"	80	0050
	82	0052
	84	0049
Major version number, ASCII	86	0031
Minor version number, ASCII	88	0030
Address sensitive unlock (0=required, 1= not required)	8A	0001
Erase suspend (2= to read and write)	8C	0002
Sector protect (N= # of sectors/group)	8E	0001
Temporary sector unprotected (1=supported)	90	0001
Sector protect/unprotected scheme	92	0004
Simultaneous R/W operation (0=not supported)	94	0000
Burst mode type (0=not supported)	96	0000
Page mode type (0=not supported)	98	0000

ORDERING INFORMATION

PLASTIC PACKAGE

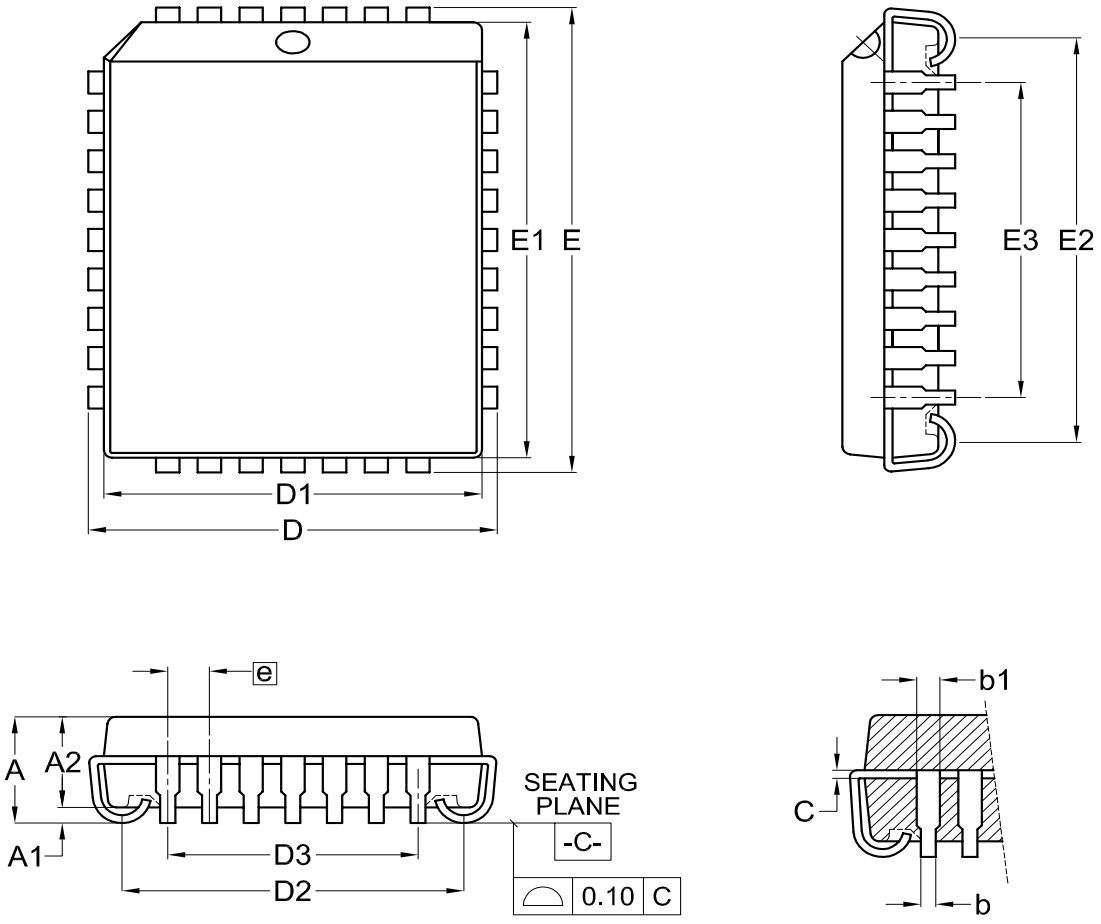
PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE	Remark
MX29LV040CTC-55R	55	30	5	32 Pin TSOP	
MX29LV040CTC-70	70	30	5	32 Pin TSOP	
MX29LV040CTC-90	90	30	5	32 Pin TSOP	
MX29LV040CTC-12	120	30	5	32 Pin TSOP	
MX29LV040CQC-55R	55	30	5	32 Pin PLCC	
MX29LV040CQC-70	70	30	5	32 Pin PLCC	
MX29LV040CQC-90	90	30	5	32 Pin PLCC	
MX29LV040CQC-12	120	30	5	32 Pin PLCC	
MX29LV040CTI-55R	55	30	5	32 Pin TSOP	
MX29LV040CTI-70	70	30	5	32 Pin TSOP	
MX29LV040CTI-90	90	30	5	32 Pin TSOP	
MX29LV040CTI-12	120	30	5	32 Pin TSOP	
MX29LV040CQI-55R	55	30	5	32 Pin PLCC	
MX29LV040CQI-70	70	30	5	32 Pin PLCC	
MX29LV040CQI-90	90	30	5	32 Pin PLCC	
MX29LV040CQI-12	120	30	5	32 Pin PLCC	
MX29LV040CTC-55Q	55	30	5	32 Pin TSOP	PB free
MX29LV040CTC-70G	70	30	5	32 Pin TSOP	PB free
MX29LV040CTC-90G	90	30	5	32 Pin TSOP	PB free
MX29LV040CTC-12G	120	30	5	32 Pin TSOP	PB free
MX29LV040CQC-55Q	55	30	5	32 Pin PLCC	PB free
MX29LV040CQC-70G	70	30	5	32 Pin PLCC	PB free
MX29LV040CQC-90G	90	30	5	32 Pin PLCC	PB free
MX29LV040CQC-12G	120	30	5	32 Pin PLCC	PB free
MX29LV040CTI-55Q	55	30	5	32 Pin TSOP	PB free
MX29LV040CTI-70G	70	30	5	32 Pin TSOP	PB free
MX29LV040CTI-90G	90	30	5	32 Pin TSOP	PB free
MX29LV040CTI-12G	120	30	5	32 Pin TSOP	PB free
MX29LV040CQI-55Q	55	30	5	32 Pin PLCC	PB free
MX29LV040CQI-70G	70	30	5	32 Pin PLCC	PB free
MX29LV040CQI-90G	90	30	5	32 Pin PLCC	PB free
MX29LV040CQI-12G	120	30	5	32 Pin PLCC	PB free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for 32L PLCC

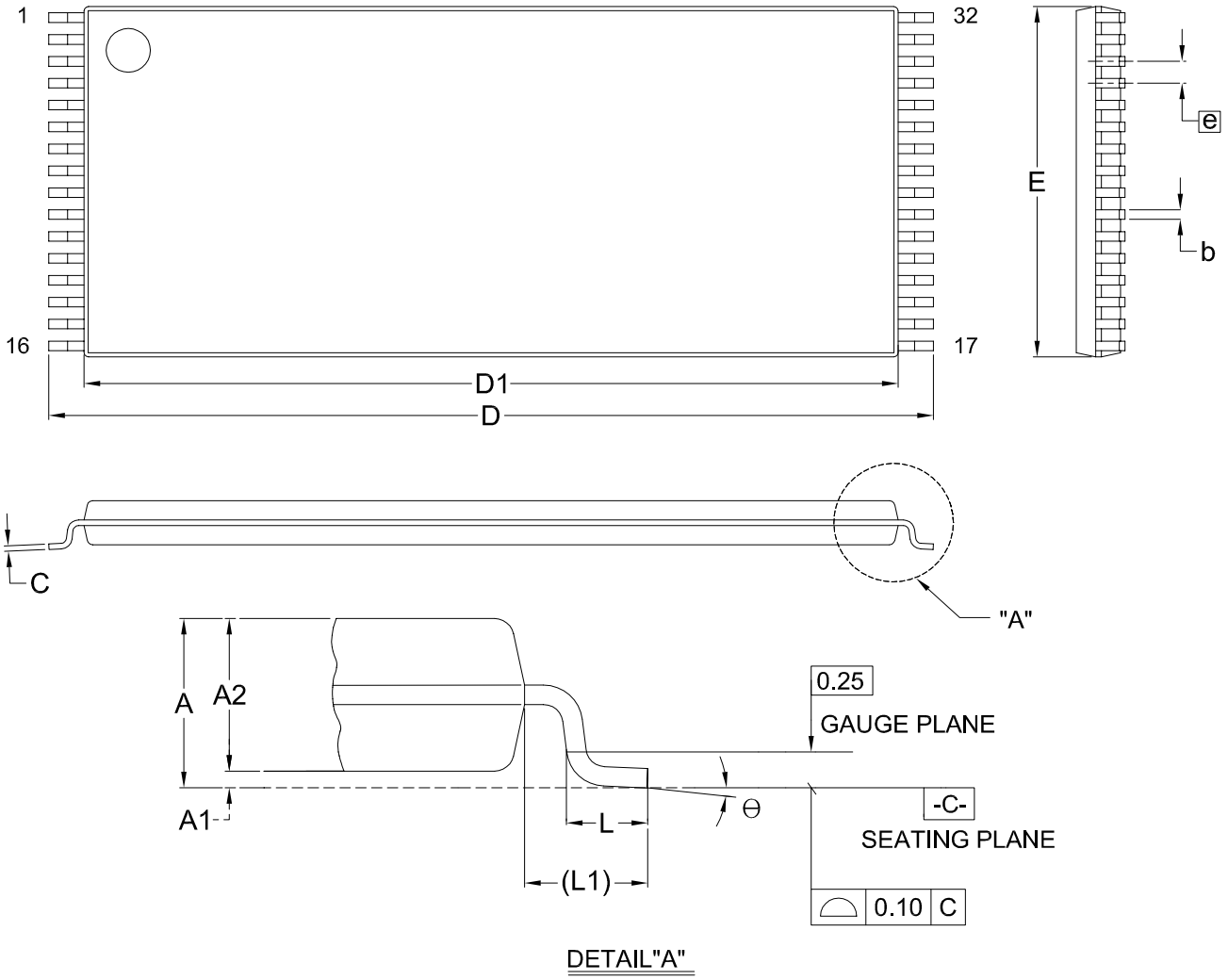


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
mm	Min.	—	0.38	2.69	0.38	0.61	0.20	12.32	11.36	10.11		14.86	13.98	12.65		
	Nom.	—	0.58	2.79	0.46	0.71	0.25	12.45	11.43	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.81	2.89	0.54	0.81	0.30	12.58	11.50	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.447	0.398		0.585	0.550	0.498		
	Nom.	---	0.023	0.110	0.018	0.028	0.010	0.490	0.450	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.032	0.114	0.021	0.032	0.012	0.495	0.453	0.422		0.595	0.556	0.522		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-2002	7	MS-016			12-10-'03

Title: **Package Outline for TSOP(I) 32L (8X20mm)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	9	MO-142			11-26-'03

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Preliminary"	P1	JUN/30/2005
	2. Added "Recommended Operating Conditions"	P43	
1.1	1. Modified "Low power consumption--active current" from 20mA(Max.) to 30mA(Max.)	P1	AUG/30/2005
	2. Added description about Pb-free devices are RoHS Compliant	P1	
1.2	1. Modified Erase Resume from delay 10ms to delay 400us	P12,32	JAN/17/2006
1.3	1. Modified table 15. CFI mode	P45,46	APR/24/2006
	2. Added VLKO description	P15,18	

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