REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Removed vendor CAGE 61772 from device types 01YX and 02YX. Technical change was made in table I. Editorial changes throughout.	1990 JUL 24	Weckman

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REV STATUS OF SHEETS	REV	A		A		A					A	A	A	A			A	A	A					
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18					

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Tim Noh

CHECKED BY: Tim Noh

APPROVED BY: William K. Heckman

DRAWING APPROVAL DATE: 1 AUGUST 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS 16-BIT MICROPROGRAM SEQUENCER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88643
A	67268	

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88643	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	49C410	16-bit CMOS microprogram sequencer with 33 deep stack
02	49C410A	16-bit CMOS microprogram sequencer with 33 deep stack

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-14, (48-lead, 2.435" x .620" x .225"), dual-in-line package
Y	See figure 1, (48-terminal, .565" x .565" x .120"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	-0.5 V dc to +7.0 V dc
DC output current	+30 mA
Power dissipation (P_D) 2/	1.0 W
Storage temperature	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	See MIL-M-38510, appendix C
Case Y	20°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature (T_C)	-55°C to +125°C
Minimum logic high voltage (V_{IH})	2.0 V dc
Maximum logic low voltage (V_{IL})	0.8 V dc

1/ All voltage referenced to GND
2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2 herein.

3.2.2 Instruction set. The instruction set shall be as specified on figure 3 herein.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 4 herein.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output	V_{OH}	V_{CC} = 4.5 V V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OH} = -300 µA	1,2,3	All	4.3		V
			I_{OH} = -12 mA			2.4		
Low level output	V_{OL}	V_{CC} = 4.5 V V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OL} = 300 µA	1,2,3	All		0.2	V
			I_{OL} = 20 mA				0.5	
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1,2,3	All		5.0	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND		1,2,3	All		-5.0	µA
Short circuit output current	I_{OS}	V_{CC} = 4.5 V, V_{OUT} = GND 1/		1,2,3	All	-30		mA
Off state high impedance output current	I_{OZ}	V_{CC} = 5.5 V	V_{OUT} = 0 V	1,2,3	All		-10	µA
			V_{OUT} = 5.5 V				10	
Quiesecent power supply current (CMOS inputs)	I_{CCQH}	V_{CC} = 5.5 V, $V_{IL} \le$ 0.2 V, $V_{IH} \ge$ 5.3 V, f_{CP} = 0, CP = H		1,2,3	All		50	mA
Quiesecent power supply current (CMOS inputs)	I_{CCQL}	V_{CC} = 5.5 V, $V_{IL} \le$ 0.2 V, $V_{IH} \ge$ 5.3 V, f_{CP} = 0, CP = L		1,2,3	All		50	
Quiesecent power supply current (TTL inputs) 2/	I_{CCT}	V_{CC} = 5.5 V, V_{IN} = 3.4 V, f_{CP} = 0		1,2,3	All		0.5	mA/ input

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic power supply current	I_{CCD}	V_{CC} = 5.5 V, $V_{IL} \le$ 0.2 V, V_{IH} = 5.3 V, outputs open, $\overline{OE}$ = L	1,2,3	All		3.0	mA/MHz
Total power supply current 3/	I_{CC}	V_{CC} = 5.5 V, f_{CP} = 10 MHz, outputs open, $V_{IH} \ge$ 5.3 V, $V_{IL} \le$ 0.2 V, $\overline{OE}$ = L, CP = 50% duty cycle	1,2,3	All		80	mA
		V_{CC} = 5.5 V, f_{CP} = 10 MHz, outputs open, V_{IH} = 3.4 V, V_{IL} = 0.4 V, $\overline{OE}$ = L, CP = 50% duty cycle				90	
Input capacitance	C_{IN}	See 4.3.1c	4	All		12	pF
Output capacitance	C_{OUT}	See 4.3.1c	4	All		15	pF
Functional test		See 4.3.1d	7, 8	All			
Setup time D_1 to R	t_{S1}	See figure 5 4/	9,10,11	01	16		ns
				02	7.0		ns
Setup time D_1 to PC	t_{S2}	See figure 5 4/	9,10,11	01	30		ns
				02	15		ns
Setup time I_{0-3}	t_{S3}	See figure 5 4/	9,10,11	01	38		ns
				02	25		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0$ V dc ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time $\overline{CC}$	t_{S4}	See figure 5 4/	9,10,11	01	35		ns
				02	18		ns
Setup time $\overline{CCEN}$	t_{S5}		9,10,11	01	35		ns
				02	18		ns
Setup time CI	t_{S6}		9,10,11	01	18		ns
				02	7.0		ns
Setup time $\overline{RLD}$	t_{S7}		9,10,11	01	20		ns
				02	12		ns
Hold time D_1 to R	t_{H1}		9,10,11	01	0		ns
				02	0		ns
Hold time D_1 to PC	t_{H2}		9,10,11	01	0		ns
				02	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0$ V dc ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time I_{0-3}	t_{H3}	See figure 5 4/	9,10,11	01	0		ns
				02	0		ns
Hold time $\overline{CC}$	t_{H4}		9,10,11	01	0		ns
				02	0		ns
Hold time $\overline{CCEN}$	t_{H5}		9,10,11	01	0		ns
				02	0		ns
Hold time CI	t_{H6}		9,10,11	01	0		ns
				02	0		ns
Hold time $\overline{RLD}$	t_{H7}		9,10,11	01	0		ns
				02	0		ns
Propagation delay D_{0-11} to Y	t_{PD1}		9,10,11	01		25	ns
				02		15	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0$ V dc ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay I_{0-3} to Y	t_{PD2}	See figure 5 4/	9,10,11	01		40	ns
				02		25	ns
Propagation delay $\overline{CC}$ to Y	t_{PD3}		9,10,11	01		36	ns
				02		20	ns
Propagation delay $\overline{CCEN}$ to Y	t_{PD4}		9,10,11	01		36	ns
				02		20	ns
Propagation delay CP to Y	t_{PD5}		9,10,11	01		46	ns
				02		33	ns
Propagation delay $\overline{OE}$ to Y (enable)	t_{PD6}		9,10,11	01		25	ns
				02		13	ns
Propagation delay $\overline{OE}$ to Y (disable) 5/	t_{PD7}		9,10,11	01		30	ns
				02		13	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0$ V dc ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay I_{0-3} to $\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	t_{PD8}	See figure 5 4/	9,10,11	01		35	ns
				02		15	ns
Propagation delay CP to $\overline{FULL}$	t_{PD9}		9,10,11	01		35	ns
				02		25	ns
Clock LOW time	t_{PW1}		9,10,11	01	25		ns
				02	20		ns
Clock HIGH time	t_{PW2}		9,10,11	01	25		ns
				02	20		ns
Clock period	t_P		9,10,11	01	51		ns
				02	40		ns

1/ Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

2/ I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4 V, subtracting out I_{CCQH}, then dividing by the total number of inputs.

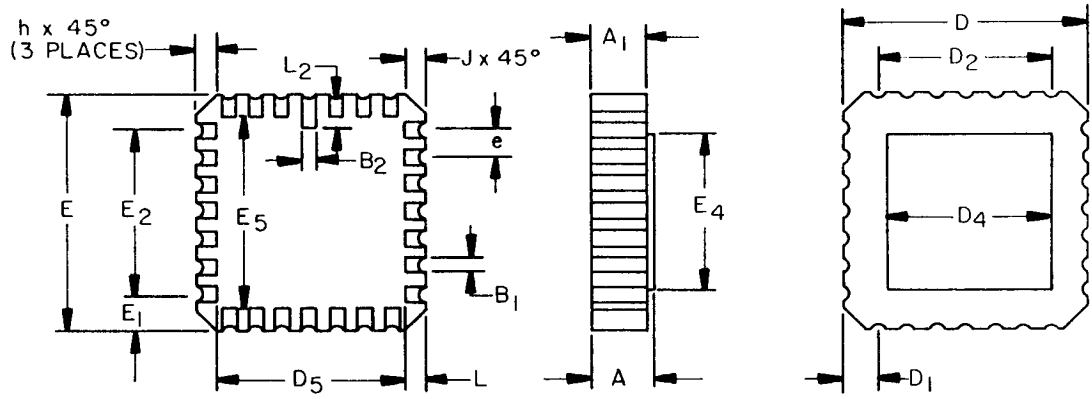
3/ $I_{CC} = I_{CCQH} (CD_H) + I_{CCQL} (1 - CD_H) + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{CP})$.

Where: CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4 V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock input frequency.

4/ Unless otherwise specified, the input pulse level shall be between 0 V to 3.0 V, input rise/fall times shall be 1.0 V/ns and input and output timing reference levels shall be 1.5 V.

5/ Disable time is measured to 0.5 V change on output voltage level with C_L = 5 pF.

Case Y



Inches	mm	Inches	mm
.012	0.30	.077	1.96
.017	0.43	.090	2.29
.020	0.51	.093	2.36
.023	0.58	.120	3.05
.033	0.84	.440	11.18
.040	1.02	.480	12.19
.045	1.14	.546	13.87
.047	1.19	.554	14.07
.055	1.40	.572	14.53
.060	1.52		

FIGURE 1. Case outline.

Number of leads (N)	48		Number of leads (N)	48	
	Min	Max		Min	Max
A	.055	.120	E_1	.060 REF	
A_1	.045	.090	E_2	.440 BSC	
B_1	.017	.023	E_4		.546
B_2	.017	.033	E_5	.480 REF	
D	.554	.572	e	.040 BSC	
D_1	.060 REF		h	.012 Radius	
D_2	.440 BSC		J	.020 REF	
D_4		.546	L	.033	.047
D_5	.480 REF		L2	.077	.093
E	.554	.572	N	48	
			ND	12	

ND = NE - Number of leads per side.

FIGURE 1. Case outline - Continued.

Cases X and Y

Pin number	Terminal connection	Pin number	Terminal connection
1	Y_{13}	25	D_{15}
2	D_{13}	26	Y_{15}
3	Y_4	27	D_8
4	D_4	28	Y_8
5	Y_5	29	D_9
6	D_5	30	Y_9
7	$\overline{VECT}$	31	D_{10}
8	$\overline{PL}$	32	Y_{10}
9	$\overline{MAP}$	33	D_{11}
10	I_3	34	Y_{11}
11	I_2	35	$\overline{OE}$
12	V_{3CC}	36	GND
13	I_1	37	CP
14	I_0	38	CI
15	$\overline{CCEN}$	39	Y_0
16	$\overline{CC}$	40	D_0
17	$\overline{RLD}$	41	Y_1
18	$\overline{FULL}$	42	D_1
19	D_6	43	Y_2
20	Y_6	44	D_2
21	D_7	45	Y_3
22	Y_7	46	D_3
23	D_{14}	47	Y_{12}
24	Y_{14}	48	D_{12}

FIGURE 2. Terminal connections.

I_3-I_0	Mnemonic	CC	Counter test	Stack	Address source	Register/ counter	Enable/ select
0	JZ	X	X	Clear	0	NC	$\overline{PL}$
1	CJS	Pass Fail	X X	Push NC	D Pc	NC NC	$\overline{PL}$ $\overline{PL}$
2	JMAP	X	X	NC	D	NC	$\overline{MAP}$
3	CJP	Pass Fail	X X	NC NC	D Pc	NC NC	$\overline{PL}$ $\overline{PL}$
4	PUSH	Pass Fail	X X	Push Push	Pc Pc	Load NC	$\overline{PL}$ $\overline{PL}$
5	JSRP	Pass Fail	X X	Push Push	D R	NC NC	$\overline{PL}$ $\overline{PL}$
6	CJV	Pass Fail	X X	NC NC	D Pc	NC NC	$\overline{VECT}$ $\overline{VECT}$
7	JRP	Pass Fail	X X	NC NC	D R	NC NC	$\overline{PL}$ $\overline{PL}$
8	RFCT	X X	= 0 Not = 0	Pop NC	Pc Stack	NC DEC	$\overline{PL}$ $\overline{PL}$
9	RPCT	X X	= 0 Not = 0	NC NC	Pc D	NC DEC	$\overline{PL}$ $\overline{PL}$
10	RPCT	Pass Fail	X X	Pop NC	Stack Pc	NC NC	$\overline{PL}$ $\overline{PL}$
11	CJPP	Pass Fail	X X	Pop NC	D Pc	NC NC	$\overline{PL}$ $\overline{PL}$
12	LDCT	X	X	NC	Pc	Load	$\overline{PL}$
13	LOOP	Pass Fail	X X	Pop NC	Pc Stack	NC NC	$\overline{PL}$ $\overline{PL}$
14	CONT	X	X	NC	Pc	NC	$\overline{PL}$
15	TWB	Pass Pass Fail Fail	= 0 Not = 0 = 0 Not = 0	Pop Pop Pop NC	Pc Pc D Stack	NC DEC NC DEC	$\overline{PL}$ $\overline{PL}$ $\overline{PL}$ $\overline{PL}$

NC = No change; DEC = Decrement

FIGURE 3. Instruction set.

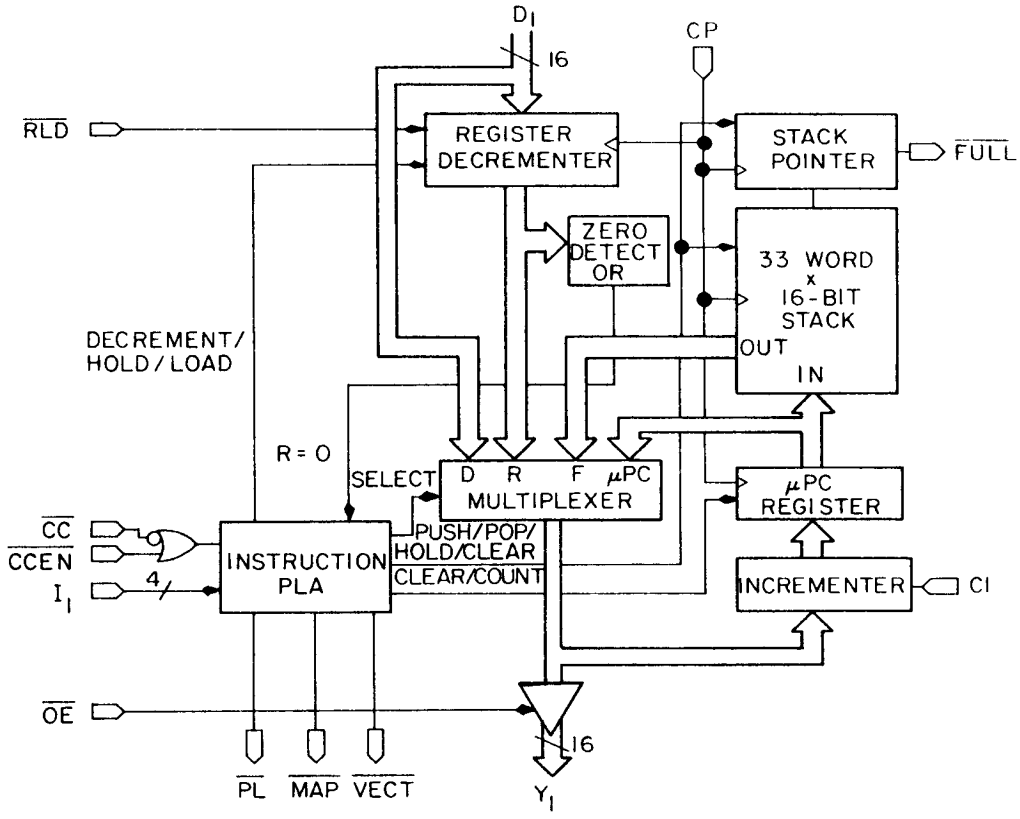


FIGURE 4. Logic diagram.

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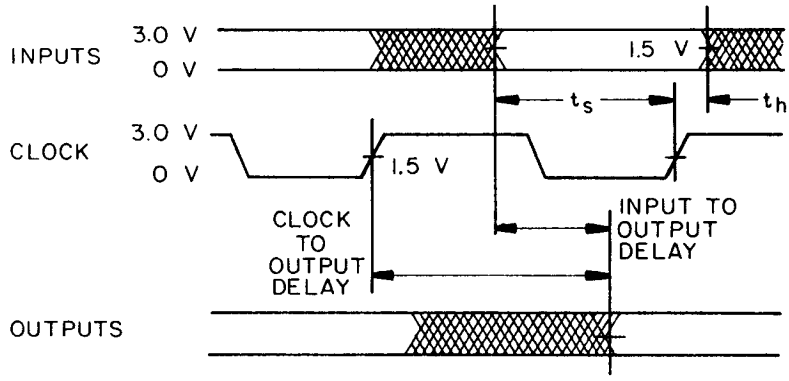
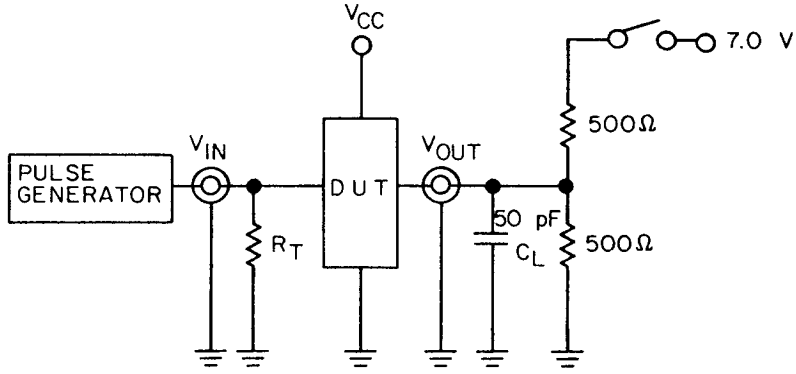
		REVISION LEVEL	SHEET 14





Test	Switch
Open drain Disable low Enable low	Closed
All other outputs	Open

C_L = Load capacitance: Includes jig and probe capacitance
R_T = Termination resistance: should be equal to Z_{OUT} of the pulse generator

FIGURE 5. Switching waveforms and test circuit.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only initially test and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 functional testing shall include the verification of instruction set.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1*, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8

* PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using Dd Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECC. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8864301XX	61772	IDT49C410CB
5962-8864301YX	2/	IDT49C410LB
5962-8864302XX	61772	IDT49C410ACB
5962-8864302YX	2/	IDT49C410ALB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Approved source of supply not available.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology Incorporated 1566 Moffett Boulevard Salinas CA 93905 Point of contact: 3236 Scott Boulevard Santa Clara CA 95054