CLASS V, 12-BIT, 500-MSPS ANALOG-TO-DIGITAL CONVERTER

Check for Samples :ADS5463-SP

FEATURES

- **500-MSPS Sample Rate**
- **12-Bit Resolution, 10-Bits Effective Number of Bits (ENOB)**
- **SNR > 64.5 dBFS at 450 MHz and 500 MSPS**
- **SFDR > 64.0 dBc at 450 MHz and 500 MSPS**
- **2.2-V_{PP} Differential Input Voltage**
- **LVDS-Compatible Outputs**
- **Total Power Dissipation: 2.2 W**
- **Offset Binary Output Format**
- **Output Data Transitions on the Rising and Falling Edges of a Half-Rate Output Clock**
- **On-Chip Analog Buffer, Track and Hold, and Reference Circuit**
- **Available in a 84-Pin Ceramic Nonconductive Tie-Bar Package (HFG).**
- **Military Temperature Range (–55°C to 125°C T_{case})**

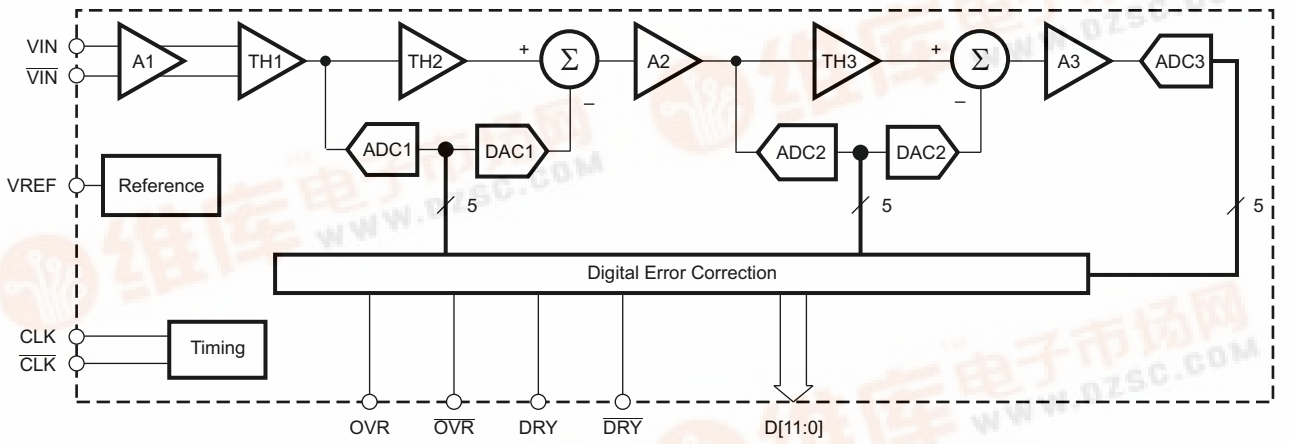
APPLICATIONS

- **Test and Measurement Instrumentation**
- **Software-Defined Radio**
- **Data Acquisition**
- **Power Amplifier Linearization**
- **Communication Instrumentation**
- **Radar**

DESCRIPTION/ORDERING INFORMATION

The ADS5463 is a 12-bit, 500-MSPS analog-to-digital converter (ADC) that operates from both a 5-V supply and 3.3-V supply, while providing LVDS-compatible digital outputs from the 3.3-V supply. The ADS5463 input buffer isolates the internal switching of the onboard track and hold (T&H) from disturbing the signal source. An internal reference generator is also provided to simplify the system design further. The ADS5463 has outstanding low noise and linearity over input frequency.

The ADS5463 is available in a 84-pin ceramic nonconductive tie-bar package (HFG). The ADS5463 is built on state-of-the-art Texas Instruments complementary bipolar process (BiCom3X) and is specified over the full military temperature range (–55°C to 125°C T_{case}).



B0061-03

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

TEMPERATURE	PACKAGE (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C T_{case}	84 / HFG	5962-0720801VXC	5962-0720801VXC ADS5463MHFG-V

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
Supply voltage	AVDD5 to GND		6	V
	AVDD3 to GND		5	
	DVDD3 to GND		5	
AIN, $\overline{AIN}$ to GND(2)	Voltage difference between pin and ground	AC signal	–0.3 to (AVDD5 + 0.3)	V
		DC signal, T_J = 105°C	0.4 to 4.4	
		DC signal, T_J = 125°C	1.0 to 3.8	
AIN to $\overline{AIN}$ (2)	Voltage difference between these pins	AC signal	–5.2 to 5.2	V
		DC signal, T_J = 105°C	–4 to 4	
		DC signal, T_J = 125°C	–2.8 to 2.8	
CLK, $\overline{CLK}$ to GND(2)	Voltage difference between pin and ground	AC signal	–0.3 to (AVDD5 + 0.3)	V
		DC signal, T_J = 105°C	0.1 to 4.7	
		DC signal, T_J = 125°C	1.1 to 3.7	
CLK to $\overline{CLK}$ (2)	Voltage difference between these pins	AC signal	–3.3 to 3.3	V
		DC signal, T_J = 105°C	–3.3 to 3.3	
		DC signal, T_J = 125°C	–2.6 to 2.6	
Data output to GND(2)	LVDS digital outputs		–0.3 to (DVDD3 + 0.3)	V
T_C	Characterized case operating temperature range		–55 to 125	°C
T_J	Maximum junction temperature		150	°C
T_{STG}	Storage temperature range		–65 to 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Valid when supplies are within recommended operating range.

Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
Supplies					
AVDD5	Analog supply voltage	4.75	5	5.25	V
AVDD3	Analog supply voltage	3	3.3	3.6	V
DVDD3	Output driver supply voltage	3	3.3	3.6	V
Analog Input					
	Differential input range		2.2		V_{pp}
V_{CM}	Input common mode		2.4		V
Digital Output					
	Maximum differential output load		10		pF
Clock Input					
	CLK input sample rate (sine wave)			500	MSPS
	Clock amplitude, differential sine wave		3		V_{pp}
	Clock duty cycle		50		%
T_c	**Operating case temperature**	–55		125	°C

Electrical Characteristics

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution					12		Bits
Analog Inputs							
	Differential input range				2.2		V_{PP}
	Input resistance (dc)	Each input to VCM			500		Ω
	Input capacitance	Each input to ground			2.5		pF
	Analog input bandwidth			1000			MHz
Internal Reference Voltage							
VREF	Reference voltage		Full Temp Range	2.38	2.4	2.42	V
Dynamic Accuracy							
	No missing codes				Assured		
DNL	Differential linearity error	f_{IN} = 210 MHz	Full Temp Range	–0.98	±0.95	1.2	LSB
INL	Integral linearity error	f_{IN} = 210 MHz	Full Temp Range	–2.9	±1.5	2.9	LSB
	Offset error		Full Temp Range	–0.5		0.5	%FS
	Offset temperature coefficient				0.0009		%FS/°C
	Gain error		Full Temp Range	–5		5	%FS
	Gain temperature coefficient				–0.02		%FS/°C
Power Supply							
I_{AVDD5}	5 V analog supply current	V_{IN} = full scale, f_{IN} = 300 MHz, F_S = 500 MSPS	Full Temp Range			335	mA
I_{AVDD3}	3.3 V analog supply current					140	mA
I_{DVDD3}	3.3 V digital supply current(includes LVDS)					88	mA
	Power dissipation					2.425	W

Electrical Characteristics

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dynamic AC Characteristics							
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz			65.4		dBFS
		f_{IN} = 70 MHz			65.3		
		f_{IN} = 100 MHz	T_C = 25°C	64.1	65.2		
			T_C = $T_{C,MAX}$	62.7			
			T_C = $T_{C,MIN}$	63.5			
		f_{IN} = 210 MHz	T_C = 25°C	63.6	65.0		
			T_C = $T_{C,MAX}$	62.4			
			T_C = $T_{C,MIN}$	63.2			
		f_{IN} = 300 MHz	T_C = 25°C	62.7	64.9		
			T_C = $T_{C,MAX}$	61.3			
			T_C = $T_{C,MIN}$	61.9			
		f_{IN} = 450 MHz			64.5		
		f_{IN} = 650 MHz			63.7		
		f_{IN} = 900 MHz			62.8		
		f_{IN} = 1.0 GHz			62.2		
SFDR	Spurious free dynamic range	f_{IN} = 10 MHz			63.5		dBc
		f_{IN} = 70 MHz			64.2		
		f_{IN} = 100 MHz	T_C = 25°C	57.9	65.0		
			T_C = $T_{C,MAX}$	58.8			
			T_C = $T_{C,MIN}$	58.6			
		f_{IN} = 210 MHz	T_C = 25°C	55.2	64.0		
			T_C = $T_{C,MAX}$	56.6			
			T_C = $T_{C,MIN}$	56.9			
		f_{IN} = 300 MHz	T_C = 25°C	54.1	64.0		
			T_C = $T_{C,MAX}$	51.3			
			T_C = $T_{C,MIN}$	56.2			
		f_{IN} = 450 MHz			64.0		
		f_{IN} = 650 MHz			61.6		
		f_{IN} = 900 MHz			54.5		
		f_{IN} = 1.0 GHz			51.6		

Electrical Characteristics (continued)

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD2	Second harmonic	f_{IN} = 10 MHz			63.5		dBc
		f_{IN} = 70 MHz			64.2		
		f_{IN} = 100 MHz	T_C = 25°C	57.9	65.4		
			T_C = $T_{C,MAX}$	58.8			
			T_C = $T_{C,MIN}$	58.6			
		f_{IN} = 210 MHz	T_C = 25°C	55.2	64.4		
			T_C = $T_{C,MAX}$	56.6			
			T_C = $T_{C,MIN}$	56.9			
		f_{IN} = 300 MHz	T_C = 25°C	54.1	64.3		
			T_C = $T_{C,MAX}$	51.3			
			T_C = $T_{C,MIN}$	56.2			
		f_{IN} = 450 MHz			64.4		
		f_{IN} = 650 MHz			67.1		
		f_{IN} = 900 MHz			62.9		
		f_{IN} = 1.0 GHz			58.6		
HD3	Third harmonic	f_{IN} = 10 MHz			104		dBc
		f_{IN} = 70 MHz			104		
		f_{IN} = 100 MHz	T_C = 25°C	69.0	87.0		
			T_C = $T_{C,MAX}$	68.5			
			T_C = $T_{C,MIN}$	65.6			
		f_{IN} = 210 MHz	T_C = 25°C	66.7	85.0		
			T_C = $T_{C,MAX}$	65.3			
			T_C = $T_{C,MIN}$	64.1			
		f_{IN} = 300 MHz	T_C = 25°C	70.1	76.0		
			T_C = $T_{C,MAX}$	61.9			
			T_C = $T_{C,MIN}$	64.8			
		f_{IN} = 450 MHz			73.3		
		f_{IN} = 650 MHz			61.6		
		f_{IN} = 900 MHz			54.5		
		f_{IN} = 1.0 GHz			51.6		

Electrical Characteristics

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dynamic AC Characteristics (continued)							
SINAD	Signal-to-noise and distortion	f_{IN} = 10 MHz			61.9		dBc
		f_{IN} = 70 MHz			62.2		
		f_{IN} = 100 MHz	T_C = 25°C	58.0	62.0		
			T_C = $T_{C,MAX}$	58.0			
			T_C = $T_{C,MIN}$	58.4			
		f_{IN} = 210 MHz	T_C = 25°C	55.8	62.0		
			T_C = $T_{C,MAX}$	56.2			
			T_C = $T_{C,MIN}$	56.7			
		f_{IN} = 300 MHz	T_C = 25°C	54.9	61.9		
			T_C = $T_{C,MAX}$	52.2			
			T_C = $T_{C,MIN}$	56.1			
		f_{IN} = 450 MHz			61.6		
		f_{IN} = 650 MHz			59.4		
		f_{IN} = 900 MHz			54.3		
		f_{IN} = 1.0 GHz			51.4		
	Worst harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz			83.1		dBc
		f_{IN} = 70 MHz			80.2		
		f_{IN} = 100 MHz	T_C = 25°C	72.2	81.8		
			T_C = $T_{C,MAX}$	70.6			
			T_C = $T_{C,MIN}$	72.6			
		f_{IN} = 210 MHz	T_C = 25°C	70.6	77.5		
			T_C = $T_{C,MAX}$	67.1			
			T_C = $T_{C,MIN}$	66.5			
		f_{IN} = 300 MHz	T_C = 25°C	69.3	78.2		
			T_C = $T_{C,MAX}$	66.3			
			T_C = $T_{C,MIN}$	66.3			
		f_{IN} = 450 MHz			80.6		
		f_{IN} = 650 MHz			80.0		
		f_{IN} = 900 MHz			79.4		
		f_{IN} = 1.0 GHz			77.6		

Electrical Characteristics (continued)

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f_{IN} = 10 MHz			63.5		dBc
		f_{IN} = 70 MHz			64		
		f_{IN} = 100 MHz	T_C = 25°C	57.8	65.2		
			T_C = $T_{C,MAX}$	58.3			
			T_C = $T_{C,MIN}$	58.1			
		f_{IN} = 210 MHz	T_C = 25°C	55.0	64.1		
			T_C = $T_{C,MAX}$	55.9			
			T_C = $T_{C,MIN}$	56.2			
		f_{IN} = 300 MHz	T_C = 25°C	53.9	63.8		
			T_C = $T_{C,MAX}$	51.0			
			T_C = $T_{C,MIN}$	55.6			
		f_{IN} = 450 MHz			63.7		
		f_{IN} = 650 MHz			60.5		
		f_{IN} = 900 MHz			53.9		
		f_{IN} = 1.0 GHz			50.8		
ENOB	Effective number of bits	f_{IN} = 100 MHz	T_C = 25°C	9.3	10.1		Bits
			T_C = $T_{C,MAX}$	9.3			
			T_C = $T_{C,MIN}$	9.4			
		f_{IN} = 210 MHz	T_C = 25°C	8.9	10.0		
			T_C = $T_{C,MAX}$	9.0			
			T_C = $T_{C,MIN}$	9.1			
		f_{IN} = 300 MHz	T_C = 25°C	8.8	9.9		
			T_C = $T_{C,MAX}$	8.3			
			T_C = $T_{C,MIN}$	9.0			
	RMS idle-channel noise	Inputs tied to common-mode			0.7		LSB
LVDS Digital Outputs							
VOD	Differential output voltage			247	350	454	mV
VOC	Common mode output voltage			1.125		1.375	V

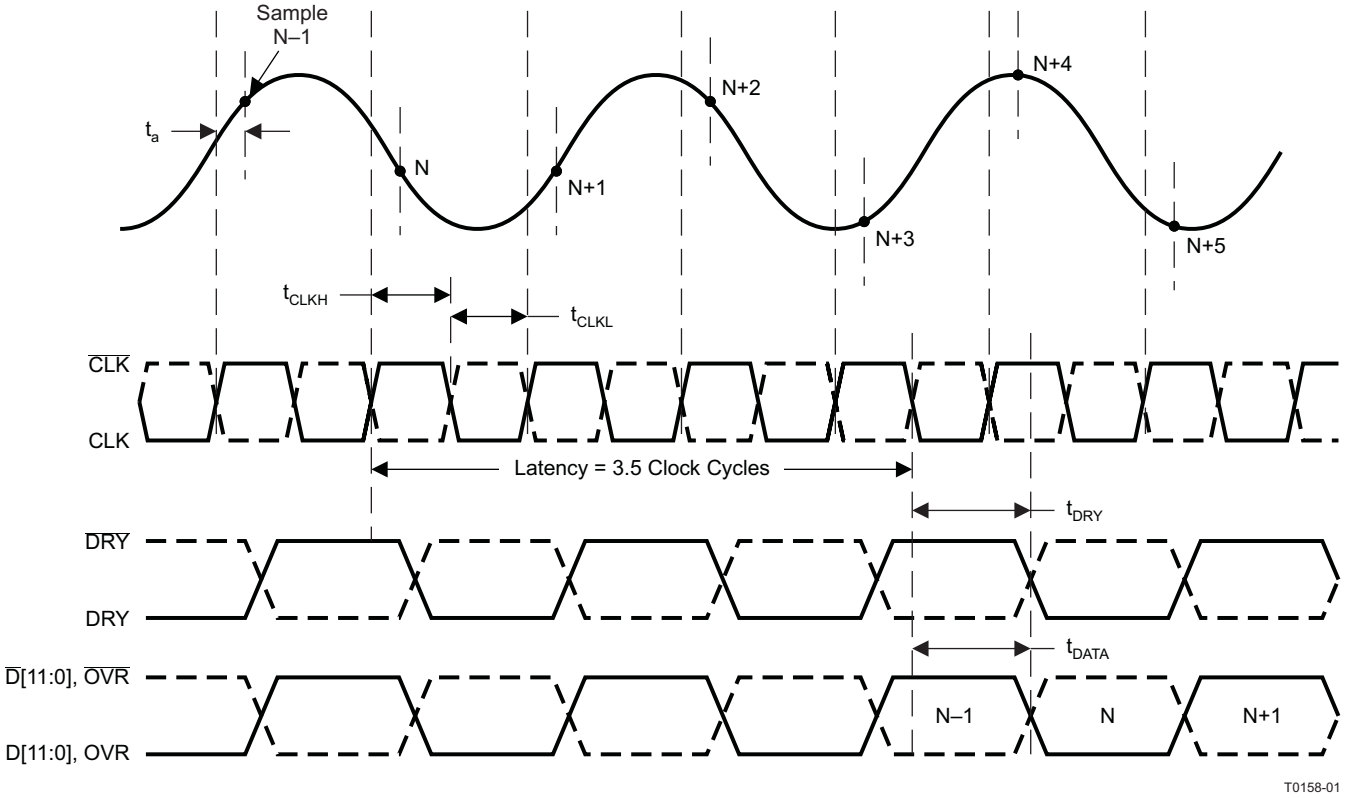


Figure 1. Timing Diagram

Timing Characteristics

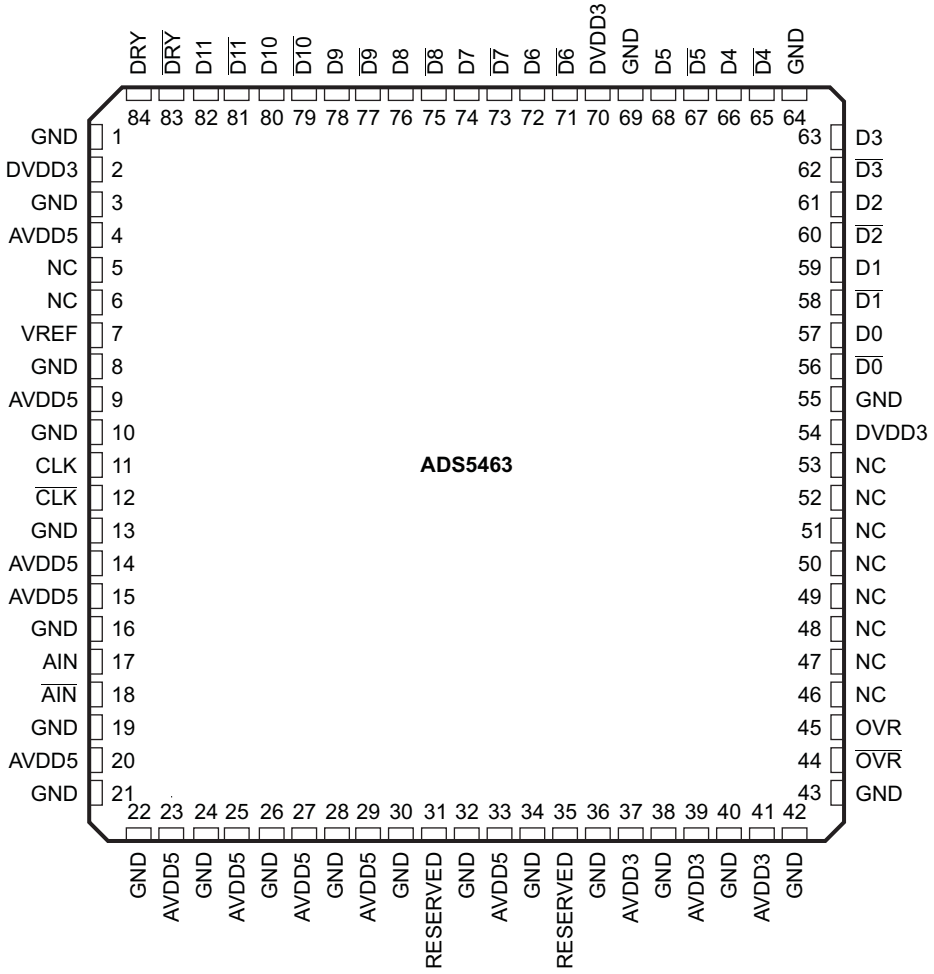
Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER (1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay			200		ps
	Aperture jitter, rms			160		fs
	Latency			3.5		cycles
t_{CLK}	Clock period		2		50	ns
t_{CLKH}	Clock pulse duration, high		1			ns
t_{CLKL}	Clock pulse duration, low		1			ns
t_{DRY}	CLK to DRY delay(2)	Zero crossing	750	1500	2500	ps
t_{DATA}	CLK to DATA/OVR delay(2)	Zero crossing	650	1150	1750	ps
t_{SKEW}	DATA to DRY skew	t_{DATA}–t_{DRY}	-1250	-400	700	ps
t_{RISE}	DRY/DATA/OVR rise time			500		ps
t_{FALL}	DRY/DATA/OVR fall time			500		ps

(1) Timing parameters are assured by design or characterization, but not production tested. <10pF load on each output pin.
(2) DRY, DATA and OVR are updated on the falling edge of CLK. The latency must be added to t_{DATA} to determine the overall propagation delay.

PIN CONFIGURATION

HFG PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AIN	17	Differential input signal (positive)
$\overline{\text{AIN}}$	18	Differential input signal (negative)
AVDD5	4, 9, 14, 15, 20, 23, 25, 27, 29, 33	Analog power supply (5 V)
AVDD3	37, 39, 41	Analog power supply (3.3 V) (Suggestion for 250 MSPS: leave option to connect to 5 V for ADS5440/4 compatibility)
DVDD3	2, 54, 70	Output driver power supply (3.3 V)
GND	1, 3, 8, 10, 13, 16, 19, 21, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 43, 55, 64, 69	Ground
CLK	11	Differential input clock (positive). Conversion initiated on rising edge.
$\overline{\text{CLK}}$	12	Differential input clock (negative)
$\overline{\text{D0}}$, D0	56, 57	LVDS digital output pair, least-significant bit (LSB)
$\overline{\text{D1}}$-D3, D1-$\overline{\text{D3}}$	58–63	LVDS digital output pair
$\overline{\text{D4}}$–D5, D4–$\overline{\text{D5}}$	65–68	LVDS digital output pairs
$\overline{\text{D6}}$–D10, D6–$\overline{\text{D10}}$	71–80	LVDS digital output pairs
$\overline{\text{D11}}$, D11	81, 82	LVDS digital output pair, most-significant bit (MSB)
$\overline{\text{DRY}}$, DRY	83, 84	Data ready LVDS output pair
NC	5–6, 46–53	No connect (5 and 6 should be left floating, 46–53 are possible future bit additions for this pinout and therefore can be connected to a digital bus or left floating)
$\overline{\text{OVR}}$, OVR	44, 45	Overrange indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
RESERVED	31, 35	Reserved for possible future control features
VREF	7	Reference voltage

Thermal Characteristics(1)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Junction-to-case thermal resistance	21.81	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	MIL-STD-883 Test Method 1012	0.849	°C/W

(1) This CQFP package has built-in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. To efficiently remove heat and provide a low-impedance ground path, a thermal land is required on the surface of the PCB directly underneath the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, the PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. TI typically recommends an 11,9 mm^2 board-mount thermal pad. This allows maximum area for thermal dissipation, while keeping leads away from the pad area to prevent solder bridging. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically at ground potential.

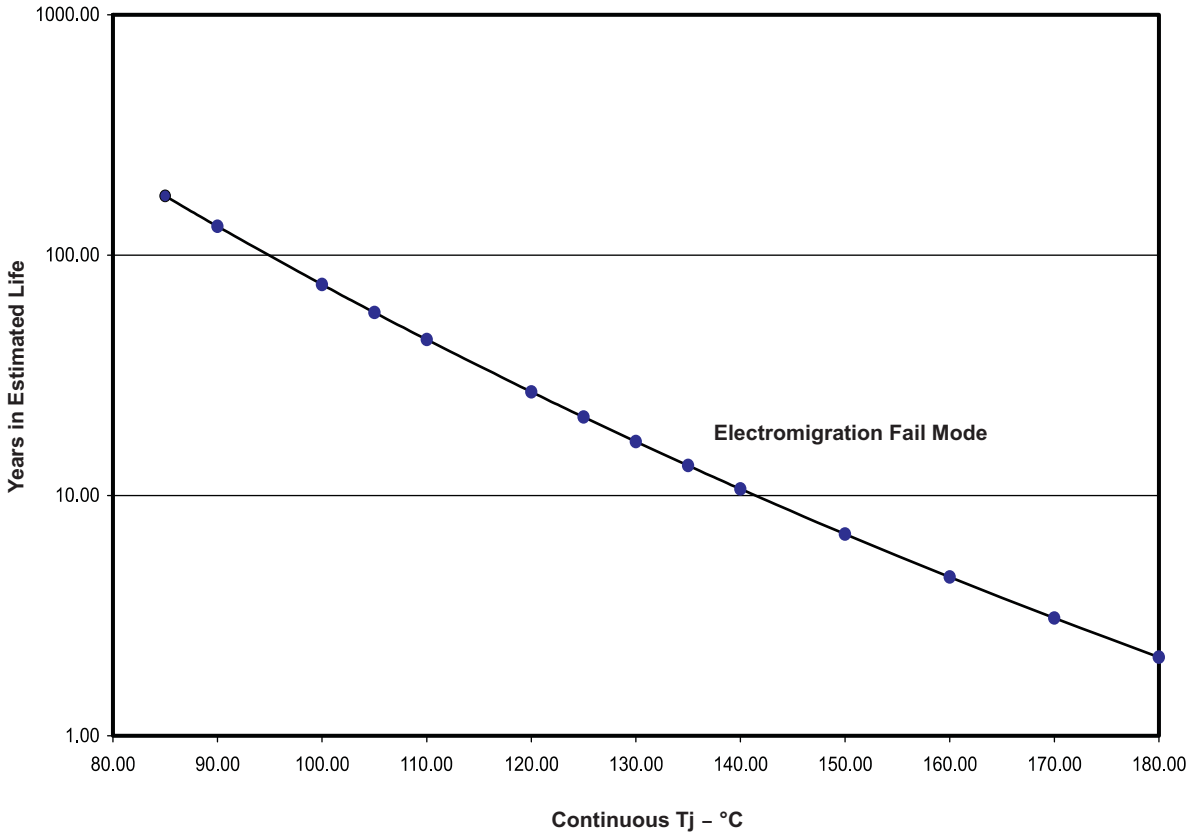


Figure 2. ADS5463 Estimated Life at Elevated Temperature Electromigration Fail Mode

TYPICAL CHARACTERISTICS

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

AC PERFORMANCE vs INPUT AMPLITUDE (100 MHz Input Signal)

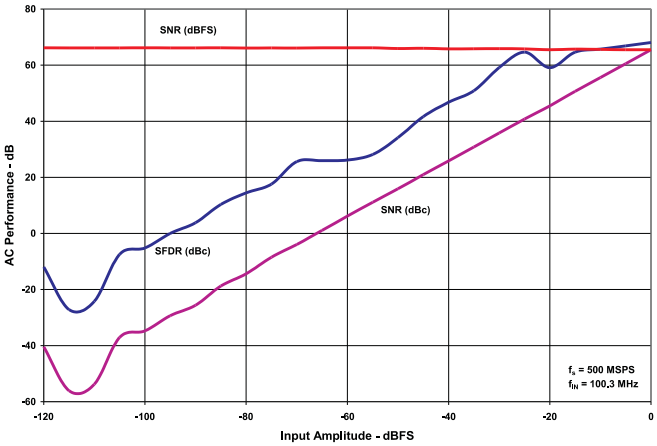


Figure 3.

AC PERFORMANCE vs INPUT AMPLITUDE (300 MHz Input Signal)

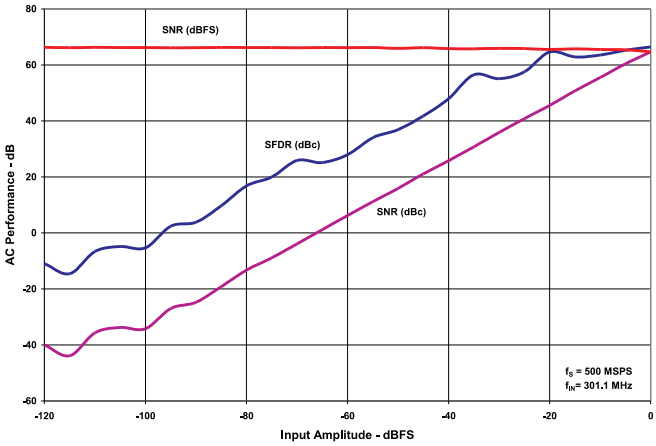


Figure 4.

SFDR vs CLOCK LEVEL

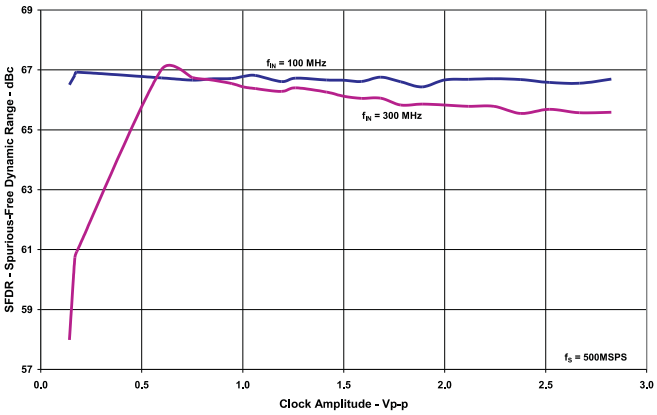


Figure 5.

SNR vs CLOCK LEVEL

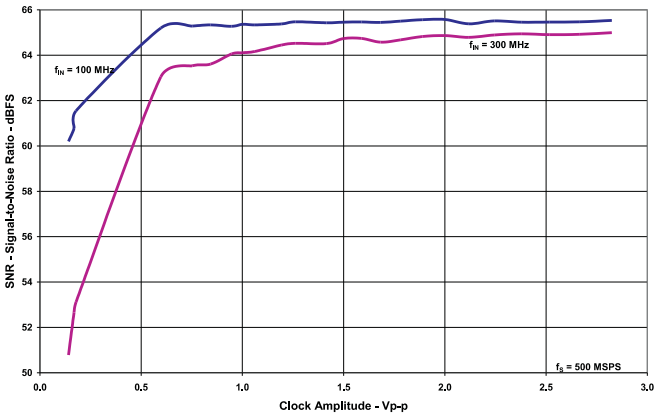


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

SFDR vs AVDD5 ACROSS TEMPERATURE

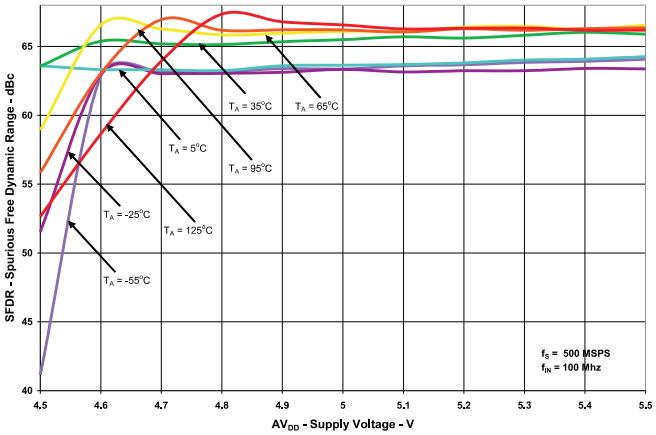


Figure 7.

SNR vs AVDD5 ACROSS TEMPERATURE

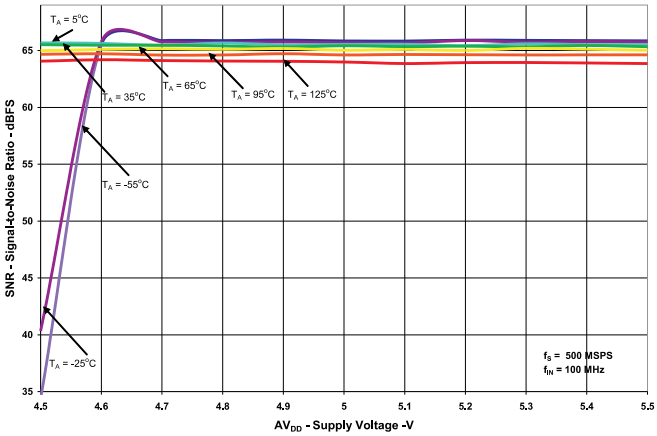


Figure 8.

SFDR vs AVDD3 ACROSS TEMPERATURE

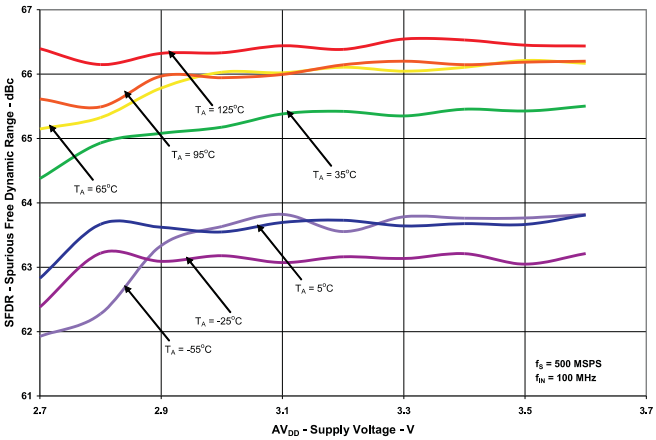


Figure 9.

SNR vs AVDD3 ACROSS TEMPERATURE

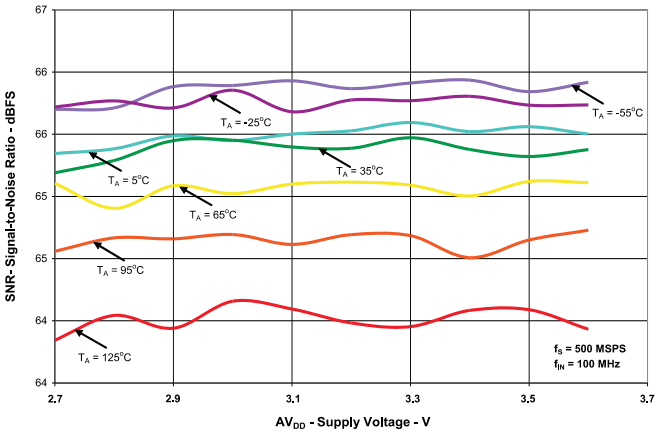


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, (unless otherwise noted)

SFDR vs DVDD3 ACROSS TEMPERATURE

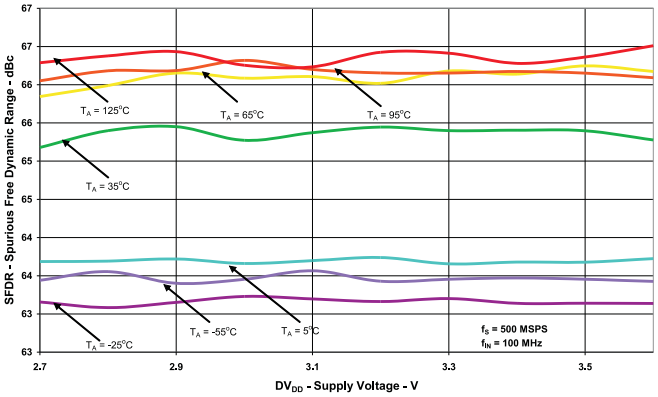


Figure 11.

SNR vs DVDD3 ACROSS TEMPERATURE

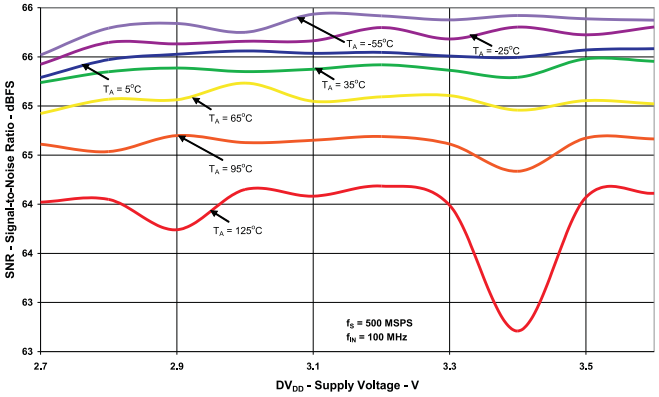


Figure 12.

SFDR vs INPUT FREQUENCY AND SAMPLING FREQUENCY

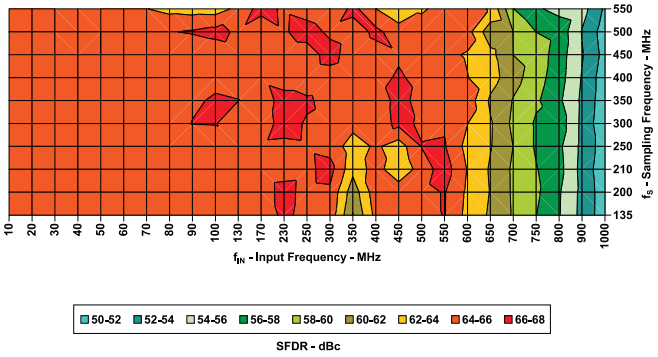


Figure 13.

SNR vs INPUT FREQUENCY AND SAMPLING FREQUENCY

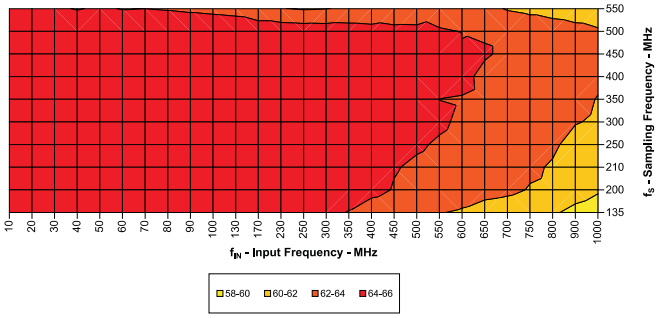


Figure 14.

APPLICATION INFORMATION

Theory of Operation

The ADS5463 is a 12-bit, 500-MSPS, monolithic-pipeline, analog-to-digital converter. Its bipolar analog core operates from 5-V and 3.3-V supplies, while the output uses a 3.3-V supply to provide LVDS-compatible outputs. The conversion process is initiated by the rising edge of the external input clock. The differential input signal is captured by the input track-and-hold (T&H), and the input sample is sequentially converted by a series of lower resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 3.5 clock cycles, after which the output data is available as a 12-bit parallel word, coded in offset binary format.

Input Configuration

The analog input for the ADS5463 consists of an analog pseudodifferential buffer followed by a bipolar transistor track-and-hold. The analog buffer isolates the source driving the input of the ADC from any internal switching. The input common mode is set internally through a 500-Ω resistor connected from 2.4 V to each of the inputs. This results in a differential input impedance of 1 kΩ.

For a full-scale differential input, each of the differential lines of the input signal (pins 17 and 18) swings symmetrically between 2.4 V + 0.55 V and 2.4 V – 0.55 V. This means that each input has a maximum signal swing of 1.1 Vpp for a total differential input signal swing of 2.2 Vpp. The maximum swing is determined by the internal reference voltage generator, eliminating the need for any external circuitry for this purpose.

The ADS5463 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 15 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. In addition, the evaluation module is configured with two back-to-back transformers, which also demonstrate good performance. If voltage gain is required, a step-up transformer can be used.

Besides the transformer configurations, Texas Instruments offers a wide selection of single-ended operational amplifiers that can be selected depending on the application. An RF gain-block amplifier, such as Texas Instruments' THS9001, also can be used for high-input-frequency applications. For large voltage gains at intermediate-frequencies in the 50-MHz – 500-MHz range, the configuration shown in Figure 16 can be used. The component values can be tuned for different intermediate frequencies. The example shown is located on the evaluation module and is tuned for an IF of 170 MHz. More information regarding this configuration can be found in the *ADS5463 EVM User Guide* (SLAU194) and the *THS9001 50 MHz to 350 MHz Cascadeable Amplifier* data sheet (SLOS426).

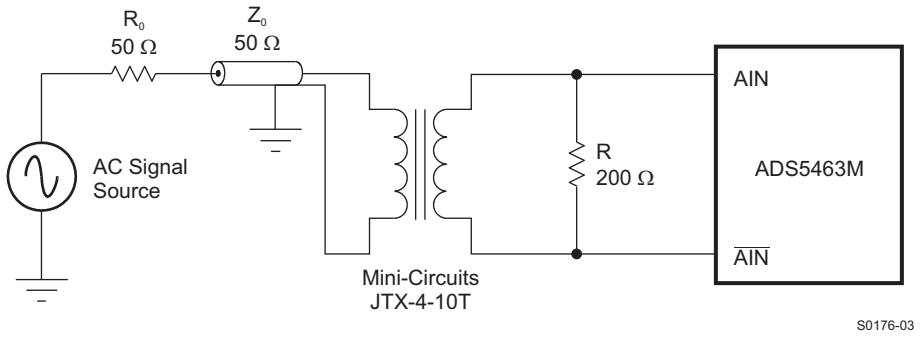


Figure 15. Converting a Single-Ended Input to a Differential Signal Using an RF Transformer

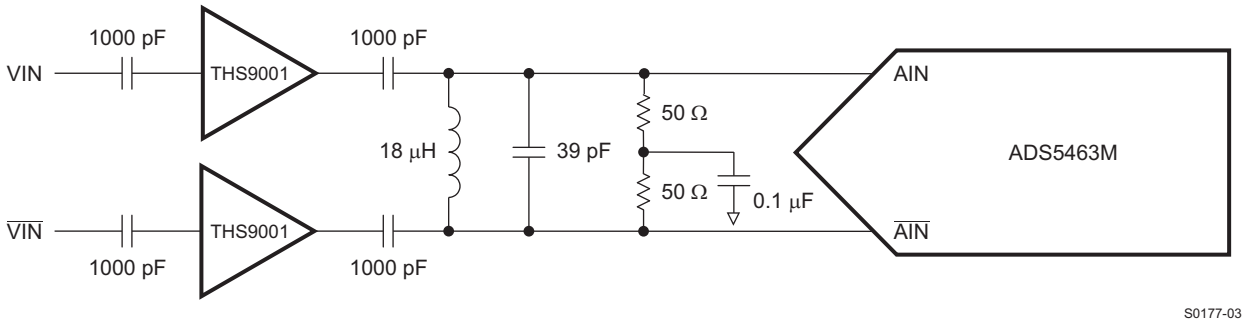


Figure 16. Using the THS9001 IF Amplifier With the ADS5463

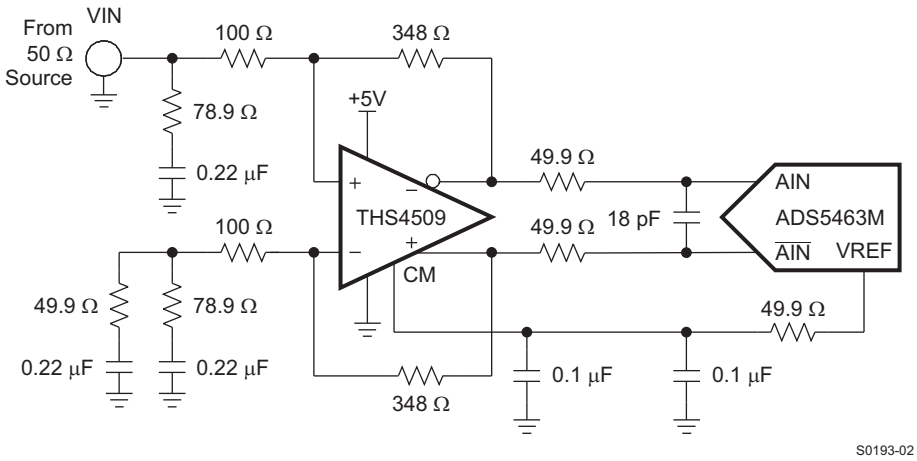


Figure 17. Using the THS4509 With the ADS5463

For applications requiring dc-coupling with the signal source, a differential input/differential output amplifier like the THS4509 (see Figure 17) is a good solution, as it minimizes board space and reduces the number of components.

In this configuration, the THS4509 amplifier circuit provides 10-dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5463. The 50-Ω resistors and 18-pF capacitor between the THS4509 outputs and ADS5463 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 70 MHz (–3 dB). Input termination is accomplished via the 78.9-Ω resistor and 0.22-µF capacitor to ground, in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor are inserted to ground across the 78.9-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. See the THS4509 data sheet for further component values to set proper 50-Ω termination for other common gains. Because the ADS5463 recommended input common-mode voltage is 2.4 V, the THS4509 is operated from a single power supply input with V S+ = 5 V and V S– = 0 V (ground). This maintains maximum headroom on the internal transistors of the THS4509.

Clock Inputs

The ADS5463 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. In low-input-frequency applications, where jitter may not be a big concern, the use of a single-ended clock (see Figure 18) could save some cost and board space without any trade-off in performance. When clocked with this configuration, it is best to connect $\overline{\text{CLK}}$ to ground with a 0.01 µF capacitor, while CLK is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 18.

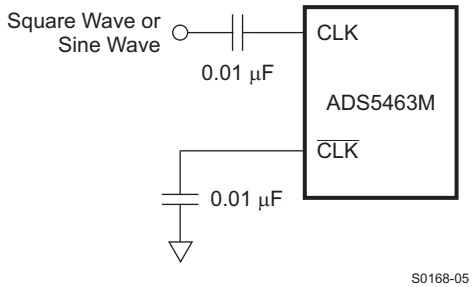


Figure 18. Single-Ended Clock

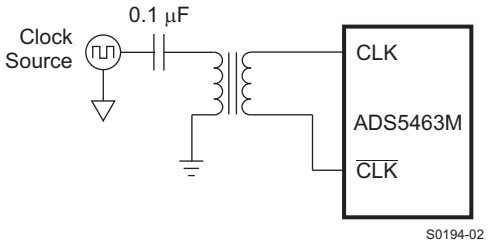


Figure 19. Differential Clock

For jitter-sensitive applications, the use of a differential clock has advantages (as with any other ADC) at the system level. The differential clock allows for common-mode noise rejection at the PCB level. With a differential clock, the signal-to-noise ratio of the ADC is better for high intermediate frequency applications because the board clock jitter is superior.

A differential clock also allows for the use of bigger clock amplitudes without exceeding the absolute maximum ratings. In the case of a sinusoidal clock, this results in higher slew rates and reduces the impact of clock noise on jitter. Figure 19 shows this approach. See *Clocking High Speed Data Converters* (SLYT075) for more details.

The common-mode voltage of the clock inputs is set internally to 2.4 V using internal 1-kΩ resistors. It is recommended to use ac coupling, but if this scheme is not possible due to, for instance, asynchronous clocking, the ADS5463 features good tolerance to clock common-mode variation. Additionally, the internal ADC core uses both edges of the clock for the conversion process. Ideally, a 50% duty-cycle clock signal should be provided.

Digital Outputs

The ADC provides 12 data outputs (D11 to D0, with D11 being the MSB and D0 the LSB), a data-ready signal (DRY), and an overrange indicator (OVR) that equals a logic high when the output reaches the full-scale limits. The output format is offset binary. It is recommended to use the DRY signal to capture the output data of the ADS5463. DRY is source-synchronous to the DATA/OVR bits and operates at the same frequency, creating a half-rate DDR interface that updates data on both the rising and falling edges of DRY. The ADS5463 digital outputs are LVDS-compatible. Due to the high data rates, care should be taken not to overload the digital outputs with too much capacitance, which shortens the data-valid timing window. The values given for timing were obtained with a measured 14-pF parasitic board capacitance to ground on each LVDS line (or 7-pF differential parasitic capacitance).

Power Supplies

The ADS5463 uses three power supplies. For the analog portion of the design, a 5-V and 3.3-V supply (AVDD5 and AVDD3) are used, while the digital portion uses a 3.3-V supply (DVDD3). The use of low-noise power supplies with adequate decoupling is recommended. Linear supplies are preferred to switched supplies; switched supplies tend to generate more noise components that can be coupled to the ADS5463. The user may be able to supply power to the device with a less-than-ideal supply and still achieve good performance. It is not possible to make a single recommendation for every type of supply and level of decoupling for all systems.

The power consumption of the ADS5463 does not change substantially over clock rate or input frequency as a result of the architecture and process.

Because there are two diodes connected in reverse between AVDD3 and DVDD3 internally, a power-up sequence is recommended. When there is a delay in power up between these two supplies, the one that lags could have current sinking through an internal diode before it powers up. The sink current can be large or small depending on the impedance of the external supply and could damage the device or affect the supply source.

The best power up sequence is one of the following options (regardless of when AVDD5 powers up):

- Power up both AVDD3 and DVDD3 at the same time (best scenario), OR
- Keep the voltage difference less than 0.8 V between AVDD3 and DVDD3 during the power up (0.8 V is not a hard specification - a smaller delta between supplies is safer).

If the above sequences are not practical then the sink current from the supply needs to be controlled or protection added externally. The max transient current (on the order of msec) for the DVDD3 or AVDD3 pin is 500 mA to avoid potential damage to the device or reduce its lifetime.

The values for the analog and clock inputs given in the Absolute Maximum Ratings are valid when the supplies are on. When the power supplies are off and the clock or analog inputs are still being actively driven, the input voltage and current need to be limited to avoid device damage. If the ADC supplies are off, max/min continuous dc voltage is ±0.95 V and max dc current is 20 mA for each input pin (clock or analog), relative to ground.

Layout Information

The evaluation board represents a good guideline of how to lay out the board to obtain the maximum performance from the ADS5463. General design rules, such as the use of multilayer boards, single ground plane for ADC ground connections, and local decoupling ceramic chip capacitors, should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. The clock signal traces also should be isolated from other signals, especially in applications where low jitter is required like high IF sampling. Besides performance-oriented rules, care must be taken when considering the heat dissipation of the device.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay

Clock Pulse Duration/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Integral Nonlinearity (INL)

INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best-fit line, measured in units of LSB.

Gain Error

Gain error is the deviation of the ADC actual input full-scale range from its ideal value. Gain error is given as a percentage of the ideal input full-scale range.

Offset Error

Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Temperature Drift

Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by $T_{MIN} – T_{MAX}$.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and in the first five harmonics.

$$SNR = 10\log_{10}\frac{P_S}{P_N} \quad (1)$$

SNR is given either in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10\log_{10}\frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is given either in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to Full Scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Resolution Bandwidth

The highest input frequency where the SNR (dB) is dropped by 3 dB for a full-scale input amplitude.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$THD = 10\log_{10}\frac{P_S}{P_D} \quad (3)$$

THD is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

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in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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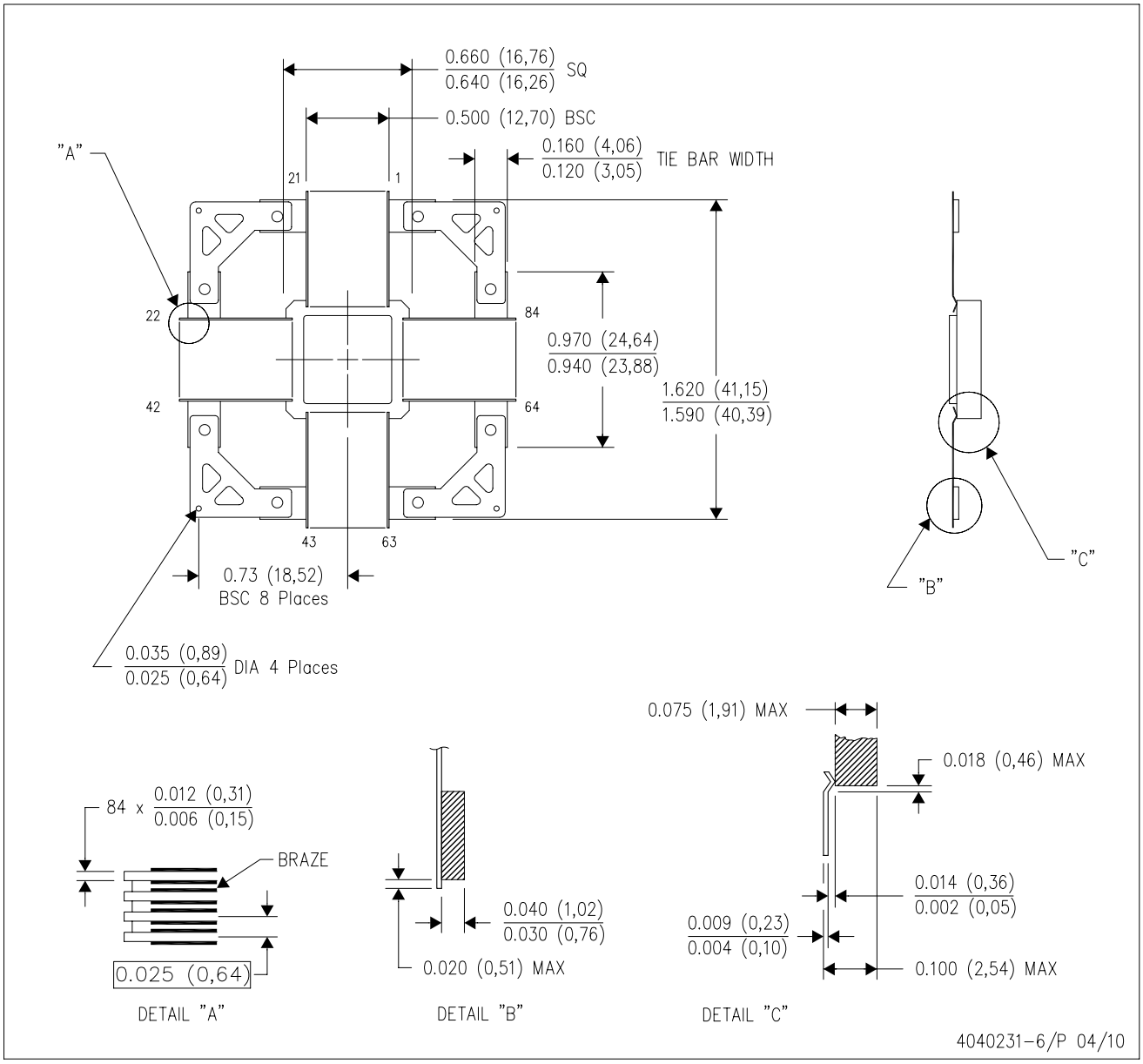
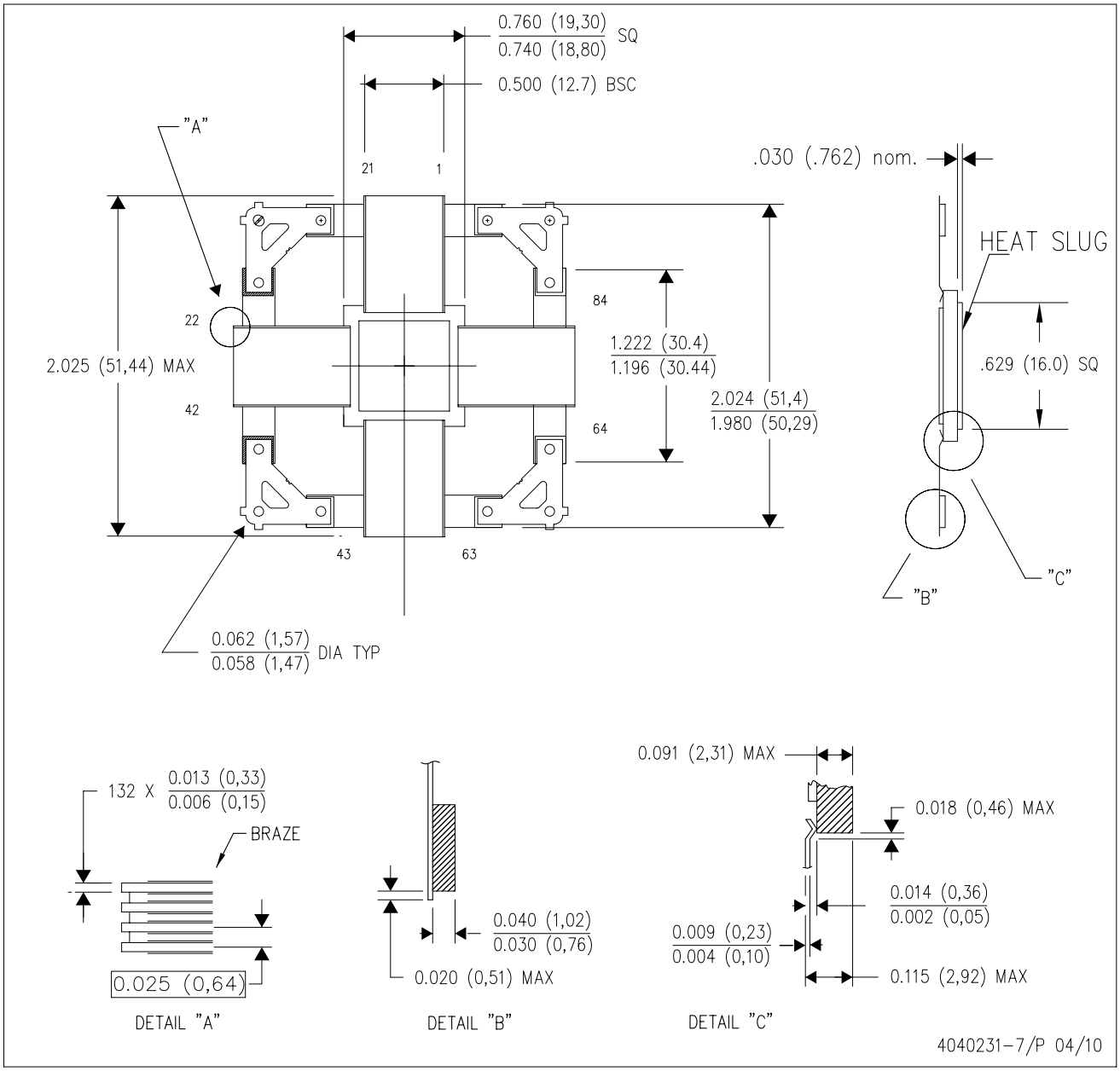


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.

HFG (S–CQFP–F84) CERAMIC QUAD FLATPACK WITH NCTB



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