SUMMARY DATASHEET

NILE

STS-12 ATM/DS3 SONET MAPPER

Features

- Processes valid combinations of SONET/SDH STS-12c/AU-4-4c, STS-3c/AU-4, or STS-1 tributaries within an STS-12/STM-4.
- Terminates and generates SONET/SDH section, line, and path layers.
- Provides DS3 mapping and demapping for 12 STS-1s and supports clear channel DS3.
- Supports ATM payload mapping into STS-12c/AU-4-4c & STS-3c/AU-4, as well as direct ATM or ATM PLCP for DS3 tributaries.
- Supports M23 and C-Bit parity clear channel DS3 mapping, as well as clear channel DS3 transparent passthrough mode.
- Provides a 77.76 MHz 8-bit bus interface on the SONET/SDH side in both the TX and RX directions.
- Provides a 50 MHz 16-bit Utopia Lvl 2 interface on the system side in both the TX and RX directions.
- Programmable Utopia addresses to support multi-PHY operation.
- Generic 8-bit microprocessor interface for configuration and status monitoring.
- Supports IEEE 1149.1 JTAG testing.
- Packaged in a 388 pin BGA.
- Implemented in 3.3V with 5V tolerant I/O.
- Loopback capability for SONET/SDH, DS3 and ATM.

General Description

The S1202 is a highly integrated chip that implements SONET/SDH processing and ATM mapping functions for STS-12/STM-4 data streams. In addition, it supports DS3 tributaries, in an STS-1 SPE, with provisionable support for M23 or C-bit parity OH, as well as clear channel pass-through, direct mapping of ATM cells, or ATM PLCP mapping. The S1202 is SONET and SDH standards compliant with Bellcore GR-253 and ANSI T1.105, and ITU G.707, respectively. The S1202 is also DS3 standards compliant with Bellcore GR-499 and ANSI T1.107-1995 and ATM standards compliant with Utopia Specification Level 2.

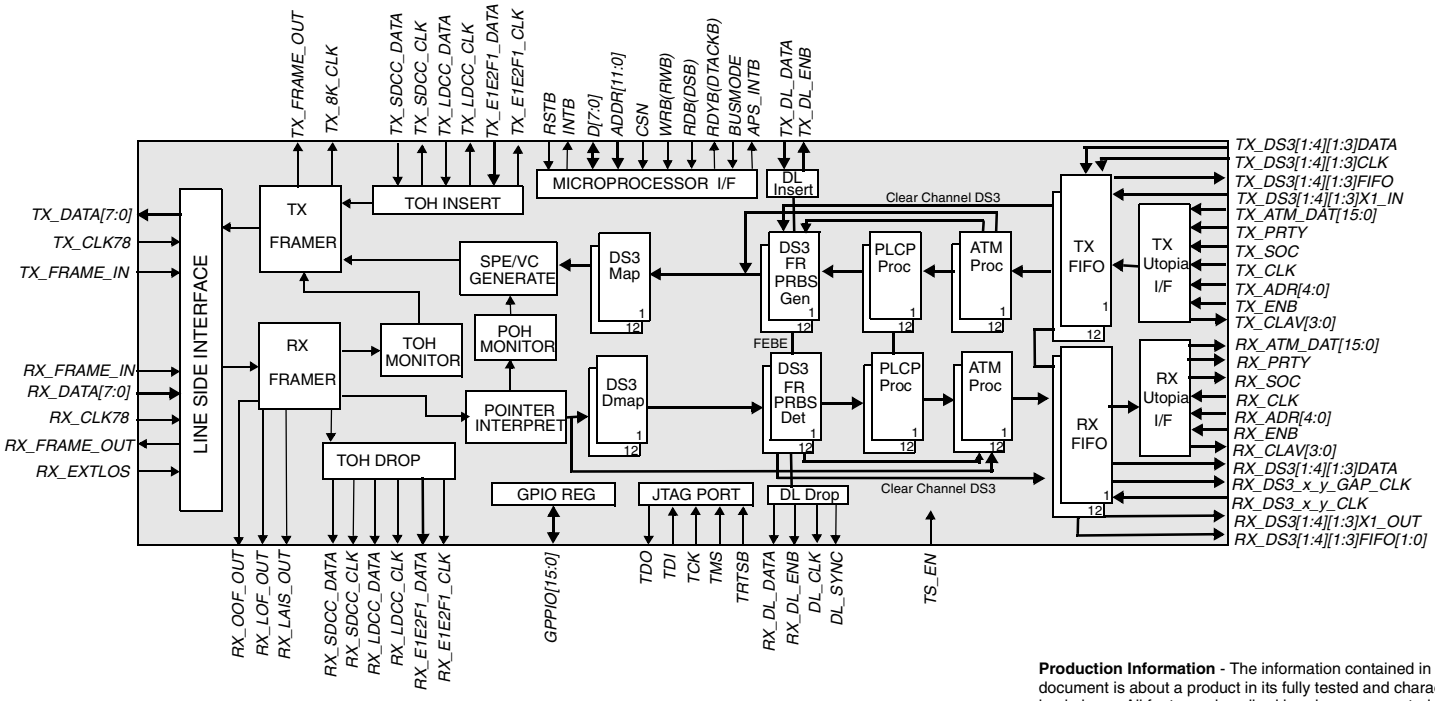
The S1202 supports full-duplex processing of SONET/SDH data streams with section, line, & path overhead processing. The device supports framing, scrambling/descrambling, alarm signal insertion/detection, and bit interleaved parity (B1/B2/B3) processing. Serial interfaces for E1, E2, F1 and Line and Section DCC are also provided.

A general purpose 8-bit microprocessor interface is provided for device initialization, control, and monitoring. The interface supports both Intel and Motorola type microprocessors, and is capable of operating in either an interrupt driven or polled-mode configuration.

Applications

- ATM switches
- Packet over SONET Routers and Switches
- SONET/SDH Add Drop Multiplexers, Terminal Multiplexers and Digital Cross Connects
- Test equipment

S1202 Block Diagram



Overview and Applications

SONET Processing

The S1202 implements SONET/SDH processing and ATM mapping functions for STS-12/STM-4 data streams. It can support any combination of STS-12c, STS-3c, or STS-1 signals within an STS-12, or any combination of AU-4-4c or AU-4 signals within an STM-4. In addition, it can support DS3 tributaries, in SONET, with provisionable support for clear channel passthrough, direct mapping of ATM cells, or ATM PLCP mapping. A TOH/SOH interface provides direct add/drop capability for E1, E2, F1, and both Section and Line DCC channels.

On the transmit side the S1202 generates section, line, & path overhead. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and generates section, line and path Bit Interleaved Parity (B1/B2/B3) for far-end performance monitoring.

On the receive side the S1202 processes section, line, & path overhead. It performs payload framing (A1, A2), descrambling, alarm detection, Bit Interleaved Parity monitoring (B1/B2/B3), and error count accumulation for performance monitoring.

ATM Processing

When configured for ATM cell processing, the S1202 transmit ATM processor will perform all necessary cell encapsulation including HEC generation, cell level scrambling ($X^{43}+1$), and idle cell insertion to adapt the cell rate to the SPE. When receiving data from the line side, it performs cell delineation, Rx header control, descrambling, and receive cell rate adaptation.

DS3 Processing

The S1202 provides DS3 mapper and de-mapper functions.

The DS3 mapper accepts data from an external DS3 input, from looped-back DS3 tributaries, or from internal DS3 frame generators. The internal DS3 frame generators are used for ATM, PLCP, or PRBS data. The S1202 maps the data into STS-1 SONET payloads.

The S1202 DS3 de-mapper support includes the ability to extracts DS3 or ATM data from the SONET signal. DS3 signals can contain ATM, PLCP, or clear channel DS3 data. For ATM or PLCP data, the S1202 frames on the DS3 and extracts these signals from the DS3 payload. For clear channel DS3 data, the S1202 generates RX serial (NRZ) data signals smoothed to match a DS3 clock input that is provided to the device, as well as a FIFO Fill Indication, provided for phase lock loop adjustment. The S1202 also provides full DS3 framing, monitoring, and extraction for full DS3 support.

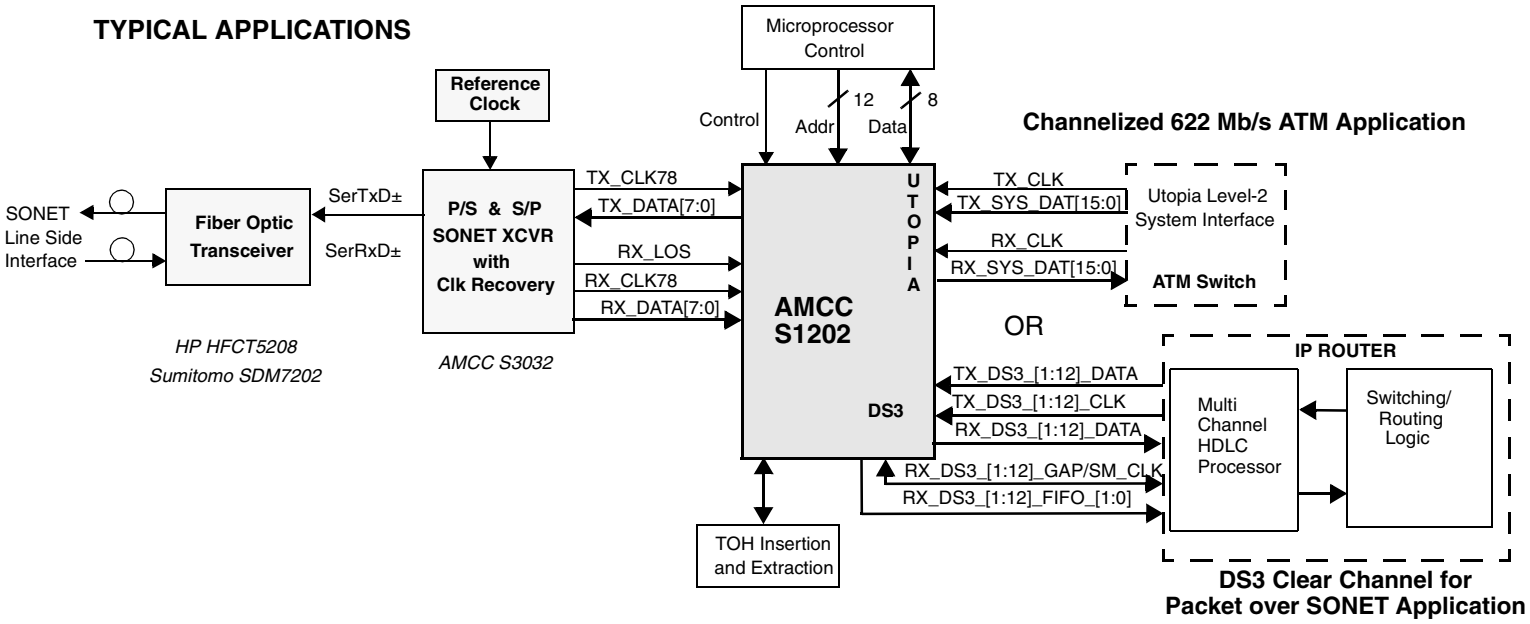
Line-side Interface

On the line-side, the S1202 supports an 8-bit parallel interface which operates at 77.76 MHz. The device is typically connected to a parallel-to-serial converter, which is in turn connected to an electrical-to-optical converter for interfacing to the fiber optic interface. (See figure below.)

System Interface

The S1202 supports a UTOPIA Level 2 interface, operating at 50 Mb/s, for providing ATM cell transfers to/from the system interface. The S1202 also supports up to 12 DS3 tributaries. For clear channel DS3 data, the S1202 generates RX serial (NRZ) data signals smoothed to match a DS3 clock input that is provided to the device, as well as a FIFO Fill Indication, provided for phase lock loop adjustment.

TYPICAL APPLICATIONS



AMCC

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