PZT751T1G

PNP Silicon Planar Epitaxial Transistor

This PNP Silicon Epitaxial transistor is designed for use in industrial and consumer applications. The device is housed in the SOT−223 package which is designed for medium power surface mount applications.

Features

- High Current: 2.0 A
- The SOT−223 Package can be soldered using wave or reflow.
- SOT−223 package ensures level mounting, resulting in improved thermal conduction, and allows visual inspection of soldered joints. The formed leads absorb thermal stress during soldering, eliminating the possibility of damage to the die
- NPN Complement is PZT651T1
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Base Voltage	V_{CBO}	80	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C (Note 1) Derate above 25°C	P_D	 0.8 6.4	W mW/°C
Storage Temperature Range	T_{stg}	−65 to 150	°C
Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance from Junction−to−Ambient in Free Air	$R_{\theta JA}$	156	°C/W
Maximum Temperature for Soldering Purposes Time in Solder Bath	T_L	260 10	°C Sec

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Device mounted on a FR−4 glass epoxy printed circuit board using minimum recommended footprint.

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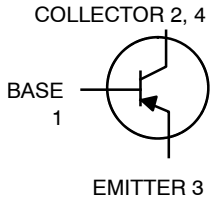
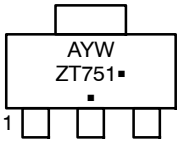
SOT−223 PACKAGE HIGH CURRENT PNP SILICON TRANSISTOR SURFACE MOUNT



MARKING DIAGRAM

SOT−223
CASE 318E
STYLE 1



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
PZT751T1G	SOT−223 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	60	−	Vdc
Collector−Emitter Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	80	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	−	Vdc
Base−Emitter Cutoff Current (V_{EB} = 4.0 Vdc)	I_{EBO}	−	0.1	μAdc
Collector−Base Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	−	100	nAdc
ON CHARACTERISTICS (Note 2)				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 2.0 Vdc) (I_C = 500 mAdc, V_{CE} = 2.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	 75 75 75 40	 − − − −	−
Collector−Emitter Saturation Voltages (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	 − −	 0.5 0.3	Vdc
Base−Emitter Voltages (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	−	1.0	Vdc
Base−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{BE(sat)}$	−	1.2	Vdc
Current−Gain−Bandwidth (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	75	−	MHz

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

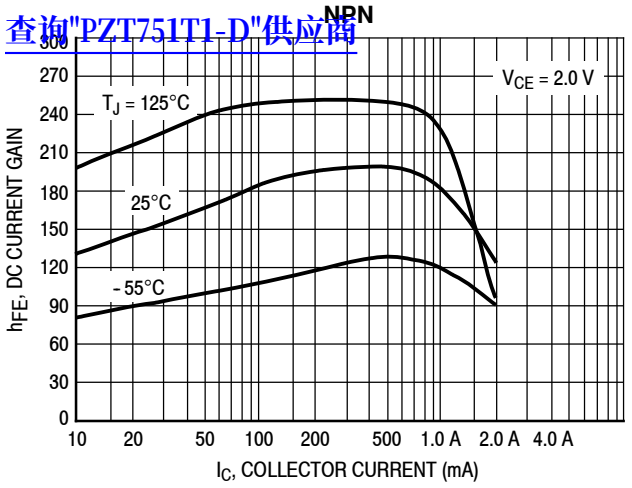


Figure 1. Typical DC Current Gain

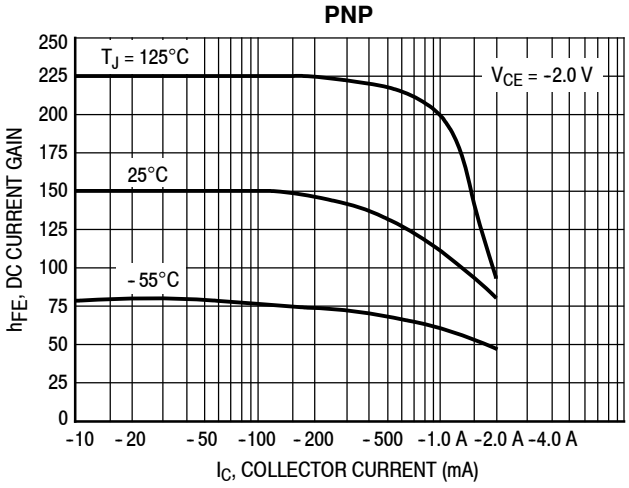


Figure 2. Typical DC Current Gain

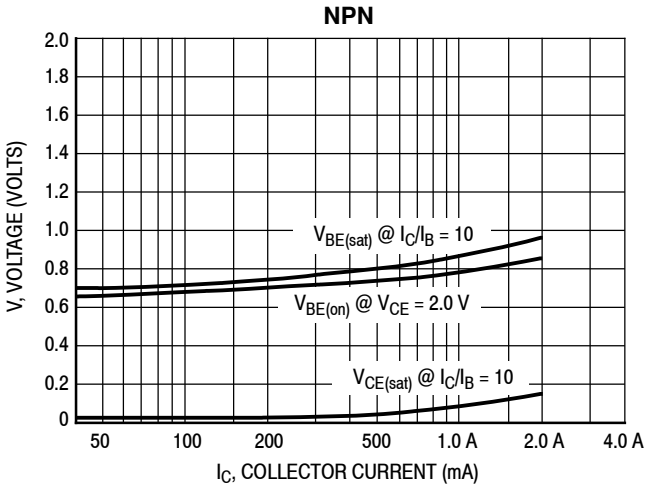


Figure 3. On Voltages

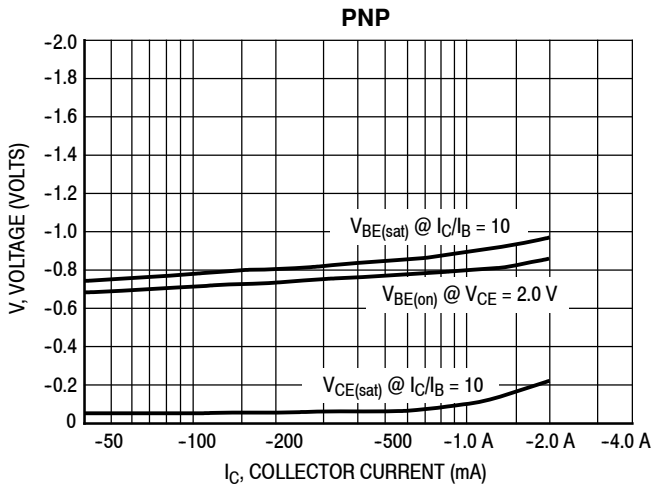


Figure 4. On Voltages

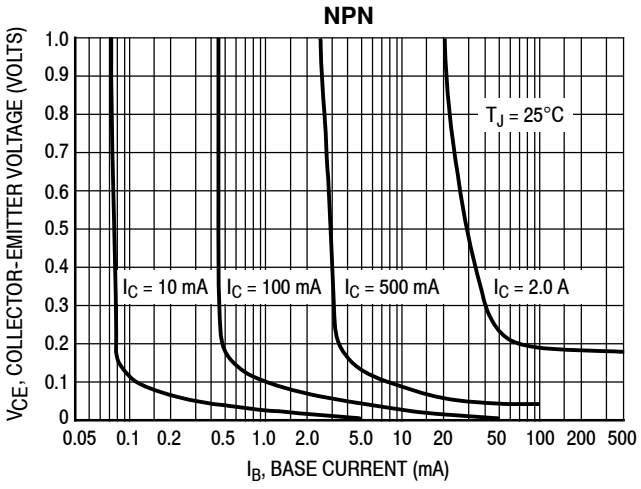


Figure 5. Collector Saturation Region

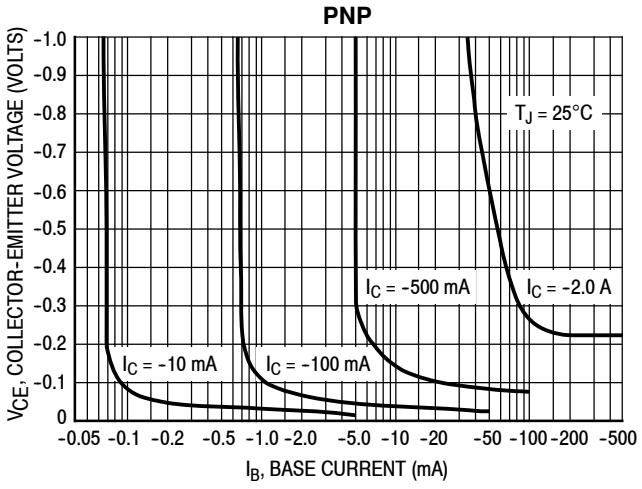
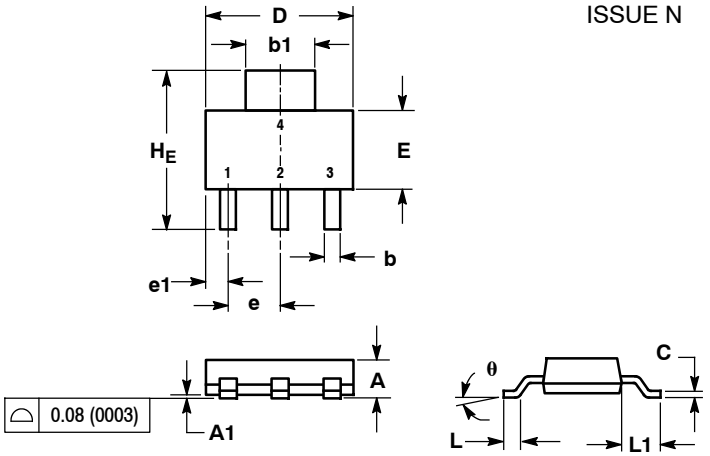


Figure 6. Collector Saturation Region

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE N

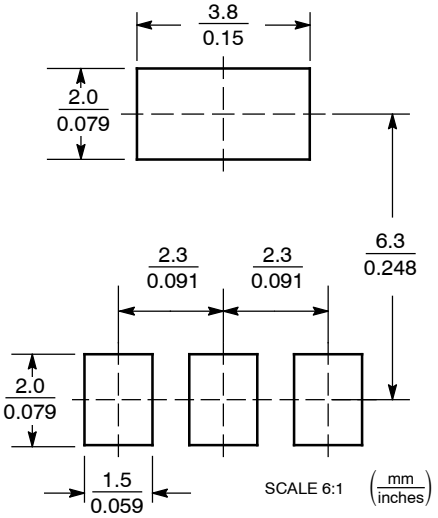


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	-	10°	0°	-	10°

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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