HD74LV165A

Parallel-Load 8-bit Shift Register

HITACHI

ADE-205-267 (Z)
1st Edition
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Description

The HD74LV165A is 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the Shift/Load input. Also included is a gated clock input and a complementary output from the eighth bit.
Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a clock inhibit function. Holding either of the clock inputs high inhibits clocking, and high enables the other clock input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the Shift/Load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.
Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- V_{CC} = 2.0 V to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.3 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Output current ±6 mA (@V_{CC} = 3.0 V to 3.6 V), ±12 mA (@V_{CC} = 4.5 V to 5.5 V)

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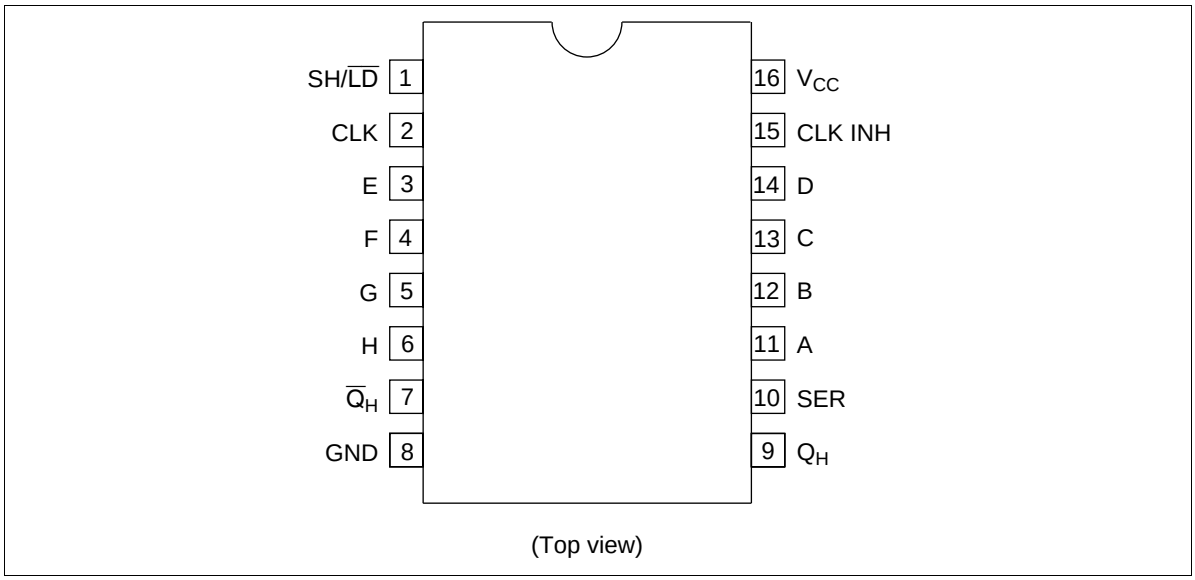
Function Table

Inputs					Internal Outputs		Output
SH/$\overline{LD}$	**CLK INH**	**CLK**	**SER**	**A ... H**	**QA**	**QB**	**QH**
L	X	X	X	a ... h	a	b	h
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	X	H	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	L	H	X	H	Q_{An}	Q_{Gn}
H	↑	L	L	X	L	Q_{An}	Q_{Gn}

Note: H: High level
L: Low level
↑: Low to high transition
X: Immaterial
a ... h: Parallel data
Q_{A0} ... Q_{H0}: Outputs remain unchanged.
Q_{An} ... Q_{Gn}: Data shifted from the previous stage on a positive edge at the clock input.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range*[1]	V_I	–0.5 to 7.0	V	
Output voltage range*[1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output: H or L
		–0.5 to 7.0		V_{CC}: OFF
Input clamp current	I_{IK}	–20	mA	V_I < 0
Output clamp current	I_{OK}	±50	mA	V_O < 0 or V_O > V_{CC}
Continuous output current	I_O	±25	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at Ta = 25°C (in still air)*[3]	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

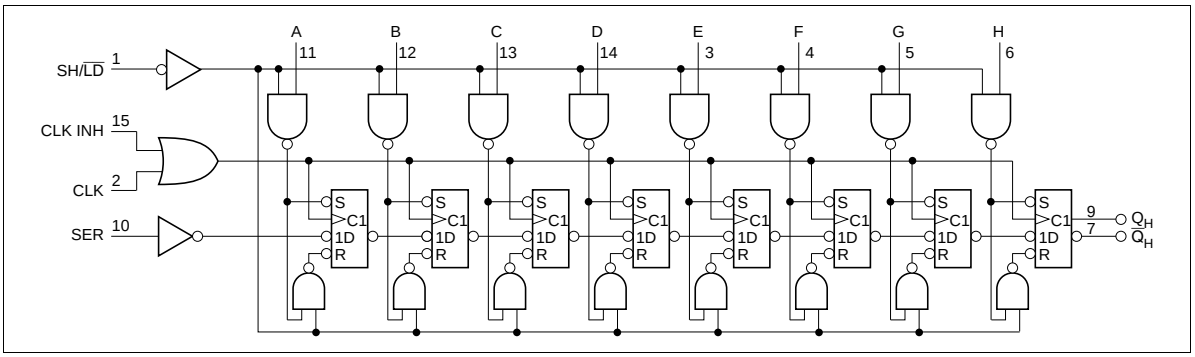
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

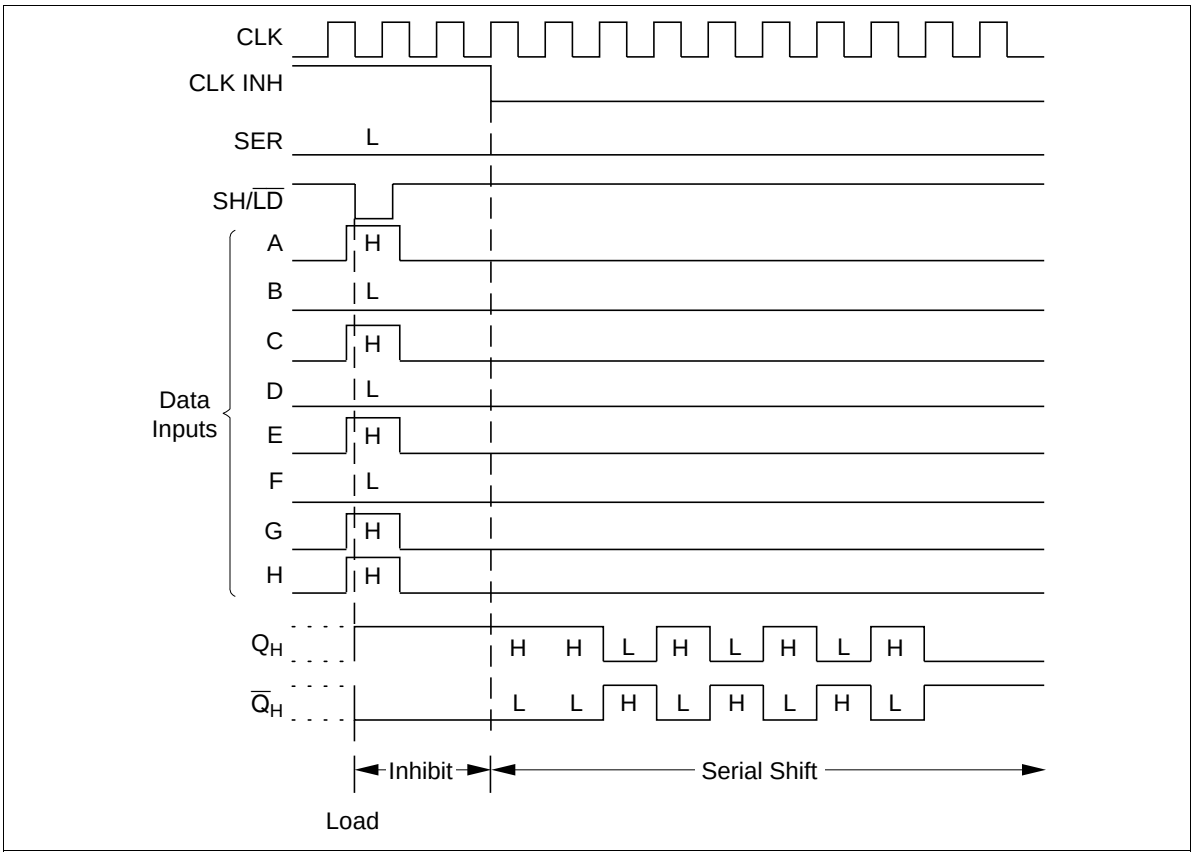
Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
Output current	I_{OH}	—	–50	µA	V_{CC} = 2.0 V
		—	–2	mA	V_{CC} = 2.3 to 2.7 V
		—	–6		V_{CC} = 3.0 to 3.6 V
		—	–12		V_{CC} = 4.5 to 5.5 V
	I_{OL}	—	50	µA	V_{CC} = 2.0 V
		—	2	mA	V_{CC} = 2.3 to 2.7 V
		—	6		V_{CC} = 3.0 to 3.6 V
		—	12		V_{CC} = 4.5 to 5.5 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	V_{CC} = 2.3 to 2.7 V
		0	100		V_{CC} = 3.0 to 3.6 V
		0	20		V_{CC} = 4.5 to 5.5 V
Operating free-air temperature	Ta	–40	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Timing Diagram



DC Electrical Characteristics

- **Ta = –40 to 85°C**

Item	Symbol	V_{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	Min to Max	V_{CC} – 0.1	—	—	V	I_{OL} = –50 µA
		2.3	2.0	—	—		I_{OL} = –2 mA
		3.0	2.48	—	—		I_{OL} = –6 mA
		4.5	3.8	—	—		I_{OL} = –12 mA
	V_{OL}	Min to Max	—	—	0.1		I_{OL} = 50 µA
		2.3	—	—	0.4		I_{OL} = 2 mA
		3.0	—	—	0.44		I_{OL} = 6 mA
		4.5	—	—	0.55		I_{OL} = 12 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	µA	V_I = 5.5 V or GND
Quiescent supply current	I_{CC}	5.5	—	—	20	µA	$V_I = V_{CC}$ or GND, I_O = 0
Output leakage current	I_{OFF}	0	—	—	5	µA	V_I or V_O = 0 V to 5.5 V
Input capacitance	C_{IN}	3.3	—	1.7	—	pF	$V_I = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- V_{CC} = 2.5 ± 0.2 V

		Ta = 25°C			Ta = –40 to 85°C					
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	**FROM (Input)**	**TO (Output)**
Maximum clock frequency	fmax	50	80	—	45	—	MHz	C_L = 15 pF		
		40	65	—	35	—		C_L = 50 pF		
Propa-gation delay time	t_{PLH}/t_{PHL}	—	13.1	21.5	1.0	23.5	ns	C_L = 15 pF	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$
		—	16.1	25.1	1.0	28.0		C_L = 50 pF		
		—	12.2	19.8	1.0	22.0		C_L = 15 pF	CLK	
		—	15.3	23.3	1.0	26.0		C_L = 50 pF		
		—	12.9	21.7	1.0	24.0		C_L = 15 pF	H	
		—	15.9	25.3	1.0	28.0		C_L = 50 pF		
Setup time	t_{su}	7.0	—	—	7.0	—	ns		CLK INH before CLK ↑	
		11.5	—	—	12.0	—			data before SH/$\overline{LD}$ ↑	
		7.0	—	—	8.5	—	ns		SH/$\overline{LD}$ high before CLK ↑	
		8.5	—	—	9.5	—			SER before CLK ↑	
Hold time	t_h	0.0	—	—	0.5	—	ns		PAR data after SH/$\overline{LD}$ ↑	
		–1.0	—	—	0.0	—			SER data after CLK ↑	
		0.0	—	—	0.0	—			SH/$\overline{LD}$ high atfer CLK ↑	
Pulse width	t_w	11.0	—	—	13.0	—	ns		SH/$\overline{LD}$ low	
		8.5	—	—	9.0	—			CLK H or L	

Switching Characteristics (cont)

- V_{CC} = 3.3 ± 0.3 V

		Ta = 25°C			Ta = –40 to 85°C					
Item	Symbol	Min	Typ	Max	Min	Max	Unit	Test Conditions	FROM (Input)	TO (Output)
Maximum clock frequency	fmax	65	115	—	55	—	MHz	C_L = 15 pF		
		60	90	—	50	—		C_L = 50 pF		
Propa-gation delay time	t_{PLH}/t_{PHL}	—	9.1	15.8	1.0	18.5	ns	C_L = 15 pF	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$
		—	11.3	19.3	1.0	22.0		C_L = 50 pF		
		—	8.6	15.4	1.0	18.0		C_L = 15 pF	CLK	
		—	10.9	18.9	1.0	21.5		C_L = 50 pF		
		—	8.9	14.1	1.0	16.5		C_L = 15 pF	H	
		—	11.1	17.6	1.0	20.0		C_L = 50 pF		
Setup time	t_{su}	5.0	—	—	5.0	—	ns		CLK INH before CLK ↑	
		7.5	—	—	8.5	—			data before SH/$\overline{LD}$ ↑	
		5.0	—	—	6.0	—	ns		SH/$\overline{LD}$ high before CLK ↑	
		5.0	—	—	6.0	—			SER before CLK ↑	
Hold time	t_h	0.5	—	—	0.5	—	ns		PAR data after SH/$\overline{LD}$ ↑	
		0.0	—	—	0.0	—			SER data after CLK ↑	
		0.0	—	—	0.0	—			SH/$\overline{LD}$ high atfer CLK ↑	
Pulse width	t_w	7.5	—	—	9.0	—	ns		SH/$\overline{LD}$ low	
		6.0	—	—	7.0	—			CLK H or L	

Switching Characteristics (cont)

- **V_{CC} = 5.0 ± 0.5 V**

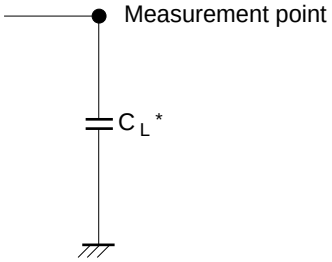
		Ta = 25°C			Ta = –40 to 85°C					
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	**FROM (Input)**	**TO (Output)**
Maximum clock frequency	fmax	110	165	—	90	—	MHz	C_L = 15 pF		
		95	125	—	85	—		C_L = 50 pF		
Propa-gation delay time	t_{PLH}/t_{PHL}	—	6.0	9.9	1.0	11.5	ns	C_L = 15 pF	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$
		—	7.7	11.9	1.0	13.5		C_L = 50 pF		
		—	6.0	9.9	1.0	11.5		C_L = 15 pF	CLK	
		—	7.7	11.9	1.0	13.5		C_L = 50 pF		
		—	6.0	9.0	1.0	10.5		C_L = 15 pF	H	
		—	7.6	11.0	1.0	12.5		C_L = 50 pF		
Setup time	t_{su}	3.5	—	—	3.5	—	ns		CLK INH before CLK ↑	
		5.0	—	—	5.0	—			data before SH/$\overline{LD}$ ↑	
		4.0	—	—	4.0	—	ns		SH/$\overline{LD}$ high before CLK ↑	
		4.0	—	—	4.0	—			SER before CLK ↑	
Hold time	t_h	1.0	—	—	1.0	—	ns		PAR data after SH/$\overline{LD}$ ↑	
		0.5	—	—	0.5	—			SER data after CLK ↑	
		0.5	—	—	0.5	—			SH/$\overline{LD}$ high atfer CLK ↑	
Pulse width	t_w	5.0	—	—	6.0	—	ns		SH/$\overline{LD}$ low	
		4.0	—	—	4.0	—			CLK H or L	

Operating Characteristics

- C_L = 50 pF

			Ta = 25°C				
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Power dissipation capacitance	C_{PD}	3.3	—	36.1	—	pF	f = 10 MHz
		5.0	—	37.5	—		

Test Circuit

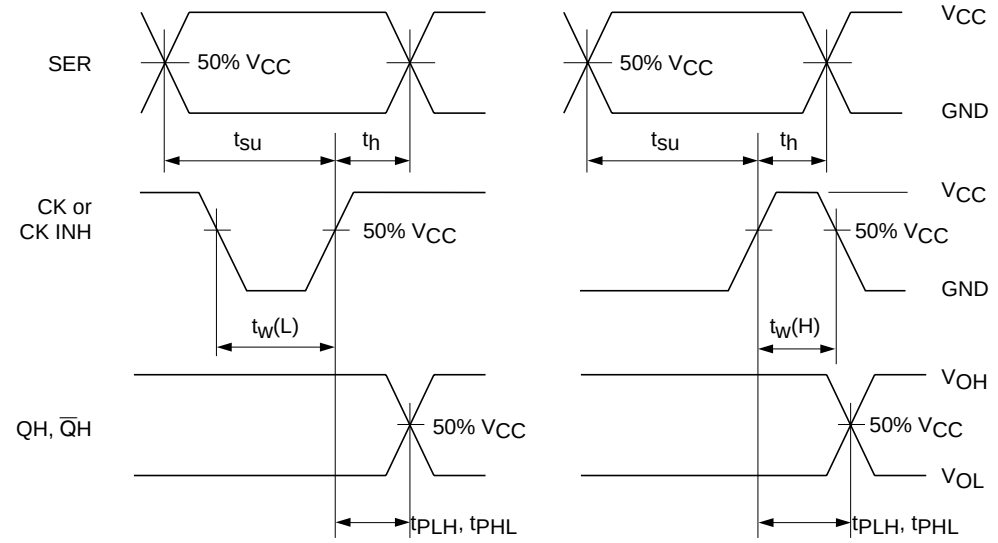


Note: C_L includes the probe and jig capacitance.

Waveform

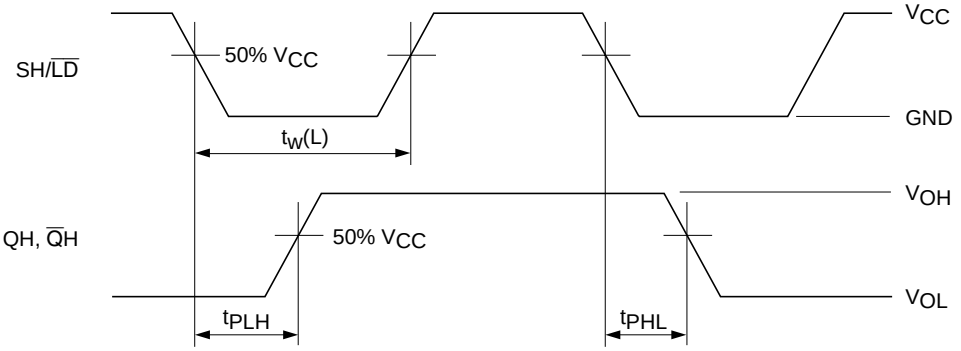
Waveform – 1

Sereial mode



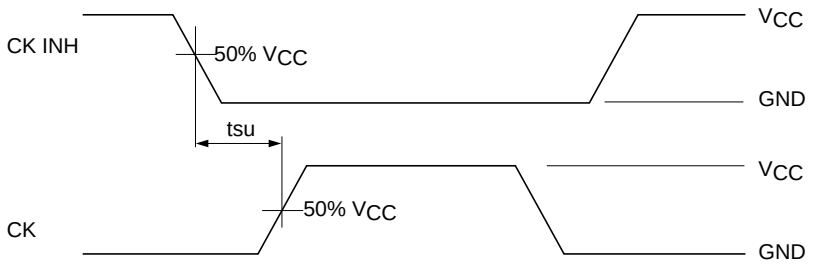
Waveform – 2

Parallel mode



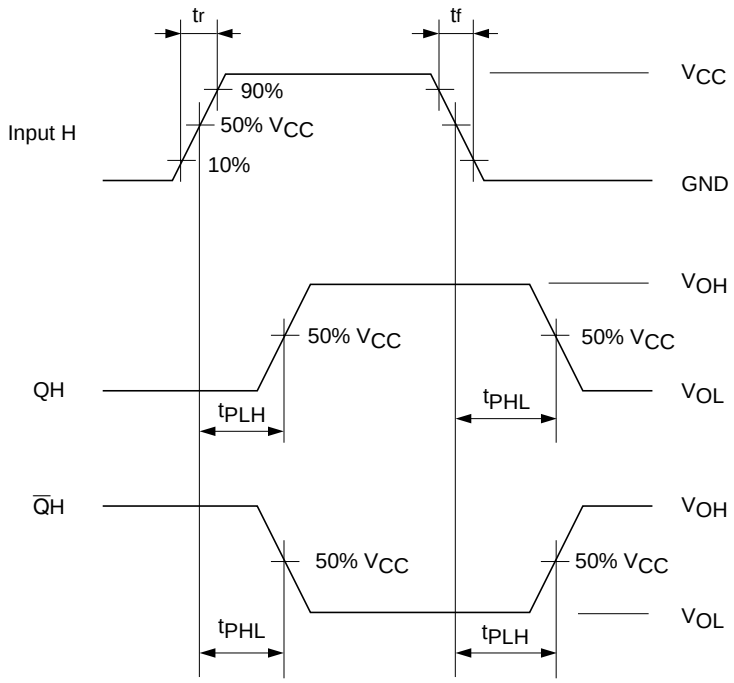
Waveform – 3

Sereial mode



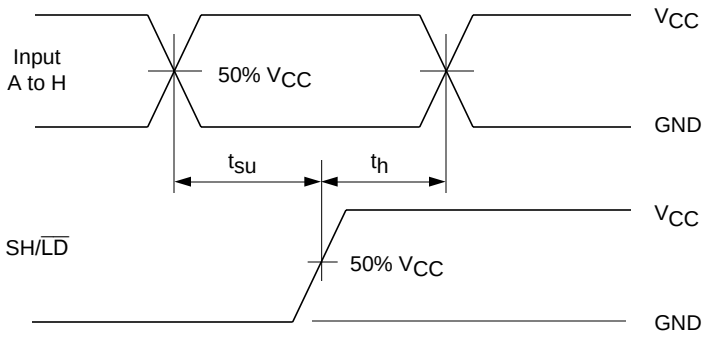
Waveform – 4

Parallel mode



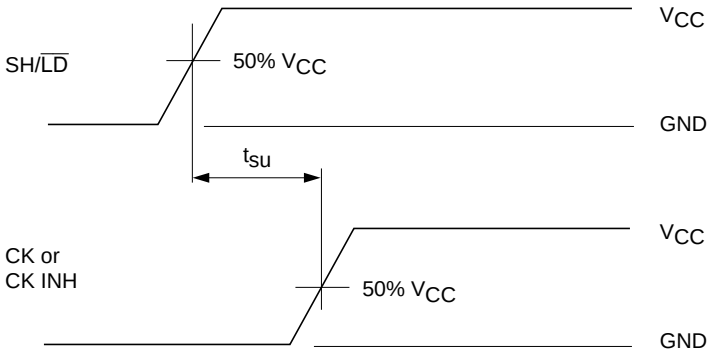
Waveform – 5

Parallel mode



Waveform – 6

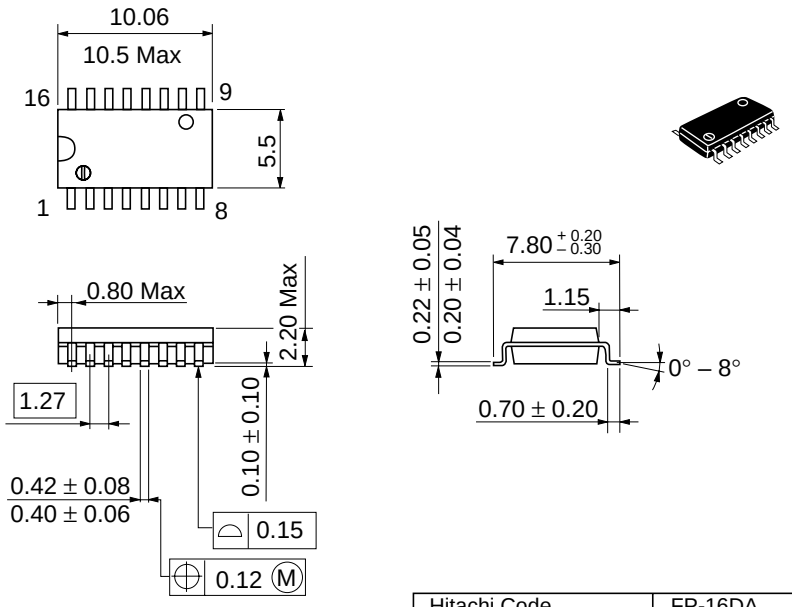
sereial mode



Notes: 1. Input waveform: PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns

2. The output are measured one at a time with one transition per measurement.

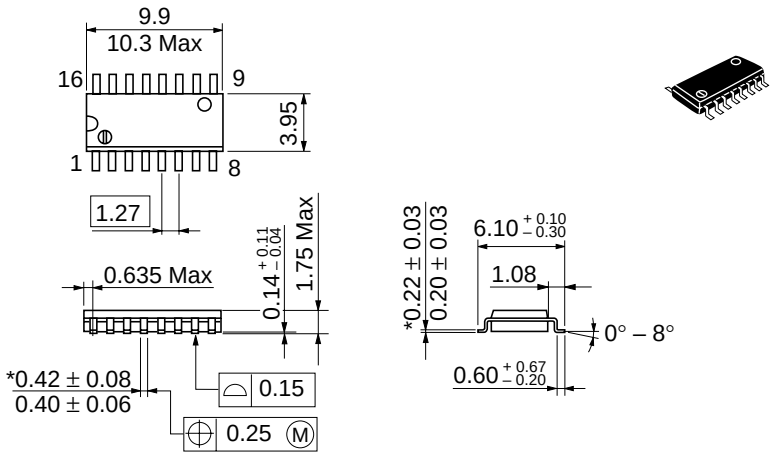
Package Dimensions



Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

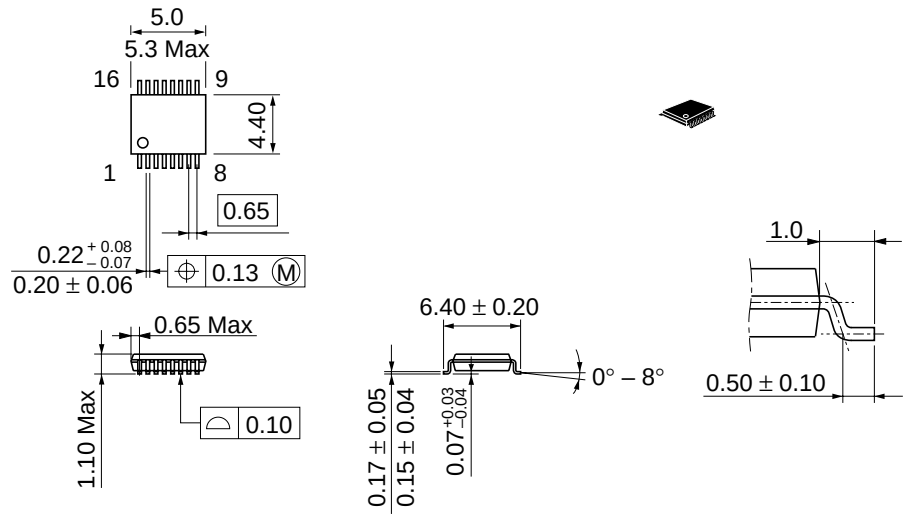
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

HD74LV165A



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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