Ordering number : ENA0816

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA6565VR — Five-Channel CD Actuator Driver (BTL: 4 channels, H bridge: 1 channel)

Overview

The LA6565VR is a four-channel BTL plus one-channel H bridge actuator driver developed for use in CD and DVD drives. The BTL driver channels 1 and 2 include built-in operational amplifiers allowing the LA6565VR to support a wide range of applications.

Functions and Features

- Five power amplifier channels on a single chip (Bridge connection (BTL): 4 channels, H bridge: 1 channel)
- I_O max: 1A
- Built-in level shifters (except for the H bridge channel)
- Muting circuits (output on/off, two systems)
  (The muting circuits operate for the BTL amplifiers. They do not apply to the H bridge or regulator circuits.)
- Built-in regulator (Uses an external PNP transistor and is set with an external resistor.)
- Output voltage setting function (loading driver)
- Built-in independent operational amplifiers
- Thermal shutdown circuit

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Allowable power dissipation	Pd max	Independent IC	0.55	W
		Mounted on a specified board	1.70	W
Maximum output current	I_O max	For each of the channel 1 to 4 and H bridge outputs	1	A
Maximum input voltage	VINB		13	V
MUTE pin voltage	VMUTE		13	V
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a specified board: 76.1mm×114.3mm×1.6mm glass epoxy

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.6 to 13	V

Electrical Characteristics at Ta = 25°C, VCCS = VCCP1 = VCCP2 = 8V, VREF = 2.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Overall]						
Quiescent current when on	I_{CC}-ON	BTL amplifier output on, loading block off *1		30	50	mA
Quiescent current when off	I_{CC}-OFF	All outputs off *1		10	15	mA
Thermal shutdown circuit operating temperature	TSD	*7	150	175	200	°C
[VREF Amplifier]						
VREF amplifier offset voltage	VREF- OFFSET		-10		10	mV
VREF input voltage range	VREF-IN		1		V_{CC}-1.5	V
VREF-OUT output current	I-VREF-OUT			1		mA
[Operational Amplifier] (Independent)						
Input voltage range	V_{IN} (OP)		0		V_{CC}-1.5	V
Output current (sink)	SINK (OP)		2			mA
Output current (source)	SOURCE (OP)		300	500		µA
Output offset voltage	VOFF (OP)		-10		10	mV
Residual current (sink)	VCE-SINK (OP)	I_O (sink side) = 1mA			0.6	V
[BTL Amplifier Block] (Channels 1 to 4)						
Output offset voltage	VOFF	The voltage difference between each channel outputs *2, *3	-50		50	mV
Input voltage range	V_{IN}	Input voltage range of the input operational amplifiers	0		V_{CC}-1.5	V
Output voltage	V_O	I_O = 0.5A, the voltage between V_O+ and V_O- in each channel	5.7	6.2		V
Closed circuit voltage gain	VG	The gain from the input to the output with the input amplifier set to 0dB *2, *3	7.2	8	9	times
Slew rate	SR	For the independent amplifier. Times 2 when between outputs *7		0.5		V/µs
Muting on voltage	VMUTE-ON	The output on voltage, for each mute function *4	2.5			V
Muting off voltage	VMUTE-OFF	The output off voltage, for each mute function *4			0.5	V
[Input Amplifier Block] (Channels 1 and 2)						
Input voltage range	V_{IN}-OP		0		V_{CC}-1.5	V
Output current (sink)	SINK-OP		2			mA
Output current (source)	SOURCE-OP	*5	300	500		µA
Output offset voltage	VOFF-OP		-10		10	mV
[Loading Block] (Channel 5, H bridge circuit)						
Output voltage	V_O-LOAD	For forward/reverse operation, I_O = 0.5A, VCONT = V_{CC}*	5.7	6.5		V
Braking output saturation voltage	V_{CE}-BREAK	The output voltage during braking *6			0.3	V
Low-level input voltage	V_{IN}-L				1	V
High-level input voltage	V_{IN}-H		2			V

*1: The total current dissipation for VCCP1, VCCP2, and VCCS with no load.

*2: The input amplifier is a buffer amplifier.

*3: The voltage difference between the two sides of the load (12Ω).

*4: When the MUTE pin is high, the output will be on, and when low, the output will be off (high-impedance state).

*5: The input operational amplifier source is constant current. Since the 11kΩ resistor between this and the next stage functions as the load, the input operational amplifier gain must be set carefully.

*6: The braking operation is a short (to ground) braking operation. The sink side output is on at this time.

*7: Design guarantee.

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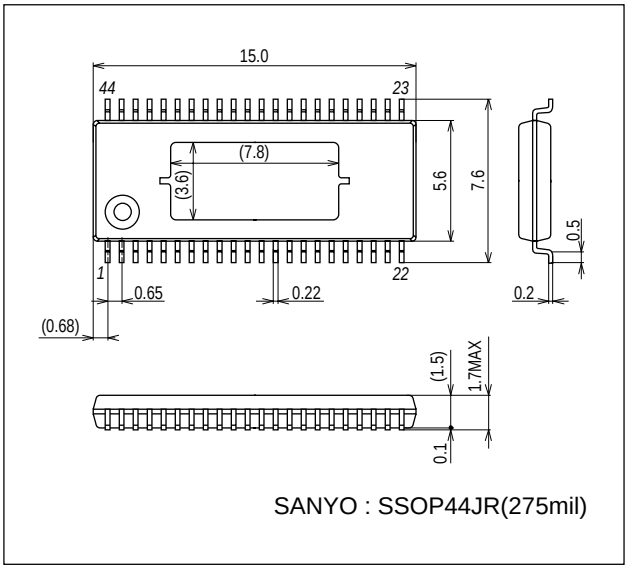
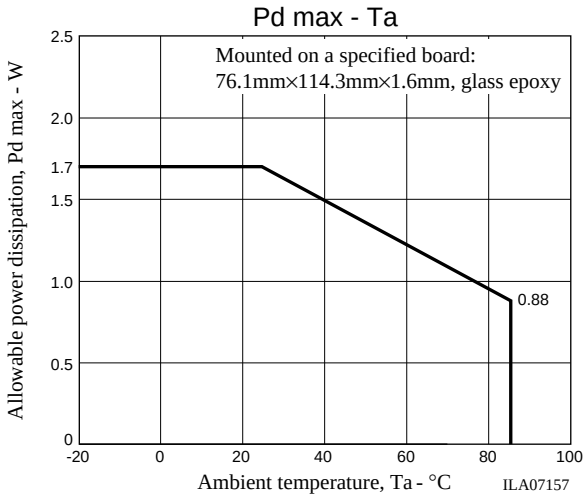
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Power Supply Block] (Uses an external 2SB632K PNP transistor)						
Power supply output	V_{OUT}	I_O = 200mA	1.260	1.285	1.310	V
REG-IN sink current	REG-IN-SINK	External PNP transistor base current	5	10		mA
Line regulation	ΔVOLN	6V ≤ V_{CC} ≤ 12V, I_O = 200mA		10	100	mV
Load regulation	ΔVOLD	5mA ≤ I_O ≤ 200mA		10	100	mV

Package Dimensions

unit : mm (typ)

3344

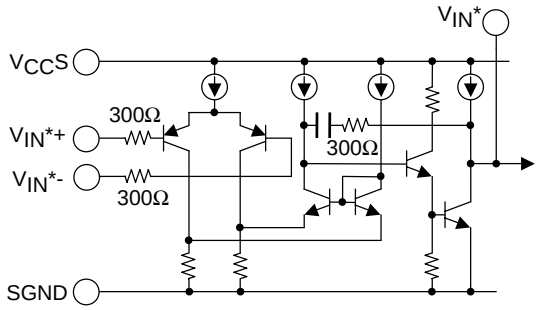
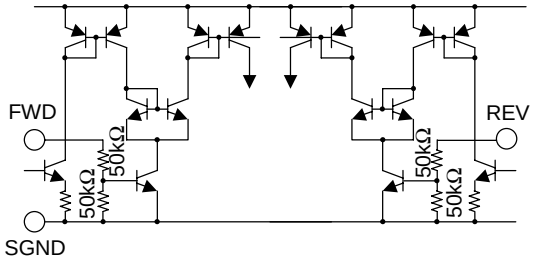
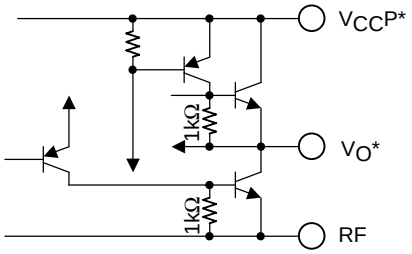
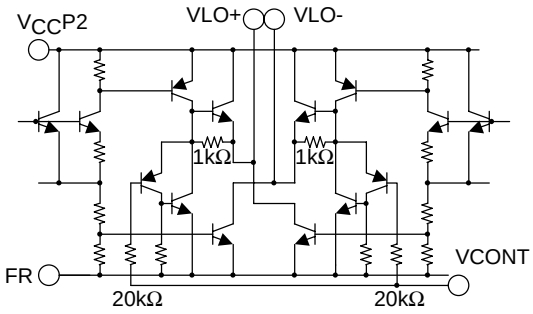
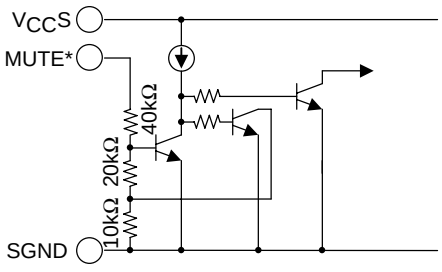




Pin Functions

Pin No.	Pin Name	Description
1	FWD	LOADING output changeover pin (FWD), LOADING logic input
2	REV	LOADING output changeover pin (REV), LOADING logic input
3	$V_{CC}2$	LOADING power-stage power supply for channel 3 and 4
4	NC	-
5	VLO^-	Loading output (-)
6	VLO^+	Loading output (+)
7	V_O4^+	Output pin (+) for channel 4
8	V_O4^-	Output pin (-) for channel 4
9	V_O3^+	Output pin (+) for channel 3
10	V_O3^-	Output pin (-) for channel 3
11	PGND2	Power system GND
12	PGND1	Power system GND
13	V_O2^+	Output pin (+) for channel 2
14	V_O2^-	Output pin (-) for channel 2
15	V_O1^-	Output pin (+) for channel 1
16	V_O1^+	Output pin (-) for channel 1
17	NC	-
18	$V_{CC}P1$	Power-stage power supply for channel 1 and 2
19	$V_{CC}S$	Signal system power supply
20	$V_{IN}1^+$	Input pin for channel 1, Input OP-AMP (+) input
21	$V_{IN}1^-$	Input pin for channel 1, Input OP-AMP (-) input
22	$V_{IN}1$	Input pin for channel 1, Input OP-AMP output
23	NC	-
24	$V_{IN}2^+$	Input pin for channel 2, Input OP-AMP (+) input
25	$V_{IN}2^-$	Input pin for channel 2, Input OP-AMP (-) input
26	$V_{IN}2$	Input pin for channel 2, Input OP-AMP output
27	NC	-
28	$V_{IN}3$-	Input pin for channel 3, Input OP-AMP (-) input
29	$V_{IN}3$	Input pin for channel 3, Input OP-AMP output
30	V_O_OP	OP-AMP, output pin
31	V_{IN}^-OP	OP-AMP, (-) input pin
32	V_{IN}^+OP	OP-AMP, (+) input pin
33	REG_IN	Regulator, error AMP output pin. Base to external PNP transistor connected
34	NC	-
35	REG_OUT	Regulator, error AMP input pin (+)
36	VREF_OUT	VREF_AMP (voltage follower) output pin
37	VREF_IN	VREF input pin. Input the external reference voltage
38	$V_{IN}4$	Input pin for channel 4, Input OP-AMP output
39	NC	-
40	$V_{IN}4^-$	Input pin for channel 4, Input OP-AMP (-) input
41	MUTE234	Output ON/OFF pin for channel 2, 3 and 4
42	MUTE1	Output ON/OFF pin for channel 1
43	VCONT	LOADING output (H voltage) setting pin
44	S_GND	Signal system GND

Pin Description

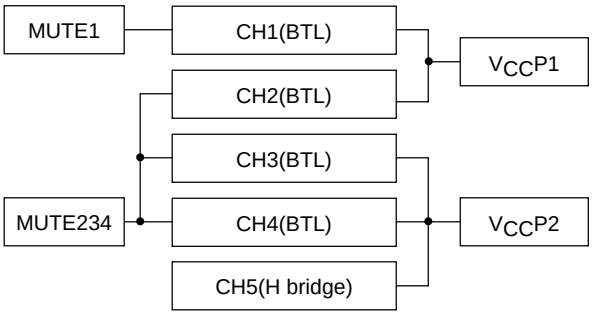
Pin No.	Pin Name	Pin Name	Description	Equivalent Circuit Diagram Description
20 21 22 24 25 26 28 29 38 40 32 31 30	$V_{IN}1^+$ $V_{IN}1^-$ $V_{IN}1$ $V_{IN}2+$ $V_{IN}2^-$ $V_{IN}2$ $V_{IN}3^-$ $V_{IN}3$ $V_{IN}4^-$ $V_{IN}4$ V_{IN}^+OP V_{IN}^-OP V_{O}_OP	Input (CH1 to 4)	Inputs (channels 1 to 4 and the independent operational amplifier)	
1 2	FWD REV	Input (H bridge)	Logic inputs The IC is set to one of four modes, forward, reverse, brake, and free running by the combination of high and low values applied to these pins.	
16 15 13 14 9 10 7 8	V_O1^+ V_O1^- V_O2^+ V_O2^- V_O3^+ V_O3^- V_O4^+ V_O4^-	Output (BTL-AMP)	Channel 1 to 4 outputs	
5 6 43	VLO- VLO+ VCONT	Output (H bridge)	H bridge (loading) output and loading output setting	
41 42	MUTE234 MUTE1	MUTE	BTL amplifier output on/off state setting. High: output on Low: output off	

Truth Table (Loading (H bridge) block)

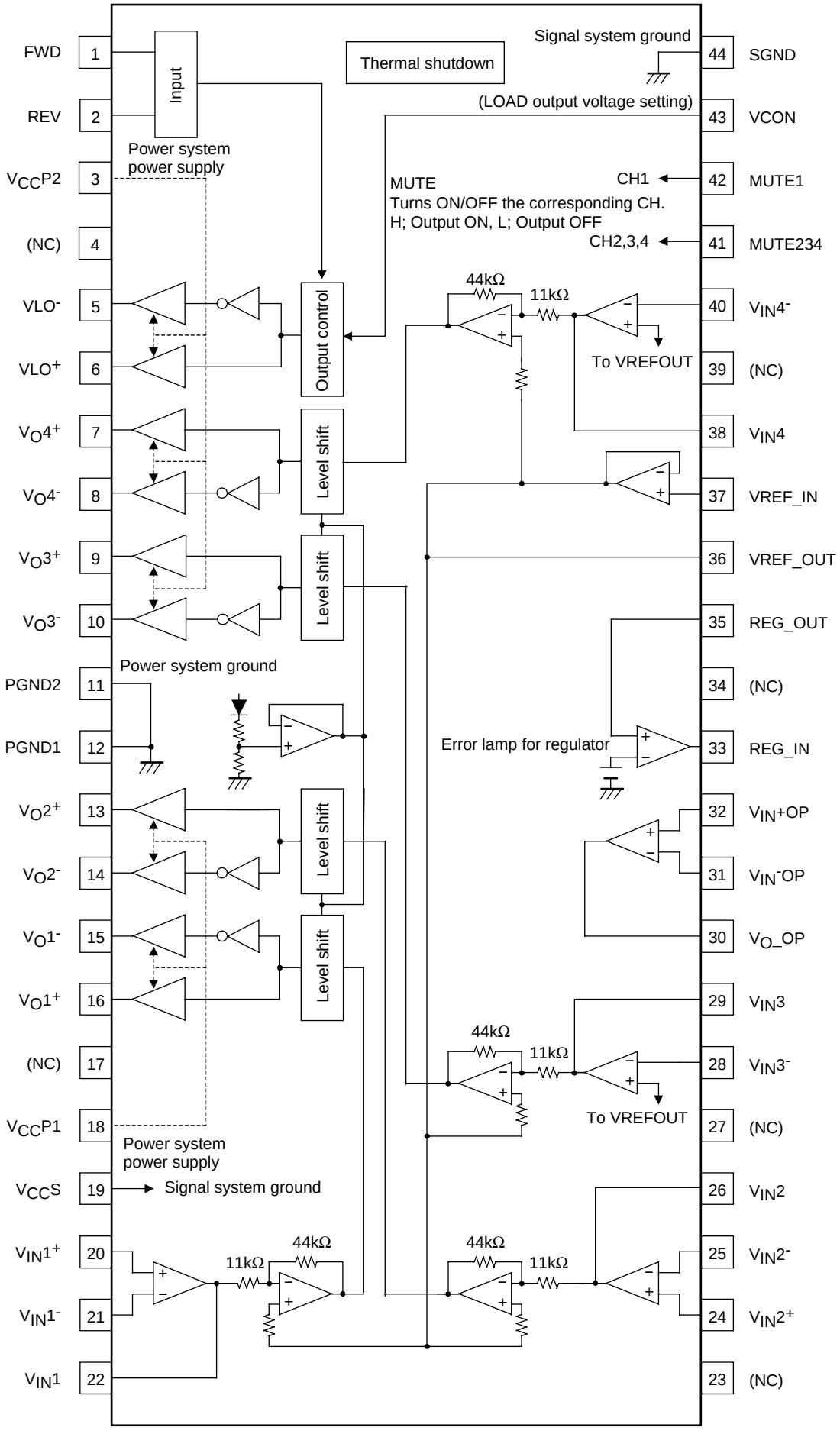
FWD	REV	VLO+	VLO-	Loading output
L	L	OFF	OFF	OFF *1
	H	H	L	Forward
H	L	L	H	Reverse
	H	L	L	Short-circuit braking *2

*1. The output goes to the high-impedance state.
*2. In braking mode, the sink side transistor is turned on (for short-circuit braking).
The VLO+ and VLO- pins go to a level that is essentially the ground level.

Relationship Between The MUTE Pins and The Power Supply Systems ($V_{CC}P$*)



Internal Block Diagram



Sample Application Circuit