REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
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REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16							

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 16 OCTOBER 1989

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 2K X 8 STATIC RAM (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89690

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1400

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89690	01	J	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.6	2K X 8 CMOS SRAM	25 ns
02	See 6.6	2K X 8 CMOS SRAM	20 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
X	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package
Y	Figure 1 (24-terminal, .308" x .408" x .078"), rectangular chip carrier package
Z	C-11 (28-terminal, .560" x .358" x .120"), rectangular chip carrier package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to 7 V dc
Input voltage range 2/	0.5 V to V_{CC} + 0.5 V
Output voltage range in high impedance state	-0.5 V dc to 7 V dc
Output current	20 mA
Storage temperature range	-65°C to +150°C
Power dissipation (P_D)	864 mW
Lead temperature (soldering, 10 seconds)	+275°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases J, K, L, X, Z, and 3	See MIL-M-38510, appendix C
Case Y	20°C/W

1/ All voltages are with respect to GND.
2/ V_{IL} (minimum) of -3 V dc for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below -1 V dc will result in excessive currents that may damage the device.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage range (V_{IH})	2.2 V dc minimum to V_{CC} + 0.5 V dc maximum
Low level input voltage range (V_{IL}) 3/	-0.5 V dc minimum to 0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard,and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3/ V_{IL} (minimum) of -3 V dc for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below -1 V dc will result in excessive currents that may damage the device.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$ unless otherwise specified 1/ 2/ 3/ 4/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating supply current	I_{CC1}	$t_{AVAV} = t_{AVAV}$ (minimum), $V_{CC} = 5.5\ V$, $\overline{CE} = V_{IL}$, all other inputs at V_{IL}	1,2,3	01		135	mA
				02		150	
Standby power supply current TTL	I_{CC2}	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, $V_{CC} = 5.5\ V$, $f = 0$ MHz	1,2,3	01		45	mA
				02		50	
Standby power supply current CMOS	I_{CC3}	$\overline{CE} \ge (V_{CC} - 0.2\ V)$, $f = 0$ MHz, $V_{CC} = 5.5\ V$, all other inputs $< 0.2\ V$ or $> (V_{CC} - 0.2\ V)$	1,2,3	All		20	mA
Input leakage current, any input	I_{ILK}	$V_{CC} = 5.5\ V$, $V_{IN} = 0\ V$ to $5.5\ V$	1,2,3	All	-10	10	µA
Off-state output leakage current	I_{OLK}	$V_{CC} = 5.5\ V$, $V_{IN} = 0\ V$ to $5.5\ V$	1,2,3	All	-10	10	µA
Output high voltage	V_{OH}	$I_{OUT} = -4.0$ mA, $V_{CC} = 4.5\ V$, $V_{IL} = 0.8\ V$, $V_{IH} = 2.2\ V$	1,2,3	All	2.4		V
Output low voltage	V_{OL}	$I_{OUT} = 8.0$ mA, $V_{CC} = 4.5\ V$, $V_{IL} = 0.8\ V$, $V_{IH} = 2.2\ V$	1,2,3	All		0.4	V
Input capacitance 5/	C_{IN}	$V_{IN} = 0\ V$, $f = 1.0$ MHz, $T_A = +25°C$, see 4.3.1c	4	All		8.0	pF
Output capacitance 5/	C_{OUT}	$V_{OUT} = 0\ V$, $f = 1.0$ MHz, $T_A = +25°C$, see 4.3.1c	4	All		8.0	pF
Read cycle time	t_{AVAV}		9,10,11	01	25		ns
				02	20		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$ unless otherwise specified 1/ 2/ 3/ 4/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address access time	t_{AVQV}		9,10,11	01		25	ns
				02		20	
Output hold after address change	t_{AVQX}		9,10,11	01	0		ns
				02	0		
Output enable to output active 5/ 6/	t_{OLQX}		9,10,11	01	0		ns
				02	0		
Output enable access time	t_{OLQV}		9,10,11	01		16	ns
				02		15	
Chip enable to output active 5/ 6/	t_{ELQX}		9,10,11	01	0		ns
				02	0		
Chip enable access time	t_{ELQV}		9,10,11	01		25	ns
				02		20	
Chip enable to output in high Z 5/ 6/	t_{EHQZ}		9,10,11	01		15	ns
				02		15	
Write recovery time	t_{WHAV}		9,10,11	01	0		ns
				02	0		
Chip enable to end-of-write	t_{ELWH}		9,10,11	01	20		ns
				02	15		
Address valid to end-of-write	t_{AVWH}		9,10,11	01	20		ns
				02	15		
Address to $\overline{WE}$ setup time	t_{AVWL}		9,10,11	01	0		ns
				02	0		
Address to $\overline{CE}$ setup time	t_{AVEL}		9,10,11	01,02	0		ns

See footnotes at end of table.

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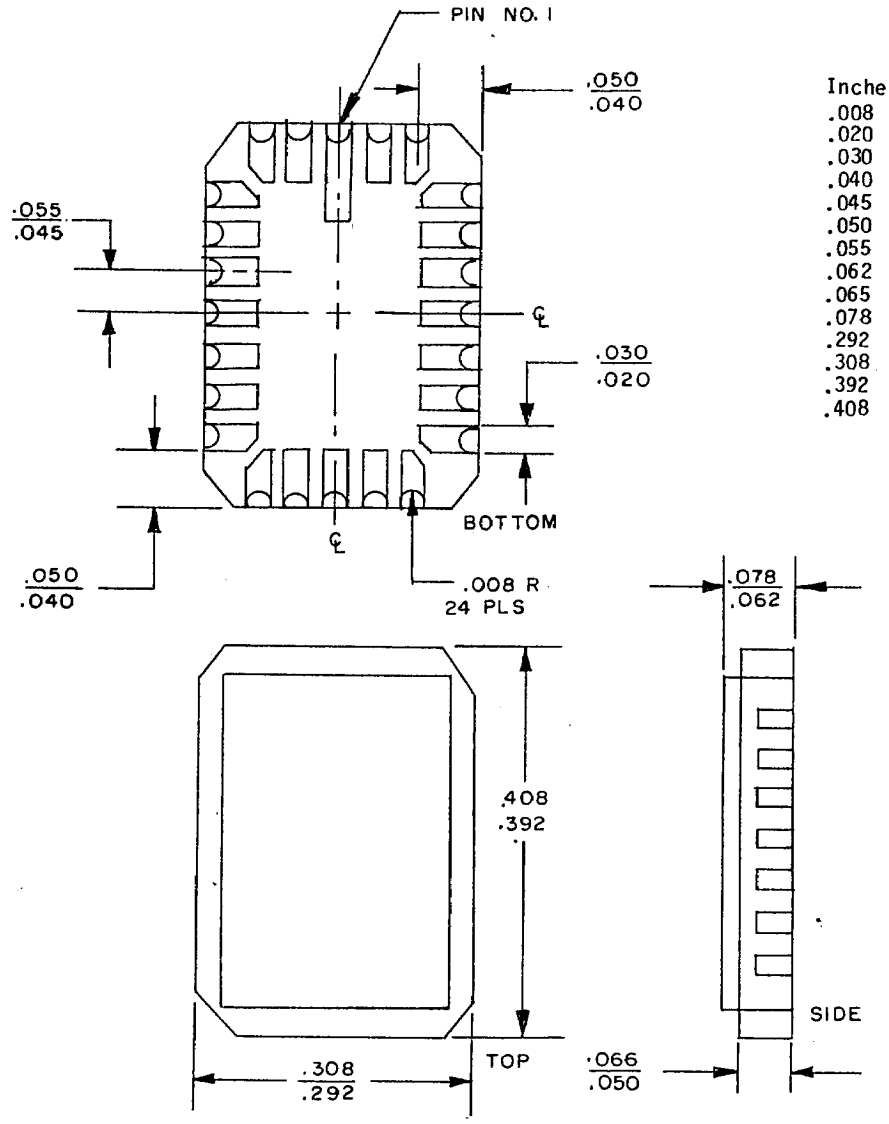
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $V_{SS} = 0\ V$ unless otherwise specified 1/ 2/ 3/ 4/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output enable to output in high Z 5/ 6/	t_{OHQZ}		9,10,11	01		16	ns
				02		15	
Write enable pulse width	t_{WLWH}		9,10,11	01	20		ns
				02	15		
Data setup to end-of-write	t_{DVWH}		9,10,11	01	15		ns
				02	12		
Data hold after end-of-write	t_{WHDX}		9,10,11	01	0		ns
				02	0		
Chip-enable pulse width during write	t_{ELEH}		9,10,11	01	20		ns
				02	15		
Write enable pulse setup time	t_{WLEH}		9,10,11	01	20		ns
				02	15		
Write enable to output in high Z 5/ 6/	t_{WLQZ}		9,10,11	01		15	ns
				02		15	

1/ All voltages referenced to V_{SS}.
2/ Negative undershoots to a minimum of -0.3 V are allowed with a maximum of 50 ns pulse width.
3/ AC measurements assume transition time $\le$ 5 ns and input levels are from V_{SS} to 3.0 V. Output load is specified on figure 4. Reference timing levels are at 1.5 V.
4/ For timing waveforms, see figure 4.
5/ Tested initially, and after any design or process change which could affect these parameters, and therefore shall be guaranteed to the limits specified in table I. Transition measured ±500 mV from steady-state value.
6/ This parameter measured ±500 mV from steady-state output voltage. Load capcitance is 5.0 pF, see figure 4.



Inches	mm
.008	0.20
.020	0.50
.030	0.76
.040	1.01
.045	1.14
.050	1.27
.055	1.39
.062	1.57
.065	1.67
.078	1.98
.292	7.41
.308	7.82
.392	9.95
.408	10.36

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. Case outline Y (24-terminal, .308" x .408" x .078"), rectangular chip carrier package.

Device types	01 and 02		
Case outlines	J,K,L,Y	3,Z	X
Terminal number	Terminal symbol		
1	A7	A7	NC
2	A6	A6	NC
3	A5	A5	NC
4	AA	A4	A7
5	A3	A3	A6
6	A2	A2	A5
7	A1	NC	A4
8	AO	NC	A3
9	I/O 0	A1	A2
10	I/O 1	AO	A1
11	I/O 2	I/O 1	AO
12	V_{SS}	I/O 2	NC
13	I/O 3	I/O 3	I/O 0
14	I/O 4	V_{SS}	I/O 1
15	I/O 5	I/O 4	I/O 2
16	I/O 6	I/O 5	V_{SS}
17	I/O 7	I/O 6	NC
18	$\overline{CE}$	I/O 7	I/O 3
19	A10	I/O 8	I/O 4
20	$\overline{OE}$	$\overline{CE}$	I/O 5
21	$\overline{WE}$	NC	I/O 6
22	A9	NC	I/O 7
23	A8	A10	$\overline{CE}$
24	V_{CC}	$\overline{OE}$	A10
25	---	$\overline{WE}$	$\overline{OE}$
26	---	A9	$\overline{WE}$
27	---	A8	NC
28	---	V_{CC}	A9
29	---	---	A8
30	---	---	NC
31	---	---	NC
32	---	---	V_{CC}

FIGURE 2. Terminal connections.

Inputs			I/O	Mode	Power
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O 0 - I/O 7		
H	X	X	HI-Z	Standby	Standby
L	H	L	Data output	Read	Active
L	H	H	HI-Z	Read	Active
L	L	X	Data input	Write	Active

FIGURE 3. Truth table.

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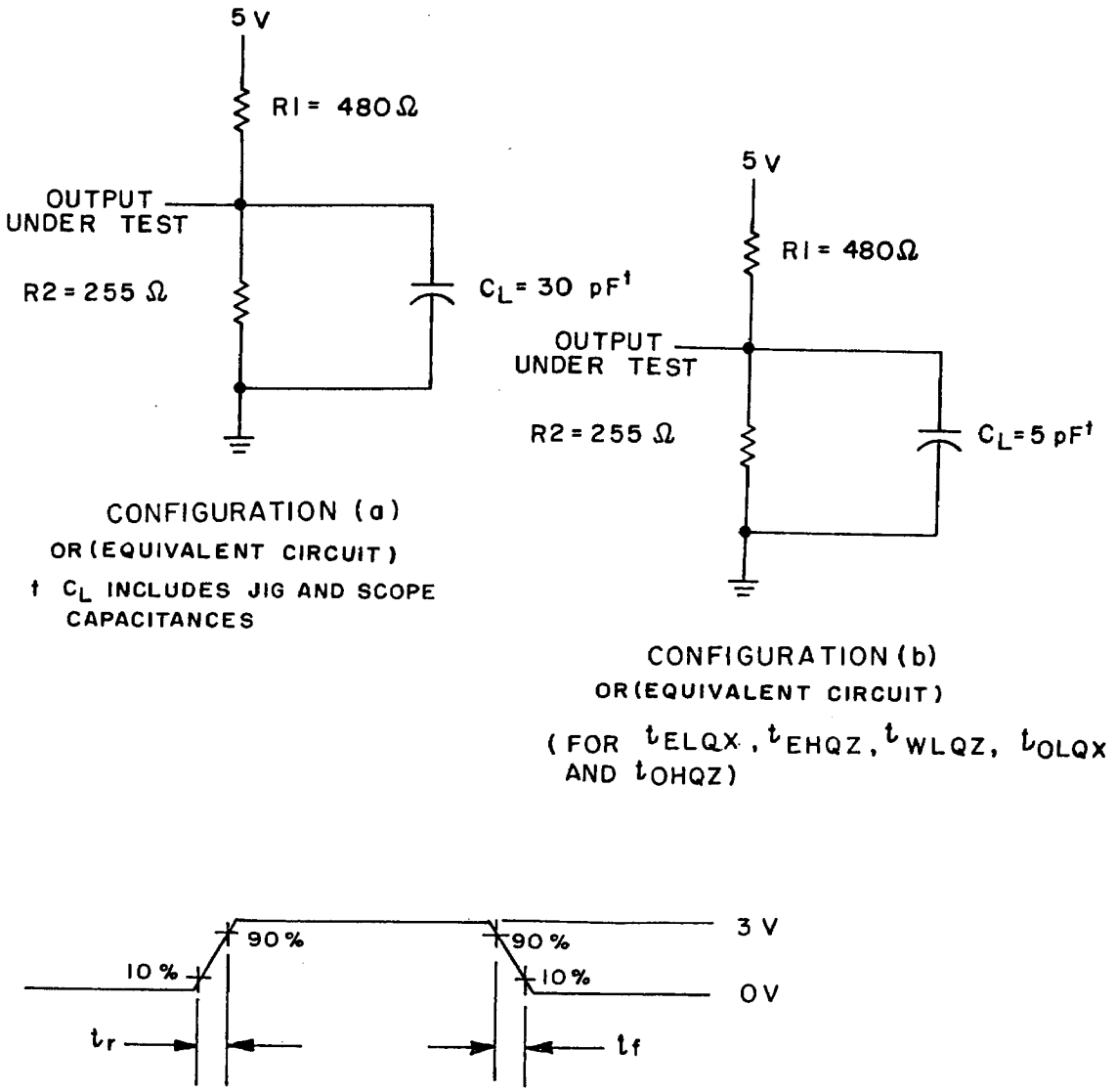
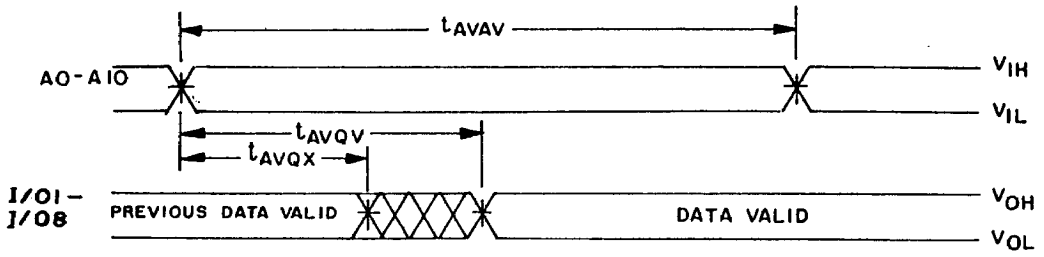


NOTES:
1. t_r and t_f ≤ 5 ns.
2. All switching characteristics and timing requirements assume test conditions as depicted in configuration (a) and configuration (b) with timing references of 1.5 V (50% reference point) as shown in the subsequent timing diagrams.

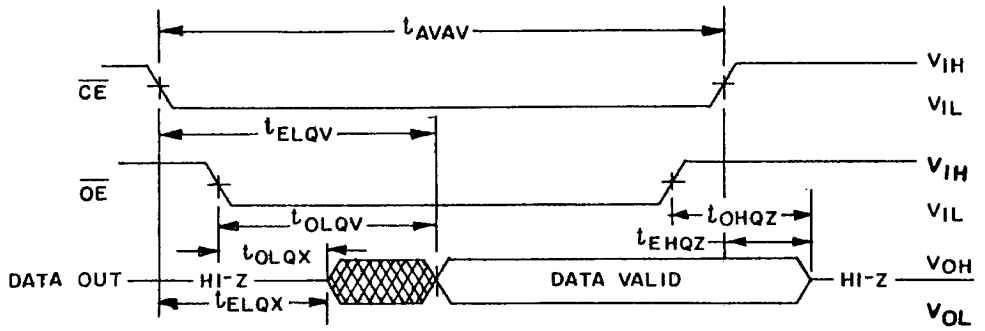
FIGURE 4. Load circuit and switching waveforms.

Read cycle timing from address (see note)



NOTE: When $\overline{WE}$ is high, $\overline{CE}$ is low, and $\overline{OE}$ is low, device is continuously selected.

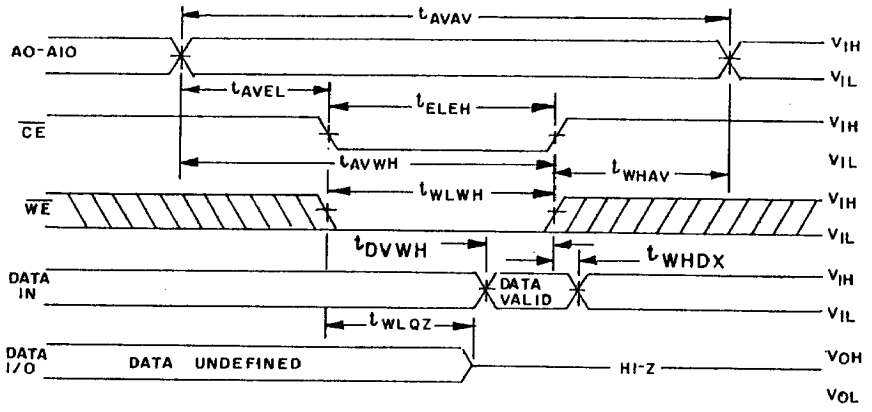
Read cycle timing from chip enable (see note)



NOTE: When $\overline{WE}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{CE}$

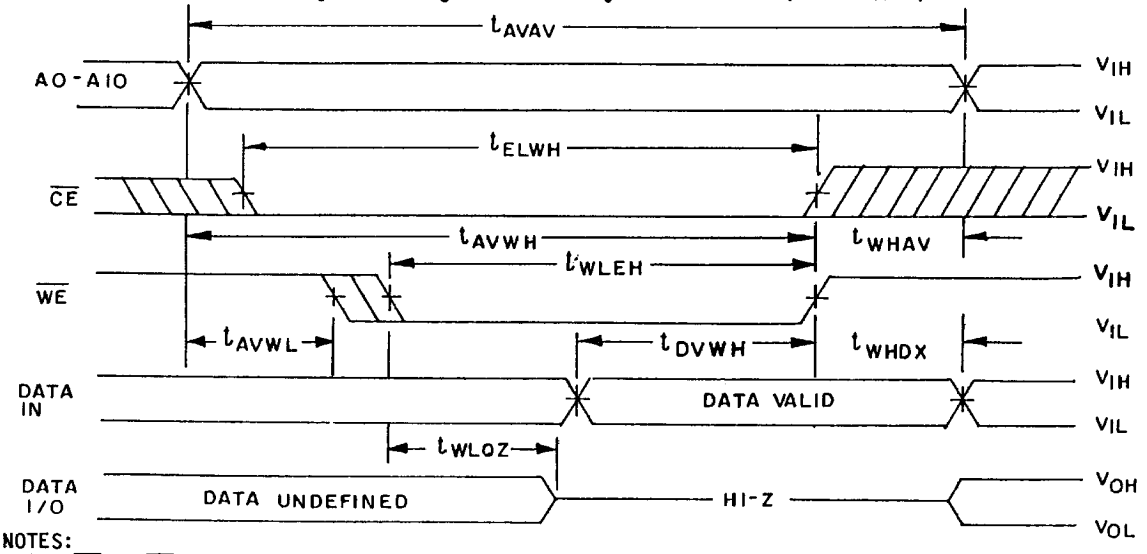
FIGURE 4. Load circuit and switching waveforms - Continued.

Write cycle timing controlled by from chip enable (see note 1)



NOTES:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
2. Data I/O pins enter high-impedance state, as shown when $\overline{CE}$ is held low during write.

Write cycle timing controlled by write enable (see note 1)



NOTES:
1. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory if defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write, and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write. Data I/O pins enter high-impedance state, as shown when $\overline{CE}$ is held low during write.

FIGURE 4. Load circuit and switching waveforms - Continued.

3.2.4 Load circuit and switching waveforms. The load circuit and switching waveforms shall be as specified on figure 4.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-M-38510, inspection lot, class B paragraph) shall be subjected to and pass the internal water vapor test (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8A, 8B,9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7***, (8A,8B)***,9,10,11
Groups C and D end-point electrical (method 5005)	2,3,7,8A,8B

* PDA applies to subgroups 1 and 7.
** See 4.3.1c.
*** See 4.3.1d.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured for the initial characterization and after any process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 tests shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8969001JX	61772 65786	IDT6116SA25DB CY6116A-25DMB
5962-8969001KX	61772 65786	IDT6116SA25EB CY7C128A-25KMB
5962-8969001LX	01295 65786 61772 75569 6Y440	SMJ68CE16-25JDM CY7C128A-25DMB IDT6116SA25TDB P4C116-25DMB MT5C1608C-25883C
5962-8969001XX	65786 61772 01295	CY6117A-25LMB IDT6116SA25L32B SMJ68CE16-25FGM
5962-8969001YX	61772 65786	IDT6116SA25L24B CY7C128A-25LMB

See footnote at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-89690013X	65786 61772	CY6116A-25LMB IDT6116SA25L28B
5962-8969001ZX	6Y440	MT5C1608EC-25883C
5962-8969002JX	61772 65786	IDT6116SA20DB CY6116A-20DMB
5962-8969002KX	61772 65786	IDT6116SA20EB CY7C128A-20KMB
5962-8969002LX	65786 61772 75569 6Y440	CY7C128A-20DMB IDT6116SA20TDB P4C116-20DMB MT5C1608C-20883C
5962-8969002XX	65786 61772	CY6117A-20LMB IDT6116SA20L32B
5962-8969002YX	61772 65786	IDT6116SA20L24B CY7C128A-20LMB
5962-8969002ZX	6Y440	MT5C1608EC-20883C
5962-89690023X	65786 61772 6Y440	CY6116A-20LMB IDT6116SA20L28B MT5C1608EC-20883C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated P.O. Box 60448 Midland, TX 79711-0448
6Y440	Micron Technology 2805 E. Columbia Road Boise, ID 83706

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Incorporated 3236 Scott Boulevard Santa Clara, CA 95054
65786	Cypress Semiconductor 3901 N. First Street San Jose, CA 95134
75569	Performance Semiconductor Corporation 610 East Weddell Drive Sunnyvale, CA 94089