MOTOROLA

MC13142

Advance Information

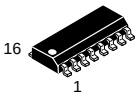
Low Power DC – 1.8 GHz LNA, Mixer and VCO

The MC13142 is intended to be used as a first amplifier, voltage controlled oscillator and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Voltage Controlled Oscillator (VCO), a buffered oscillator output, a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section. The wide mixer IF bandwidth allows this part also to be used as an up converter and exciter amplifier.

- Wide RF Bandwidth: DC–1.8 GHz
- Wide LO Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–1.8 GHz
- Low Power: 13 mA @ V_{CC} = 2.7 – 6.5 V
- High Mixer Linearity: $P_{i1.0\ dB}$ = 3.0 dBm
- Linearity Adjustment Increases IP_{3in} Up to 20 dBm
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Open Collector Mixer Output
- Single Transistor Oscillator with Collector, Base and Emitter Pinned Out
- Buffered Oscillator Output

LOW POWER DC – 1.8 GHz LNA, MIXER and VCO

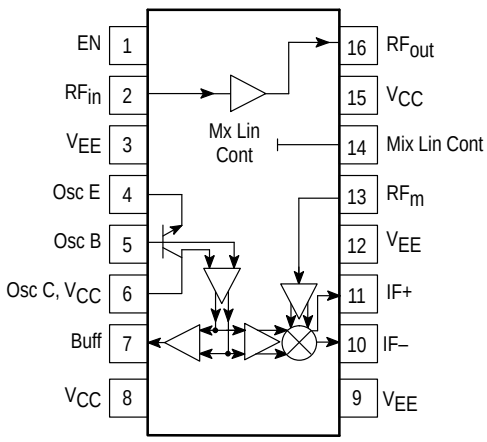
SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS

SO–16



This device contains 176 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13142D	T_A = –40° to +85°C	SO–16

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Rev 1

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range	V_{CC}	2.7 to 6.5	Vdc

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V, T_A = 25°C, LO_{in} = –10 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Disable) Pin 15 with Pin 1 @ 0 V Pin 10 and 11 with Pin 1 @ 0 V Pin 6 with Pin 1 @ 0 V	I_{CC_Total} I_{CC_15} I_{CC_Mix} I_{CC_6}	–230 –110 –20 –100	– – – –	230 110 20 100	µA
Supply Current (Enable) Pin 15 with Pin 1 @ 3.0 V Pin 10 with Pin 1 @ 3.0 V Pin 6 with Pin 1 @ 3.0 V	I_{CC_Total} I_{CC_15} I_{CC_Mix} I_{CC_6}	8.25 1.0 1.25 6.0	13.5 – – –	26 4.5 7.5 14	mA
Amplifier Gain (50 Ω Insertion Gain)	S_{21}	6.5	12	13	dB
Amplifier Reverse Isolation	S_{12}	–	–33	–	dB
Amplifier Input Match	$\Gamma_{in\ amp}$	–	–10	–	dB
Amplifier Output Match	$\Gamma_{out\ amp}$	–	–15	–	dB
Amplifier 1.0 dB Gain Compression	$Pin_{–1.0\ dB}$	–18	–15	–8.0	dBm
Amplifier Input Third Order Intercept	$IP3_{in}$	–	–5.0	–	dBm
Amplifier Noise Figure (Application Circuit)	NF	1.0	1.8	4.0	dB
Amplifier Gain @ N.F.	G_{NF}	–	17	–	dB
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	9.0	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–7.0	–3.0	–2.0	dB
Mixer Input Match	$\Gamma_{in\ M}$	–	–20	–	dB
Mixer SSB Noise Figure	NF_{SSBM}	–	12	–	dB
Mixer 1.0 dB Gain Compression	$Pin_{–1.0\ dBM}$	–	3.0	–	dBm
Mixer Input Third Order Intercept	$IP3_{InM}$	–	–1.0	–	dBm
Oscillator Buffer Drive (50 Ω)	P_{VCO}	–19.5	–16	–12	dBm
Oscillator Phase Noise @ 25 kHz Offset	N_Φ	–	–90	–	dBc/Hz
RF_{in} Feedthrough to RF_m	$P_{RFin–RFm}$	–	–35	–	dB
RF_{out} Feedthrough to RF_m	$P_{RFout–RFm}$	–	–35	–	dB
LO Feedthrough to IF	$P_{LO–IF}$	–	–35	–	dBm
LO Feedthrough to RF_{in}	$P_{LO–RFin}$	–	–35	–	dBm
LO Feedthrough to RF_m	$P_{LO–RFm}$	–	–35	–	dBm
Mixer RF Feedthrough to IF	$P_{RFm–IF}$	–	–25	–	dB
Mixer RF Feedthrough to RF_{in}	$P_{RFm–RFin}$	–	–25	–	dB

CIRCUIT DESCRIPTION

General

The MC13142 is a low power LNA, double–balanced Mixer, and VCO. This device is designated for use as the frontend section in analog and digital FM systems such as Digital European Cordless Telephone (DECT), PHS, PCS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto program the mixer dynamic range, an enable function and a wideband IF so the IC may be used either as a down converter or an up converter. Further details are covered in the Pin by Pin Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators are controlled by the enable function in which “high” powers up the IC.

Low Noise Amplifier (LNA)

The LNA is internally biased at low supply current (approximately 2.0 mA emitter current) for optimal noise figure and gain. The LNA output is biased internally with a 600 Ω resistor to V_{CC}. Input and output matching may be achieved at various frequencies using few external components. Matching the LNA for Maximum stable gain (MSG) yields noise performance within a few tenths of a dB of the minimum noise figure.

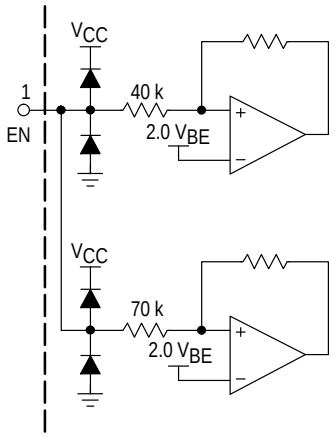
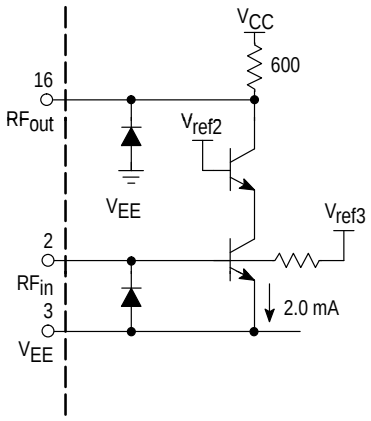
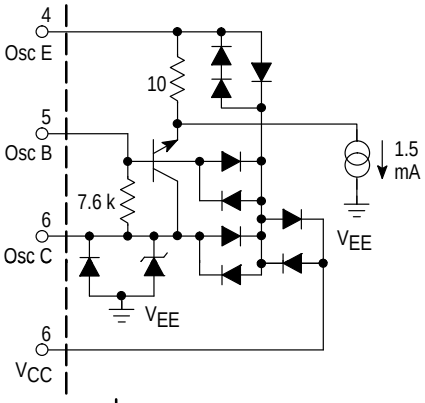
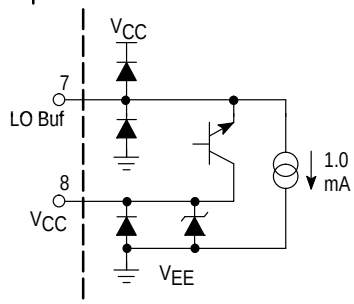
Mixer

The mixer is a double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm may be achieved. All 3 ports of the mixer are designed to work up to 1.8 GHz. The mixer has a 50 Ω single–ended RF input and open collector differential IF outputs. An on–board Local Oscillator transistor has the emitter, base and collector pinned out to implement a low phase noise VCO in various configurations. Additionally, a buffered LO output is provided for operation with a frequency synthesizer. The linear gain of the mixer is approximately 0 dB with a SSB noise figure of 12 dB in the IF output circuit configuration shown in the application example.

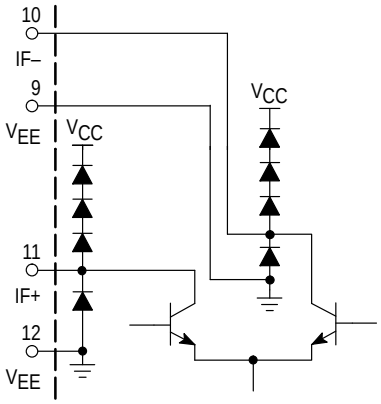
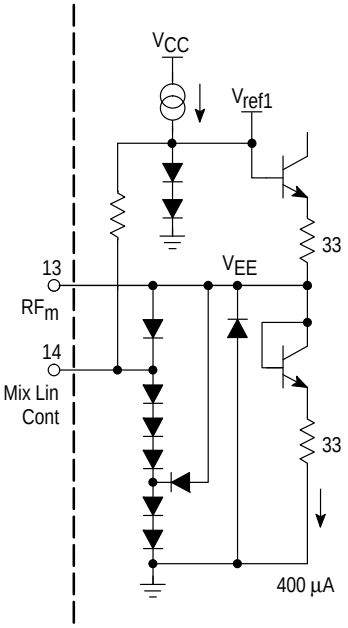
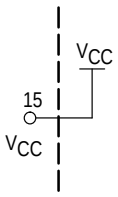
Local Oscillator

The on–chip transistor operates with coaxial transmission line or LC resonant elements to over 2.0 GHz. Biasing is done with a temperature compensated current source in the emitter and a collector to base internal resistor of 7.6 kΩ; however, an RFC from V_{CC} to base is recommended. The application circuit shows a voltage controlled Clapp oscillator operating at center frequency of 975 MHz.

PIN FUNCTION DESCRIPTION

Pin 16 Pin SOIC	Symbol	Equivalent Internal Circuit (20 Pin LQFP)	Description
1	EN		**Enable, E Osc** In SO–16, both enables, (for the Oscillator/LO Buffer and LNA/Mixer) are bonded to Pin 1. Enable by pulling up to V_{CC} or to greater than 2.0 V_{BE}.
2	RF_{in}		**RF Input** The input is the base of an NPN low noise amplifier. Minimum external matching is required to optimize the input return loss and gain.
3	V_{EE}		**V_{EE} – Negative Supply** V_{EE} pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A two sided PCB is implemented so that ground returns can be easily made through via holes.
16	RF_{out}		**RF Output** The output is from the collector of the LNA; it is internally biased with a 600 Ω resistor to V_{CC}. As shown in the 926 MHz application receiver the output is conjugately matched with a shunt L, and series L and C network.
4 5 6	Osc E Osc B Osc C		**On–Board VCO Transistor** The transistor has the emitter, base and collector + V_{CC} pins available. Internal biasing which is compensated for stability over temperature is provided. It is recommended that the base pin is pulled up to V_{CC} through an RFC chosen for the particular oscillator center frequency. The application circuit shows a modified Colpitts or Clapp oscillator configuration and its design is discussed in detail in the application section.
6 8	V_{CC} V_{CC}		**Supply Voltage (V_{CC})** Two V_{CC} pins are provided for the Local Oscillator and LO Buffer Amplifier. The operating supply voltage range is from 2.7 Vdc to 6.5 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as feasible to minimize inductive reactances along the trace. V_{CC} should be decoupled to V_{EE} at the IC pin as shown in the component placement view.
7	LO Buff		**Local Oscillator Buffer** This is a buffered output providing –16 dBm (50 Ω termination) to drive the f_{in} pin of a PLL synthesizer. Impedance matching to the synthesizer may be necessary to deliver the optimal signal and to improve the phase noise performance of the VCO.

PIN FUNCTION DESCRIPTION (continued)

Pin 16 Pin SOIC	Symbol	Equivalent Internal Circuit (20 Pin LQFP)	Description
9, 12	V_{EE}		**V_{EE}, Negative Supply** These pins are V_{EE} supply for the mixer IF output. In the application PC board these pins are tied to a common V_{EE} trace with other V_{EE} pins.
10, 11	IF–, IF+		**IF Output** The IF is a differential open collector configuration which designed to use over a wide frequency range for up conversion as well as down conversion. Differential to single–ended circuit configuration and matching options are discussed in the application section. 6.0 dB of additional Mixer gain can be achieved by conjugately matching at the desired IF frequency.
13	RF_m		**Mixer RF Input** The mixer input impedance is broadband 50 Ω for applications up to 1.8 GHz. It easily interfaces with a RF ceramic filter as shown in the application schematic.
14	Mix Lin Cont		**Mixer Linearity Control** The mixer linearity control circuit accepts approximately 0 to 2.3 mA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 20 dBm may be achieved at 2.3 mA of control current (approximately 7.0 mA of additional supply current).
15	V_{CC}		**V_{CC}, Power Supply**

APPLICATIONS INFORMATION

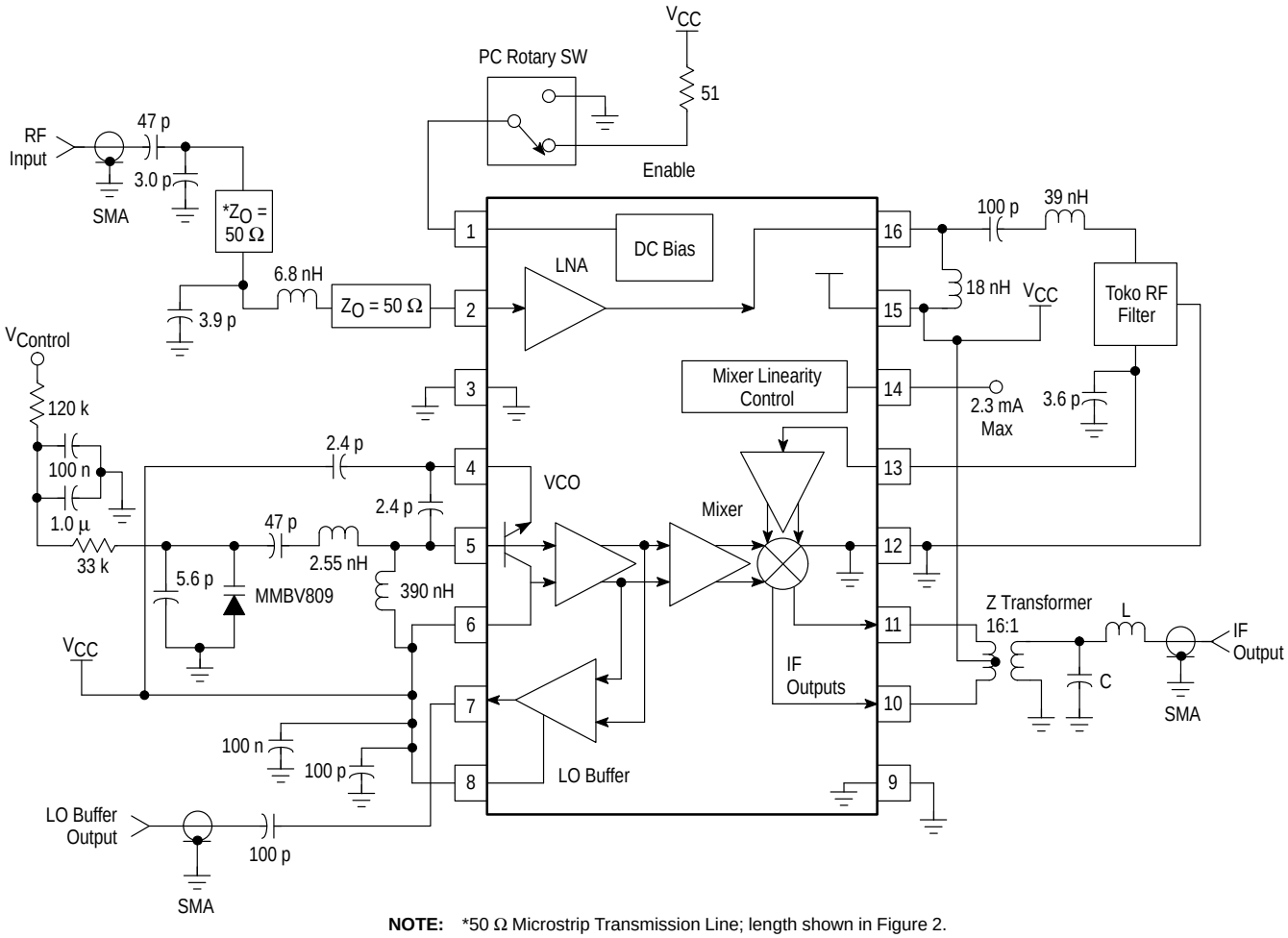
Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board accommodates all SMT components on the circuit side (see Circuit Side Component Placement View). This evaluation board will be discussed and referenced in this section.

Component Selection

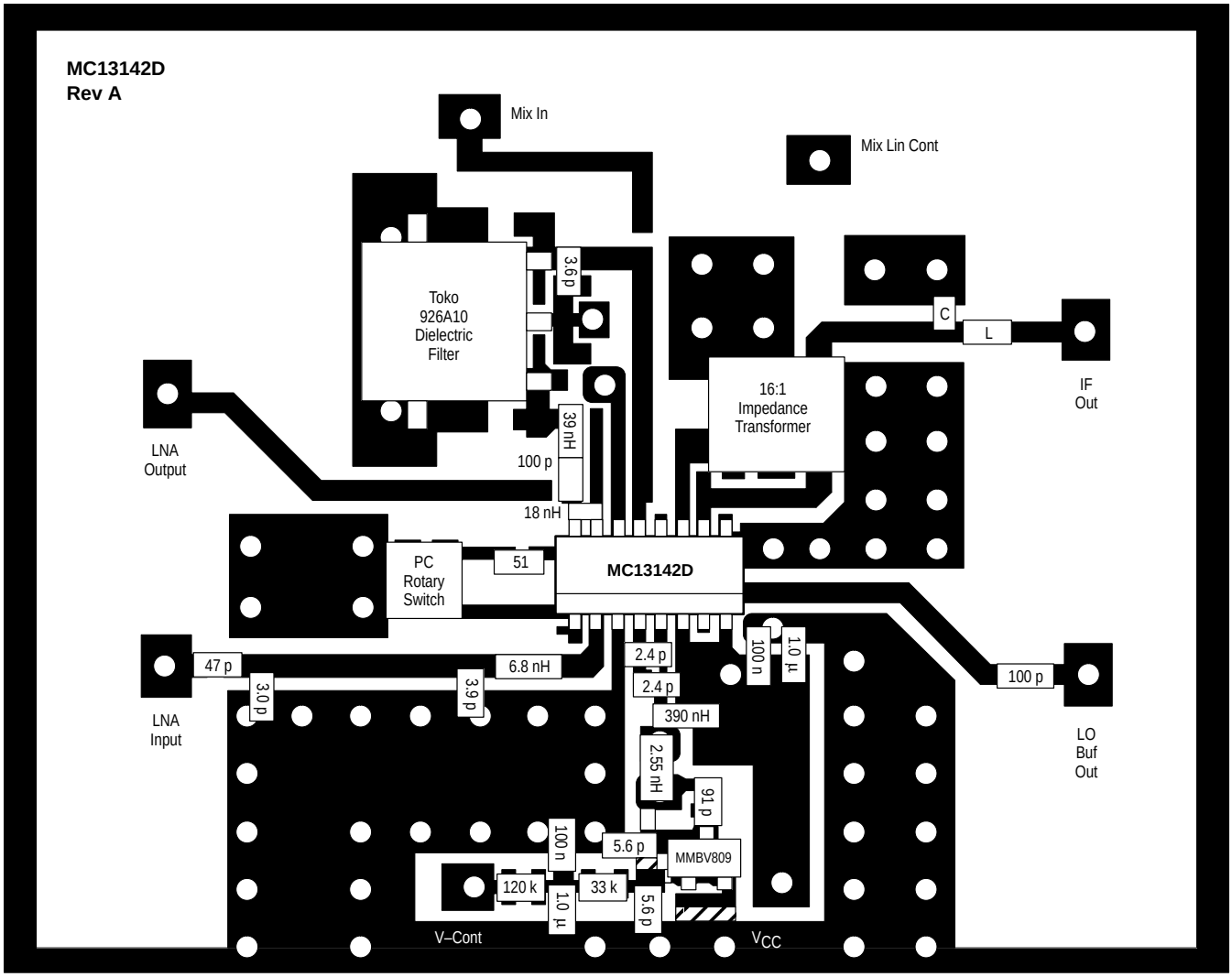
The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers. The circuit side placement view is illustrated for the components specified in the application circuit. The application circuit schematic specifies particular components that were used to achieve the results given and specified in the tables but alternate components of the same Q and value should give equivalent results.

Figure 1. Application Circuit
(926.5 MHz)



NOTE: *50 Ω Microstrip Transmission Line; length shown in Figure 2.

Figure 2. 900 MHz Circuit Side Component Placement View



NOTES: The PCB is laidout for the 4DFA (2 pole SMD type) and 4DFB (3 pole SMD type) filters which are available for applications in cellular and GSM,GPS (1.2–1.5 GHz), DECT, PHS and PCS (1.8–2.0 GHz) and ISM Bands (902–928 MHz and 2.4–2.5 GHz). In the component placement shown above, the 926.5 MHz dielectric type image filter is used (Toko Part # 4DFA–926A10).

The PCB also accommodates a surface mount SAW filter in an eight or six pin ceramic package for the cellular base and handset frequencies. Recommended manufacturers are Siemens and Murata.

Traces are provided on the PCB to evaluate the LNA and mixer separately. The component placement view shows external circuit components used for the 926.5 MHz application circuit. Note: some traces must be cut to accommodate placement of components; likewise some traces must be shorted. The voltage controlled oscillator is shown with the varactor referenced to V_{EE} ground. The PCB is modified as shown to do this.

16:1 broadband impedance transformer is mini circuits part #TX16–R3T; it is in the leadless surface mount "TX" package. Components L and C comprise a low pass filter used to provide narrowband matching at a given IF frequency. For example at 49 MHz C = 36 p and L = 330 nH.
The microstrip trace on the ground side of the PCB is intended for a microstrip resonator; it is cut free when using a lump inductor as done above.

Input Matching/Components

The MC13142 uses an RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. The PC board layout accommodates both ceramic and SAW RF filters which are offered by various suppliers such as Siemens, Toko and Murata.

Interface matching between the LNA, RF filter and the mixer will be required. The interface matching networks shown in the application circuit are designed for 50 Ω interfaces.

In the application circuit, the LNA is conjugately matched to 50 Ω input and output for 3.0 to 5.0 Vdc V_{CC}. 17 dB gain and 1.8 dB noise figure is typical at 926 MHz. The mixer measures 0 dB gain and 12 dB noise figure as shown in the application circuit. Typical insertion loss of the Toko ceramic filter is 3.0 dB. Thus, the overall gain of the frontend receiver is 14 dB with a 3.3 dB noise figure.

System Noise Considerations

The block diagram shows the cascaded noise stages of the MC13142 in the frontend receiver subsystem; it represents the application circuit. In the cascaded noise analysis the system noise equation is:

Fsystem = F1 + [(F2 –1)/G1] + [(F3–1)]/[(G1)(G2)]

where:

F1 = the Noise Factor of the MC13142 LNA
G1 = the Gain of the LNA
F2 = the Noise factor of the RF Ceramic Filter
G2 = the Gain of the Ceramic Filter
F3 = the Noise factor of the Mixer

Note: the above terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

F = Log $^{-1}$ [(NF in dB)/10] and similarly
G = Log $^{-1}$ [(Gain in dB)/10].

Calculating in terms of gain and noise factor yields the following:

F1 = 1.51; G1 = 50.11
F2 = 1.99; G2 = 0.5
F3 = 15.85

Thus, substituting in the equation for system noise factor:

Fsystem = 2.12; NFsystem = 3.3 dB

Figure 3. Frontend Subsystem Block Diagram for Noise Analysis

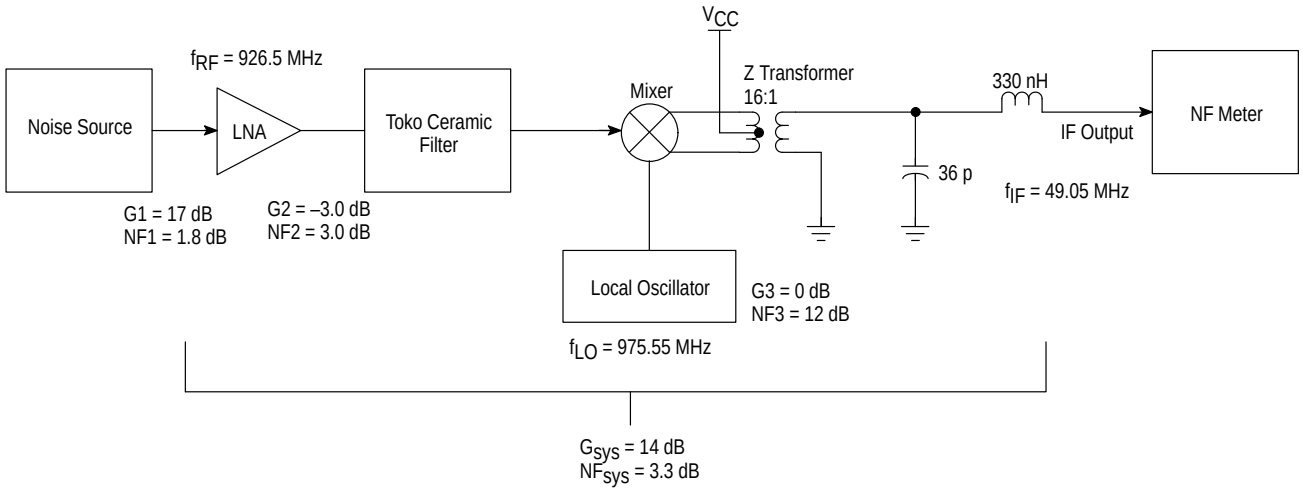
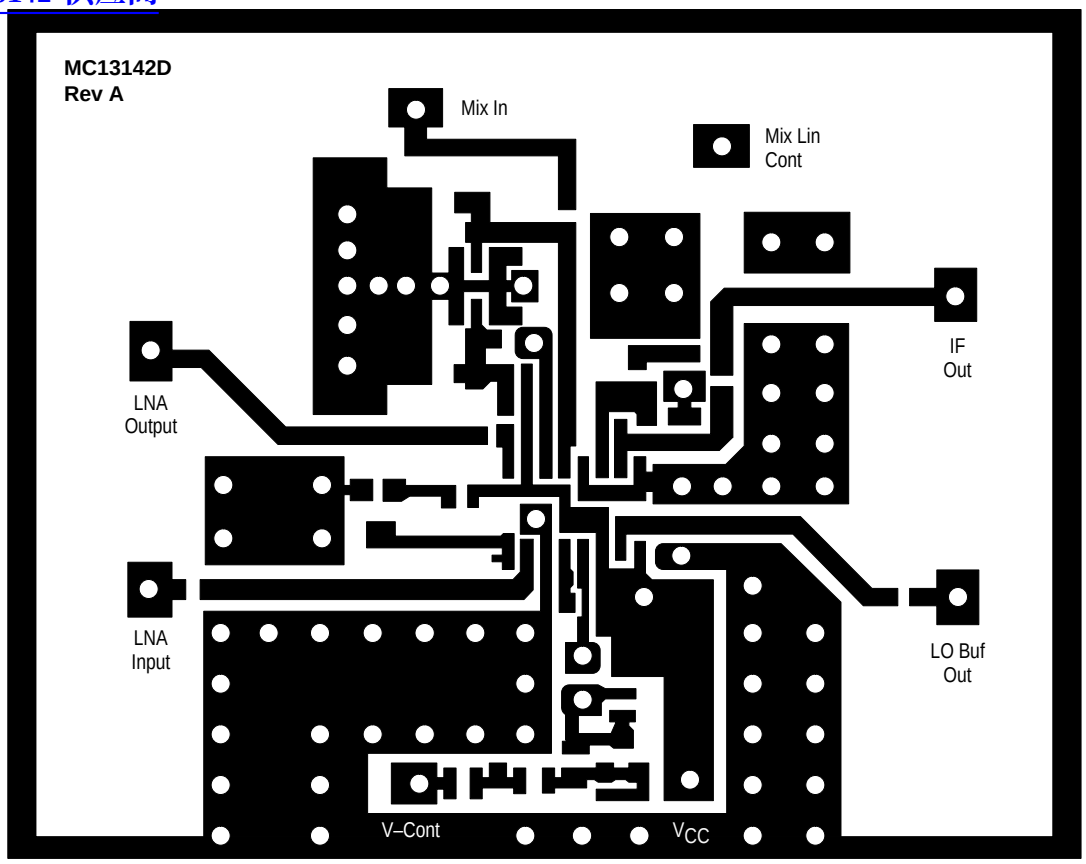
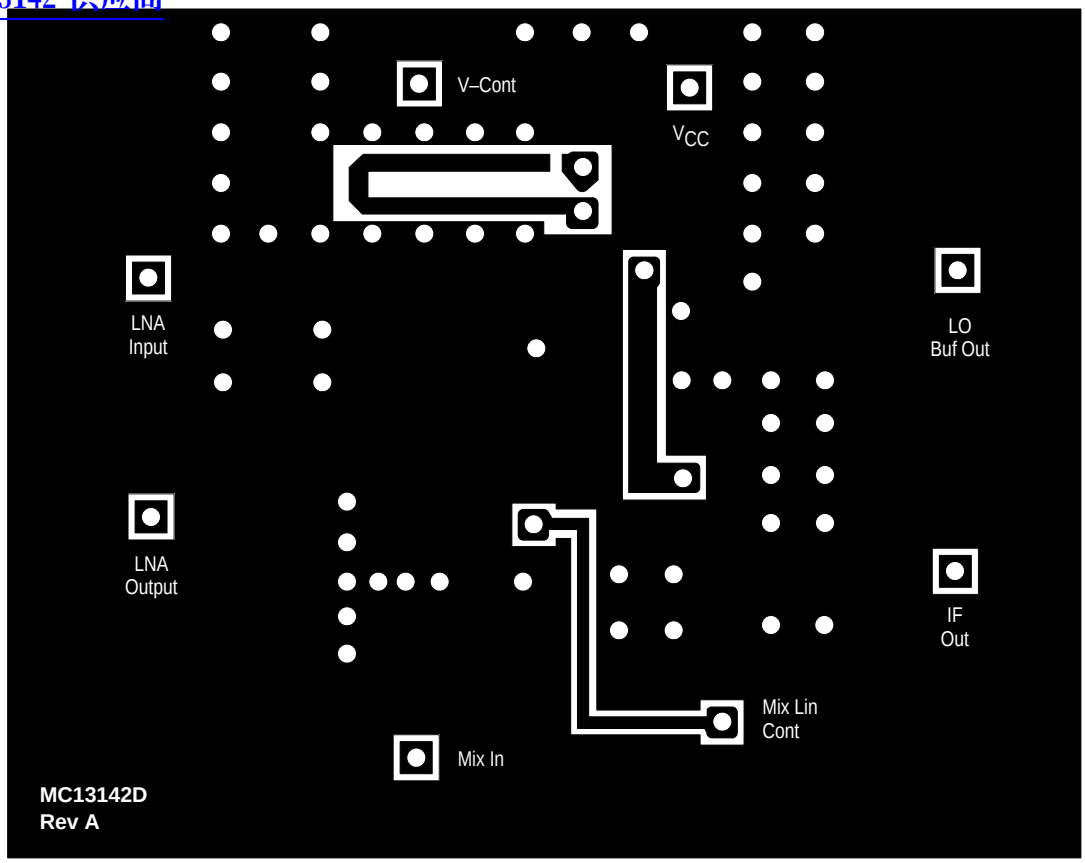


Figure 4. Circuit Side View



NOTES: Critical dimensions are 50 mil centers lead to lead in SO–16 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 5. Ground Side View



NOTES: FR4 PCB, 1/32 inch.

1.9 GHz FRONT–END FOR WIRELESS SYSTEMS

This application is applicable to both Analog and Digital systems. With the correct VCO tuning and the appropriate filter, it will do the front–end for DECT, PHS or PCS. The MC13142D is available in a SOIC 16 pin package. The part requires minimal external components, leading to a low cost system. A circuit board layout with a circuit diagram to evaluate the IC is shown. Except for the PLL control, all the wireless systems front–ends will look the same and have the same basic performance characteristic as the test circuit.

Circuit Operation:

LNA Input/Output

An LC filter is incorporated before the LNA to provide some selectivity. In addition to selectivity, its other function is to match the antenna impedance (50 Ω) to the LNA input for best gain and sensitivity (low noise figure). The network reflects about a 200 Ω source impedance to the device.

The output circuit is a pie network consisting of; the LNA output capacity, the inductance (the bond wire, package pin and L2), and the input capacity of the dielectric filter, along with some added shunt. A 2.4 pF with Toko 4DFA 2 pole filter. The 2.4 pF is for matching the in–band filter impedance to the LNA output and has little effect on tuning.

Both networks are tuned to band center by adjusting L1 and L2. L1 and L2, as well as L3, are short length of wire formed in a half loop. Once the correct length is determined in centering the tuning range, adjustment is accomplished by moving the loop toward or away from some conductive surface such as a ground plane.

The dielectric filter is referenced to the dc supply which lessen the parts count and adds distributive capacity for high frequency bypassing. DC feed to the LNA is through a low value resistor (220 to 330 Ω) tapped at the filter input, so as not to load the circuit unnecessarily. There is a small voltage drop across the resistor, as well as some signal loss. The signal loss is about 0.73 dB for a 220 Ω resistor and less for larger values. If one can not afford the voltage drop, an inductor could replace the resistor at a somewhat increased cost.

Mixer

Looking from the dielectric filter's output, the Mixer input is 50 Ω in series with an inductor. This inductor consists of the printed circuit run, the package pin and bond wire, all in series. It is modified, to some extent, by the package pin distributive capacity, but overall at the bandpass frequency remains inductive. Matching the filter impedance to the Mixer input only requires a capacitor with a value that, when placed in series, will resonate with this inductor at the filter bandpass frequency.

The single–ended input signal is converted internally into balanced current signals. The two signals drive the two low impedance inputs (emitters) of a Gilbert Cell. They appear as

current sources to the Cell and can be programmed (via Pin 15) for more current. The current is often adjusted for minimum third order response. In this Fixture it is fixed biased for most conversion gain.

The Mixer circuit is balanced where both oscillator and RF are suppressed. This provides IF signals at Pins 9 and 10 which are equal in amplitude and 180 degrees out of phase. To realize a positive gain one needs to reflect a higher impedance from the load impedance (50 Ω for this fixture) to the Mixer output or outputs. Maximum signal transfer would require a balance to unbalance network. Center tapped tuned transformers can perform this function but are quite expensive. If one can afford 3.0 dB less signal, a simple LC circuit at one of the outputs will work well. The other output is unused and bypassed to ground.

The most gain is realized when no shunt capacity is added and L4 is selected to resonate with the terminal capacity. Adding shunt capacity will lower the gain and increase the circuit's bandwidth. A small value series capacitor C4 to the 50 Ω output will control the reflected impedance and complete the circuit. L4 and C4 will vary in value depending on the IF frequency.

VCO

The base of the device is the source for driving both the Gilbert cell and prescaler buffer stages. Because of this, the oscillator device will operate and drive the Mixer only in the grounded collector configuration. Additional dc bias is added through a 1.3 kΩ resistor (tapped for minimum VCO loading) to reduce the off–set between base and supply.

The external circuit is a modified Colpitts where the capacitance between base and emitter (Pins 4 and 5), along with a capacitor from emitter to ac ground, forms the circuit capacity and the feedback that sustains oscillations. The effective circuit inductance (looking from the top of the circuit, the transistor base) consist of L3 in series with varactor diode D1 and a blocking capacitor. This circuit must appear inductive for the VCO to operate properly. If the capacity is too small, the feedback ratio is reduced and the VCO can cease oscillating. When it becomes to large, it will not vary the frequency due to the limiting effect of the series loop capacitance.

In this application, the VCO is not required to cover a large tuning range. Limiting the tuning range to no more than is required to cover the band (making allowance for temperature and aging effects) will result in a VCO less susceptible to on board noise sources. To assure oscillation while controlling the tuning range the varactor (plus series capacitor) minimum capacity is chosen to be about equal to the capacity from Pin 5 (transistor base) to RF ground. The maximum tuning ratio could be no greater than 1.41 because the circuit capacity could only double whatever the upper value capacity the varactor attained. An upper limit on the varactor capacity along with the effects of the series capacitor reduces the VCO tuning range to about 1.2 times. The varactors chosen for the test fixtures were Loral KV2111.

The VCO buffer, as most emitter follower circuits, has the potential of generating a parasitic oscillation. When a collector is RF bypassed, a tuned LC circuit is formed consisting of the bypass capacitor, bond wire plus package pin inductance and the device effective output capacity. If the base is low impedance, there is normally enough distributive collector to emitter capacity for the device to oscillate in the common base mode. A simple fix without affecting the buffer otherwise, is to place a small value series resistor in the collector lead. This will lower the Q of the circuit where it cannot sustain oscillations. Without the series resistor at Pin 8 or some other damping element, the buffer will oscillate.

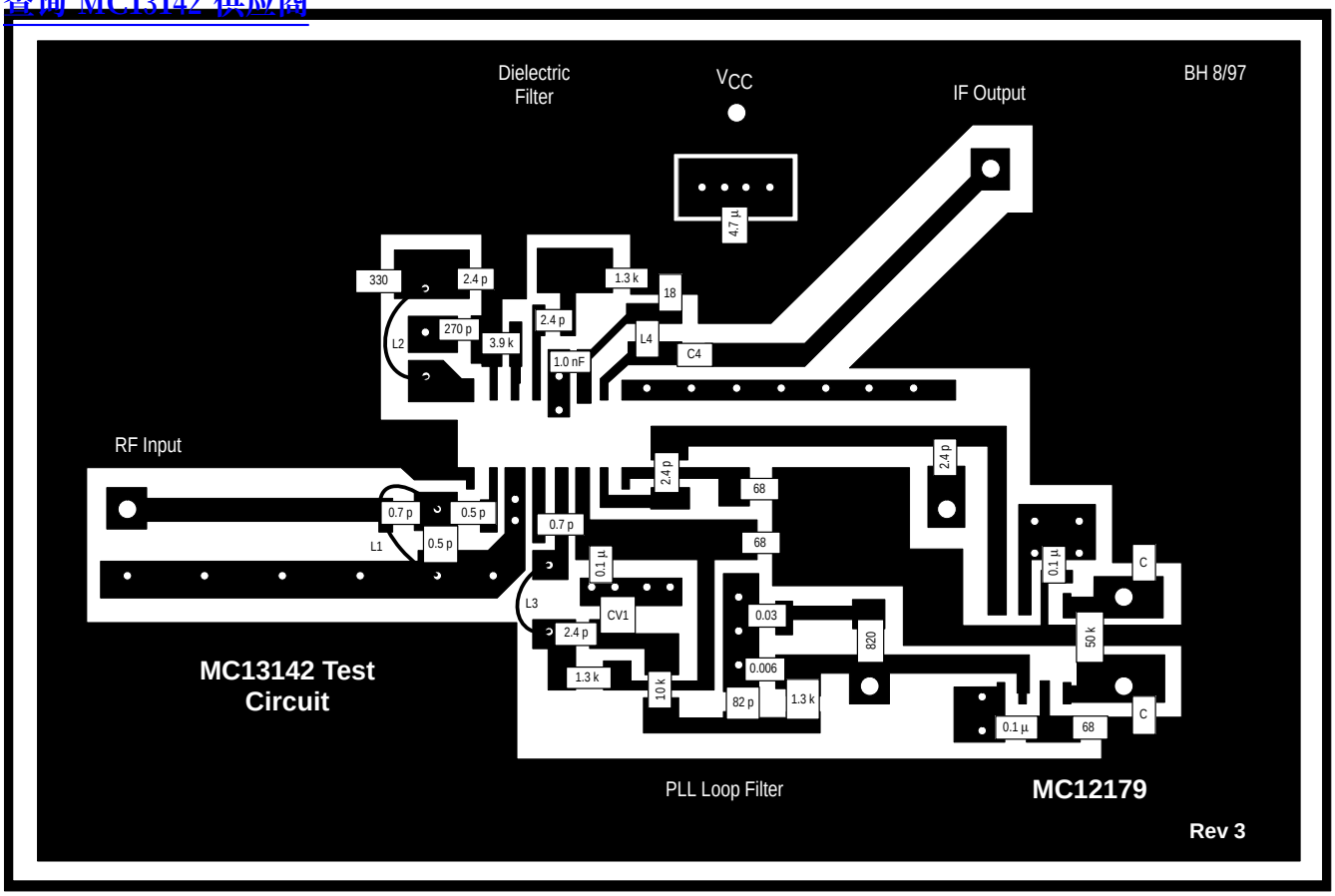
PLL

A phase lock loop is added to the test board to evaluate the VCO. The MC12179 multiplies the crystal reference frequency by 256 to obtain lock. In a frequency agile system, the MC12210 would control the VCO and its reference derived from a crystal. The crystal frequency would be selected to coincide with the required VCO frequencies and channels spacing requirements.

Expected Performance

As stated earlier, the MC13142 performance in any of the systems should mirror the performance obtained in the test fixture. Fixture power gains of 15 dBm and noise figures of 5.5 dB are typical. The Mixer current can be varied to enhances battery life as well as alter its output characteristic for peak performance of a desired or undesired response.

Figure 6. 1.9 GHz Circuit Component Placement View



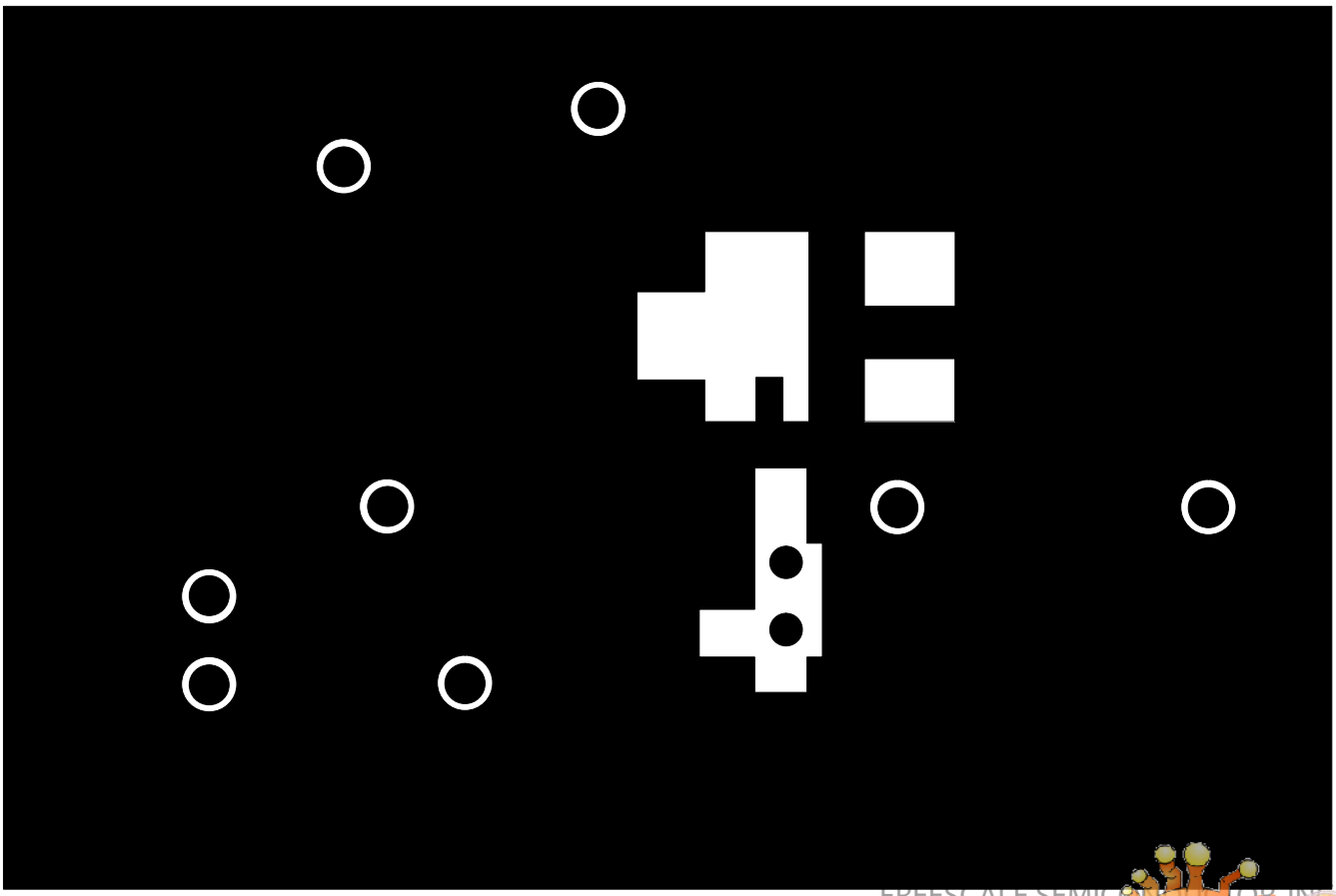
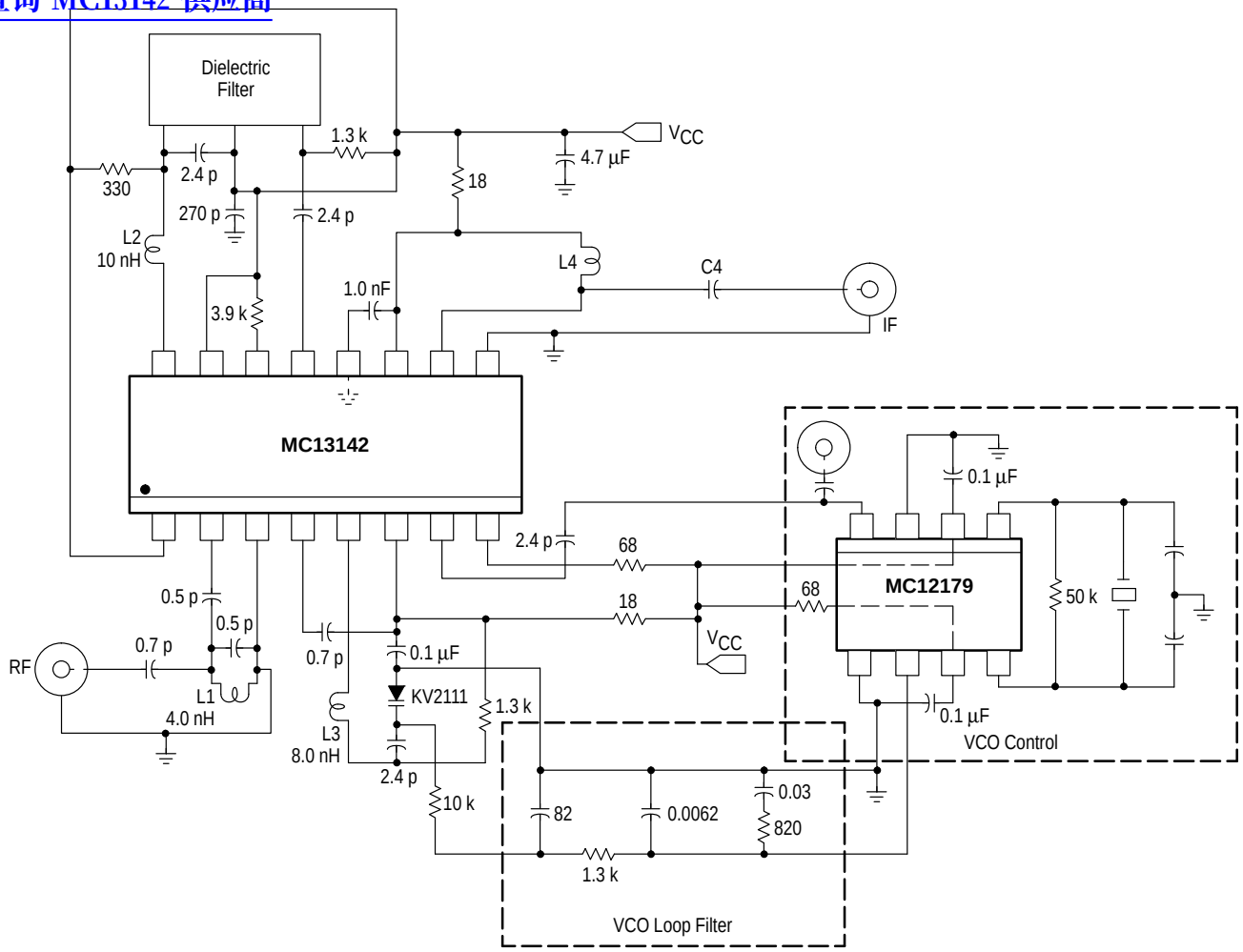
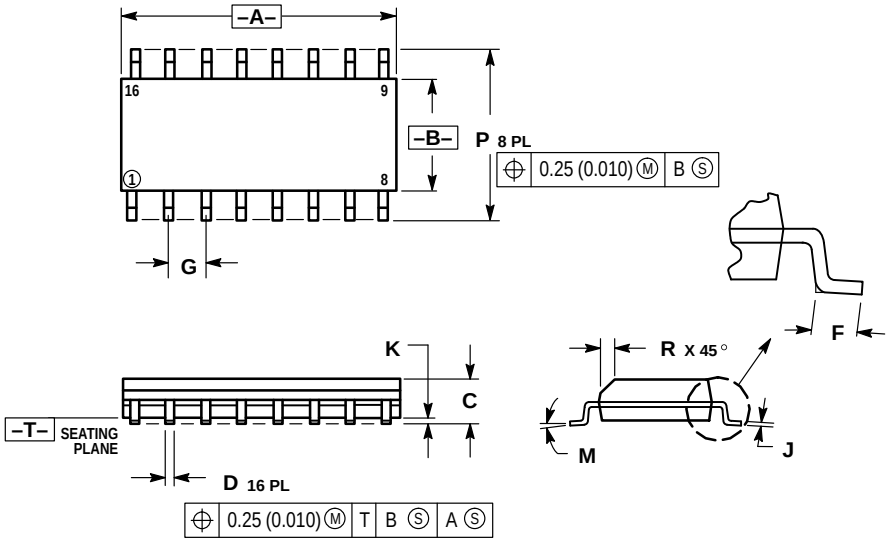


Figure 7. 1.9 GHz Application Circuit



OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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