



# FDB3860

## N-Channel PowerTrench® MOSFET

100 V, 30 A, 37 mΩ

### Features

- Max  $r_{DS(on)}$  = 37 mΩ at  $V_{GS} = 10$  V,  $I_D = 5.9$  A
- High performance trench technology for extremely low  $r_{DS(on)}$
- 100% UIL tested
- RoHS Compliant

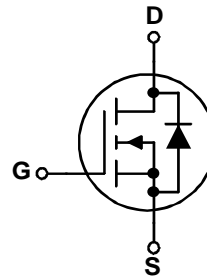
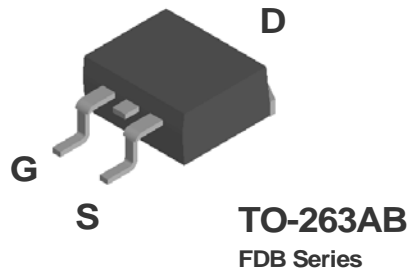


### General Description

This N-Channel MOSFET is rugged gate version of Fairchild Semiconductor's advanced Power Trench® process. This part is tailored for low  $r_{DS(on)}$  and low Qg figure of merit, with avalanche ruggedness for a wide range of switching applications.

### Applications

- DC-AC Conversion
- Synchronous Rectifier



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	30	A
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	6.4	
	-Pulsed	60	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	96	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	71	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.75	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB3860	FDB3860	TO-263AB	330 mm	24 mm	800 units

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## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		104		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2.5	3.8	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-11		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5.9\text{ A}$		31	37	m $\Omega$
		$V_{GS} = 10\text{ V}$ , $I_D = 5.9\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		56	67	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 5.9\text{ A}$		18		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1310	1740	pF
$C_{oss}$	Output Capacitance			100	130	pF
$C_{rss}$	Reverse Transfer Capacitance			40	65	pF
$R_g$	Gate Resistance			1.7		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$ , $I_D = 5.9\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		12	22	ns
$t_r$	Rise Time			6	12	ns
$t_{d(off)}$	Turn-Off Delay Time			17	31	ns
$t_f$	Fall Time			3	10	ns
$Q_g$	Total Gate Charge at $10\text{ V}$			21	30	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 50\text{ V}$ , $I_D = 5.9\text{ A}$		6.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5.4		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.0\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 5.9\text{ A}$ (Note 2)		0.8	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 5.9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		35	56	ns
$Q_{rr}$	Reverse Recovery Charge			37	60	nC

#### Notes:

1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.

- $40\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper
- $62.5\text{ }^\circ\text{C/W}$  when mounted on a minimum pad.

2: Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3: Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 8\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

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**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

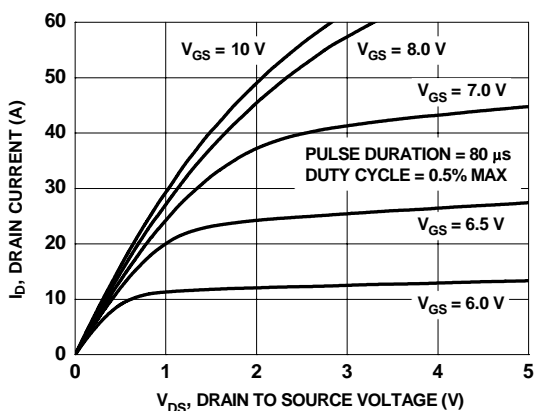


Figure 1. On Region Characteristics

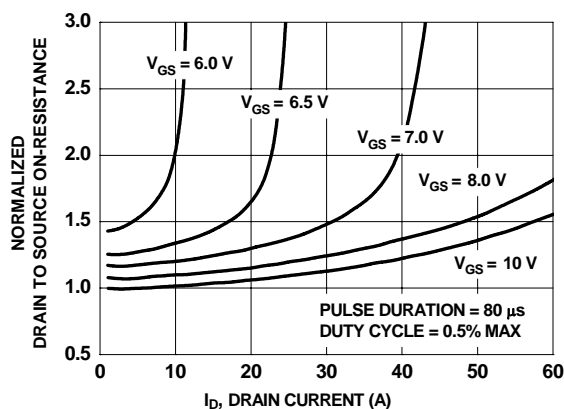


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

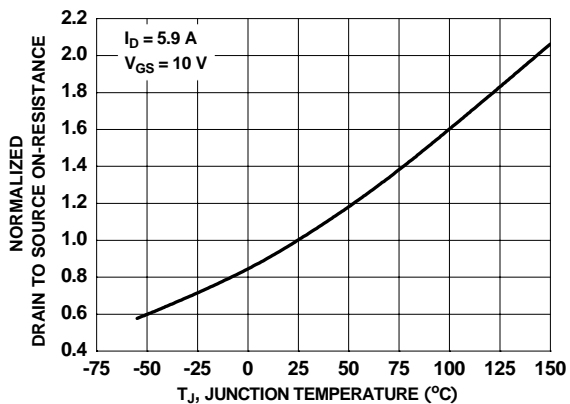


Figure 3. Normalized On Resistance vs Junction Temperature

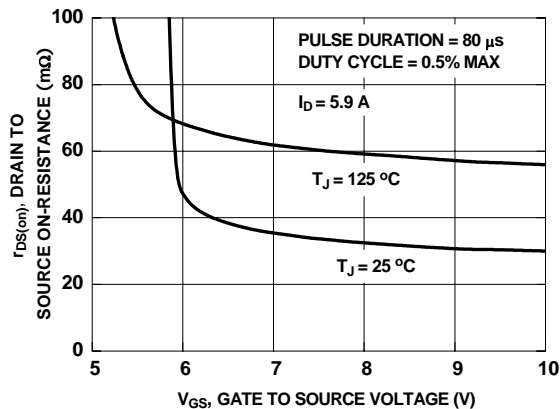


Figure 4. On-Resistance vs Gate to Source Voltage

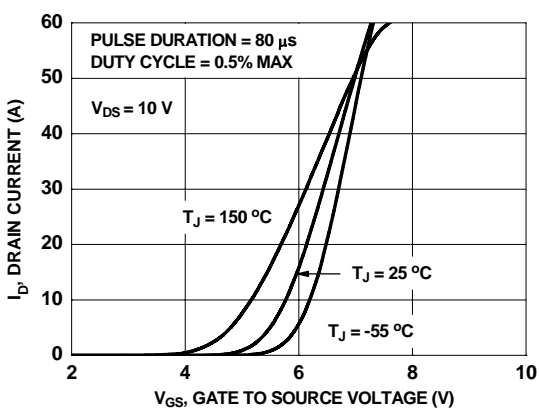


Figure 5. Transfer Characteristics

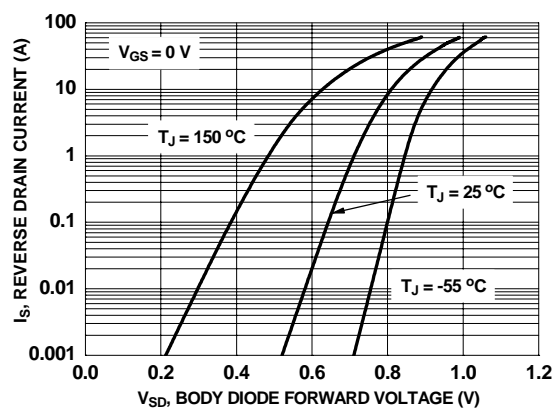
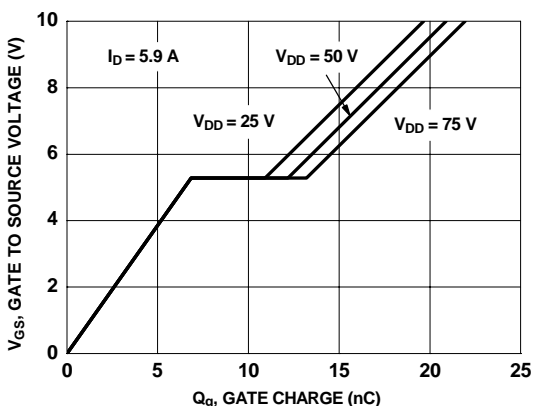


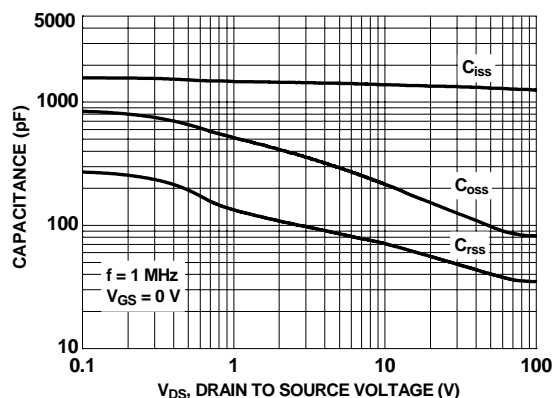
Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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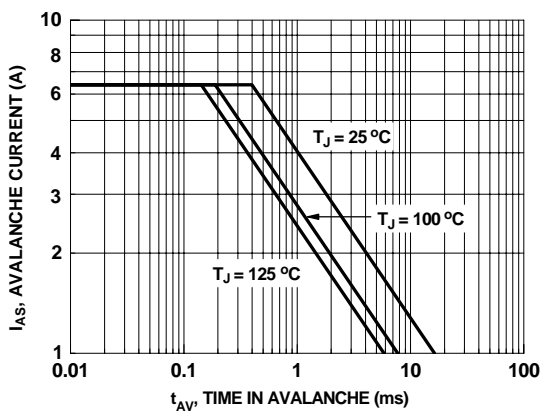
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



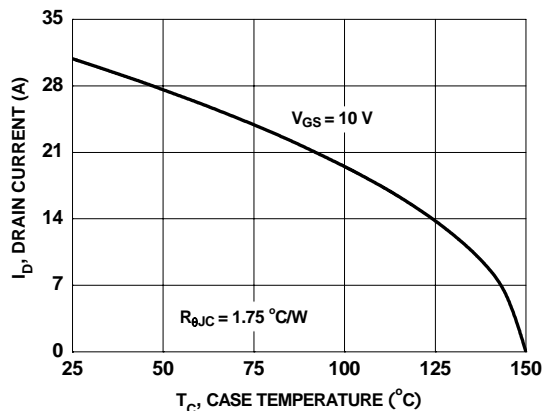
**Figure 7. Gate Charge Characteristics**



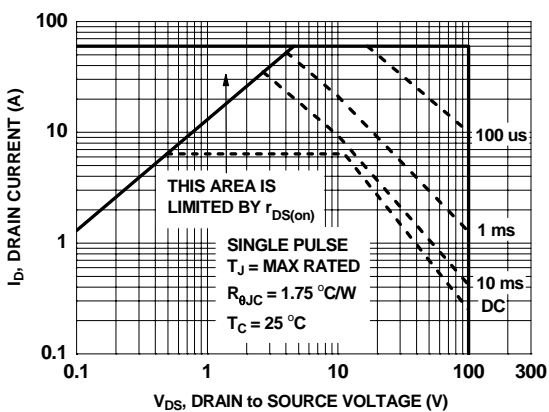
**Figure 8. Capacitance vs Drain to Source Voltage**



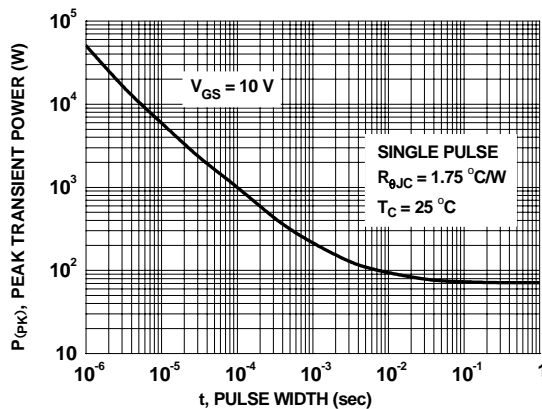
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**



**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

Typical Characteristics  $T_J = 25^\circ\text{C}$  unless otherwise noted

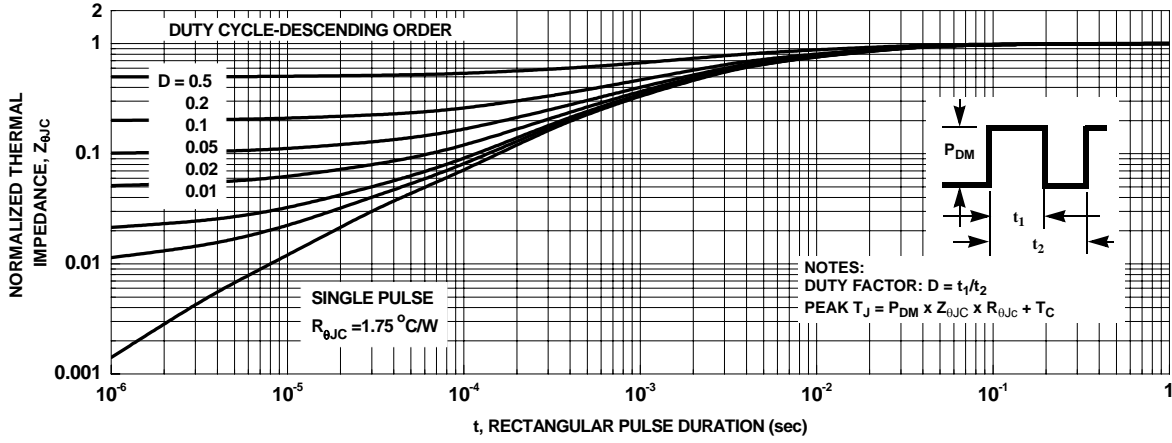


Figure 13. Junction-to-Case Transient Thermal Response Curve

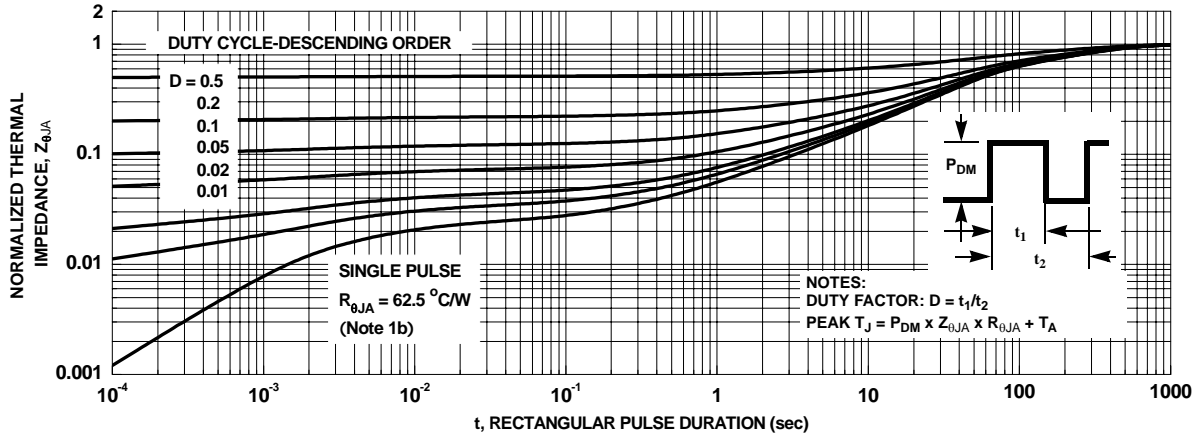


Figure 14. Junction-to-Ambient Transient Thermal Response Curve






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