PRELIMINARY

M28F010
1024K (128K x 8) CMOS FLASH MEMORY

- **Flash Electrical Chip-Erase**
  - **5 Second Typical**
- **Quick-Pulse Programming Algorithm**
  - **10 μs Typical Byte-Program**
  - **2 Second Typical Chip-Program**
- **Single High Voltage for Writing and Erasing**
- **CMOS Low Power Consumption**
  - **30 mA Maximum Active Current**
  - **100 μA Maximum Standby Current**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - **±10% V_{CC} Tolerance**
  - **Maximum Latch-Up Immunity through EPI Processing**
- **ETOX-III Flash-Memory Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**
- **Compatible with JEDEC-Standard Byte-Wide EPROM Pinouts**
- **10,000 Program/Erase Cycles Minimum**
- **Available in Three Product Grades:**
  - **QML: −55°C to +125°C (T_C)**
  - **SE2: −40°C to +125°C (T_C)**
  - **SE3: −40°C to +110°C (T_C)**

Intel's M28F010 is a 1024-Kbit byte-wide, in-system re-writable, CMOS nonvolatile flash memory. It is organized as 131,072 bytes of 8 bits and is available in a 32-pin hermetic CERDIP package. The M28F010 is also available in 32-contact leadless chip carrier, J-lead, and Flatpack surface mount packages. It offers the most cost-effective and reliable alternative for updatable nonvolatile memory. The M28F010 adds electrical chip-erasure and reprogramming to EPROM technology. Memory contents of the M28F010 can be erased and reprogrammed 1) in a socket; 2) in a PROM programmer socket; 3) on-board during subassembly test; 4) in-system during final test; and 5) in-system after-sale.

The M28F010 increases memory flexibility while contributing to time- and cost-savings. It is targeted for alterable code-, data-storage applications where traditional EEPROM functionality (byte erasure) is either not required or is not cost-effective. Use of the M28F010 is also appropriate where EPROM ultraviolet erasure is impractical or too time consuming.

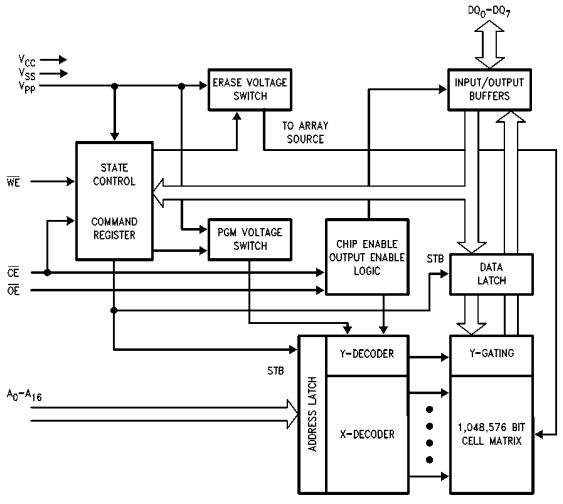


Figure 1. M28F010 Block Diagram

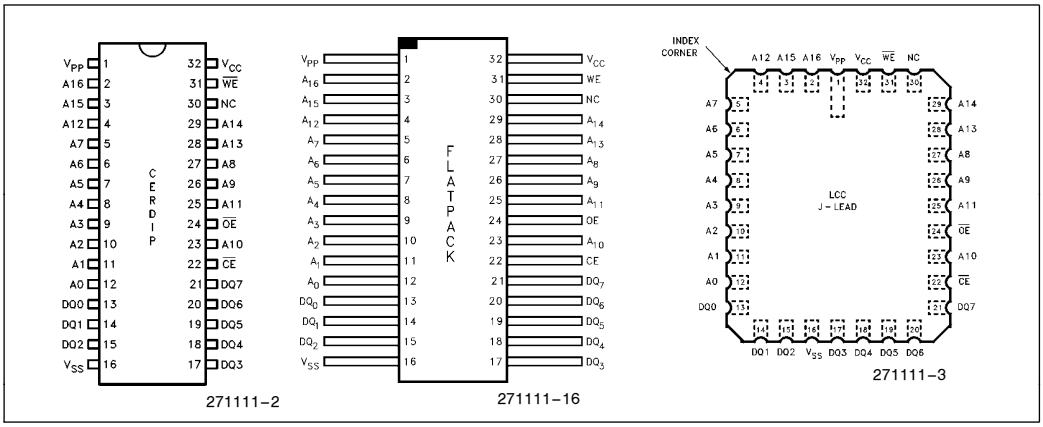


Figure 2. M28F010 Pin Configurations

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{16}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates the devices output through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. **Note:** With $V_{PP} \leq V_{CC} + 2V$, memory contents cannot be altered.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY** (5V ±10%)
V_{SS}		**GROUND**
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.

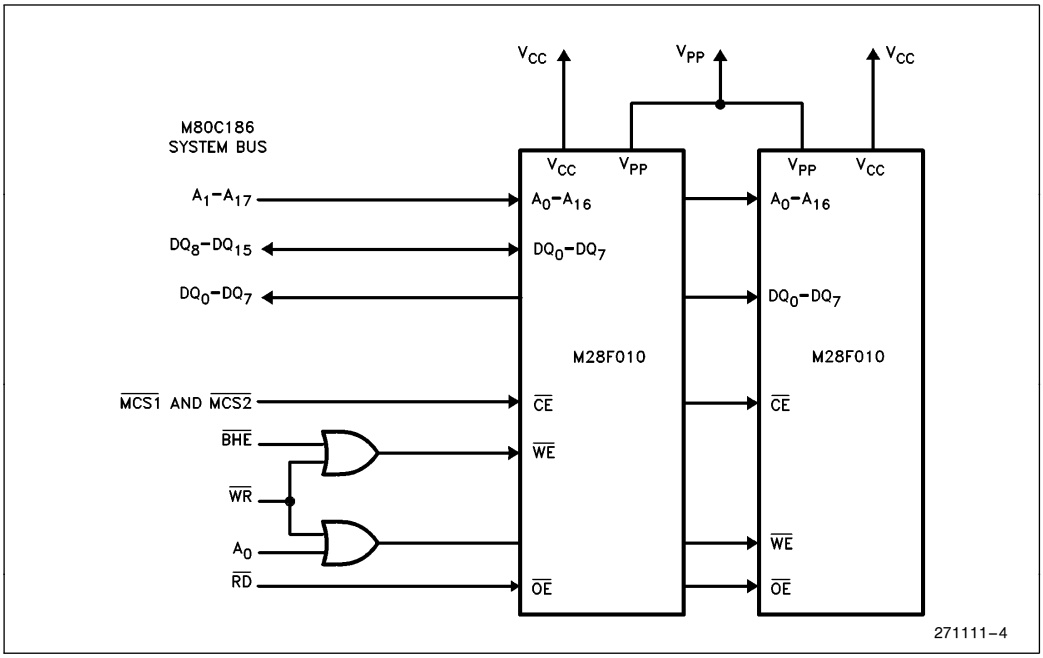


Figure 3. M28F010 in a M80C186 System

PRINCIPLES OF OPERATION

Flash-memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The M28F010 introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supplies during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the M28F010 is a read-only memory. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and intelligent Identifier operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables erasure and programming of the device. All functions associated with altering memory contents—intelligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the intelligent Identifier codes, or output data for erase and program verification.

The command register is only alterable when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When high voltage is removed, the contents of the register default to the read command, making the M28F010 a read-only memory. Memory contents cannot be altered.

Table 2. M28F010 Bus Operations

Operation	Pins	V_{PP}(1)	A_0	A_9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_0–DQ_7
READ-ONLY	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	intelligent Identifier (Mfr)(2)	V_{PPL}	V_{IL}	V_{ID}(7)	V_{IL}	V_{IL}	V_{IH}	Data = 89H
	intelligent Identifier (Device)(2)	V_{PPL}	V_{IH}	V_{ID}(7)	V_{IL}	V_{IL}	V_{IH}	Data = B4H
READ/WRITE	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out(3)
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby(4)	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data In(5)

NOTES:
1. V_{PPL} may be ground, a no-connect with a resistor tied to ground, or as defined in the Characteristics Section. V_{PPH} is the programming voltage specified for the device. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. Read operations with $V_{PP} = V_{PPH}$ may access array data or the intelligent Identifier codes.
4. With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
5. Refer to Table 3 for valid Data-In during a write operation.
6. X can be V_{IL} or V_{IH}.
7. V_{ID} is the intelligent Identifier high voltage. Refer to DC Characteristics.

Or, the system designer may choose to ''hardwire'' V_{PP}, making the high voltage supply constantly available. In this instance, all operations are performed in conjunction with the command register. The M28F010 is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

Integrated Stop Timer

Sucessive command write cycles define the durations of program and erase operations; specifically, the program or erase time durations are normally terminated by associated program or erase verify commands. An integrated stop timer provides simplified timing control over these operations; thus eliminating the need for maximum program/erase timing specifications. Programming and erase pulse durations are minimums only. When the stop timer terminates a program or erase operation, the device enters an inactive state and remains inactive until receiving the appropriate verify or reset command.

Write Protection

The command register is only active when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When $V_{PP} = V_{PPL}$, the contents of the register default to the read command, making the 28F010 a read-only memory. In this mode, the memory contents cannot be altered.

Or, the system designer may choose to ''hardwire'' V_{PP}, making the high voltage supply constantly available. In this case, all Command Register functions are inhibited whenever V_{CC} is below the write lockout voltage V_{LKO}. (See Power Up/Down Protection) The 28F010 is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

BUS OPERATIONS

Read

The M28F010 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable ($\overline{CE}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Figure 6 illustrates read timing waveforms.

When V_{PP} is high (V_{PPH}), the read operation can be used to access array data, to output the intelligent Identifier codes, and to access data for program/erase verification. When V_{PP} is low (V_{PPL}), the read operation can **only** access the array data.

Output Disable

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high-impedance state.

Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the M28F010's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the Output-Enable signal. If the M28F010 is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

intelligent Identifier Operation

The intelligent Identifier operation outputs the manufacturer code (89H) and device code (B4H). Programming equipment automatically matches the device with its proper erase and programming algorithms.

With Chip-Enable and Output-Enable at a logic low level, raising A9 to high voltage V_{ID} activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the M28F010 is erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (B4H).

Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

The three high-order register bits (R7, R6, R5) encode the control functions. All other register bits, R4 to R0, must be zero. The only exception is the reset command, when FFH is written to the register. Register bits R7–R0 correspond to data inputs D7–D0.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these M28F010 register commands.

Table 3. Command Definitions

Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
	Req'd	Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read intelligent Identifier Codes(4)	2	Write	X	90H	Read	IA	ID
Set-up Erase/Erase(5)	2	Write	X	20H	Write	X	20H
Erase Verify(5)	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program(6)	2	Write	X	40H	Write	PA	PD
Program Verify(6)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operations are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. ID = Data read from location IA during device identification (Mfr = 89H, Device = B4H).
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Following the Read int$_e$ligent ID command, two read operations access manufacturer and device codes.
5. Figure 5 illustrates the Quick-Erase Algorithm.
6. Figure 4 illustrates the Quick-Pulse Programming Algorithm.
7. The second bus cycle must be followed by the desired command register write.

Read Command

While V_{PP} is high, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hard-wired to the M28F010, the device powers-up and remains enabled for reads until the command-register contents are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Intelligent Identifier Command

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The M28F010 contains an intelligent Identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of B4H. To terminate the operation, it is necessary to write another valid command into the register.

Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pin. In the absence of this high voltage, memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

The M28F010 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. Figure 5, the Quick-Erase algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the M28F010. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-up Program/Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to AC Program-

ming Characteristics and Waveforms for specific timing parameters.

Program-Verify Command

The M28F010 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

The M28F010 applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 4, the M28F010 Quick-Pulse Programming algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX-II flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure—increasing time to wearout by a factor of 100,000,000.

The device is programmed and erased using Intel's Quick-Pulse Programming and Quick-Erase algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

QUICK-PULSE PROGRAMMING ALGORITHM

The Quick-Pulse Programming algorithm uses programming operations of 10 μs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 4 illustrates the Quick-Pulse Programming algorithm.

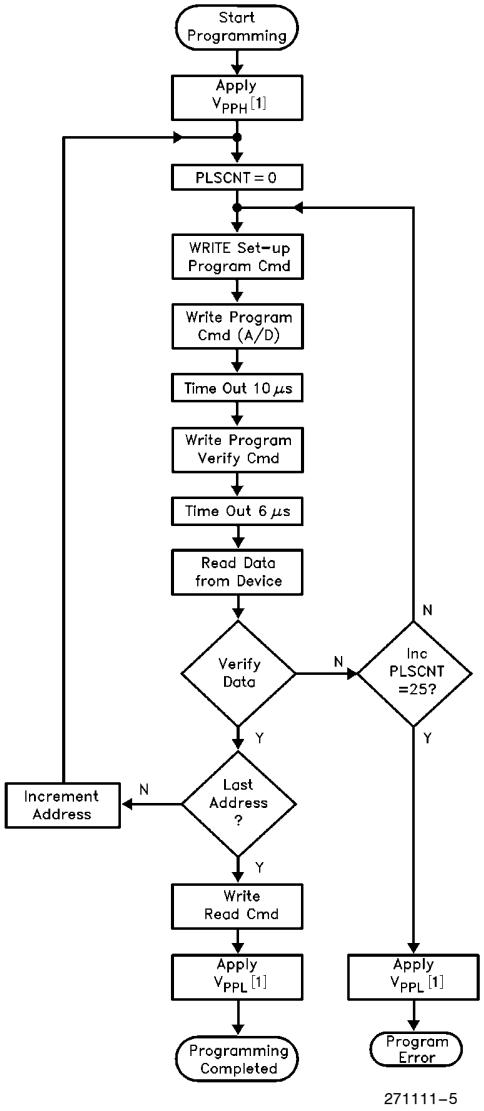
QUICK-ERASE ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The M28F010 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately two seconds.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 5 illustrates the Quick-Erase algorithm.



Bus Operation	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Pulse-Count
Write	Set-up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Program Operation (t_{WHWH1})
Write	Program(2) Verify	Data = C0H; Stops Program Operation
Standby		t_{WHGL}
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

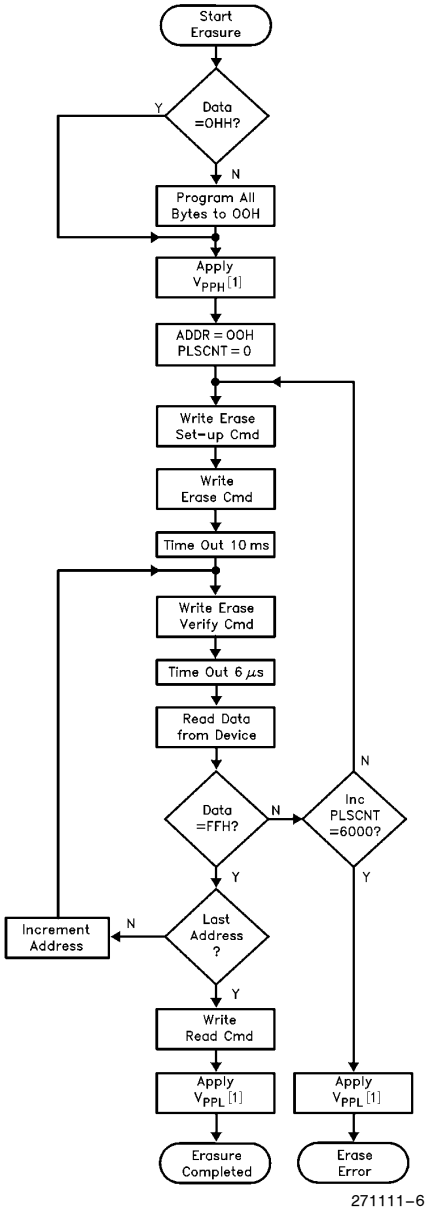
NOTES:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no-connect with a resistor tied to ground, or as defined in Characteristics Section. Refer to Principles of Operation.

2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.

3. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Figure 4. M28F010 Quick-Pulse Programming Algorithm



Bus Operation	Command	Comments
		Entire Memory Must = 00H Before Erasure
		Use Quick-Pulse Programming Algorithm (Figure 4)
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Addresses and Pulse-Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase Verify	Addr = Byte to Verify; Data = A0H; Stops Erase Operation
Standby		t_{WHGL}
Read		Read Byte to Verify Erasure
Standby		Compare Output to FFH Increment Pulse-Count
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

NOTES:
1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no-connect with a resistor tied to ground, or as defined in Characteristics Section. Refer to Principles of Operation.
2. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.
3. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 5. M28F010 Quick-Erase Algorithm

DESIGN CONSIDERATIONS

Two-Line Output Control

Flash-memories are often used in larger memory arrays. Intel provides two read-control inputs to accommodate multiple memory connections. Two-line control provides for:

a. the lowest possible memory power dissipation and,

b. complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address-decoder output should drive chip-enable, while the system's read signal controls all flash-memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

Power Supply Decoupling

Flash-memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the rnagnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection, between V_{CC} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Programming flash-memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

Power Up/Down Protection

The M28F010 is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, the M28F010 is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first Power supply sequencing is not required. Internal circuitry in the M28F010 ensures that the command register is reset to the read mode on power up.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either to V_{IH} will inhibit writes. The control register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

M28F010 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases the usable battery life of your system because the M28F010 does not consume any power to retain code or data when the system is off. Table 4 illustrates the power dissipated when updating the M28F010.

Table 4. M28F010 Typical Update Power Dissipation(4)

Operation	Notes	Power Dissipation (Watt-Seconds)
Array Program/Program Verify	1	0.171
Array Erase/Erase Verify	2	0.136
One Complete Cycle	3	0.478

NOTES:

1. Formula to calculate typical Program/Program Verify Power = [$V_{PP} \times$ # Bytes $\times$ typical # Prog Pulses ($t_{WHWH1} \times I_{PP2}$ typical + $t_{WHGL} \times I_{PP4}$ typical)] + [$V_{CC} \times$ # Bytes $\times$ typical # Prog Pulses ($t_{WHWH1} \times I_{CC2}$ typical + $t_{WHGL} \times I_{CC4}$ typical].
2. Formula to calculate typical Erase/Erase Verify Power = [V_{PP} (V_{PP3} typical $\times$ t_{ERASE} typical + I_{PP5} typical $\times$ $t_{WHGL} \times$ # Bytes)] + [V_{CC} (I_{CC3} typical $\times$ t_{ERASE} typical + I_{CC5} typical $\times$ $t_{WHGL} \times$ # Bytes)].
3. One Complete Cycle = Array Preprogram + Array Erase + Program.
4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias . . . −55°C to +125°C

Storage Temperature . . . . . −65°C to +150°C

Voltage on Any Pin with Respect to Ground . . . . . −2.0V to +7.0V(1)

Voltage on Pin A_9 with Respect to Ground . . . . . −2.0V to +13.5V(1, 2)

V_{PP} Supply Voltage with Respect to Ground During Erase/Program . . . . −2.0V to +14.0V(1, 2)

V_{CC} Supply Voltage with Respect to Ground . . . . . −2.0V to +7.0V(1)

Output Short Circuit Current . . . . . 100 mA(3)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:
1. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
2. Maximum DC voltage on A_9 or V_{PP} may overshoot to +14.0V for periods less than 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units	Comments
V_{PPL}	V_{PP} during Read-Only Operations	0.00	V_{CC} + 2.0V	V	**NOTE:** Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations	11.40	12.60	V	

MIL-STD-883

Symbol	Description	Min	Max	Units
T_C	Operating Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

Extended Temperature

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−40	+110	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

Avionics Grade

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	μA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current		±10	μA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current		1.0	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current		30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current		30	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current		30	mA	Erasure in Progress
I_{PPS}	V_{PP} Leakage Current		±10	μA	$V_{PP} = V_{PPL}$
I_{PP1}	V_{PP} Read Current		200	μA	$V_{PP} = V_{PPH}$ Max
			±10		$V_{PP} = V_{PPL}$
I_{PP2}	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$ Max Programming in Progress
I_{PP3}	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$ Max Erasure in Progress
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage	2.4		V	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifer Voltage	11.50	13.00	V	
I_{ID}	A_9 intelligent Identifier Current		500	μA	$A_9 = V_{ID}$

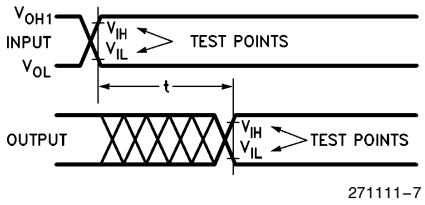
DC CHARACTERISTICS—CMOS COMPATIBLE (Over Specified Operating Conditions)

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	μA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current		±10	μA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current		100	μA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} \pm 0.2V$
I_{CC1}	V_{CC} Active Read Current		30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current		30	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current		30	mA	Erasure in Progress
I_{PPS}	V_{PP} Leakage Current		±10	μA	$V_{PP} = V_{PPL}$
I_{PP1}	V_{PP} Read Current		200	μA	$V_{PP} = V_{PPH}$ Max
			±10		$V_{PP} = V_{PPL}$
I_{PP2}	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$ Max Programming in Progress
I_{PP3}	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$ Max Erasure in Progress
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage	0.85 V_{CC}		V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ Min
V_{OH2}		V_{CC} − 0.4			I_{OH} = −100 μA, $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifer Voltage	11.50	13.00	V	
I_{ID}	A_9 intelligent Identifier Current		500	μA	$A_9 = V_{ID}$

CAPACITANCE T_C = 25°C, f = 1.0 MHz

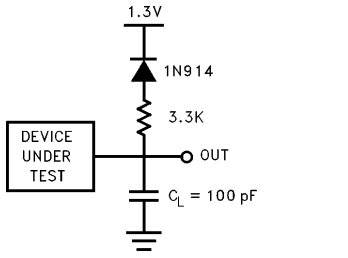
Symbol	Parameter	Limits		Unit	Conditions
		Min	Max		
C_{IN}	Address/Control Capacitance		6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

AC TESTING INPUT/OUTPUT WAVEFORM



AC Testing: Inputs are driven at V_{OH1} for a logic "1" and V_{OL} for a logic "0". Testing measurements are made at V_{IH} for a logic "1" and V_{IL} for a logic "0". Rise/Fall time ≤ 10 ns.

AC LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

AC TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns
Input Pulse Levels . . . . . V_{OL} and V_{OH1}
Input Timing Reference Level . . . . . V_{IL} and V_{IH}
Output Timing Reference Level . . . . . V_{IL} and V_{IH}

AC CHARACTERISTICS—Read-Only Operations

Versions		M28F010-90		M28F010-12		M28F010-15		M28F010-20		M28F010-25		Unit
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{AVAV}/t_{RC}	Read Cycle Time	90		120		150		200		250		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time		90		120		150		200		250	ns
t_{AVQV}/t_{ACC}	Address Access Time		90		120		150		200		250	ns
t_{GLQV}/t_{OE}	Output Enable Access Time		40		50		55		60		65	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	0		0		0		0		0		ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	0		0		0		0		0		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z		30		30		35		45		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change(1)	0		0		0		0		0		ns
t_{WHGL}	Write Recovery Time before Read	6		6		6		6		6		μs

NOTE:
1. Whichever occurs first.

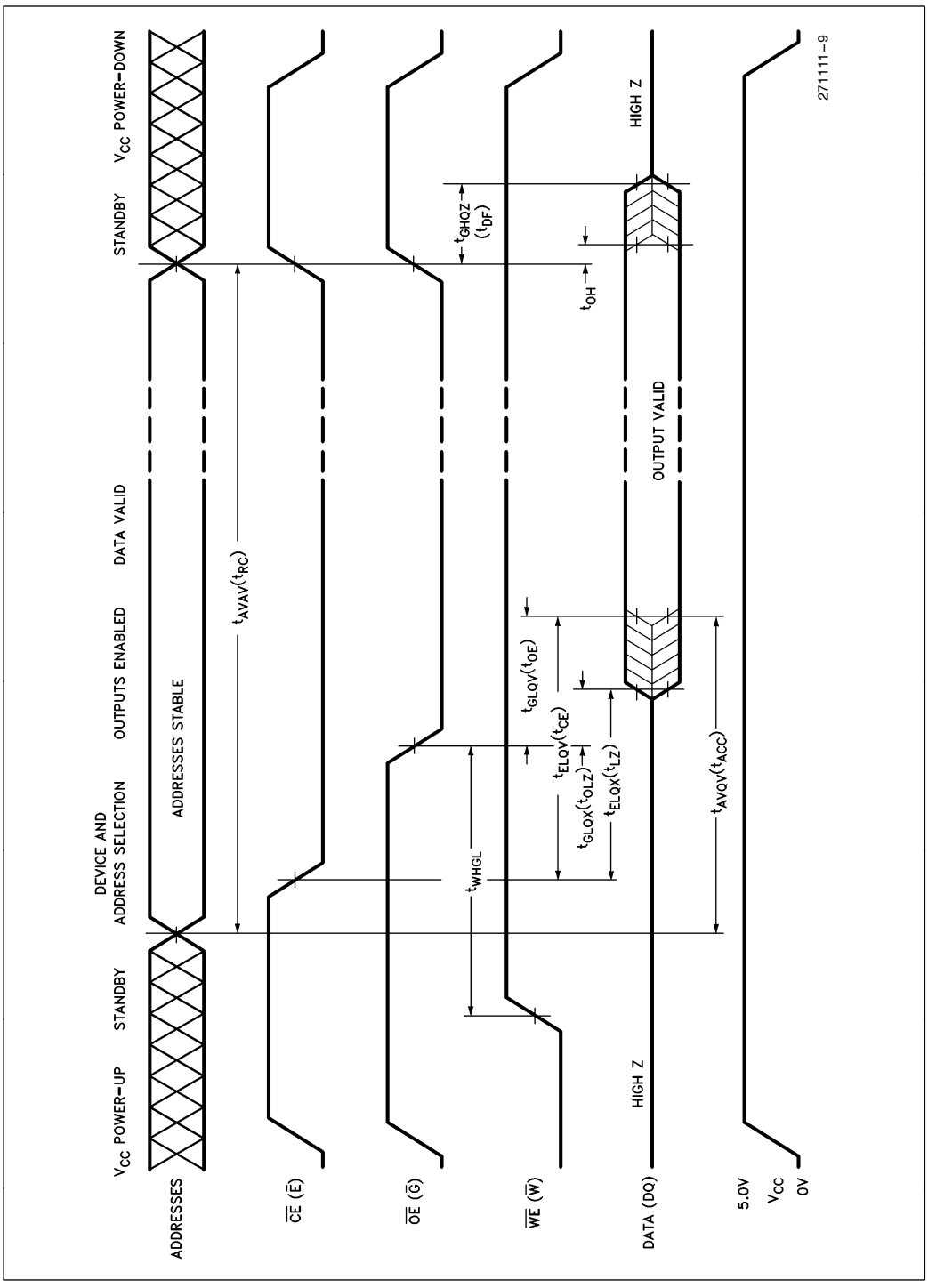


Figure 6. AC Waveforms for Read Operations

AC CHARACTERISTICS—Write/Erase/Program Operations[1,2]

Versions		M28F010-90		M28F010-12		M28F010-15		M28F010-20		M28F010-25		Unit
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{AVAV}/t_{WC}	Write Cycle Time	90		120		150		200		250		ns
t_{AVWL}/t_{AS}	Address Set-Up Time	0		0		0		0		0		ns
t_{WLAX}/t_{AH}	Address Hold Time			60		60		60		90		ns
t_{DVWH}/t_{DS}	Data Set-up Time	50		50		50		50		50		ns
t_{WHDX}/t_{DH}	Data Hold Time	10		10		10		10		10		ns
t_{WHGL}	Write Recovery Time before Read	6		6		6		6		6		µs
t_{GHWL}	Read Recovery Time before Write	0		0		0		0		0		µs
t_{ELWL}/t_{CS}	Chip Enable Set-Up Time before Write	20		20		20		20		20		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time	0		0		0		0		0		ns
t_{WLWH}/t_{WP}	Write Pulse Width	80		80		80		80		80		ns
t_{ELEH}	Alternative Write Pulse Width	80		80		80		80		80		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High	20		20		20		20		20		ns
t_{WHWH1}	Duration of Programming Operation	10	25	10	25	10	25	10	25	10	25	µs
t_{WHWH2}	Duration of Erase Operation	9.5	10.5	9.5	10.5	9.5	10.5	9.5	10.5	9.5	10.5	ms
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low	100		100		100		100		100		ns

NOTES:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the write pulse width (within a longer Write-Enable timing waveform) all set-up, hold, and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Chip Erase Time		5(1)	30	Sec	Excludes 00H Programming Prior to Erasure
Chip Program Time		2(1)	24(2)	Sec	Excludes System-Level Overhead
Erase/Program Cycles	10,000	100,000		Cycles	

NOTES:
1. 25°C, 12.0V V_{PP}, 10,000 Cycles.
2. Minimum byte programming time excluding system overhead is 16 μsec (10 μsec program + 6 μsec write recovery), while maximum is 400 μsec/byte (16 μsec x 25 loops allowed by algorithm). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.

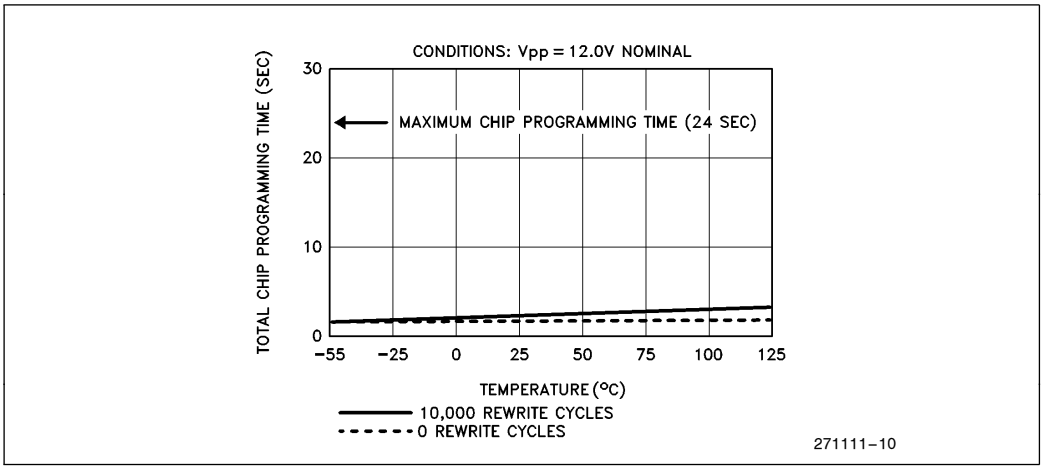


Figure 7. M28F010 Typical Programming Time vs. Temperature

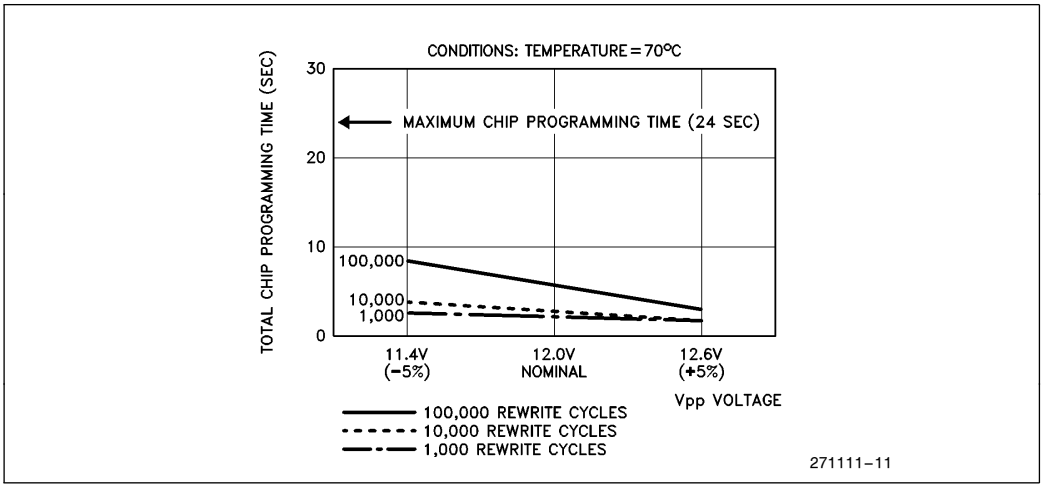


Figure 8. M28F010 Typical Programming Time vs. V_{PP} Voltage

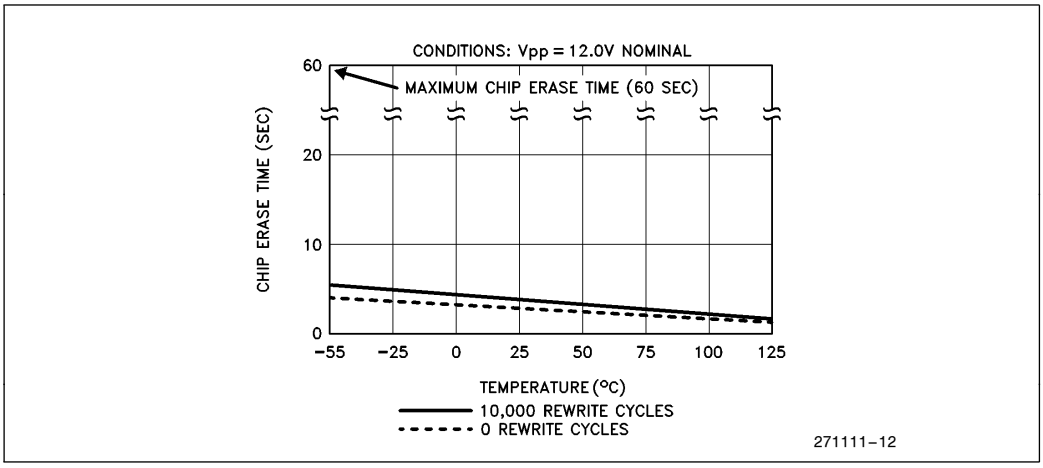


Figure 9. M28F010 Typical Erase Time vs. Temperature

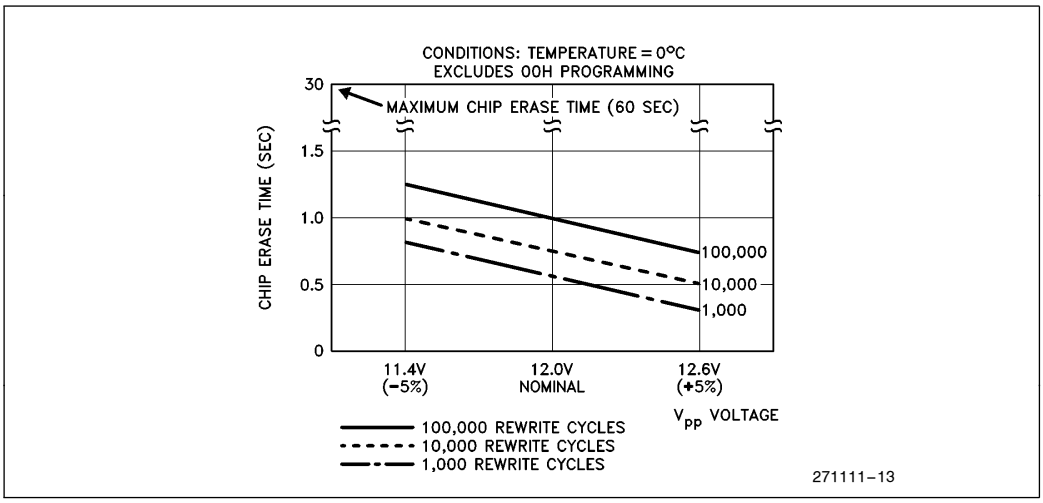


Figure 10. M28F010 Typical Erase Time vs. V_{PP} Voltage

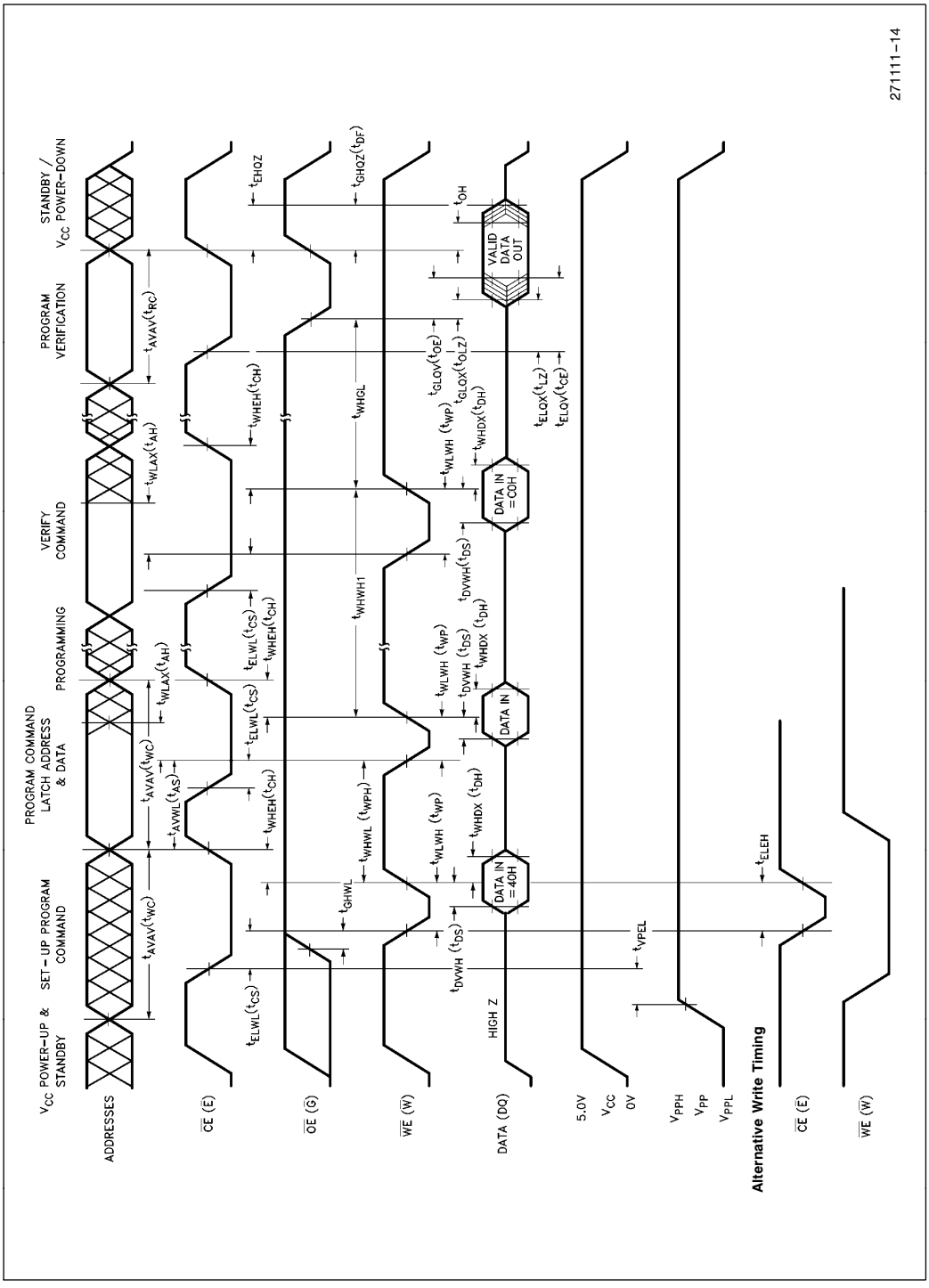


Figure 11. AC Waveforms for Programming Operations

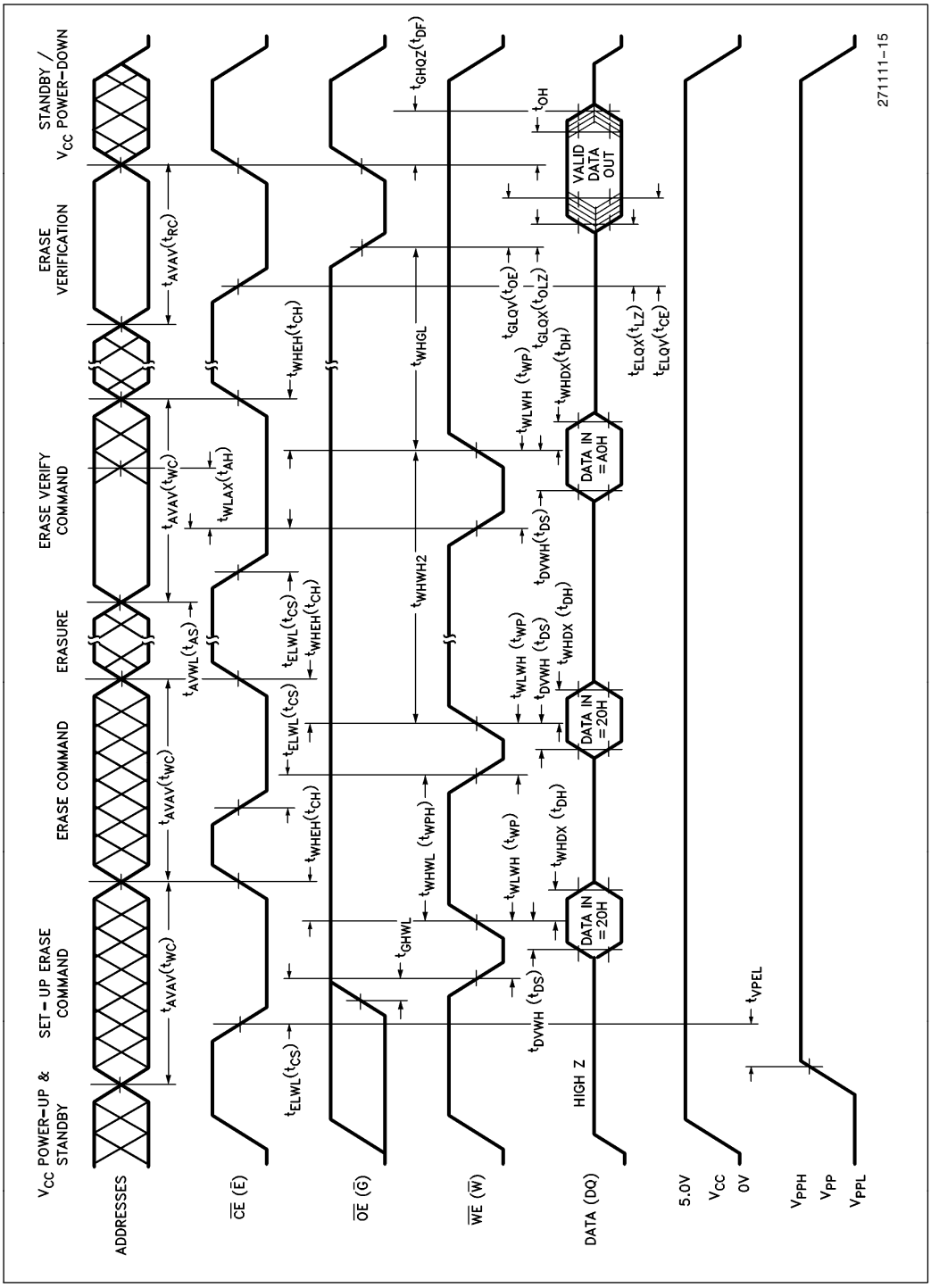


Figure 12. AC Waveforms for Erase Operations

ADDITIONAL INFORMATION

	Order Number
ER-20, ''ETOX II Flash Memory Technology	294005
ER-24, ''The Intel 28F010 Flash Memory''	294008
RR-60, ''ETOX II Flash Memory Reliability Data Summary''	293002
AP-316, ''Using Flash Memory for In-System Reprogrammable Nonvolatile Storage''	292046
AP-325, ''Guide to Flash Memory Reprogramming''	292059