71M6533/H and 71M6534/H Energy Meter IC

Simplifying System Integration™

DATA SHEET

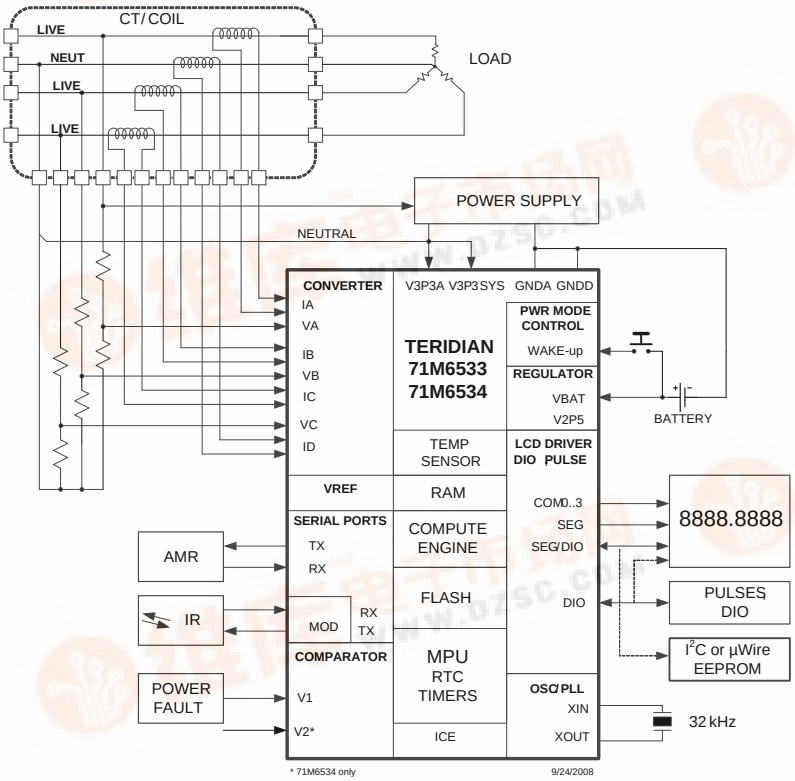
November 2009

GENERAL DESCRIPTION

The 71M6533 and 71M6534 are Teridian's 3rd-generation poly-phase metering SOCs with a 10MHz 8051-compatible MPU core, low-power RTC, FLASH and LCD driver. Teridian's patented Single Converter Technology® with a 22-bit delta-sigma ADC, seven analog inputs, digital temperature compensation, precision voltage reference and a 32-bit computation engine (CE) supports a wide range of metering applications with very few external components.

The 71M6533 and 71M6534 add several new features to Teridian's flagship 71M6513 poly-phase meters including an SPI interface, advanced power management with <1 µA sleep current, 4 KB shared RAM and 128 KB (71M6533/H, 71M6534) or 256 KB (71M6534H) Flash which may be programmed in the field with new code and/or data during meter operation. Higher processing and sampling rates and larger memory offer a powerful metering platform for commercial and industrial meters with up to class 0.2 accuracy.

A complete array of ICE and development tools, programming libraries and reference designs enable rapid development and certification of meters that meet all ANSI & IEC electricity metering standards worldwide.



FEATURES

- Accuracy < 0.1% over 2000:1 range
- Exceeds IEC62053 / ANSI C12.20 standards
- Seven sensor inputs with neutral current measurement
- Low-jitter Wh and VARh plus two additional pulse test outputs (4 total, 10 kHz maximum) with pulse count
- Four-quadrant metering
- Phase sequencing
- Line frequency count for RTC
- Digital temperature compensation
- Independent 32-bit compute engine
- 46-64 Hz line frequency range with same calibration. Phase compensation (± 7°)
- Three battery back-up modes with wake-up on timer or push-button:
  - Brownout mode (82 µA typ., 71M6533)
  - LCD mode (21 µA typ., DAC active)
  - Sleep mode (0.7 µA typ.)
- Energy display during mains power failure
- 39 mW typical consumption @ 3.3 V, MPU clock frequency 614 kHz
- 8-bit MPU (80515), 1 clock cycle per instruction, 10 MHz maximum, with integrated ICE for debug
- LCD driver with 4 common segment drivers:
  - Up to 228 (71M6533) or 300 (71M6534) pixels
- 4 dedicated plus 35 (71M6533) or 48 (71M6534) multi-function DIO pins
- RTC for TOU functions with clock-rate adjust register
- Hardware watchdog timer, power fail monitor
- I2C/Microwire EEPROM Interface
- High-speed slave SPI interface to data RAM
- Two UARTs for IR and AMR, IR driver with modulation
- Flash memory with security and in-system program update:
  - 128 KB (71M6533/H, 71M6534)
  - 256 KB (71M6534H)
- 4 KB RAM
- Industrial temperature range
- 100-pin (71M6533/H) or 120-pin (71M6534/H) lead free LQFP package

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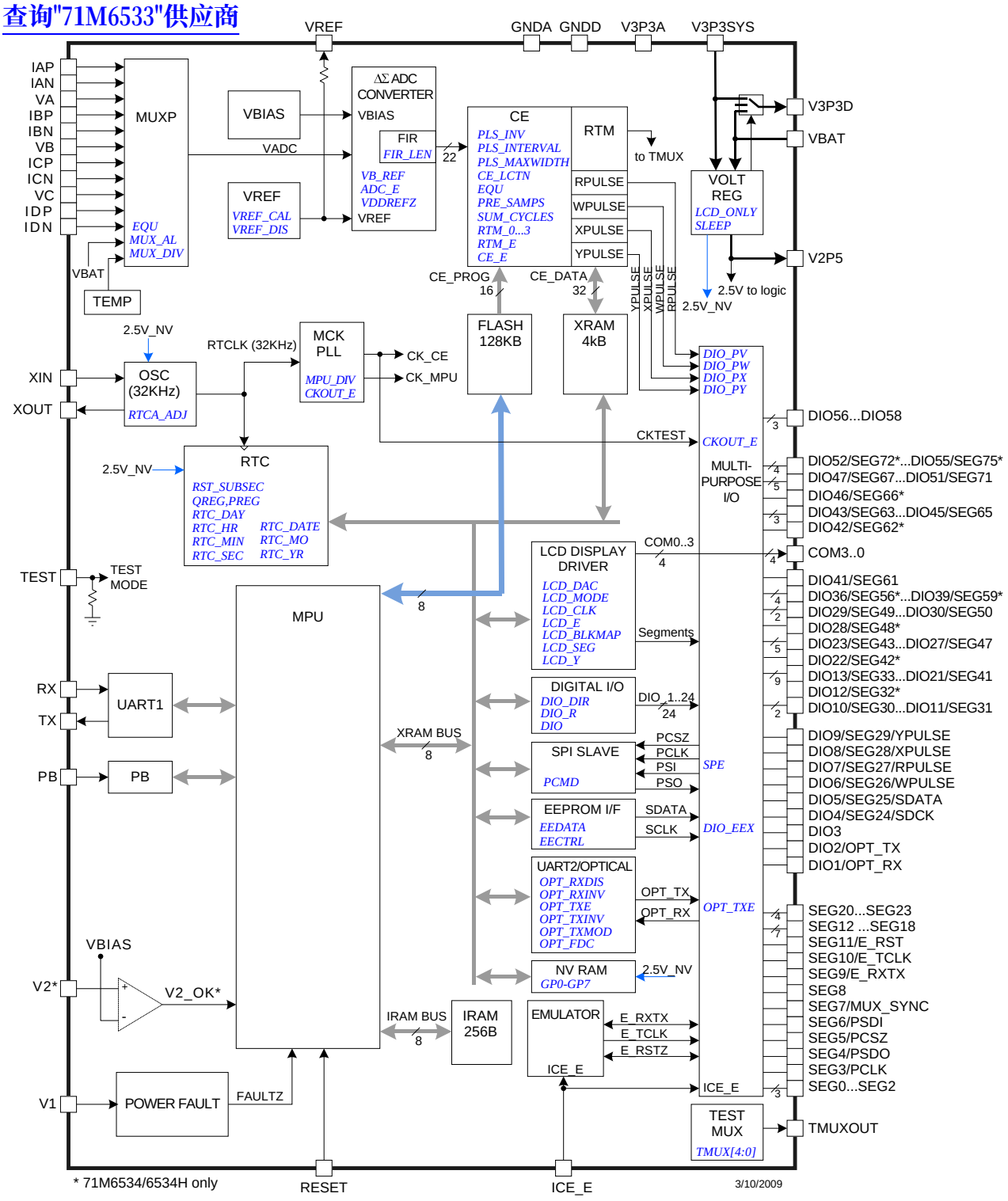


Figure 1: IC Functional Block Diagram

1 Hardware Description

1.1 Hardware Overview

The Teridian 71M6533 and 71M6534 single-chip energy meter integrate all primary functional blocks required to implement a solid-state electricity meter. Included on the chip are:

- An analog front end (AFE)
- An Independent digital computation engine (CE)
- An 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515)
- A voltage reference
- A temperature sensor
- LCD drivers
- RAM and Flash memory
- A real time clock (RTC)
- A variety of I/O pins

Various current sensor technologies are supported including Current Transformers (CT), Resistive Shunts and Rogowski coils.

In a typical application, the 32-bit compute engine (CE) of the 71M6533/71M6534 sequentially processes the samples from the voltage inputs on analog input pins and performs calculations to measure active energy (Wh) and reactive energy (VARh), as well as A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

In addition to advanced measurement functions, the real time clock function allows the 71M6533/71M6534 to record time of use (TOU) metering information for multi-rate applications and to time-stamp tamper events. Measurements can be displayed on 3.3 V LCDs commonly used in low-temperature environments. Flexible mapping of LCD display segments facilitate integration of existing custom LCDs. Design trade-off between the number of LCD segments and DIO pins can be implemented in software to accommodate various requirements.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement and RTC accuracy, e.g. to meet the requirements of ANSI and IEC standards. Temperature dependent external components such as a crystal oscillator, current transformers (CTs) and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

One of the two internal UARTs is adapted to support an Infrared LED with internal drive and sense configuration and can also function as a standard UART. The optical output can be modulated at 38 kHz. This flexibility makes it possible to implement AMR meters with an IR interface. A block diagram of the IC is shown in Figure 1.

1.2 Analog Front End (AFE)

The AFE of the 71M6533/71M6534 consists of an input multiplexer, a delta-sigma A/D converter and a voltage reference.

1.2.1 Signal Input Pins

All analog signal input pins are sensitive to voltage. The VA, VB, and VC pins are single-ended. Pins IAP/IAN, IBP/IBN, ICP/ICN, and IDP/IDN can be programmed individually to be differential or single-ended. The differential signal is applied between the InP and InN input pins. Single-ended signals are applied to the InP input while the common signal, return, is the V3P3A pin. When using the differential mode, inputs can be chopped, i.e. a connection from V3P3A to InP or InN alternates in each multiplexer cycle.

1.2.2 Input Multiplexer

The input multiplexer applies the input signals from the pins IAP/IAN, VA, IBP/IBN, VB, ICP/ICN, VC, and IDP/IDN to the input of the ADC. Additionally, using the alternate multiplexer selection, it has the ability to select temperature and the battery voltage. One input is applied per time slot.

The multiplexer can implement from one to 10 time slots (states) per frame as controlled by the I/O RAM register *MUX_DIV*. The multiplexer always starts at state 1 and proceeds until as many states as defined by *MUX_DIV* have been converted.

The multiplexer can be operated in two modes:

- During a normal multiplexer cycle (*MUX_ALT* = 0), the signals selected in the *SLOTn_SEL* registers (I/O RAM) are processed. These are typically the signals from the IA, IB, IC, ID and VA, VB, and VC pins.
- During the alternate multiplexer cycle (*MUX_ALT* = 1), the signals selected in the *SLOTn_SEL* registers (I/O RAM) are processed. These signals typically comprise the temperature signal (TEMP), the battery monitor (VBAT) and some of the voltage signals such as VA, VB, and VC. To prevent unnecessary drainage on the battery, the battery monitor is enabled only with the BME bit (0x2020[6]) in the I/O RAM.

The alternate multiplexer cycles are usually performed infrequently (every second or so) by the MPU. In order to prevent disruption of the voltage tracking mechanism and voltage allpass networks of the CE, VA, VB, and VC are not replaced in the alternate cycles.

The current inputs can be configured to be used in differential mode, using the pin pairs IAP/IAN, IBP/IBN, ICP/ICN, and IDP/IDN. The fourth current input is available to support measurement of a fourth or neutral phase.

In a typical application, IAP/IAN, IBP/IBN, ICP/ICN, and IDP/IDN are connected to current transformers that sense the current on each phase of the line voltage. VA, VB, and VC are typically connected to the phase voltages via resistor dividers.

Multiplexer advance, FIR initiation and VREF chopping are controlled by the internal MUX_CTRL signal. Additionally, MUX_CTRL launches each pass through the CE program. Conceptually, MUX_CTRL is clocked by CK32, the 32768Hz clock from the PLL block. The behavior of MUX_CTRL is governed by *MUX_ALT*, *EQU*, *CHOP_E*, and *MUX_DIV*.

The *MUX_ALT* bit requests an alternative multiplexer frame. The bit may be asserted on any MPU cycle and may be subsequently deasserted on any cycle including the next one. A rising edge on MUX_ALT will cause MUX_CTRL to wait until the next multiplexer frame and implement a single alternate multiplexer frame.

The inputs converted during normal and alternate frames are selectable using the pointers to signals. *SLOTn_SEL* selects the input signal for the nth state in a standard multiplexer frame, while *SLOTn_ALTSEL* selects the input for the nth state in an alternate multiplexer frame. For example, if *SLOT0_SEL* contains 0 and *SLOT1_SEL* contains 1, signal selection 0, equivalent to IA (see Table 1), will be applied for the first time slot, while signal 1, equivalent to VA, will be applied for the second time slot. See Table 1 for a typi-

cal assignment of values for the *SLOTn_SEL* and *SLOTn_ALTSEL* registers assuming seven time slots (*MUX_DIV* = 7) for the processing of three voltage and current phases plus an additional neutral current.

The correlation between signal numbers, CE memory addresses, and analog signals is given in Table 3.

For the processing of three voltage and current phases in a typical poly-phase meter without neutral measurement, *MUX_DIV* is set to 6, and *SLOT6_SEL* as well as *SLOT6_ALTSEL* would be empty.

Table 1: Signals Selected for the ADC with *SLOTn_SEL* and *SLOTn_ALTSEL* (*MUX_DIV* = 7)

Time Slot	Regular Slot			Alternate Slot		
	Register	Typical Selections		Register	Typical Selections	
		Signal Number	Signal for ADC		Signal Number	Signal for ADC
0	*SLOT0_SEL*	0	IA	*SLOT0_ALTSEL*	A	**TEMP**
1	*SLOT1_SEL*	1	VA	*SLOT1_ALTSEL*	1	VA
2	*SLOT2_SEL*	2	IB	*SLOT2_ALTSEL*	B	**VBAT**
3	*SLOT3_SEL*	3	VB	*SLOT3_ALTSEL*	3	VB
4	*SLOT4_SEL*	4	IC	*SLOT4_ALTSEL*	4	IC
5	*SLOT5_SEL*	5	VC	*SLOT5_ALTSEL*	5	VC
6	*SLOT6_SEL*	6	ID	*SLOT6_ALTSEL*	6	ID
	SLOT7_SEL	–	–	*SLOT7_ALTSEL*		
	SLOT8_SEL	–	–	*SLOT8_ALTSEL*		
	SLOT9_SEL	–	–	*SLOT9_ALTSEL*		

The duration of each multiplexer state depends on the number of ADC samples processed by the FIR, which is set by *FIR_LEN*. Each multiplexer state will start on the rising edge of CK32. FIR conversions require 1, 2, or 3 CK32 cycles. The number of CK32 cycles is determined by *FIR_LEN*.

1.2.3 A/D Converter (ADC)

A single delta-sigma A/D converter digitizes the voltage and current inputs to the 71M6533/71M6534. The resolution of the ADC is programmable using the I/O RAM registers *M40MHZ* and *M26MHZ* (see Table 2).

Table 2: ADC Resolution

Setting for [*M40MHZ, M26MHZ*]	*FIR_LEN*	FIR CE Cycles	Resolution
[00], [10] or [11]	0	138	18 bits
	1	288	21 bits
	2	384	22 bits
[01]	0	186	19 bits
	1	384	22 bits
	2	588	24 bits

Initiation of each ADC conversion is controlled by MUX_CTRL as described above. At the end of each ADC conversion, the FIR filter output data is stored into the CE RAM location determined by the MUX selection.

1.2.4 FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the fixed CE RAM location determined by the multiplexer selection as shown in Table 3. FIR data is stored LSB justified, but shifted left by eight bits.

Table 3: ADC RAM Locations

Signal Number	Address (HEX)	Name
0	0x00	IA
1	0x01	VA
2	0x02	IB
3	0x03	VB
4	0x04	IC
5	0x05	VC
6	0x06	ID
0x0A	0x0A	TEMP
0x0B	0x0B	VBAT

1.2.5 Voltage References

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques. The reference of the 71M6533H/71M6534H is trimmed in production to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient.

The amplifier within the reference is chopper stabilized, i.e. the polarity can be switched by the MPU using the I/O RAM register *CHOP_E* (0x2002[5:4]). The two bits in the *CHOP_E* register enable the MPU to operate the chopper circuit in regular or inverted operation, or in toggling mode. When the chopper circuit is toggled in between multiplexer cycles, DC offsets on the measured signals will automatically be averaged out.

The general topology of a chopped amplifier is shown in Figure 2.

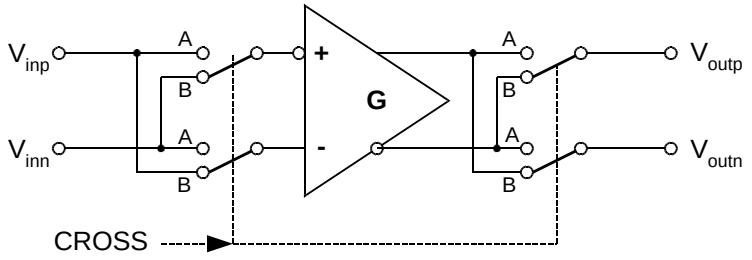


Figure 2: General Topology of a Chopped Amplifier

It is assumed that an offset voltage Voff appears at the positive amplifier input. With all switches, as controlled by CROSS, in the A position, the output voltage is:

Voutp – Voutn = G (Vinp + Voff – Vinn) = G (Vinp – Vinn) + G Voff

With all switches set to the B position by applying the inverted CROSS signal, the output voltage is:

Voutn – Voutp = G (Vinn – Vinp + Voff) = G (Vinn – Vinp) + G Voff, or

Voutp – Voutn = G (Vinp – Vinn) - G Voff

Thus, when CROSS is toggled, e.g. after each multiplexer cycle, the offset will alternately appear on the output as positive and negative, which results in the offset effectively being eliminated, regardless of its polarity or magnitude.

When CROSS is high, the connection of the amplifier input devices is reversed. This preserves the overall polarity of that amplifier gain; it inverts its input offset. By alternately reversing the connection, the amplifier's offset is averaged to zero. This removes the most significant long-term drift mechanism in the

voltage reference. The *CHOP_E* bits control the behavior of CROSS. The CROSS signal will reverse the amplifier connection in the voltage reference in order to negate the effects of its offset. On the first CK32 rising edge after the last multiplexer state of its sequence, the multiplexer will wait one additional CK32 cycle before beginning a new frame. At the beginning of this cycle, the value of CROSS will be updated according to the *CHOP_E* bits. The extra CK32 cycle allows time for the chopped VREF to settle. During this cycle, MUXSYNC is held high. The leading edge of MUXSYNC initiates a pass through the CE program sequence. The beginning of the sequence is the serial readout of the four RTM words.

CHOP_E has four states: positive, reverse, and two toggle states. In the positive state, *CHOP_E* = 01, CROSS and CHOP_CLK are held low. In the reverse state, *CHOP_E* = 10, CROSS and CHOP_CLK are held high. In the first toggle state, *CHOP_E* = 00, CROSS is automatically toggled near the end of each multiplexer frame and an ALT frame is forced during the last multiplexer frame in each SUM cycle. It is desirable that CROSS take on alternate values during each ALT frame. For this reason, if *CHOP_E* = 00, CROSS will not toggle at the end of the multiplexer frame immediately preceding the ALT frame in each accumulation interval.

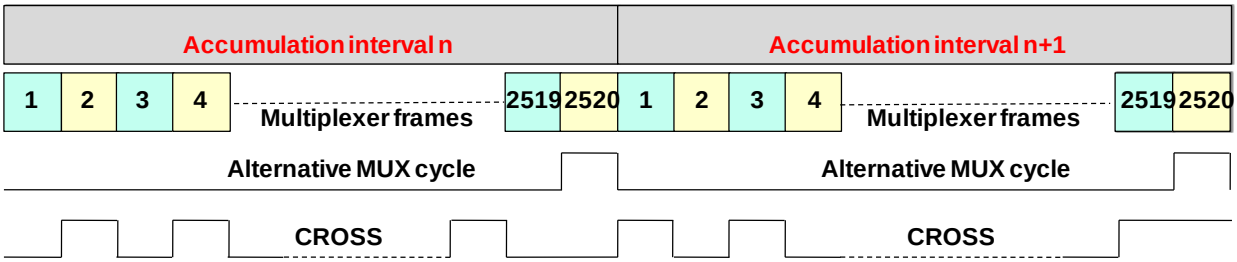


Figure 3: CROSS Signal with CHOP_E = 00

Figure 3 shows CROSS over two accumulation intervals when *CHOP_E* = 00: At the end of the first interval, CROSS is low, at the end of the second interval, CROSS is high. The offset error for the two temperature measurements taken during the ALT multiplexer frames will be averaged to zero. Note that the number of multiplexer frames in an accumulation interval is always even. Operation with *CHOP_E* = 00 does not require control of the chopping mechanism by the MPU while eliminating the offset for temperature measurement.

In the second toggle state, *CHOP_E* = 11, no ALT frame is forced during the last multiplexer cycle in an accumulation interval, and CROSS always toggles near the end of each multiplexer frame.

The internal bias voltage, VBIAS (typically 1.6 V), is used by the ADC as a reference when measuring the temperature and battery monitor signals.

1.2.6 Temperature Sensor

The 71M6533 and 71M6534 include an on-chip temperature sensor implemented as a bandgap reference. It is used to determine the die temperature. The MPU may request an alternate multiplexer cycle containing the temperature sensor output by asserting *MUX_ALT*.

The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see Section 3.5 Temperature Compensation).

1.2.7 Battery Monitor

The battery voltage is measured by the ADC during alternative multiplexer frames if the *BME* (Battery Measure Enable) bit in the I/O RAM is set. While *BME* is set, an on-chip 45 kΩ load resistor is applied to the battery and a scaled fraction of the battery voltage is applied to the ADC input. After each alternative MUX frame, the result of the ADC conversion is available at XRAM address 0x07. *BME* is ignored and assumed zero when system power is not available (V1 < VBIAS). See Section 5.4.5 Battery Monitor for details regarding the ADC LSB size and the conversion accuracy.

1.2.8 AFE Functional Description

The AFE functions as a data acquisition system, controlled by the MPU. The main signals (IA, VA, IB, VB, etc.) are sampled and the ADC counts obtained are stored in XRAM where they can be accessed by

the CE and, if necessary, by the MPU. Alternate multiplexer cycles are initiated less frequently by the MPU to gather access to the slow temperature and battery signals.

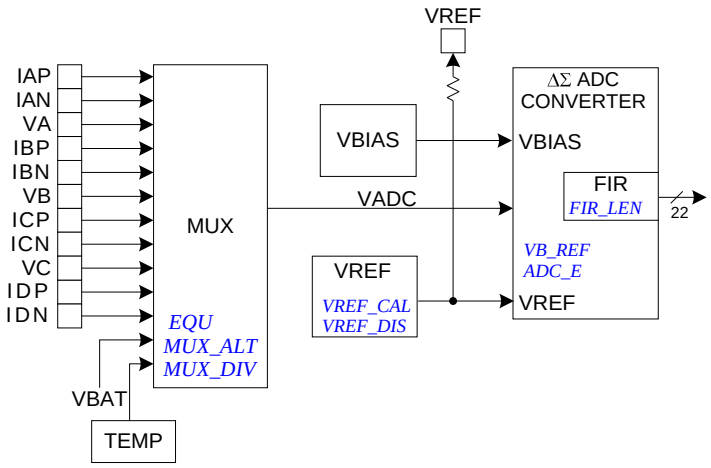


Figure 4: AFE Block Diagram

1.2.9 Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- Frequency-insensitive delay cancellation on all six channels (to compensate for the delay between samples caused by the multiplexing scheme).
- 90° phase shifter (for VAR calculations).
- Pulse generation.
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on calibration coefficients. Scaling of all samples based on temperature compensation information.

The CE program resides in flash memory. Common access to flash memory by the CE and MPU is controlled by a memory share circuit. Each CE instruction word is two bytes long. Allocated flash space for the CE program cannot exceed 4096 16-bit words (8 KB). The CE program counter begins a pass through the CE code each time multiplexer state 0 begins. The code pass ends when a HALT instruction is executed. For proper operation, the code pass must be completed before the multiplexer cycle ends (see Section 2.2 System Timing Summary).

The CE program must begin on a 1 KB boundary of the flash address. The I/O RAM register *CE_LCTN[7:0]* defines which 1 KB boundary contains the CE code. Thus, the first CE instruction is located at 1024**CE_LCTN[7:0]*.

The CE can access up to 4 KB of data RAM (XRAM), or 1024 32-bit data words, starting at RAM address 0x0000.

The XRAM can be accessed by the FIR filter block, the RTM circuit, the CE, and the MPU. Assigned time slots are reserved for FIR and MPU, respectively, to prevent bus contention for XRAM data access by the CE.
The MPU can read and write the XRAM shared between the CE and MPU as the primary means of data communication between the two processors.

Table 4 shows the CE addresses in XRAM allocated to analog inputs from the AFE.

Table 4: XRAM Locations for ADC Results

Address (HEX)	Name	Description
0x00	IA	Phase A current
0x01	VA	Phase A voltage
0x02	IB	Phase B current
0x03	VB	Phase B voltage
0x04	IC	Phase C current
0x05	VC	Phase C voltage
0x06	ID	Neutral current
0x07 – 0x09	–	Not used
0x0A	TEMP	Temperature
0x0B	VBAT	Battery Voltage

The CE is aided by support hardware to facilitate implementation of equations, pulse counters, and accumulators. This hardware is controlled through I/O RAM locations *EQU* (equation assist), *DIO_PV* and *DIO_PW* (pulse count assist), and *PRE_SAMPS* and *SUM_CYCLES* (accumulation assist).

PRE_SAMPS and *SUM_CYCLES* support a dual-level accumulation scheme where the first accumulator accumulates results from *PRE_SAMPS* samples and the second accumulator accumulates up to *SUM_CYCLES* of the first accumulator results. The integration time for each energy output is *PRE_SAMPS* * *SUM_CYCLES*/2520.6 (with *MUX_DIV* = 6). CE hardware issues the XFER_BUSY interrupt when the accumulation is complete.

1.2.10 Meter Equations

The 71M6533 and 71M6534 provide hardware assistance to the CE in order to support various meter equations. This assistance is controlled through I/O RAM location *EQU* (equation assist). The Compute Engine (CE) firmware for industrial configurations can implement the equations listed in Table 5. *EQU* specifies the equation to be used based on the meter configuration and on the number of phases used for metering.

Table 5: Inputs Selected in Regular and Alternate Multiplexer Cycles

EQU	Description	Wh and VARh formula			Mux Sequence	ALT Mux Sequence
		Element 0	Element 1	Element 2		
0	1 element, 2 W, 1ϕ with neutral current sense	VA · IA	VA · IB	N/A	Sequence is programmable with *SLOTn_SEL*	Sequence is programmable with *SLOTn_ALTSEL*
1	1 element, 3 W, 1ϕ	VA(IA-IB)/2	N/A	N/A		
2	2 element, 3 W, 3ϕ Delta	VA · IA	VB · IB	N/A		
3	2 element, 4 W, 3ϕ Delta	VA(IA-IB)/2	VC ·IC	N/A		
4	2 element, 4 W, 3ϕ Wye	VA(IA-IB)/2	VB(IC-IB)/2	N/A		
5	3 element, 4 W, 3ϕ Wye	VA · IA	VB · IB	VC · IC		

1.2.11 Real-Time Monitor

The CE contains a Real-Time Monitor (RTM), which can be programmed to monitor four selectable XRAM locations at full sample rate. The four monitored locations are serially output to the TMUXOUT pin via the digital output multiplexer at the beginning of each CE code pass. The RTM can be enabled and disabled with *RTM_E*. The RTM output is clocked by CKTEST. Each RTM word is clocked out in 35 cycles and contains a leading flag bit. See Figure 19 for the RTM output format. RTM is low when not in use.

1.2.12 Pulse Generators

The 71M6533 and 71M6534 provide four pulse generators, RPULSE, WPULSE, XPULSE and YPULSE, as well as hardware support for the RPULSE and WPULSE pulse generators. The pulse generators can be used to output CE status indicators, SAG for example, to DIO pins.

The polarity of the pulses may be inverted with *PLS_INV*. When this bit is set, the pulses are active high, rather than the more usual active low. *PLS_INV* inverts all the pulse outputs.

XPULSE and YPULSE

Pulses generated by the CE may be exported to the XPULSE and YPULSE pulse outputs. Pins DIO8 and DIO9 are used for these pulses. Generally, the XPULSE and YPULSE outputs are updated once on each pass of the CE code, resulting in a pulse frequency up to a maximum of 1260Hz (assuming a MUX frame is 13 CK32 cycles).

Standard CE code permits the selection of either an energy indication or signaling of a sag event for the YPULSE output. See Section 4.3 CE Interface Description for details.

RPULSE and WPULSE

During each CE code pass, the hardware stores exported WPULSE AND RPULSE sign bits in an 8-bit FIFO and outputs them at a specified interval. This permits the CE code to calculate the RPULSE and WPULSE outputs at the beginning of its code pass and to rely on hardware to spread them over the MUX frame. The FIFO is reset at the beginning of each MUX frame. *PLS_INTERVAL[7:0]* controls the delay to the first pulse update and the interval between subsequent updates. The LSB of *PLS_INTERVAL[7:0]* is equivalent to 4 CK_FIR cycles. If zero, the FIFO is deactivated and the pulse outputs are updated immediately. Thus, NINTERVAL is *4*PLS_INTERVAL.*

Since the FIFO resets at the beginning of each MUX frame, the user must specify *PLS_INTERVAL* so that all of the pulse updates are output before the MUX frame completes. For instance, if the CE code outputs 6 updates per MUX interval, and if the MUX interval is 1950 cycles long, the ideal value for the interval is 1950/6/4 = 81.25. If *PLS_INTERVAL* = 82, the fifth output will occur too late and be lost. In this case, the proper value for *PLS_INTERVAL* is 81.

Hardware also provides a maximum pulse width feature: *PLS_MAXWIDTH[7:0]* selects a maximum negative pulse width to be Nmax updates according to the formula: Nmax = (2**PLS_MAXWIDTH*+1). If *PLS_MAXWIDTH*=255, no width checking is performed.

The WPULSE and RPULSE pulse generator outputs are available on DIO6 and DIO7, respectively. They can also be output on OPT_TX (see *OPT_TXE[1:0]* for details).

1.2.13 Data RAM (XRAM)

In the 71M6533/71M6534, the CE and MPU use a single general-purpose Data RAM (also referred to as XRAM). The Data RAM is 1024 32-bit words, shared between the CE and the MPU using a time-multiplex method. This reduces MPU wait states when accessing CE data. When the MPU and CE are clocking at maximum frequency (10 MHz), the DRAM will make up to four accesses during each 100 ns interval. These consist of two MPU accesses, one CE access and one SPI access.

The Data RAM is 32 bits wide and uses an external multiplexer so as to appear byte-wide to the MPU. The Data RAM hardware will convert an MPU byte write operation into a read-modify-write operation that requires two Data RAM accesses. The second access is guaranteed to be available because the MPU cannot access the XRAM on two consecutive instructions unless it is using the same address.

In addition to the reduction of wait states, this arrangement permits the MPU to easily use unneeded CE data memory. Likewise, the amount of memory the CE uses is not limited by the size of a dedicated CE data RAM.

1.2.14 CE Functional Overview

The ADC processes one sample per channel per multiplexer cycle. Figure 5 shows the timing of the samples taken during one multiplexer cycle (phases A, B, and C being processed). During an ALT multiplexer sequence, missing samples are filled in by the CE.

The number of samples processed during one accumulation cycle is controlled by the I/O RAM registers *PRE_SAMPS* (0x2001[7:6]) and *SUM_CYCLES* (0x2001[5:0]). The integration time for each energy output is:

PRE_SAMPS * *SUM_CYCLES* / 2520.6, where 2520.6 is the sample rate in Hz

For example, *PRE_SAMPS* = 42 and *SUM_CYCLES* = 50 will establish 2100 samples per accumulation cycle. *PRE_SAMPS* = 100 and *SUM_CYCLES* = 21 will result in the exact same accumulation cycle of 2100 samples or 833 ms. After an accumulation cycle is completed, the XFER_BUSY interrupt signals to the MPU that accumulated data are available.

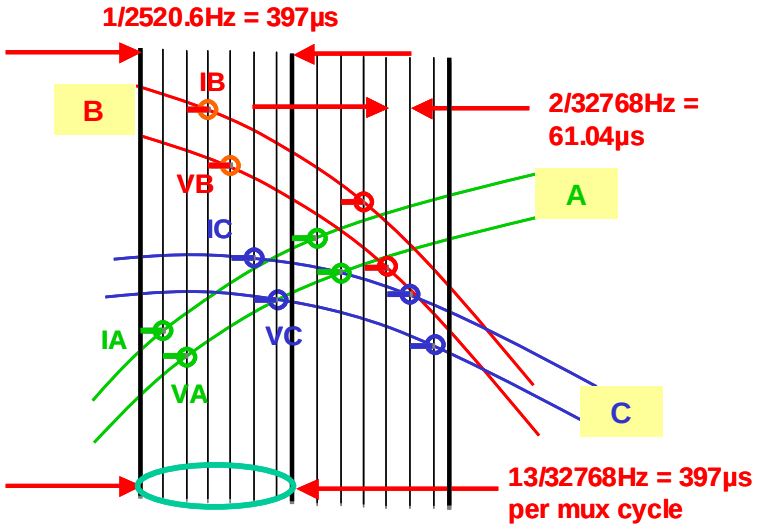


Figure 5: Samples from Multiplexer Cycle

The end of each multiplexer cycle is signaled to the MPU by the CE_BUSY interrupt. At the end of each multiplexer cycle, status information, such as sag data and the digitized input signal, is available to the MPU.

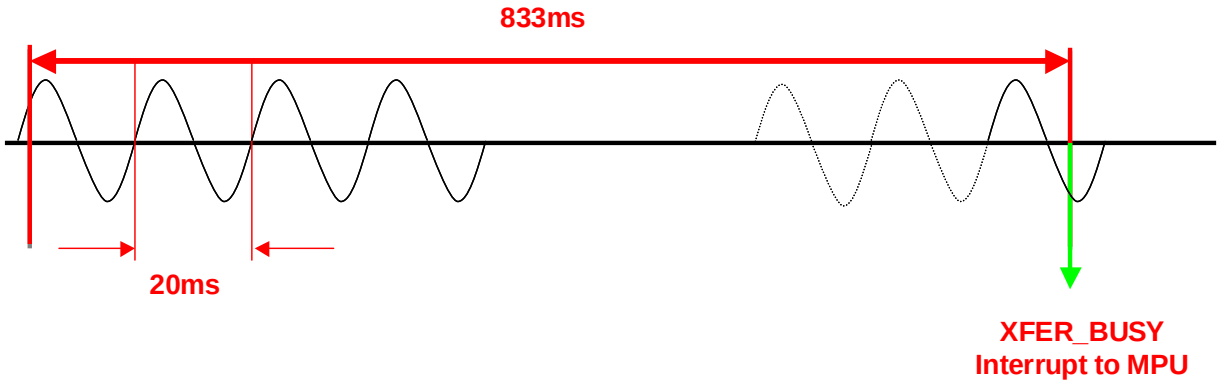


Figure 6: Accumulation Interval

Figure 6 shows the accumulation interval resulting from *PRE_SAMPS* = 42 and *SUM_CYCLES* = 50, consisting of 2100 samples of 397µs each, followed by the XFER_BUSY interrupt. The sampling in this example is applied to a 50 Hz signal.

- There is no correlation between the line signal frequency and the choice of *PRE_SAMPS* or *SUM_CYCLES* (even though when *SUM_CYCLES* = 42, one set of *SUM_CYCLES* happens to sample a period of 16.6 ms). Furthermore, sampling does not have to start when the line voltage crosses the zero line, and the length of the accumulation interval need not be an integer multiple of the signal cycles.

1.3 80515 MPU Core

The 71M6533 and 71M6534 include an 80515 MPU (8-bit, 8051-compatible) that processes most instructions in one clock cycle. Using a 10 MHz clock results in a processing throughput of 10 MIPS. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally, a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single machine cycle (MPU clock cycle). This leads to an 8x average performance improvement (in terms of MIPS) over the Intel® 8051 device running at the same clock frequency.

Table 6 shows the CKMPU frequency as a function of the allowed combinations of the MPU clock divider *MPU_DIV[2:0]* and the MCK divider registers *M40MHZ* and *M26MHZ*. Actual processor clocking speed can be adjusted to the total processing demand of the application (metering calculations, AMR management, memory management, LCD driver management and I/O management) using the I/O RAM register *MPU_DIV[2:0]* and the MCK divider registers *M40MHZ* and *M26MHZ*, as shown in Table 6.

Table 6: CKMPU Clock Frequencies

MPU_DIV [2:0]	[*M40MHZ, M26MHZ*] Values		
	[1,0]	**[0,1]**	**[0,0]**
000	10 MHz	6.6 MHz	5 MHz
001	5 MHz	3.3 MHz	2.5 MHz
010	2.5 MHz	1.65 MHz	1.25 MHz
011	1.25 MHz	825 kHz	625 kHz
100	625 kHz	412.5 kHz	312.5 kHz
101	312.5 kHz	206.25 kHz	156.25 kHz
110	156.25 kHz	103.13 kHz	78.13 kHz
111	156.25 kHz	103.13 kHz	78.13 kHz

Typical measurement and metering functions based on the results provided by the internal 32-bit compute engine (CE) are available for the MPU as part of the Teridian standard library. A standard ANSI C 80515 application programming interface library is available to help reduce design cycle.

1.3.1 Memory Organization and Addressing

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces. Memory organization in the 80515 is similar to that of the industry standard 8051. There are four memory areas: Program memory (Flash, shared by MPU and CE), external RAM (Data RAM, shared by the CE and MPU), Configuration RAM and internal data memory (Internal RAM). Table 7 shows the memory map.

Program Memory

The 80515 can address up to 64 KB of program memory space from 0x0000 to 0xFFFF. Program memory is read when the MPU fetches instructions or performs a MOVC operation. Access to program memory above 0x7FFF is controlled by the *FL_BANK[2:0]* register (SFR 0xB6).

After reset, the MPU starts program execution from program memory location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0x0003.

MPU External Data Memory (XRAM)

Both internal and external memory is physically located on the 71M6533/71M6534 device. The external memory referred to in this documentation is only external to the 80515 MPU core.

4 KB of RAM starting at address 0x0000 is shared by the CE and MPU. The CE normally uses the first 1 KB, leaving 3 KB for the MPU. Different versions of the CE code use varying amounts. Consult the documentation for the specific code version being used for the exact limit.

If the MPU overwrites the CE's working RAM, the CE's output may be corrupted. If the CE is disabled, the first 0x40 bytes of RAM are still unusable because the 71M6533/71M6534 ADC writes to these locations.

The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction (SFR PDATA provides the upper 8 bytes for the MOVX A,@Ri instruction).

Internal and External Memory Map

Table 7 shows the address, type, use and size of the various memory components.

Only the memory ranges shown in Table 7 contain physical memory.

Table 7: Memory Map

Address (hex)	Memory Technology	Memory Type	Name	Typical Usage	Memory Size (bytes)
00000-1FFFF	Flash Memory	Non-volatile	Program memory	MPU Program and non-volatile data	128 KB
00000-3FFFF*	Flash Memory	Non-volatile	Program memory	MPU Program and non-volatile data	256 KB*
on 1K boundary	Flash Memory	Non-volatile	Program memory	CE program	8 KB max.
0000-0FFF	Static RAM	Volatile	External RAM (XRAM)	Shared by CE and MPU	4 KB
2000-20BF, 20C8-20FF	Static RAM	Volatile	Configuration RAM (I/O RAM)	Hardware control	256
20C0-20C7	Static RAM	Non-volatile (battery)	Configuration RAM (I/O RAM)	Battery-buffered memory	8
0000-00FF	Static RAM	Volatile	Internal RAM	Part of 80515 Core	256

* For the 71M6534 only.

MOVX Addressing

There are two types of instructions differing in whether they provide an 8-bit or 16-bit indirect address to the external data RAM.

In the first type, MOVX A,@Ri, the contents of R0 or R1 in the current register bank provide the eight lower-ordered bits of address. The eight high-ordered bits of the address are specified with the *PDATA* SFR. This method allows the user paged access (256 pages of 256 bytes each) to all ranges of the external data RAM.

In the second type of MOVX instruction, MOVX A,@DPTR, the data pointer generates a 16-bit address. This form is faster and more efficient when accessing very large data arrays (up to 64 KB), since no additional instructions are needed to set up the eight high ordered bits of the address.

It is possible to mix the two MOVX types. This provides the user with four separate data pointers, two with direct access and two with paged access, to the entire 64 KB of external memory range.

Dual Data Pointer

The Dual Data Pointer accelerates the block moves of data. The standard *DPTR* is a 16-bit register that is used to address external memory or peripherals. In the 80515 core, the standard data pointer is called *DPTR*, the second data pointer is called *DPTR1*. The data pointer select bit, located in the LSB of the *DPS* register (*DPS*[0]), chooses the active pointer. *DPTR* is selected when *DPS*[0] = 0 and *DPTR1* is selected when *DPS*[0] = 1.

The user switches between pointers by toggling the LSB of the *DPS* register. The values in the data pointers are not affected by the LSB of the *DPS* register. All *DPTR* related instructions use the currently selected *DPTR* for any activity.

The second data pointer may not be supported by certain compilers.

DPTR1 is useful for copy routines, where it can make the inner loop of the routine two instructions faster compared to the reloading of *DPTR* from registers. Any interrupt routine using *DPTR1* must save and restore *DPS*, *DPTR* and *DPTR1*, which increases stack usage and slows down interrupt latency.

By selecting the Evatronics R80515 core in the Keil compiler project settings and by using the compiler directive "MODC2", dual data pointers are enabled in certain library routines.

An alternative data pointer is available in the form of the *PDATA* register (SFR 0xBF, sometimes referred to as *USR2*). It defines the high byte of a 16-bit address when reading or writing XDATA with the instruction MOVX A,@Ri or MOVX @Ri,A.

Internal Data Memory Map and Access

The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always 1 byte wide. Table 8 shows the internal data memory map.

The Special Function Registers (SFR) occupy the upper 128 bytes. The SFR area of internal data memory is available only by direct addressing. Indirect addressing of this area accesses the upper 128 bytes of Internal RAM. The lower 128 bytes contain working registers and bit addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (*PSW*) select which bank is in use. The next 16 bytes form a block of bit addressable memory space at addresses 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing.

Table 8: Internal Data Memory Map

Address	Direct Addressing	Indirect Addressing
0xFF	Special Function Registers (SFRs)	RAM
0x80		
0x7F	Byte addressable area	
0x30		
0x2F	Bit addressable area	
0x20		
0x1F	Register banks R0…R7	
0x00		

1.3.2 Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 9.

Only a few addresses in the SFR memory space are occupied, the others are not implemented. A read access to unimplemented addresses will return undefined data, while a write access will have no effect. SFRs specific to the 71M6533/71M6534 are shown in **bold** print on a gray field. The registers at 0x80, 0x88, 0x90, etc., are bit addressable, all others are byte addressable.

Table 9: Special Function Register Map

Hex/ Bin	Bit Addressable	Byte Addressable							Bin/ Hex
	X000	X001	X010	X011	X100	X101	X110	X111	
F8	***INTBITS***								FF
F0	*B*								F7
E8	***IFLAGS***								EF
E0	*A*								E7
D8	*WDCON*								DF
D0	*PSW*								D7
C8	*T2CON*								CF
C0	*IRCON*								C7
B8	*IEN1*	*IP1*	*S0RELH*	*S1RELH*				*PDATA*	BF
B0	***P3***		***FLSHCTL***				***FL_BANK***	***PGADR***	B7
A8	*IEN0*	*IP0*	*S0RELL*						AF
A0	***P2***	***DIR2***	***DIR0***						A7
98	*S0CON*	*S0BUF*	*IEN2*	*S1CON*	*S1BUF*	*S1RELL*	***EEDATA***	***EECTRL***	9F
90	***P1***	***DIR1***	*DPS*		***ERASE***				97
88	*TCON*	*TMOD*	*TL0*	*TL1*	*TH0*	*TH1*	*CKCON*		8F
80	*P0*	*SP*	*DPL*	*DPH*	*DPL1*	*DPH1*		*PCON*	87

1.3.3 Generic 80515 Special Function Registers

Table 10 shows the location, description and reset or power-up value of the generic 80515 SFRs. Additional descriptions of the registers can be found at the page numbers listed in the table.

Table 10: Generic 80515 SFRs - Location and Reset Values

Name	Address (Hex)	Reset value (Hex)	Description	Page
P0	0x80	0xFF	Port 0	24
SP	0x81	0x07	Stack Pointer	24
DPL	0x82	0x00	Data Pointer Low 0	24
DPH	0x83	0x00	Data Pointer High 0	24
DPL1	0x84	0x00	Data Pointer Low 1	24
DPH1	0x85	0x00	Data Pointer High 1	24
PCON	0x87	0x00	UART Speed Control, Idle and Stop mode Control	28
TCON	0x88	0x00	Timer/Counter Control	32
TMOD	0x89	0x00	Timer Mode Control	29
TL0	0x8A	0x00	Timer 0, low byte	29
TL1	0x8B	0x00	Timer 1, high byte	29
TH0	0x8C	0x00	Timer 0, low byte	29
TH1	0x8D	0x00	Timer 1, high byte	29
CKCON	0x8E	0x01	Clock Control (Stretch=1)	24
DPS	0x92	0x00	Data Pointer select Register	20
S0CON	0x98	0x00	Serial Port 0, Control Register	28
S0BUF	0x99	0x00	Serial Port 0, Data Buffer	26
IEN2	0x9A	0x00	Interrupt Enable Register 2	31
S1CON	0x9B	0x00	Serial Port 1, Control Register	28

Name	Address (Hex)	Reset value (Hex)	Description	Page
S1BUF	0x9C	0x00	Serial Port 1, Data Buffer	26
S1RELL	0x9D	0x00	Serial Port 1, Reload Register, low byte	26
IEN0	0xA8	0x00	Interrupt Enable Register 0	31
IP0	0xA9	0x00	Interrupt Priority Register 0	34
S0RELL	0xAA	0xD9	Serial Port 0, Reload Register, low byte	26
IEN1	0xB8	0x00	Interrupt Enable Register 1	31
IP1	0xB9	0x00	Interrupt Priority Register 1	34
S0RELH	0xBA	0x03	Serial Port 0, Reload Register, high byte	26
S1RELH	0xBB	0x03	Serial Port 1, Reload Register, high byte	26
PDATA	0xBF	0x00	High address byte for MOVX@Ri - also called *USR2*	20
IRCON	0xC0	0x00	Interrupt Request Control Register	32
T2CON	0xC8	0x00	Polarity for INT2 and INT3	32
PSW	0xD0	0x00	Program Status Word	23
WDCON	0xD8	0x00	Baud Rate Control Register (only WDCON[7] bit used)	26
A	0xE0	0x00	Accumulator	23
B	0xF0	0x00	B Register	23

Accumulator (*ACC, A*):

ACC is the accumulator register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to accumulator as *A*, not *ACC*.

***B* Register:**

The *B* register is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

Program Status Word (*PSW*):

This register contains various flags and control bits for the selection of the register banks (see Table 11).

Table 11: *PSW* Bit Functions (SFR 0xD0)

PSW Bit	Symbol	Function
7	*CV*	Carry flag.
6	*AC*	Auxiliary Carry flag for BCD operations.
5	*F0*	General purpose Flag 0 available for user. F0 is not to be confused with the F0 flag in the *CESTATUS* register.
4	*RS1*	Register bank select control bits. The contents of *RS1* and *RS0* select the working register bank:
3	*RS0*	
2	*OV*	Overflow flag.
1	–	User defined flag.
0	*P*	Parity flag, affected by hardware to indicate odd or even number of one bits in the Accumulator, i.e. even parity.

RS1/RS0	Bank selected	Location
00	Bank 0	0x00 – 0x07
01	Bank 1	0x08 – 0x0F
10	Bank 2	0x10 – 0x17
11	Bank 3	0x18 – 0x1F

Stack Pointer (SP):

The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

Data Pointer:

The data pointer (*DPTR*) is 2 bytes wide. The lower part is *DPL*, and the highest is *DPH*. It can be loaded as two registers (e.g. MOV DPL,#data8). It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Program Counter:

The program counter (*PC*) is 2 bytes wide and initialized to 0x0000 after reset. This register is incremented when fetching operation code or when operating on data from program memory.

Port Registers:

The I/O ports are controlled by Special Function Registers *P0*, *P1* and *P2*. The contents of the SFR can be observed on corresponding pins on the chip. Writing a 1 to any of the ports (see Table 12) causes the corresponding pin to be at high level (V3P3). Writing a 0 causes the corresponding pin to be held at a low level (GND). The data direction registers *DIR0*, *DIR1*, and *DIR2* define individual pins as input or output pins (see Section 1.4.7 Digital I/O for details).

Table 12: Port Registers

Register	SFR Address	R/W	Description
P0	0x80	R/W	Register for port 0 read and write operations.
DIR0	0xA2	R/W	Data direction register for port 0. Setting a bit to 1 means that the corresponding pin is an output.
P1	0x90	R/W	Register for port 1 read and write operations.
DIR1	0x91	R/W	Data direction register for port 1.
P2	0xA0	R/W	Register for port 2 read and write operations.
DIR2	0xA1	R/W	Data direction register for port 2.

All DIO ports on the chip are bi-directional. Each of them consists of a Latch (SFR *P0* to *P2*), an output driver and an input buffer, therefore the MPU can output or read data through any of these ports. Even if a DIO pin is configured as an output, the state of the pin can still be read by the MPU, for example when counting pulses issued via DIO pins that are under CE control.

The technique of reading the status of or generating interrupts based on DIO pins configured as outputs can be used to implement pulse counting.

Clock Stretching (*CKCON*)

The three low order bits of the *CKCON* register define the stretch memory cycles that are used for MOVX instructions when accessing external peripherals. The practical value of this register for the 71M6533/71M6534 is to guarantee access to XRAM between CE, MPU, and SPI. The default setting of *CKCON* (001) should not be changed.

Table 13 shows how the signals of the External Memory Interface change when stretch values are set from 0 to 7. The widths of the signals are counted in MPU clock cycles. The post-reset state of the *CKCON* register (001), which is shown in **bold** in the table, performs the MOVX instructions with a stretch value equal to 1.

Table 13: Stretch Memory Cycle Width

CKCON[2:0]	Stretch Value	Read Signal Width		Write Signal Width	
		memaddr	memrd	memaddr	memwr
000	0	1	1	2	1
001	**1**	**2**	**2**	**3**	**1**
010	2	3	3	4	2
011	3	4	4	5	3
100	4	5	5	6	4
101	5	6	6	7	5
110	6	7	7	8	6
111	7	8	8	9	7

1.3.4 71M6533/71M6534-Specific Special Function Registers

Table 14 shows the location and description of the 71M6533/71M6534-specific SFRs.

Table 14: 71M6533/71M6534 Specific SFRs

Register (Alternate Name)	SFR Address	Bit Field Name	R/W	Description
EEDATA	0x9E		R/W	I^2C EEPROM interface data register.
EECTRL	0x9F		R/W	I^2C EEPROM interface control register. See Section 1.4.10 EEPROM Interface for a description of the command and status bits available for *EECTRL*.
ERASE (FLSH_ERASE)	0x94		W	This register is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. See the Flash Memory section for details.
FL_BANK[2:0]	0xB6[2:0]		R/W	Flash Bank Selection.
PGADDR (FLSH_PGADR)	0xB7		R/W	Flash Page Erase Address register. Contains the flash memory page address (page 0 through page 127) that will be erased (default = 0x00). Must be re-written for each new Page Erase cycle.
FLSHCRL	0xB2[0]	*FLSH_PWE*	R/W	Program Write Enable: 0: MOVX commands refer to XRAM Space, normal operation (default). 1: MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR.
	0xB2[1]	*FLSH_MEEN*	W	Mass Erase Enable: 0: Mass Erase disabled (default). 1: Mass Erase enabled. Must be re-written for each new Mass Erase cycle.
	0xB2[4]	*WRPROT_CE*		Protects flash from address *CE_LCTN**1024 to the end of memory from flash page erase.
	0xB2[5]	*WRPROT_BT*		Protects flash from address 0 to address *BOOT_SIZE**1024 from flash page erase.
	0xB2[6]	*SECURE*	R/W	Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.
	0xB2[7]	*PREBOOT*	R	Indicates that the preboot sequence is active.

Register (Alternate Name)	SFR Address	Bit Field Name	R/W	Description
IFLAGS	0xE8[0]	*IE_XFER*	R/W	This flag monitors the XFER_BUSY interrupt. It is set by hardware and must be cleared by the interrupt handler.
	0xE8[1]	*IE_RTC*	R/W	This flag monitors the RTC_1SEC interrupt. It is set by hardware and must be cleared by the interrupt handler.
	0xE8[2]	*FW_COL0*	R/W	This flag indicates that a flash write was attempted while the CE was busy.
	0xE8[3]	*FW_COL1*	R/W	This flag indicates that a flash write was in progress when the CE was attempting to begin a code pass.
	0xE8[4]	*IE_PB*	R/W	This flag indicates that the wake-up pushbutton was pressed.
	0xE8[5]	*IE_WAKE*	R/W	This flag indicates that the MPU was awakened by the autowake timer.
	0xE8[6]	*PLL_RISE*	R/W	PLL_RISE Interrupt Flag: Write 0 to clear the *PLL_RISE* interrupt flag.
	0xE8[7]	*PLL_FALL*	R/W	PLL_FALL Interrupt Flag: Write 0 to clear the *PLL_FALL* interrupt flag.
INTBITS (INT0 … INT6)	0xF8[6:0]	*INT6 ... INT0*	R	Interrupt inputs. The MPU may read these bits to see the status of external interrupts INT0 up to INT6. These bits do not have any memory and are primarily intended for debug use.
	0xF8[7]	*WD_RST*	W	The WDT is reset when a 1 is written to this bit.
	✓ Only byte operations on the entire *INTBITS* register should be used when writing. The byte must have all bits set except the bits that are to be cleared.			

1.3.5 Instruction Set

All instructions of the generic 8051 microcontroller are supported. A complete list of the instruction set and of the associated op-codes is contained in the *71M653X Software User's Guide (SUG)*.

1.3.6 UARTs

The 71M6533 and 71M6534 include a UART (UART0) that can be programmed to communicate with a variety of AMR modules and other external devices. A second UART (UART1) is connected to the optical port, as described in the 1.4.6 UART and Optical Interface section.

The UARTs are dedicated 2-wire serial interfaces, which can communicate with an external host processor at up to 38,400 bits/s (with MPU clock = 1.2288 MHz). The operation of the RX and TX UART0 pins is as follows:

- UART0 RX: Serial input data are applied at this pin. Conforming to RS-232 standard, the bytes are input LSB first.
- UART0 TX: This pin is used to output the serial data. The bytes are output LSB first.

The 71M6533 and 71M6534 have several UART-related registers for the control and buffering of serial data.

The serial buffers consist of sets of two separate registers (one set for each UART), a transmit buffer (*S0BUF*, *S1BUF*) and a receive buffer (*R0BUF*, *R1BUF*). Writing data to the transmit buffer starts the

transmission by the associated UART. Received data are available by reading from the receive buffer. Both UARTs can simultaneously transmit and receive data.

WDCON[7] selects whether timer 1 or the internal baud rate generator is used. All UART transfers are programmable for parity enable, parity, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 38400 bps. Table 15 shows how the baud rates are calculated. Table 16 shows the selectable UART operation modes.

Table 15: Baud Rate Generation

	Using Timer 1 (*WDCON[7]* = 0)	**Using Internal Baud Rate Generator (*WDCON[7]* = 1)**
UART0	$2^{smod} * f_{CKMPU} / (384 * (256-TH1))$	$2^{smod} * f_{CKMPU} / (64 * (2^{10}-S0REL))$
UART1	N/A	$f_{CKMPU} / (32 * (2^{10}-S1REL))$

S0REL and *S1REL* are 10-bit values derived by combining bits from the respective timer reload registers. *SMOD* is the *SMOD* bit in the SFR *PCON* register. *TH1* is the high byte of timer 1.

Table 16: UART Modes

	UART 0	**UART 1**
Mode 0	N/A	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator)
Mode 1	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator or timer 1)	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator)
Mode 2	Start bit, 8 data bits, parity, stop bit, fixed baud rate 1/32 or 1/64 of f_{CKMPU}	N/A
Mode 3	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator or timer 1)	N/A

Parity of serial data is available through the P flag of the accumulator. 7-bit serial modes with parity, such as those used by the FLAG protocol, can be simulated by setting and reading bit 7 of 8-bit output data. 7-bit serial modes without parity can be simulated by setting bit 7 to a constant 1. 8-bit serial modes with parity can be simulated by setting and reading the 9th bit, using the control bits *TB80* (*S0CON*[3]) and *TB81* (*S1CON[3]*) in the *S0CON* and *S1CON* SFRs for transmit and *RB81* (*S1CON[2]*) for receive operations.

The feature of receiving 9 bits (Mode 3 for UART0, Mode A for UART1) can be used as handshake signals for inter-processor communication in multi-processor systems. In this case, the slave processors have bit *SM20* (*S0CON[5]*) for UART0, or *SM21* (*S1CON[5]* for UART1, set to 1. When the master processor outputs the slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their address. If there is a match, the addressed slave will clear *SM20* or *SM21* and receive the rest of the message. The rest of the slave's will ignore the message. After addressing the slave, the host outputs the rest of the message with the 9th bit set to 0, so no additional serial port receive interrupts will be generated.

UART Control Registers:

The functions of UART0 and UART1 depend on the setting of the Serial Port Control Registers *S0CON* and *S1CON* shown in Table 17 and Table 18, respectively, and the *PCON* register shown in Table 19.

The UARTs require software to clear the interrupt bits. It is recommended to use bit manipulation instructions rather than byte instructions when using UART1 in full duplex mode. For example, the CLR *TI0* instruction should be used instead of ANL #0FDH,*S0CON*. Further measures in code involve reducing and combining the write operations to *S1CON* and reducing the time between the read and write operations on

S1CON. It is also recommended to have a timeout slightly longer than one character time on both interrupts that restarts the transmit or receive logic.

Table 17: The *S0CON* (UART0) Register (SFR 0x98)

Bit	Symbol	Function
S0CON[7]	*SM0*	The *SM0* and *SM1* bits set the UART0 mode: Mode / Description / SM0 / SM1 0 / N/A / 0 / 0 1 / 8-bit UART / 0 / 1 2 / 9-bit UART / 1 / 0 3 / 9-bit UART / 1 / 1
S0CON[6]	*SM1*	
S0CON[5]	*SM20*	Enables the inter-processor communication feature.
S0CON[4]	*REN0*	If set, enables serial reception. Cleared by software to disable reception.
S0CON[3]	*TB80*	The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.)
S0CON[2]	*RB80*	In Modes 2 and 3 it is the 9th data bit received. In Mode 1, *SM20* is 0, *RB80* is the stop bit. In mode 0, this bit is not used. Must be cleared by software.
S0CON[1]	*TI0*	Transmit interrupt flag; set by hardware after completion of a serial transfer. Must be cleared by software.
S0CON[0]	*RI0*	Receive interrupt flag; set by hardware after completion of a serial reception. Must be cleared by software.

Table 18: The *S1CON* (UART1) Register (SFR 0x9B)

Bit	Symbol	Function
S1CON[7]	*SM*	Sets the baud rate and mode for UART1. *SM* / Mode / Description / Baud Rate 0 / A / 9-bit UART / variable 1 / B / 8-bit UART / variable
S1CON[5]	*SM21*	Enables the inter-processor communication feature.
S1CON[4]	*REN1*	If set, enables serial reception. Cleared by software to disable reception.
S1CON[3]	*TB81*	The 9th transmitted data bit in Mode A. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.)
S1CON[2]	*RB81*	In Modes A and B, it is the 9th data bit received. In Mode B, if *SM21* is 0, *RB81* is the stop bit. Must be cleared by software
S1CON[1]	*TI1*	Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.
S1CON[0]	*RI1*	Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

Table 19: *PCON* Register Bit Description (SFR 0x87)

Bit	Symbol	Function
PCON[7]	*SMOD*	The *SMOD* bit doubles the baud rate when set
PCON[6:2]	–	Not used.
PCON[1]	*STOP*	Stops MPU flash access and MPU peripherals including timers and UARTs when set until an external interrupt is received.
PCON[0]	*IDLE*	Stops MPU flash access when set until an internal interrupt is received.

1.3.7 Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle, i.e. it counts up once for every 12 periods of the MPU clock. In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from certain DIO pins, see Section 1.4.7 Digital I/O). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the clock frequency (CKMPU). There are no restrictions on the duty cycle, however to ensure proper recognition of the 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1, as shown in Table 20 and Table 21. The *TMOD* Register, shown in Table 22, is used to select the appropriate mode. The timer/counter operation is controlled by the *TCON* Register, which is shown in Table 23. Bits *TR1* (*TCON[6]*) and *TR0* (*TCON[4]*) in the *TCON* register start their associated timers when set.

Table 20: Timers/Counters Mode Description

M1	M0	Mode	Function
0	0	Mode 0	13-bit Counter/Timer mode with 5 lower bits in the *TL0* or *TL1* register and the remaining 8 bits in the *TH0* or *TH1* register (for Timer 0 and Timer 1, respectively). The 3 high order bits of *TL0* and *TL1* are held at zero.
0	1	Mode 1	16-bit Counter/Timer mode.
1	0	Mode 2	8-bit auto-reload Counter/Timer. The reload value is kept in *TH0* or *TH1*, while *TL0* or *TL1* is incremented every machine cycle. When *TL(*x) overflows, a value from *TH(*x) is copied to *TL*(x) (where x is 0 for counter/timer 0 or 1 for counter/timer 1.
1	1	Mode 3	If Timer 1 *M1* and *M0* bits are set to 1, Timer 1 stops. If Timer 0 *M1* and *M0* bits are set to 1, Timer 0 acts as two independent 8-bit Timer/Counters.

In Mode 3, *TL0* is affected by *TR0* and gate control bits, and sets the *TF0* flag on overflow, while *TH0* is affected by the *TR1* bit, and the *TF1* flag is set on overflow.

Table 21 specifies the combinations of operation modes allowed for Timer 0 and Timer 1.

Table 21: Allowed Timer/Counter Mode Combinations

	Timer 1		
	Mode 0	**Mode 1**	**Mode 2**
Timer 0 - mode 0	YES	YES	YES
Timer 0 - mode 1	YES	YES	YES
Timer 0 - mode 2	Not allowed	Not allowed	YES

Table 22: *TMOD* Register Bit Description (SFR 0x89)

Bit	Symbol	Function
Timer/Counter 1:		
TMOD[7]	*Gate*	If set, enables external gate control (signal INT1). When INT1 is high, and the *TR1* bit is set (see the *TCON* register), a counter is incremented every falling edge on T1 input signal
TMOD[6]	*C/T*	Selects timer or counter operation. When set to 1, a counter operation is performed. When cleared to 0, the corresponding register will function as a timer.
TMOD[5:4]	*M1:M0*	Selects the mode for Timer/Counter 1 as shown in Table 20.

Timer/Counter 0		
TMOD[3]	*Gate*	If set, enables external gate control (signal INT0). When INT0 is high, and the *TR0* bit is set (see the *TCON* register), a counter is incremented every falling edge on T0 input signal.
TMOD[2]	*C/T*	Selects timer or counter operation. When set to 1, a counter operation is performed. When cleared to 0, the corresponding register will function as a timer.
TMOD[1:0]	*M1:M0*	Selects the mode for Timer/Counter 0, as shown in Table 20.

Table 23: The *TCON* Register Bit Functions (SFR 0x88)

Bit	Symbol	Function
TCON[7]	*TF1*	The Timer 1 overflow flag is set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed.
TCON[6]	*TR1*	Timer 1 run control bit. If cleared, Timer 1 stops.
TCON[5]	*TF0*	Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed.
TCON[4]	*TR0*	Timer 0 Run control bit. If cleared, Timer 0 stops.
TCON[3]	*IE1*	Interrupt 1 edge flag is set by hardware when the falling edge on external pin int1 is observed. Cleared when an interrupt is processed.
TCON[2]	*IT1*	Interrupt 1 type control bit set by the MPU. Selects either the falling edge or low level on input pin to cause an external interrupt.
TCON[1]	*IE0*	Interrupt 0 edge flag is set by hardware when the falling edge on external pin int0 is observed. Cleared when an interrupt is processed.
TCON[0]	*IT0*	Interrupt 0 type control bit. Selects either the falling edge or low level on input pin to cause interrupt.

1.3.8 WD Timer (Software Watchdog Timer)

There is no internal software watchdog timer. Use the standard watchdog timer instead (see Section 1.4.12 Hardware Watchdog Timer).

1.3.9 Interrupts

The 80515 provides 11 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register (*TCON, IRCON,* and *SCON*). Each interrupt requested by the corresponding flag can be individually enabled or disabled by the enable bits in SFRs *IEN0, IEN1*, and *IEN2*. Figure 7 shows the device interrupt structure.

Interrupt Overview

When an interrupt occurs, the MPU will vector to the predetermined address as shown in Table 36. Once the interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction, RETI. When an RETI is performed, the processor will return to the instruction that would have been next when the interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, then samples are polled by the hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then the interrupt request flag is set. On the next instruction cycle, the interrupt will be acknowledged by hardware forcing an LCALL to the appropriate vector address, if the following conditions are met:

- No interrupt of equal or higher priority is already in progress.
- An instruction is currently being executed and is not completed.
- The instruction in progress is not RETI or any write access to the registers *IEN0, IEN1, IEN2, IP0* or *IP1*.

Special Function Registers for Interrupts

The following SFR registers control the interrupt functions:

- The interrupt enable registers: IEN0, IEN1 and IEN2 (see Table 24, Table 25 and Table 26).
- The Timer/Counter control registers, TCON and T2CON (see Table 27 and Table 28).
- The interrupt request register, IRCON (see Table 29).
- The interrupt priority registers: IP0 and IP1 (see Table 34).

Table 24: The *IEN0* Bit Functions (SFR 0xA8)

Bit	Symbol	Function
IEN0[7]	*EAL*	*EAL* = 0 disables all interrupts.
IEN0[6]	*WDT*	Not used for interrupt control.
IEN0[5]	–	Not Used.
IEN0[4]	*ES0*	*ES0* = 0 disables serial channel 0 interrupt.
IEN0[3]	*ET1*	*ET1* = 0 disables timer 1 overflow interrupt.
IEN0[2]	*EX1*	*EX1* = 0 disables external interrupt 1.
IEN0[1]	*ET0*	*ET0* = 0 disables timer 0 overflow interrupt.
IEN0[0]	*EX0*	*EX0* = 0 disables external interrupt 0.

Table 25: The *IEN1* Bit Functions (SFR 0xB8)

Bit	Symbol	Function
IEN1[7]	–	Not used.
IEN1[6]	–	Not used.
IEN1[5]	*EX6*	*EX6* = 0 disables external interrupt 6.
IEN1[4]	*EX5*	*EX5* = 0 disables external interrupt 5.
IEN1[3]	*EX4*	*EX4* = 0 disables external interrupt 4.
IEN1[2]	*EX3*	*EX3* = 0 disables external interrupt 3.
IEN1[1]	*EX2*	*EX2* = 0 disables external interrupt 2.
IEN1[0]	–	Not Used.

Table 26: The *IEN2* Bit Functions (SFR 0x9A)

Bit	Symbol	Function
IEN2[0]	*ES1*	*ES1* = 0 disables the serial channel 1 interrupt.

Table 27: *TCON* Bit Functions (SFR 0x88)

Bit	Symbol	Function
TCON[7]	*TF1*	Timer 1 overflow flag.
TCON[6]	*TR1*	Not used for interrupt control.
TCON[5]	*TF0*	Timer 0 overflow flag.
TCON[4]	*TR0*	Not used for interrupt control.
TCON[3]	*IE1*	External interrupt 1 flag.
TCON[2]	*IT1*	External interrupt 1 type control bit: 0 = interrupt on low level. 1 = interrupt on falling edge.
TCON[1]	*IE0*	External interrupt 0 flag
TCON[0]	*IT0*	External interrupt 0 type control bit: 0 = interrupt on low level. 1 = interrupt on falling edge.

Table 28: The *T2CON* Bit Functions (SFR 0xC8)

Bit	Symbol	Function
T2CON[7]	–	Not used.
T2CON[6]	*I3FR*	Polarity control for INT3: 0 = falling edge. 1 = rising edge.
T2CON[5]	*I2FR*	Polarity control for INT2: 0 = falling edge. 1 = rising edge.
T2CON[4:0]	–	Not used.

Table 29: The *IRCON* Bit Functions (SFR 0xC0)

Bit	Symbol	Function
IRCON[7]	–	Not used
IRCON[6]	–	Not used
IRCON[5]	*IEX6*	1 = External interrupt 6 occurred and has not been cleared.
IRCON[4]	*IEX5*	1 = External interrupt 5 occurred and has not been cleared.
IRCON[3]	*IEX4*	1 = External interrupt 4 occurred and has not been cleared.
IRCON[2]	*IEX3*	1 = External interrupt 3 occurred and has not been cleared.
IRCON[1]	*IEX2*	1 = External interrupt 2 occurred and has not been cleared.
IRCON[0]	–	Not used.

TF0 and *TF1* (Timer 0 and Timer 1 overflow flags) will be automatically cleared by hardware when the service routine is called (Signals T0ACK and T1ACK – port ISR – active high when the service routine is called).

External MPU Interrupts

External interrupts are the interrupts external to the 80515 core, i.e. signals that originate in other parts of the 71M6533/71M6534, for example the CE, DIO, RTC, EEPROM interface.

The MPUs of the 71M6533 and 71M6534 allow seven external interrupts. These are connected as shown in Table 30. The polarity of interrupts 2 and 3 is programmable in the MPU via the *I3FR* and *I2FR* bits in *T2CON*. Interrupts 2 and 3 should be programmed for falling sensitivity (*I3FR* = *I2FR* = 0). The generic 8051 MPU literature states that interrupts 4 through 6 are defined as rising-edge sensitive. Thus, the hardware signals attached to interrupts 5 and 6 are inverted to achieve the edge polarity shown in Table 30.

Table 30: External MPU Interrupts

External Interrupt	Connection	Polarity	Flag Reset
0	Digital I/O High Priority	see Section 1.4.7	automatic
1	Digital I/O Low Priority	see Section 1.4.7	automatic
2	FWCOL0, FWCOL1, SPI	falling	automatic
3	CE_BUSY	falling	automatic
4	PLL_OK (rising), PLL_OK (falling)	rising	automatic
5	EEPROM busy	falling	automatic
6	XFER_BUSY, RTC_1SEC or WD_NROVF	falling	manual

External interrupt 0 and 1 can be mapped to pins on the device using DIO resource maps. See Section 1.4.7 Digital I/O for more information.
FWCOLx interrupts occur when the CE collides with a flash write attempt. See the flash write description in the Flash Memory section for more detail.

SFR enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit, which is set by the interrupt hardware, and reset by the MPU interrupt handler. XFER_BUSY, RTC_1SEC, WD_NROVF, FWCOL0, FWCOL1, SPI, PLLRISE and PLLFALL have their own enable and flag bits in addition to the interrupt 6, 4 and enable and flag bits (see Table 31).

IE0 through IEX6 are cleared automatically when the hardware vectors to the interrupt handler. The other flags, IE_XFER through IE_PB, are cleared by writing a zero to them.

Since these bits are in an SFR bit addressable byte, common practice would be to clear them with a bit operation, but this must be avoided. The hardware implements bit operations as a byte wide read-modify-write hardware macro. If an interrupt occurs after the read, but before the write, its flag will be cleared unintentionally.

The proper way to clear the flag bits is to write a byte mask consisting of all ones except for a zero in the location of the bit to be cleared. The flag bits are configured in hardware to ignore ones written to them.

Table 31: Interrupt Enable and Flag Bits

Interrupt Enable		Interrupt Flag		Interrupt Description
Name	Location	Name	Location	
EX0	SFR A8[0]	*IE0*	SFR 88[1]	External interrupt 0
EX1	SFR A8[2]	*IE1*	SFR 88[3]	External interrupt 1
EX2	SFR B8[1]	*IEX2*	SFR C0[1]	External interrupt 2
EX3	SFR B8[2]	*IEX3*	SFR C0[2]	External interrupt 3
EX4	SFR B8[3]	*IEX4*	SFR C0[3]	External interrupt 4
EX5	SFR B8[4]	*IEX5*	SFR C0[4]	External interrupt 5
EX6	SFR B8[5]	*IEX6*	SFR C0[5]	External interrupt 6
EX_XFER	2002[0]	*IE_XFER*	SFR E8[0]	XFER_BUSY interrupt (INT 6)
EX_RTC	2002[1]	*IE_RTC*	SFR E8[1]	RTC_1SEC interrupt (INT 6)
IEN_WD_NROVF	20B0[0]	*WD_NROVF_FLAG*	20B1[0]	WDT near overflow (INT 6)

IEN_SPI	20B0[4]	*SPI_FLAG*	20B1[4]	SPI Interface (INT2)
EX_FWCOL	2007[4]	*IE_FWCOL0*	SFR E8[3]	FWCOL0 interrupt (INT 2)
		IE_FWCOL1	SFR E8[2]	FWCOL1 interrupt (INT 2)
EX_PLL	2007[5]	*IE_PLLRISE*	SFRE8[6]	PLL_OK rise interrupt (INT 4)
		IE_PLLFALL	SFRE8[7]	PLL_OK fall interrupt (INT 4)
		IE_WAKE	SFRE8[5]	AUTOWAKE flag
		IE_PB	SFRE8[4]	PB flag

The *AUTOWAKE* and *PB* flag bits are shown in Table 31 because they behave similarly to interrupt flags, even though they are not actually related to an interrupt. These bits are set by hardware when the MPU wakes from a push button or wake timeout. The bits are reset by writing a zero. Note that the PB flag is set whenever the PB is pushed, even if the part is already awake.

Interrupt Priority Level Structure

All interrupt sources are combined in groups, as shown in Table 32:

Table 32: Interrupt Priority Level Groups

Group	Group Members		
0	External interrupt 0	Serial channel 1 interrupt	-
1	Timer 0 interrupt	–	External interrupt 2
2	External interrupt 1	–	External interrupt 3
3	Timer 1 interrupt	–	External interrupt 4
4	Serial channel 0 interrupt	–	External interrupt 5
5	–	–	External interrupt 6

Each group of interrupt sources can be programmed individually to one of four priority levels (as shown in Table 33) by setting or clearing one bit in the SFR interrupt priority register *IP0* and one in *IP1* (Table 34). If requests of the same priority level are received simultaneously, an internal polling sequence as shown in Table 35 determines which request is serviced first.

Changing interrupt priorities while interrupts are enabled can easily cause software defects. It is best to set the interrupt priority registers only once during initialization before interrupts are enabled.

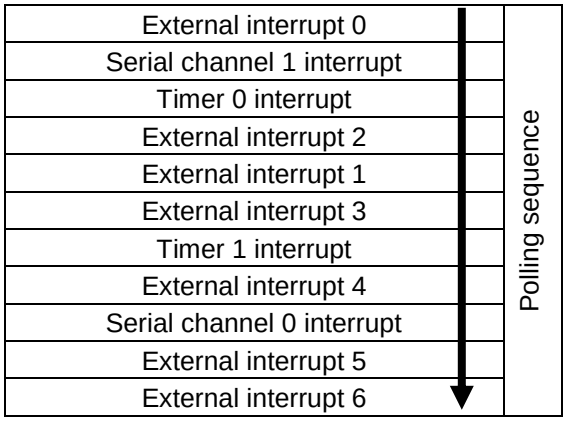
Table 33: Interrupt Priority Levels

***IP1*[x]**	***IP0*[x]**	**Priority Level**
0	0	Level 0 (lowest)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest)

Table 34: Interrupt Priority Registers (*IP0* and *IP1*)

Register	Address	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
IP0	SFR 0xA9	–	–	*IP0[5]*	*IP0[4]*	*IP0[3]*	*IP0[2]*	*IP0[1]*	*IP0[0]*
IP1	SFR 0xB9	–	–	*IP1[5]*	*IP1[4]*	*IP1[3]*	*IP1[2]*	*IP1[1]*	*IP1[0]*

Table 35: Interrupt Polling Sequence



Interrupt Sources and Vectors

Table 36 shows the interrupts with their associated flags and vector addresses.

Table 36: Interrupt Vectors

Interrupt Request Flag	Description	Interrupt Vector Address
IE0	External interrupt 0	0x0003
TF0	Timer 0 interrupt	0x000B
IE1	External interrupt 1	0x0013
TF1	Timer 1 interrupt	0x001B
RI0/TI0	Serial channel 0 interrupt	0x0023
RI1/TI1	Serial channel 1 interrupt	0x0083
IEX2	External interrupt 2	0x004B
IEX3	External interrupt 3	0x0053
IEX4	External interrupt 4	0x005B
IEX5	External interrupt 5	0x0063
IEX6	External interrupt 6	0x006B

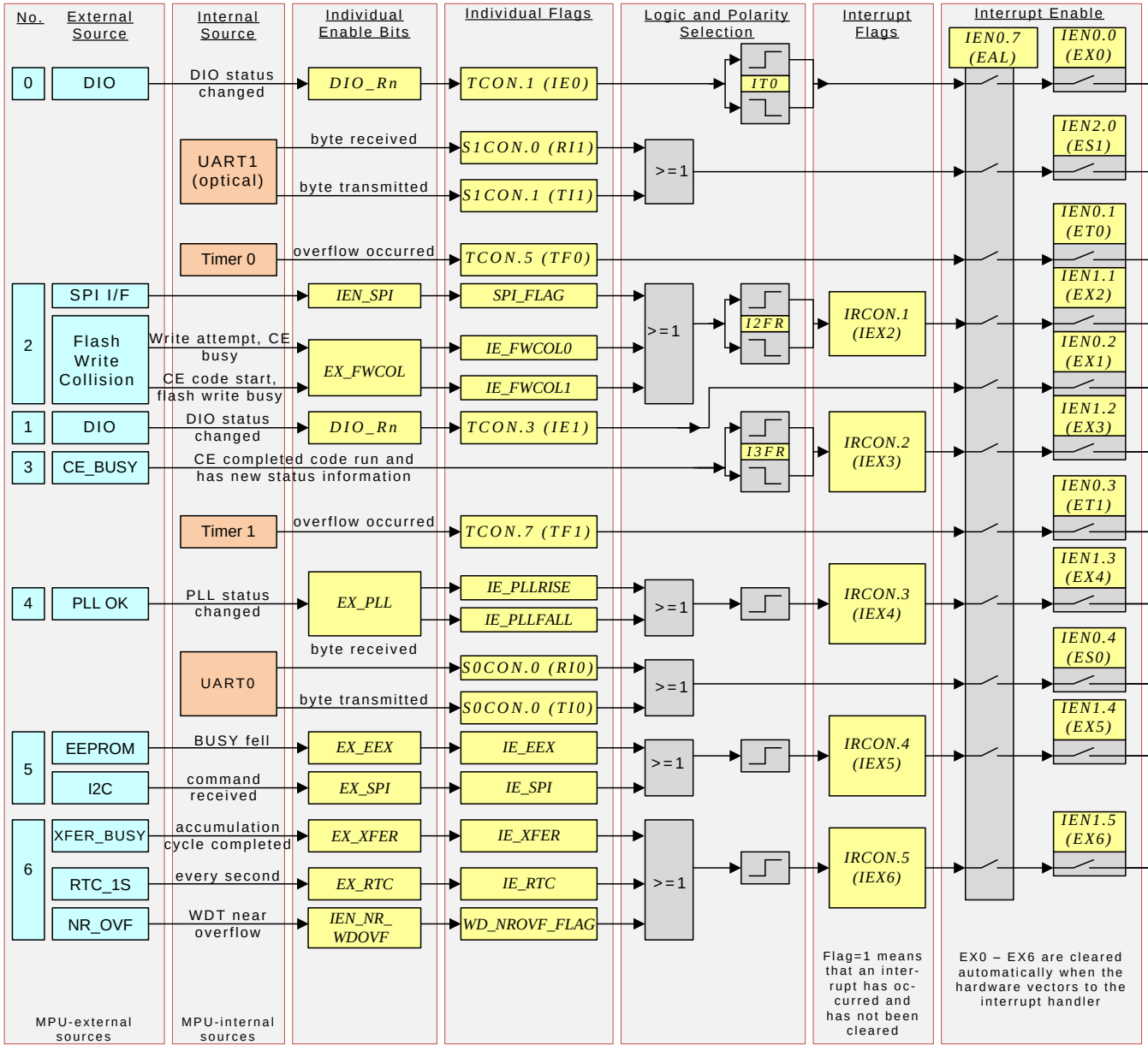


Figure 7: Interrupt Structure

1.4 On-Chip Resources

1.4.1 Oscillator

The 71M6533/71M6534 oscillator drives a standard 32.768 kHz watch crystal. These crystals are accurate and do not require a high-current oscillator circuit. The oscillator has been designed specifically to handle these crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery attached to VBAT.

Oscillator calibration can improve the accuracy of both the RTC and metering. Refer to Section 1.4.3 Real-Time Clock (RTC) for more information.

The oscillator is powered directly and only from VBAT, which therefore must be connected to a DC voltage source. The oscillator requires approximately 100 nA, which is negligible compared to the internal leakage of a battery.

The oscillator may appear to work when VBAT is not connected, but this mode of operation is not recommended.

If VBAT is connected to a drained battery or disconnected, a battery test that sets BME may drain VBAT's supply and cause the oscillator to stop. A stopped oscillator may force the device to reset. Therefore, an unexpected reset during a battery test should be interpreted as a battery failure.

1.4.2 PLL and Internal Clocks

Timing for the device is derived from the 32.768 kHz crystal oscillator output. On-chip timing functions include:

- The MPU clock (CKMPU)
- The emulator clock (2 x CKMPU)
- The clock for the CE (CKCE)
- The clock driving the delta-sigma ADC along with the FIR (CKADC, CKFIR)
- A real time clock (RTC).

The two general-purpose counter/timers contained in the MPU are controlled by CKMPU (see Section 1.3.7 Timers and Counters). Table 37 provides a summary of the clock functions provided.

Table 37: Clock System Summary

Clock	Derived From	MCK Divider / [*M40MHZ, M26MHZ*]			Brownout Mode
		÷2 / [1,0]	÷3 / [0,1]	÷4** / [0,0]	32 kHz
CKPLL	Crystal	80 MHz	80 MHz	80 MHz	off
MCK	CKPLL	40 MHz	26.7 MHz	20 MHz	112 kHz
CKCE	MCK	5 MHz† / 10 MHz†	6.6 MHz	5 MHz	off
CKADC / CKFIR	MCK	5 MHz	6.6 MHz	5 MHz	28 kHz
CKMPU maximum	MCK	10 MHz***	6.6 MHz***	5 MHz***	28 kHz
CK32	MCK	32 kHz	32 kHz	32 kHz	

** Default state at power-up
*** This is the maximum CKMPU frequency. CKMPU can be reduced from this rate using *MPU_DIV*.
† CKCE = 10 MHz when *CE10MHZ* is set, 5 MHz otherwise.

The master clock, MCK, is generated by an on-chip PLL that multiplies the crystal oscillator output frequency (CK32) by 2400 to provide 80 MHz (78.6432 MHz). A divider controlled by the I/O RAM registers *M40MHZ* and *M26MHZ* permits scaling of MCK by ½, ⅓, and ¼. All other clocks are derived from this scaled MCK output (making them multiples of 32768 Hz), and the clock skew is matched so that the rising edges of CKADC, CKCE, CK32, and CKMPU are aligned.

The PLL has a 2x emulator clock which is controlled by *ECK_DIS*. Since clock noise from this feature may disturb the ADC, it is recommended that this option be avoided when possible.

The MPU clock frequency CKMPU is determined by another divider controlled by the I/O RAM register *MPU_DIV* and can be set to MCK/$2^{(MPU\_DIV+2)}$ Hz where *MPU_DIV* varies from 0 to 6. The circuit also generates the 2 x CKMPU clock for use by the emulator. The emulator clock is not generated when *ECK_DIS* is asserted.

During a power-on reset, [*M40MHZ, M26MHZ*] defaults to [0,0], and the MCK divider is set to divide by 4. When [*M40MHZ*, *M26MHZ*] = [1,0], the CE clock frequency may be set to 5 MHz or 10 MHz, using the I/O RAM register *CE10MHZ*. In this mode, the ADC and FIR clock frequencies remain at 5 MHz. When [*M40MHZ*, *M26MHZ*] = [0,1], the CE, ADC, FIR, and MPU clock frequencies are shifted to 6.6 MHz. This increases the ADC sample rate by 33%. In sleep mode, the *M40MHZ* and *M26MHZ* inputs to the clock generator are forced low.

In brownout mode, the clocks are derived from the crystal oscillator, and the clock frequencies are scaled by 7/8.

1.4.3 Real-Time Clock (RTC)

The RTC is driven directly by the crystal oscillator. It is powered by the net RTC_NV (battery-backed up supply). The RTC consists of a counter chain and output registers. The counter chain consists of registers for seconds, minutes, hours, day of week, day of month, month, and year. The RTC is capable of processing leap years. Each counter has its own output register. The RTC registers will not be affected by the reset pin, watchdog timer resets, or by transitions between the battery modes and mission mode.

Whenever the MPU reads the seconds register, all other output registers are automatically updated. Since the RTC clock is not coherent to the MPU clock, the MPU must read the seconds register until two consecutive reads are the same (this requires either 2 or 3 reads). At this point, all RTC output registers will have the correct time. Regardless of the MPU clock speed, RTC reads require one wait state.

RTC time is set by writing to the *RTC_SEC* through *RTC_YR* registers. Each write operation must be preceded by a write operation to the *WE* register in I/O RAM. The value written to the *WE* register is unimportant.

Time adjustments are written to the *RTCA_ADJ*, *PREG* and *QREG* registers. Updates to *PREG* and *QREG* must occur after the one second interrupt, and must be finished before reaching the next one-second boundary. The new values are loaded into the counters at the next one-second boundary.

PREG and *QREG* are separate registers in the device hardware, but the bits are 16-bit contiguous so the MPU firmware can treat them as a single register. A single binary number can be calculated and then loaded into them at the same time.

The 71M6533 and 71M6534 have two rate adjustment mechanisms. The first is an analog rate adjustment, using *RTCA_ADJ*[6:0], which trims the crystal load capacitance. Setting *RTCA_ADJ[6:0]* to 00 minimizes the load capacitance, maximizing the oscillator frequency. Setting *RTCA_ADJ[6:0]* to 0x3F maximizes the load capacitance, minimizing the oscillator frequency. The adjustable capacitance is approximately:

$$C_{ADJ} = \frac{RTCA\_ADJ}{128} \cdot 16.5\,pF$$

The adjustment range is approximately -12 ppm to +22 ppm. The precise amount of adjustment will depend on the crystal properties. The adjustment may occur at any time, and the resulting clock frequency can be measured over a one-second interval.

The second rate adjustment is a digital rate adjust using *PREG* and *QREG*, which can be used to adjust the clock rate up to ± 988 ppm, with a resolution of 3.8 ppm. Updates must occur after a one second in-

terrupt, and must finish before the next one second boundary. The rate adjustment will be implemented starting at the next one-second boundary. Since the LSB results in an adjustment every four seconds, the frequency should be measured over an interval that is a multiple of four seconds.

To adjust the clock rate using the digital rate adjust, the appropriate values must be written to *PREG[16:0]* and *QREG[1:0]*. The default frequency is 32,768 RTCLK cycles per second. To shift the clock frequency by Δ ppm, calculate *PREG* and *QREG* using the following equation:

$$4 \cdot \mathrm{PREG} + \mathrm{QREG} = \mathrm{floor}\left(\frac{32768 \cdot 8}{1 + \Delta \cdot 10^{-6}} + 0.5 \right)$$

For example, for a shift of -988 ppm, 4·*PREG* + *QREG* = 262403 = 0x40103. *PREG* = 0x10040, and *QREG* = 0x03. The default values of *PREG* and *QREG*, corresponding to zero adjustment, are 0x10000 and 0x0, respectively.

Default values for *RTCA_ADJ*, *PREG* and *QREG* should be nominal values, at the center of the adjustment range. Uncalibrated extreme values (zero, for example) can cause incorrect operation.

If the crystal temperature coefficient is known, the MPU can integrate temperature and correct the RTC time as necessary.

The sub-second register of the RTC, *SUBSEC*, can be read by the MPU after the one-second interrupt and before reaching the next one second boundary. *SUBSEC* contains the count remaining, in 1/256 second nominal clock periods, until the next one-second boundary. When the *RST_SUBSEC* bit is written, the *SUBSEC* counter is restarted. Reading and resetting the sub-second counter can be used as part of an algorithm to accurately set the RTC.

When setting the *RTC_SEC* register, it is important to take into account that the associated write operation will be performed only in the next second boundary. This means that to set the *RTC_SEC* register to n, the value n+1 has to be written. Similarly, increment and decrement operations need to be adjusted, i.e. to increment the *RTC_SEC* register that is at count n, the value n+2 has to be written, and to decrement the *RTC_SEC* register that is at count n, the value n has to be written.

1.4.4 Temperature Sensor

The device includes an on-chip temperature sensor for determining the temperature of the bandgap reference. If automatic temperature measurement is not performed by selecting *CHOP_E* = 00, the MPU may request an alternate multiplexer frame containing the temperature sensor output by asserting *MUX_ALT*. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see Section 3.5 Temperature Compensation).

1.4.5 Physical Memory

Flash Memory

The device includes 128 KB (71M6533/H, 71M6534) or 256 KB (71M6534H) of on-chip flash memory. The flash memory primarily contains MPU and CE program code. It also contains images of the CE RAM, MPU RAM and I/O RAM. On power-up, before enabling the CE, the MPU copies these images to their respective locations.

The flash memory is segmented into individually erasable pages that contain 1024 bytes.

Flash space allocated for the CE program is limited to 4096 16-bit words (8 KB). The CE program must begin on a 1 KB boundary of the flash address space. The *CE_LCTN[7:0]* word defines which 1 KB boundary contains the CE code. Thus, the first CE instruction is located at 1024**CE_LCTN[7:0]*.

Flash Write Procedures

The MPU may write to the flash memory. This is one of the non-volatile storage options available to the user in addition to external EEPROM.

FLSH_PWE (flash program write enable) differentiates 80515 data store instructions (MOVX@DPTR,A) between Flash and XRAM writes. This bit must be cleared by the MPU after each byte write operation. Write operations to this bit are inhibited when interrupts are enabled.

The MPU cannot write to flash while the CE is executing its code from flash. Two interrupts warn of collisions between the MPU firmware and the CE timing. If a flash write operation is attempted while the CE is busy, the flash write will not execute and the FW_COL0 interrupt will be issued. If a flash write is still in progress when the CE would otherwise begin a code pass, the code pass is skipped, the write operation is completed, and the FW_COL1 interrupt is issued.
The simplest flash write procedure disables the CE during the write operation and interpolates the metering measurements. However, this results in the loss of at least one second of data, because the CE has to resynchronize with the mains voltage.

There is a brief guaranteed interval (typically 1/32768 s) between CE executions which occurs 2520 times per second. The start of the interval can be detected with the CE_BUSY interrupt which occurs on the falling edge of CE_BUSY (an internal signal measurable from TMUXOUT). However, this guaranteed idle time (30.5 µs) is too short to write a byte which takes 42 µs or to erase a page of flash memory which takes at least 20 ms. Some CE code has substantially longer idle times, but in those cases, firmware interrupt latencies can easily consume the available write time. If a flash write fails in this scheme, the failure can be detected with the FWCOL0 or FWCOL1 interrupt and the write can be retried.

It is practical to pre-erase pages, disable interrupts and poll the CE_BUSY interrupt flag, *IRCON[2]*. This method avoids problems with interrupt latency, but can still result in a write failure if the CE code takes too much time. As mentioned above, polling FWCOL0 and FWCOL1 can detect write failures. However, the speed in a polling write is only 2520 bytes per second and the firmware cannot respond to interrupts.

As an alternative to using flash, a small EEPROM can store data without compromises. EEPROM interfaces are included in the device.

Updating Individual Bytes in Flash Memory

The original state of a flash byte is 0xFF (all ones). Once a value other than 0xFF is written to a flash memory cell, overwriting with a different value usually requires that the cell be erased first. Since cells cannot be erased individually, the page has to be copied to RAM, followed by a page erase. After this, the page can be updated in RAM and then written back to the flash memory.

Flash Erase Procedures

Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

The mass erase sequence is:

1. Write 1 to the *FLSH_MEEN* bit (SFR address 0xB2[1].
2. Write the pattern 0xAA to *FLSH_ERASE* (SFR address 0x94).

The mass erase cycle can only be initiated when the ICE port is enabled.

The page erase sequence is:

1. Write the page address to *FLSH_PGADR* (SFR address 0xB7[7:2].
2. Write the pattern 0x55 to *FLSH_ERASE* (SFR address 0x94).

Bank-Switching

The program memory of the 71M6533/71M6534 consists of a fixed lower bank of 32 KB, addressable at 0x0000 to 0x7FFF plus an upper banked area of 32 KB, addressable at 0x8000 to 0xFFFF. The I/O RAM register *FL_BANK*is used to switch one of four (71M6533/H, 71M6534) or eight (71M6534H) memory banks of 32 KB each into the address range from 0x8000 to 0xFFFF. Note that when *FL_BANK* = 0, the upper bank is the same as the lower bank. Table 38 illustrates the bank switching mechanism.

Table 38: Bank Switching with *FL_BANK[2:0]*

71M6533/H 71M6534 *FL_BANK[1:0]*	71M6534H *FL_BANK[2:0]*	Address Range for Lower Bank (0x000-0x7FFF)	Address Range for Upper Bank (0x8000-0xFFFF)
00	000	0x0000-0x7FFF	0x0000-0x7FFF
01	001	0x0000-0x7FFF	0x8000-0xFFFF
10	010	0x0000-0x7FFF	0x10000-0x17FFF
11	011	0x0000-0x7FFF	0x18000-0x1FFFF
Not applicable in 71M6533/H and 71M6534	100	0x0000-0x7FFF	0x20000-0x27FFF
	101	0x0000-0x7FFF	0x28000-0x2FFFF
	110	0x0000-0x7FFF	0x30000-0x37FFF
	111	0x0000-0x7FFF	0x38000-0x3FFFF

Program Security

When enabled, the security feature limits the ICE to global flash erase operations only. All other ICE operations are blocked. This guarantees the security of the user's MPU and CE program code. Security should be enabled by MPU code that is executed during the pre-boot interval (60 CKMPU cycles before the primary boot sequence begins). Once security is enabled, the only way to disable it is to perform a global erase of the flash, followed by a chip reset.

The first 60 cycles of the MPU boot code are called the pre-boot phase because during this phase the ICE is inhibited. A read-only status bit, *PREBOOT*, identifies these cycles to the MPU. Upon completion of pre-boot, the ICE can be enabled and is permitted to take control of the MPU.

The security enable bit, *SECURE,* is reset whenever the chip is reset. Hardware associated with the bit permits only ones to be written to it. Thus, pre-boot code may set *SECURE* to enable the security feature but may not reset it. Once *SECURE* is set, the pre-boot code is protected and no external read of program code is possible

Specifically, when *SECURE* is set, the following applies:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory, the preferred location for the user's pre-boot code, may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase.
- Writes to page zero, whether by MPU or ICE are inhibited.

MPU/CE RAM

The 71M6533 and 71M6534 includes 4K-bytes of static RAM memory on-chip (XRAM) plus 256 bytes of internal RAM in the MPU core. The 4K-bytes of static RAM are used for data storage for both MPU and CE operations.

1.4.6 UART and Optical Interface

In addition to the regular UART (UART0) the device includes an interface to implement an IR/optical port. The pin OPT_TX is designed to directly drive an external LED for transmitting data on an optical link. The pin OPT_RX has the same threshold as the RX pin, but can also be used to sense the input from an external photo detector used as the receiver for the optical link. OPT_TX and OPT_RX are connected to a dedicated UART port (UART1).

The OPT_TX and OPT_RX pins can be inverted with configuration bits *OPT_TXINV* and *OPT_RXINV*, respectively. Additionally, the OPT_TX output may be modulated at 38 kHz. Modulation is available when system power is present (i.e. not in BROWNOUT mode). The *OPT_TXMOD* bit enables modulation. The duty cycle is controlled by *OPT_FDC[1:0],* which can select 50%, 25%, 12.5%, and 6.25% duty cycle. A 6.25% duty cycle means OPT_TX is low for 6.25% of the period. Figure 8 illustrates the OPT_TX generator.

When not needed for the optical UART, the OPT_TX pin can alternatively be configured as DIO2, WPULSE, or VARPULSE. The configuration bits are *OPT_TXE[1:0]*. Likewise, OPT_RX can alternately be configured as DIO_1. Its control is *OPT_RXDIS.*

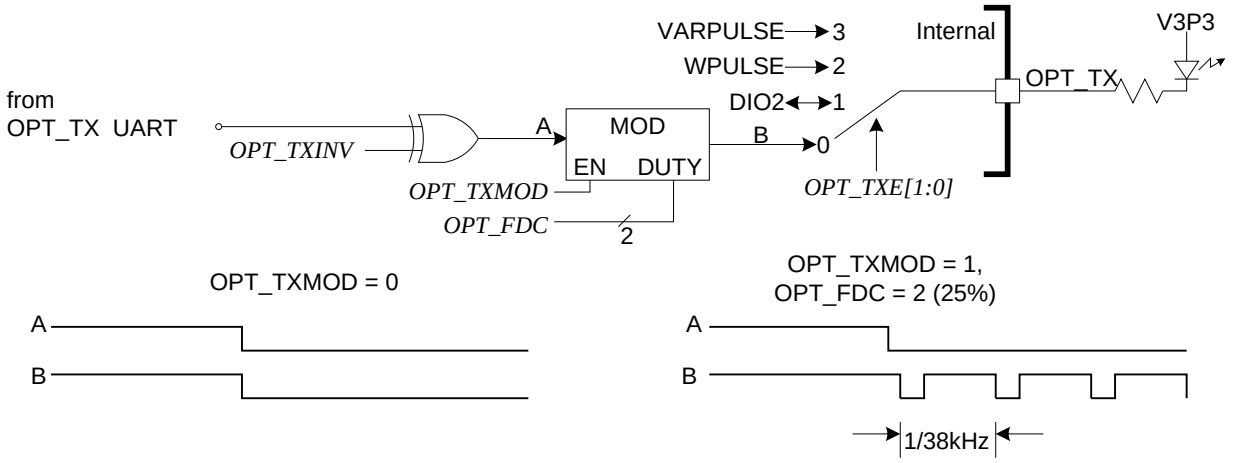


Figure 8: Optical Interface

In the 71M6534, a multiplexer allows the selection of alternate pins DIO18/MTX and DIO22/RTX for UART1. This function is controlled with the I/O RAM registers *UMUX_E* and *UMUX_SEL*.

1.4.7 Digital I/O

The device includes up to 40 pins (71M6533) or 53 pins (71M6534) of general purpose digital I/O. These pins are compatible with 5 V inputs (no current limiting resistors are needed). The Digital I/O pins can be categorized as follows:

- Dedicated DIO pins (5 pins): DIO3, DIO56, DIO57, DIO58, PB
- DIO/LCD segment pins
  - A total of 33 pins for the 71M6533:
    DIO4/SEG24 - DIO11/SEG31 (8 pins)
    DIO13/SEG33 - DIO21/SEG41 (9 pins)
    DIO23/SEG43 – DIO27/SEG47 (5 pins)
    DIO29/SEG49 - DIO30/SEG50 (2 pins)
    DIO41/SEG61 (1 pin)
    DIO43/SEG63 - DIO45/SEG65 (3 pins)
    DIO47/SEG67 – DIO51/SEG71 (5 pins)
  - A total of 46 pins for the 71M6534:
    DIO4/SEG24 – DIO30/SEG50 (27 pins)
    DIO36/SEG56 – DIO39/SEG59 (4 pins)
    DIO41/SEG61 – DIO55/SEG75 (15 pins)
- DIO pins combined with other functions (2 pins): DIO2/OPT_TX, DIO1/OPT_RX

On reset or power-up, all DIO pins are inputs until they are configured for the desired direction under MPU control. The pin function can be configured by the I/O RAM registers *LCD_BITMAPn*. Setting *LCD_BITMAPn* = 1 configures the pin for LCD, setting *LCD_BITMAPn* = 0 configures it for DIO.

Once a pin is configured as DIO, it can be configured independently as an input or output with the *DIO_DIR* bits or the *LCD_SEGn* registers. Input and output data are written to or read from the pins using SFR registers *P0, P1*, and *P2*.

Table 39 shows all the DIO pins with their configuration, direction control and data registers. Table entries marked with an asterisk and grayed are applicable to the 71M6534 only.

Table 39: Data/Direction Registers and Internal Resources for DIO Pin Groups

DIO	PB	1	2	3	4	5	6	7	8	9	10	11	12*	13	14	15
LCD Segment	–	–	–	–	24	25	26	27	28	29	30	31	32*	33	34	35
71M6533 Pin #	97	91	3	17	60	61	62	63	67	68	69	70	–	44	29	30
71M6534 Pin #	114	109	3	22	70	71	72	73	77	78	79	80	120	50	35	36
Configuration (DIO or LCD segment)	Always DIO				0	1	2	3	4	5	6	7	0*	1	2	3
					LCD_BITMAP[31:24]								*LCD_BITMAP[39:32]*			
Data Register	0	1	2	3	4	5	6	7	0	1	2	3	4*	5	6	7
	DIO0 = P0 (SFR 0x80)								*DIO1 = P1* (SFR 0x90)							
Direction Register 0 = input, 1 = output	–	1	2	3	4	5	6	7	0	1	2	3	4*	5	6	7
	DIO_DIR0 (SFR 0xA2)								*DIO_DIR1* (SFR 0x91)							
Internal Resources Configurable	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	–

DIO	16	17	18	19	20	21	22*	23	24	25	26	27	28*	29	30	–
LCD Segment	36	37	38	39	40	41	42*	43	44	45	46	47	48*	49	50	–
71M6533 Pin #	33	12	13	64	65	66	–	54	46	43	42	41	–	32	35	–
71M6534 Pin #	39	17	18	74	75	76	115	64	52	49	48	47	81	38	41	
Configuration (DIO or LCD segment)	4	5	6	7	0	1	2*	3	4	5	6	7	0*	1	2	–
	LCD_BITMAP[39:32]				*LCD_BITMAP[47:40]*								*LCD_BITMAP[55:48]*			
Data Register	0	1	2	3	4	5	6*	7	0	1	2	3	4*	5	6	–
	DIO2 = P2 (SFR 0xA0)								*DIO3 = P3* (SFR 0xB0)							
Direction Register 0 = input, 1 = output	0	1	2	3	4	5	6*	7	*LCD_SEG44[3]*	*LCD_SEG45[3]*	*LCD_SEG46[3]*	*LCD_SEG47[3]*	*LCD_SEG48[3]**	*LCD_SEG49[3]*	*LCD_SEG50[3]*	
	DIO_DIR2 (SFR 0xA1)															

DIO	–	–	–	–	36*	37*	38*	39*	–	41	42*	43	44	45	46*	47
LCD Segment	–	–	–	–	56*	57*	58*	59*	–	61	62*	63	64	65	66*	67
71M6533 Pin #	–	–	–	–	–	–	–	–	–	99	–	40	31	38	–	22
71M6534 Pin #	–	–	–	–	87	88	89	90	–	117	118	46	37	44	5	27
Configuration (DIO or LCD segment)	–	–	–	–	0*	1*	2*	3*	–	5	6*	7	0	1	2*	3
	LCD_BITMAP[55:48]				*LCD_BITMAP[63:56]*								*LCD_BITMAP[71:64]*			
Data Register	–	–	–	–	*LCD_SEG56[0]**	*LCD_SEG57[0]**	*LCD_SEG58[0]**	*LCD_SEG59[0]**	–	*LCD_SEG61[0]*	*LCD_SEG62[0]**	*LCD_SEG63[0]*	*LCD_SEG64[0]*	*LCD_SEG65[0]*	*LCD_SEG66[0]**	*LCD_SEG67[0]*
Direction Register 0 = input, 1 = output	–	–	–	–	*LCD_SEG56[3]**	*LCD_SEG57[3]**	*LCD_SEG58[3]**	*LCD_SEG59[3]**		*LCD_SEG61[3]*	*LCD_SEG62[3]**	*LCD_SEG63[3]*	*LCD_SEG64[3]*	*LCD_SEG65[3]*	*LCD_SEG66[3]**	*LCD_SEG67[3]*

DIO	48	49	50	51	52*	53*	54*	55*	56	57	58
LCD Segment	**68**	**69**	**70**	**71**	**72***	**73***	**74***	**75***	**–**	**–**	**–**
71M6533 Pin #	**23**	**24**	**25**	**50**	**–**	**–**	**–**	**–**	**14**	**15**	**16**
71M6534 Pin #	**28**	**29**	**30**	**56**	**57**	**58**	**59**	**60**	**19**	**20**	**21**
Configuration (DIO or LCD segment)	4	5	6	7	0*	1*	2*	3*	Always DIO		
	LCD_BITMAP[71:64]				*LCD_BITMAP[80:72]*						
Data Register	*LCD_SEG68[0]*	*LCD_SEG69[0]*	*LCD_SEG70[0]*	*LCD_SEG71[0]*	*LCD_SEG72[0]**	*LCD_SEG73[0]**	*LCD_SEG74[0]**	*LCD_SEG75[0]**	*DIO_56[4]*	*DIO_57[4]*	*DIO_58[4]*
Direction Register 0 = input, 1 = output	*LCD_SEG68[3]*	*LCD_SEG69[3]*	*LCD_SEG70[3]*	*LCD_SEG71[3]*	*LCD_SEG72[3]**	*LCD_SEG73[3]**	*LCD_SEG74[3]**	*LCD_SEG75[3]**	*DIO_DIR56[7]*	*DIO_DIR57[7]*	*DIO_DIR58[7]*

See the tables in the I/O RAM Description (Section 4.2) for exact bit locations. For example, DIO43 is controlled by *LCD_SEG63*[0] which resolves to I/O RAM location 0x2045[4].

DIO24 and higher do not have SFR registers for direction control. DIO36 and higher do not have SFR registers for data access. The direction control of these pins is achieved with the *LCD_SEGn[3]* registers and data access is controlled with the *LCD_SEGn[0]* registers in I/O RAM. DIO56 through DIO58 are dedicated DIO pins. They are controlled with *DIO_DIR56[7]* through *DIO_DIR58[7]* (direction) and with *DIO_56[4]* through *DIO_58[4]* (data) in I/O RAM.

Since the control for DIO_24 through DIO_55 is shared with the control for LCD segments, the firmware must take care not to disturb the DIO pins when accessing the LCD segments and vice versa. Usually, this requires reading the I/O RAM register, applying a mask and writing back the modified byte.

The PB pin is a dedicated digital input. In addition, if the optical UART is not used, OPT_TX and OPT_RX can be configured as dedicated DIO pins, DIO1and DIO2, respectively (see Section 1.4.6 UART and Optical Interface).

DIO4 and DIO5 can be configured to implement the EEPROM Interface.

Additionally, if DIO6 and DIO7 are configured as DIO and defined as outputs, they can be used as dedicated pulse outputs (WPULSE = DIO6, VARPULSE = DIO7) using the *DIO_PW* and *DIO_PV* registers. In this case, DIO6 and DIO7 are under CE control. Similarly, DIO8 and DIO9 can be declared pulse outputs (XPULSE = DIO8, YPULSE = DIO9).

Tracking DIO pins configured as outputs is useful for pulse counting without external hardware. Either the interrupts or the counter/timer clocks can be used to count the pulse outputs, or interrupt on the CE's power failure output.

A 3-bit configuration word, I/O RAM register *DIO_Rn* (0x2009[2:0] through 0x200E[6:4]) can be used for certain pins (when configured as DIO) to individually assign an internal resource such as an interrupt or a timer control (*DIO_RRX* configures the RX pin). This way, DIO pins can be tracked even if they are configured as outputs. See Table 39 for DIO pins available for this option. Table 40 lists the internal resources which can be assigned using *DIO_R0* (also called *DIO_RPB*) through *DIO_R7*. If more than one input is connected to the same resource, the resources are combined using a logical OR.

Table 40: Selectable Resources using the *DIO_Rn* Bits

*DIO_R*n	Resource Selected for DIO Pin
0	None
1	Reserved
2	T0 (counter0 clock)
3	T1 (counter1 clock)
4	High priority I/O interrupt (INT0 rising)
5	Low priority I/O interrupt (INT1 rising)
6	High priority I/O interrupt (INT0 falling)
7	Low priority I/O interrupt (INT1 falling)

When driving LEDs, relay coils etc., the DIO pins should sink the current into GNDD (as shown in Figure 9, right), not source it from V3P3D (as shown in Figure 9, left). This is due to the resistance of the internal switch that connects V3P3D to either V3P3SYS or VBAT.

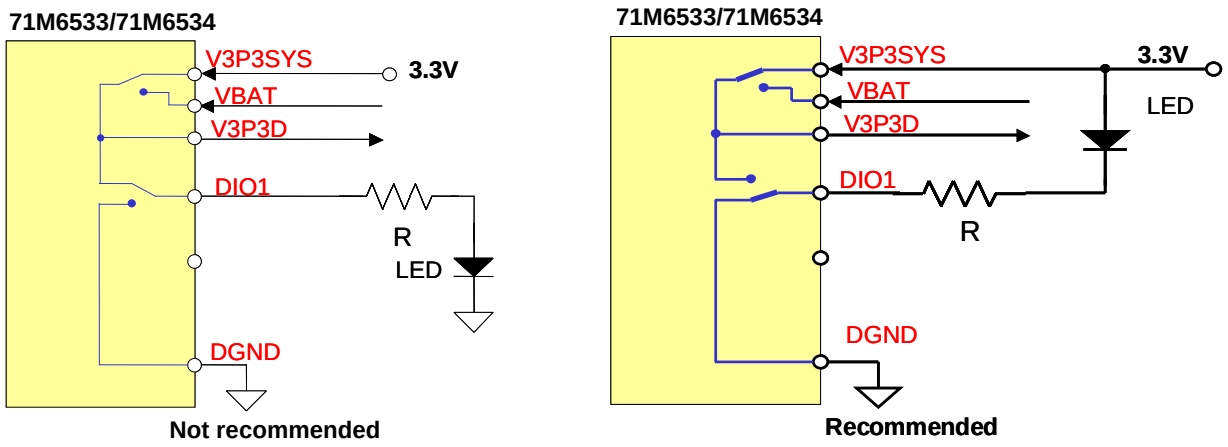


Figure 9: Connecting an External Load to DIO Pins

1.4.8 LCD Drivers

The device contains a total of 57 (71M6533) or 75 (71M6534) dedicated and multiplexed LCD drivers, which are grouped as follows:

- 15 dedicated LCD segment drivers (SEG0 to SEG2, SEG8, SEG12 to SEG18, SEG20 to SEG23)
- 4 drivers multiplexed with the SPI port (SEG3 to SEG6)
- 2 drivers multiplexed with MUX_SYNC and CKTEST (SEG7 and SEG19)
- 3 or 8 drivers multiplexed with the ICE interface
  - 71M6533 – 3 drivers (SEG9 to SEG11)
  - 71M6534 – 8 drivers (SEG9 to SEG11 and SEG51 to SEG55)
- 33 or 46 multi-use LCD/DIO pins described in Section 1.4.7 Digital I/O
  - 71M6533 – 33 pins
  - 71M6534 – 46 pins

With a minimum of 15 driver pins always available and a total of 57 (71M6533) or 75 (71M6534) driver pins in the maximum configuration, the device is capable of driving between 60 to 228 pixels (71M6533) or 60 to 300 pixels (71M6534) of an LCD display with 25% duty cycle. At eight pixels per digit, this corresponds to 7.5 to 28 digits for the 71M6533 or 7.5 to 37 digits for the 71M6534.

For each multi-use pin, the corresponding *LCD_BITMAP*[] register (as described in Section 1.4.7 Digital I/O) is used to select the pin for DIO or LCD operation. The mapping of the *LCD_BITMAP*[] registers is specified in Section 4.1 I/O RAM Map –Functional Order.

LCD segment data is written to the *LCD_SEGn*[3:0] I/O RAM registers as described in section 4.2 I/O RAM Description – Alphabetical Order. Note that even though the register names call out bit numbers 3 to 0 some registers use physical bits 4 to 7.

The LCD drivers are grouped into four commons (COM0 – COM3) and up to 56 (71M6533) or 74 (71M6534) segment drivers. The LCD interface is flexible and can drive 7-segment digits, 14- segments digits or enunciator symbols.

The segment driver SEG18 can be configured to blink at either 0.5 Hz or 1 Hz. The blink rate is controlled by *LCD_Y*. There can be up to four pixels/segments connected to this driver pin. The I/O RAM register *LCD_BLKMAP18[3:0]* identifies which pixels, if any, are to blink.

The LCD bias may be compensated for temperature using the *LCD_DAC* bits in I/O RAM. The bias may be adjusted from 1.4 V below the 3.3 V supply (V3P3SYS in mission mode and brownout modes, VBAT in LCD mode). When the *LCD_DAC* bits are set to 000, the DAC is bypassed and powered down. This can be used to reduce current in LCD mode.

1.4.9 Battery Monitor

The battery voltage is measured by the ADC during alternative MUX frames if the *BME* (Battery Measure Enable) bit is set. While *BME* is set, an on-chip 45 kΩ load resistor is applied to the battery and a scaled fraction of the battery voltage is applied to the ADC input. After each alternative MUX frame, the result of the ADC conversion is available at XRAM address 0x07. *BME* is ignored and assumed zero when system power is not available.

✓ If VBAT is connected to a drained battery or disconnected, a battery test that sets *BME* may drain VBAT's supply and cause the oscillator to stop. A stopped oscillator may force the device to reset. Therefore, an unexpected reset during a battery test should be interpreted as a battery failure.

Battery measurement is not very linear but is very reproducible. The best way to perform the calibration is to set the battery input to the desired failure voltage and then have the MPU firmware record that measurement. After this, the MPU firmware's battery measurement logic may use the recorded value as the battery failure limit. The same value can also be a calibration offset for any battery voltage display.

See Section 5.4.5 Battery Monitor for details regarding the ADC LSB size and the conversion accuracy.

1.4.10 EEPROM Interface

The 71M6533 and 71M6534 provides hardware support for either a two-pin or a three-wire (µ-wire) type of EEPROM interface. The interfaces use the *EECTRL* and *EEDATA* registers for communication.

Two-pin EEPROM Interface

The dedicated 2-pin serial interface communicates with external EEPROM devices. The interface is multiplexed onto the DIO4 (SCK) and DIO5 (SDA) pins and is selected by setting *DIO_EEX* = 1. The MPU communicates with the interface through the SFR registers *EEDATA* and *EECTRL*. If the MPU wishes to write a byte of data to the EEPROM, it places the data in *EEDATA* and then writes the Transmit code to *EECTRL*. This initiates the transmit operation which is finished when the *BUSY* bit falls. INT5 is also asserted when *BUSY* falls. The MPU can then check the *RX_ACK* bit to see if the EEPROM acknowledged the transmission.

A byte is read by writing the Receive command to *EECTRL* and waiting for the *BUSY* bit to fall. Upon completion, the received data is in *EEDATA*. The serial transmit and receive clock is 78 kHz during each transmission, and then holds in a high state until the next transmission. The *EECTRL* bits when the two-pin interface is selected are shown in Table 41.

Table 41: *EECTRL* Bits for 2-pin Interface

Status Bit	Name	Read/ Write	Reset State	Polarity	Description
7	*ERROR*	R	0	Positive	1 when an illegal command is received.
6	*BUSY*	R	0	Positive	1 when serial data bus is busy.
5	*RX_ACK*	R	1	Negative	0 indicates that the EEPROM sent an ACK bit.
4	*TX_ACK*	R	1	Negative	0 indicates when an ACK bit has been sent to the EEPROM.
3:0	*CMD[3:0]*	W	0000	Positive	

CMD[3:0]	Operation
0000	No-op command. Stops the I^2C clock (SCK, DIO4). If not issued, SCK keeps toggling.
0010	Receive a byte from the EEPROM and send ACK.
0011	Transmit a byte to the EEPROM.
0101	Issue a STOP sequence.
0110	Receive the last byte from the EEPROM and do not send ACK.
1001	Issue a START sequence.
Others	No operation, set the *ERROR* bit.

The EEPROM interface can also be operated by controlling the DIO4 and DIO5 pins directly. In this case, a resistor has to be used in series with SDA to avoid data collisions due to limits in the speed at which the SDA pin can be switched from output to input. However, controlling DIO4 and DIO5 directly is discouraged, because it may tie up the MPU to the point where it may become too busy to process interrupts.

Three-wire (µ-Wire) EEPROM Interface

A 500 kHz three-wire interface, using SDATA, SCK, and a DIO pin for CS is available. The interface is selected by setting *DIO_EEX* = 3. The *EECTRL* bits when the three-wire interface is selected are shown in Table 42. When *EECTRL* is written, up to 8 bits from *EEDATA* are either written to the EEPROM or read from the EEPROM, depending on the values of the *EECTRL* bits.

CAUTION The µ-Wire EEPROM interface is only functional when *MPU_DIV[2:0]* = 000.

Table 42: *EECTRL* Bits for the 3-wire Interface

Control Bit	Name	Read/ Write	Description
7	*WFR*	W	Wait for Ready. If this bit is set, the trailing edge of BUSY will be delayed until a rising edge is seen on the data line. This bit can be used during the last byte of a Write command to cause the INT5 interrupt to occur when the EEPROM has finished its internal write sequence. This bit is ignored if HiZ=0.
6	*BUSY*	R	Asserted while the serial data bus is busy. When the BUSY bit falls, an INT5 interrupt occurs.
5	*HiZ*	W	Indicates that the SD signal is to be floated to high impedance immedi-ately after the last SCK rising edge.
4	*RD*	W	Indicates that *EEDATA* is to be filled with data from EEPROM.

3:0	*CNT[3:0]*	W	Specifies the number of clocks to be issued. Allowed values are 0 through 8. If RD=1, CNT bits of data will be read MSB first, and right justified into the low order bits of *EEDATA*. If RD=0, CNT bits will be sent MSB first to the EEPROM, shifted out of the MSB of *EEDATA*. If *CNT[3:0]* is zero, SDATA will simply obey the HiZ bit.

The timing diagrams in Figure 10 through Figure 14 describe the 3-wire EEPROM interface behavior. All commands begin when the *EECTRL* register is written. Transactions start by first raising the DIO pin that is connected to CS. Multiple 8-bit or less commands such as those shown in Figure 10 through Figure 14 are then sent via *EECTRL* and *EEDATA*.

When the transaction is finished, CS must be lowered. At the end of a Read transaction, the EEPROM will be driving SDATA, but will transition to HiZ (high impedance) when CS falls. The firmware should then immediately issue a write command with CNT=0 and HiZ=0 to take control of SDATA and force it to a low-Z state.

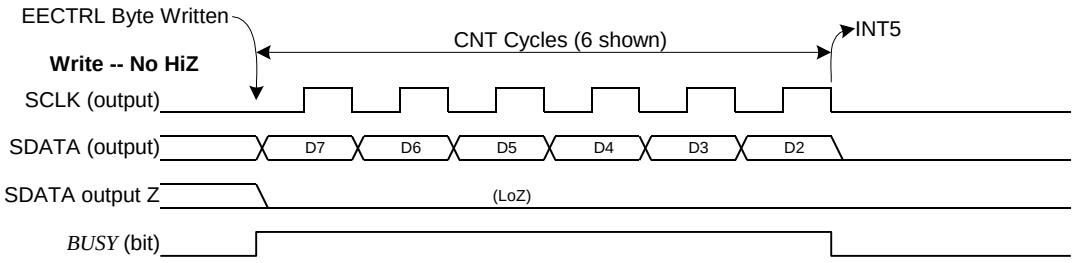


Figure 10: 3-wire Interface. Write Command, HiZ=0.

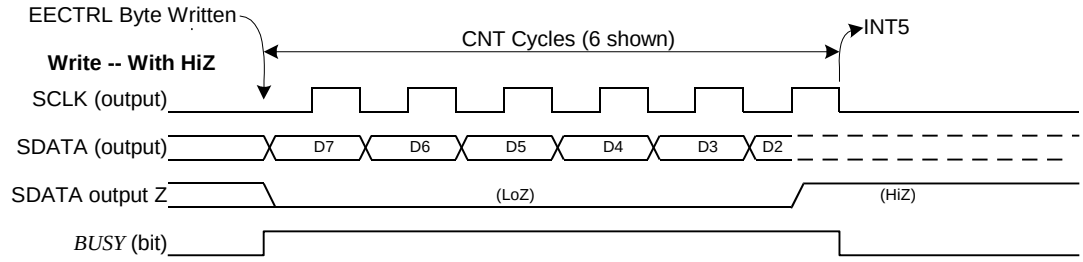


Figure 11: 3-wire Interface. Write Command, HiZ=1

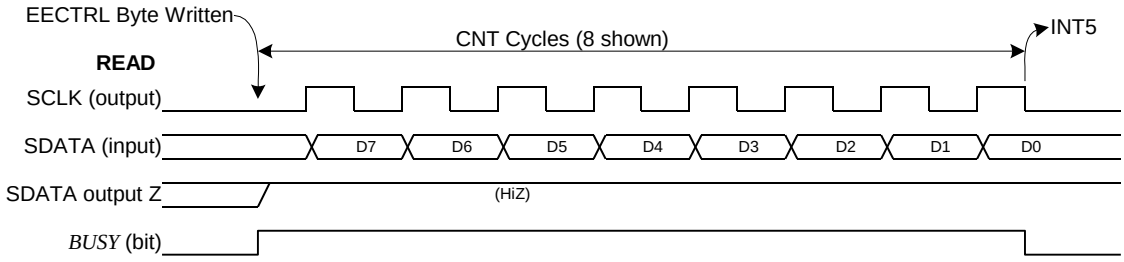


Figure 12: 3-wire Interface. Read Command.

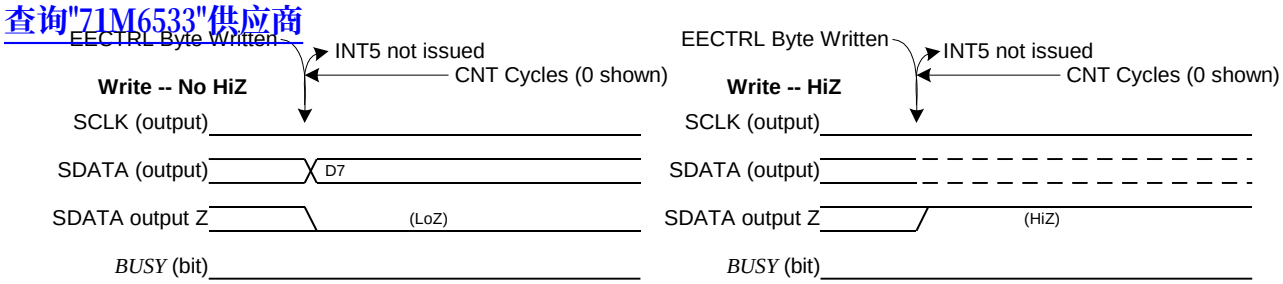


Figure 13: 3-Wire Interface. Write Command when CNT=0

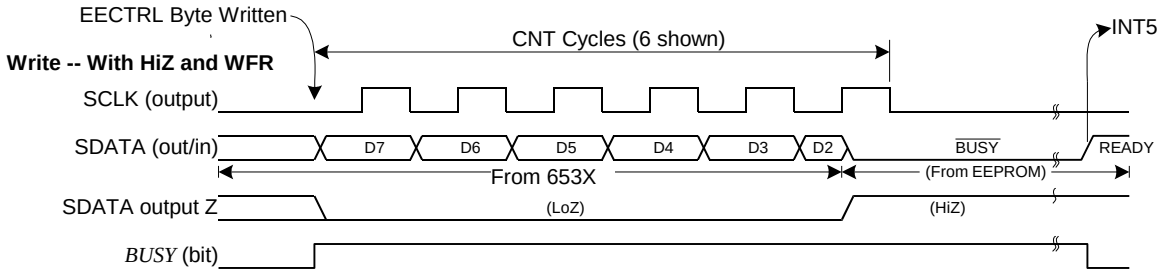


Figure 14: 3-wire Interface. Write Command when HiZ=1 and WFR=1.

1.4.11 SPI Slave Port

The slave SPI port communicates directly with the MPU data bus and is able to read and write Data RAM locations. It is also able to send commands to the MPU. The interface to the slave port consists of the PCSZ, PCLK, PSDI and PSDO pins. These pins are multiplexed with the LCD segment driver pins SEG3 to SEG6. The port pins default to LCD driver pins. The port is enabled by setting the *SPE* bit in I/O RAM.

Access to I/O RAM (Configuration RAM) should not be attempted via the SPI Port.

A typical SPI transaction is as follows: While PCSZ is high, the port is held in an initialized/reset state. During this state, PSDO is held in HiZ state and all transitions on PCLK and PSDI are ignored. When PCSZ falls, the port will begin the transaction on the first rising edge of PCLK. A transaction consists of an 8-bit command, a 16-bit address, and then one or more bytes of data. The transaction ends when PCSZ is raised. Some transactions may consist of a command only.

The last issued SPI command and address (if part of the command) are available to the MPU in registers *SP_CMD* and *SP_ADDR*.

The SPI port supports data transfers at 1 Mb/s in mission mode, and 16 kb/s in brownout mode. Figure 15 illustrates the read and write timing of the SPI Interface. The SPI commands are described in Table 43.

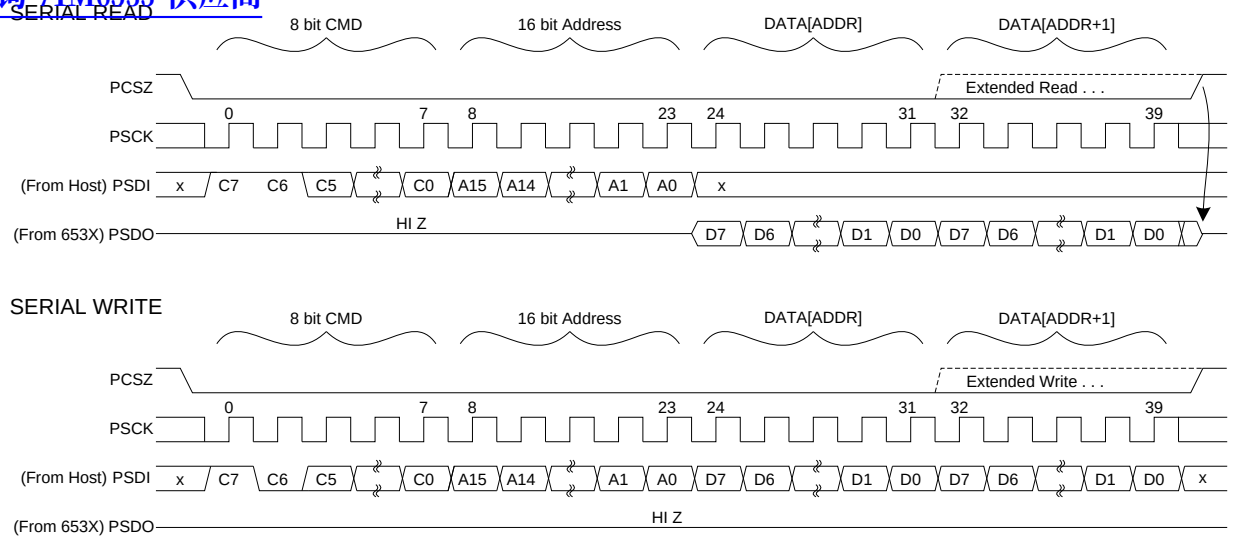


Figure 15: SPI Slave Port: Typical Read and Write operations

Table 43: SPI Command Description

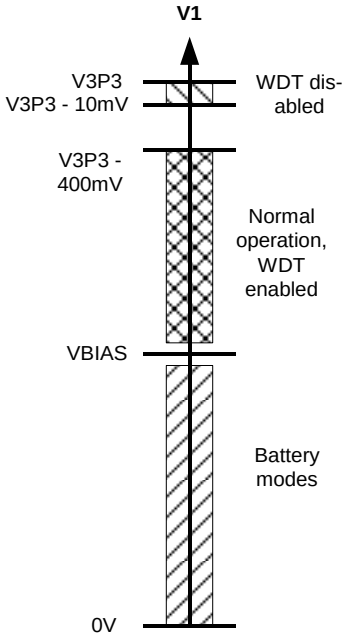
Command	Description
11xx xxxx ADDR Byte0 ... ByteN	Read data starting at ADDR. The ADDR will auto-increment until PCSZ is raised. Upon completion: *SP__CMD*=11xx xxxx, *SP_ADDR*=ADDR+N+1. No MPU interrupt is generated if the command is 1100 0000. Otherwise, an SPI interrupt is generated.
10xx xxxx ADDR Byte0 ... ByteN	Write data starting at ADDR. The ADDR will auto-increment until PCSZ is raised. Upon completion: *SP_CMD*=10xx xxxx, *SP_ADDR*=ADDR+N+1. No MPU interrupt is generated if the command is 1000 0000. Otherwise, an SPI interrupt is generated.

Possible applications for the SPI interface are:

1) An external host reads data from CE locations to obtain metering information. This can be used in applications where the 71M6533 or 71M6534 function as a smart front-end with preprocessing capability. Since the addresses are in 16-bit format, any type of XRAM data can be accessed: CE, MPU, I/O RAM, but not SFRs or the 80515-internal register bank.
2) A communication link can be established via the SPI interface: By writing into MPU memory locations, the external host can initiate and control processes in the 71M6533/71M6534 MPU. Writing to a CE or MPU location normally generates an interrupt, a function that can be used to signal to the MPU that the byte that had just been written by the external host must be read and processed. Data can also be inserted by the external host without generating an interrupt.
3) An external DSP can access front-end data generated by the ADC. This mode of operation uses the 71M6533 or 71M6534 as an analog front-end (AFE).

1.4.12 Hardware Watchdog Timer

An independent, robust, fixed-duration, watchdog timer (WDT) is included in the 71M6533/71M6534. It uses the RTC crystal oscillator as its time base and must be refreshed by the MPU firmware at least every 1.5 seconds. When not refreshed on time, the WDT overflows and the part is reset as if the RESET pin were pulled high, except that the I/O RAM bits will be in the same state as after a wake-up from SLEEP or LCD modes (see the I/O RAM description in Section 4.2 for a list of I/O RAM bit states after RESET and wake-up). 4100 oscillator cycles (or 125 ms) after the WDT overflow, the MPU will be launched from program address 0x0000.



A status bit, *WD_OVF*, is set when the WDT overflow occurs. This bit is powered by the nonvolatile supply and can be read by the MPU when WAKE rises to determine if the part is initializing after a WDT overflow event or after a power-up. After it is read, the MPU firmware must clear *WD_OVF*. The *WD_OVF* bit is also cleared by the RESET pin.

There is no internal digital state that deactivates the WDT. The WDT can be disabled by tying the V1 pin to V3P3 (see Figure 16). Of course, this also deactivates V1 power fault detection. Since there is no method in firmware to disable the crystal oscillator or the WDT, it is guaranteed that whatever state the part might find itself in, upon watchdog overflow, the part will be reset to a known state.

Asserting ICE_E will also deactivate the WDT. This is the only method that will work in BROWNOUT mode. In normal operation, the WDT is reset by periodically writing a one to the *WDT_RST* bit.

Figure 16: Functions defined by V1

The watchdog timer is also reset when the internal signal WAKE=0 (see Section 2.5 Wake Up Behavior).

If enabled with the *IEN_WD_NROVF* register in I/O RAM, an interrupt occurs roughly 1 ms before the WDT resets the chip. This can be used to determine the cause of a WDT reset since it allows the code to log its state (e.g. the current PC value, loop counters, flags, etc.) before a WDT reset occurs.

1.4.13 Test Ports (TMUXOUT Pin)

One of the digital or analog signals listed in Table 44 can be selected to be output on the TMUXOUT pin. The function of the multiplexer is controlled with the I/O RAM register *TMUX* (0x20AA[4:0]), as shown in Table 44.

The TMUXOUT pin may be used for diagnosis purposes or in production test. The RTC 1-second output may be used to calibrate the crystal oscillator. The RTC 4-second output provides even higher precision.

Table 44: *TMUX[4:0]* Selections

TMUX[4:0]	Mode	Function
0	Analog	DGND
1	Analog	Reserved
2	Analog	DGND
3	Analog	Reserved
4	Analog	PLL_2P5
5	Analog	Output of the 2.5 V low-power regulator
6	Analog	Internal VBIAS voltage (nominally 1.6V)
7	Analog	Not used
8 - 0x0F	–	Reserved
0x10	Digital	RTC 1-second output
0x11	Digital	RTC 4-second output
0x12	–	Not used
0x13	Digital	V1 comparator output, synchronized to RTCLK
0x14	Digital	Real-time output from the CE
0x15	Digital	WDTR_EN (comparator 1 output AND V1LT3)
0x16	Digital	V2 comparator output (71M6534 only)
0x17	Digital	V1 comparator output, unsynchronized
0x18	Digital	RXD (from Optical interface, w/ optional inversion)
0x19	Digital	MUX_SYNC
0x1A	–	Not used
0x1B	Digital	CKMPU (MPU clock)
0x1C	Digital	Pulse output
0X1D	Digital	RTCLK (output of the oscillator circuit, nominally 32,786Hz)
0X1E	Digital	CE_BUSY (busy interrupt generated by CE, 396µs)
0X1F	Digital	XFER_BUSY (transfer busy interrupt generated by the CE, nominally every 999.7ms)

1.4.14 V2 Comparator (71M6534/6534H only)

The 71M6534/6534H offers a pin that is connected to an internal comparator. The voltage applied to this pin is compared to the internal reference voltage (VBIAS). If the voltage at the V2 pin is above VBIAS, the comparator output will be high (1). The comparator output is reflected at the TMUXOUT pin, when 0x16 is selected for *TMUX[4:0]*.

2 Functional Description

2.1 Theory of Operation

The energy delivered by a power source into a load can be expressed as:

$$E = \int_0^t V(t)I(t)dt$$

Assuming phase angles are constant, the following formulae apply:

- P = Real Energy [Wh] = V * A * cos φ* t
- Q = Reactive Energy [VARh] = V * A * sin φ * t
- S = Apparent Energy [VAh] = $\sqrt{P^2+Q^2}$

For a practical meter, not only voltage and current amplitudes, but also phase angles and harmonic content may change constantly. Thus, simple RMS measurements are inherently inaccurate. A modern solid-state electricity meter IC such as the Teridian 71M6533 and 71M6534 functions by emulating the integral operation above, i.e. it processes current and voltage samples through an ADC at a constant frequency. As long as the ADC resolution is high enough and the sample frequency is beyond the harmonic range of interest, the current and voltage samples, multiplied with the time period of sampling will yield an accurate quantity for the momentary energy. Summing up the momentary energy quantities over time will result in accumulated energy.

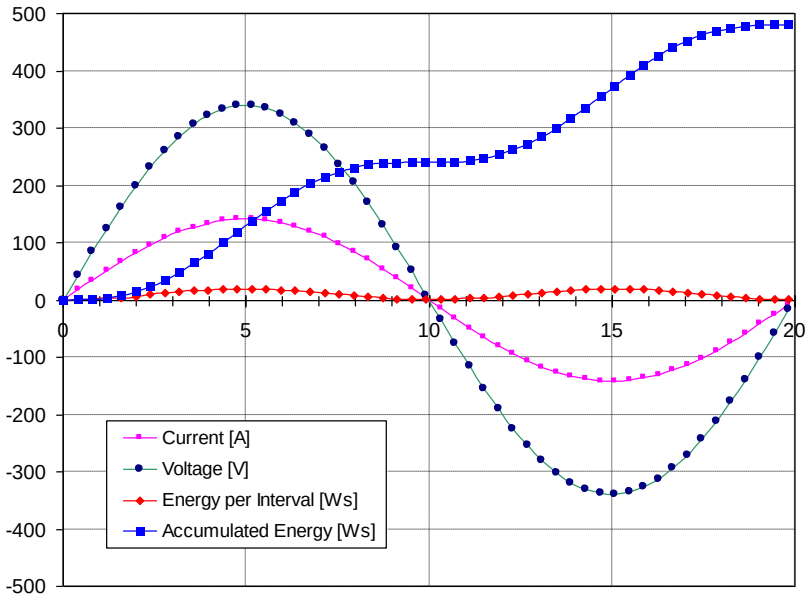


Figure 17: Voltage, Current, Momentary and Accumulated Energy

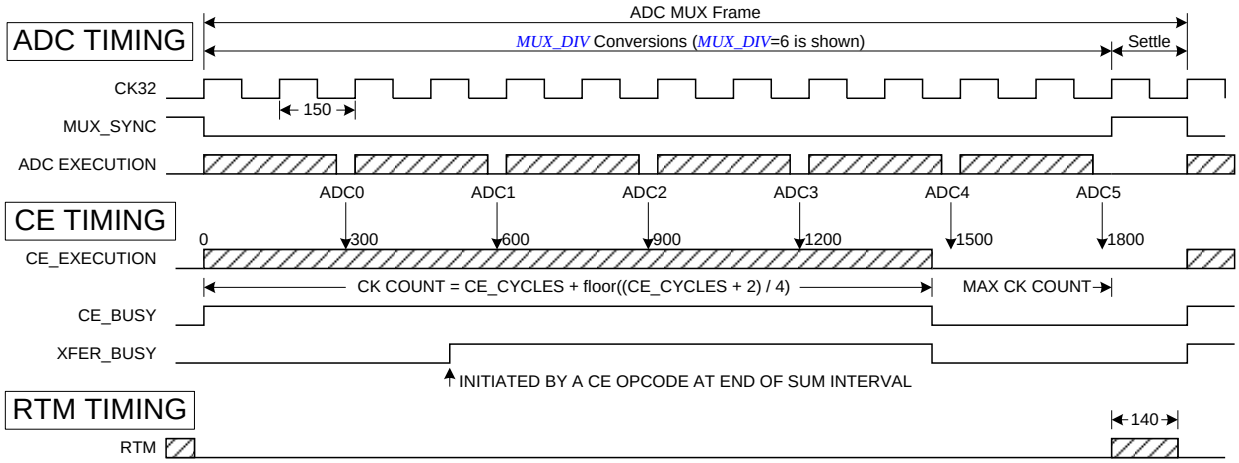
Figure 17 shows the shapes of V(t), I(t), the momentary power and the accumulated power, resulting from 50 samples of the voltage and current signals over a period of 20 ms. The application of 240 VAC and 100 A results in an accumulation of 480 Ws (= 0.133 Wh) over the 20 ms period, as indicated by the accumulated power curve. The described sampling method works reliably, even in the presence of dynamic phase shift and harmonic distortion.

2.2 System Timing Summary

Figure 18 summarizes the timing relationships between the input MUX states, the CE_BUSY signal and the two serial output streams. In this example, *MUX_DIV*=6 and *FIR_LEN*=2 (384). The duration of each MUX frame is (*M40MHZ/M26MHZ* = 00, 10, or 11 assumed):

- 1 + *MUX_DIV* * 1, if *FIR_LEN* = 0 (138 CE cycles), complete MUX frame = 7 CK32 cycles
- 1 + *MUX_DIV* * 2, if *FIR_LEN* = 1 (288 CE cycles) , complete MUX frame = 13 CK32 cycles
- 1 + *MUX_DIV* * 3, if *FIR_LEN* = 2 (384 CE cycles) , complete MUX frame = 19 CK32 cycles

An ADC conversion will always consume an integer number of CK32 clocks. Following this is a single CK32 cycle where the bandgap voltage is allowed to recover from the change in CROSS. Figure 18 shows a typical MUX frame with if *FIR_LEN* = 1and *MUX_DIV* = 6.



NOTES:
1. ALL DIMENSIONS ARE 4.9152 MHz CK COUNTS.
2. XFER_BUSY OCCURS ONCE EVERY (PRESAMPS * SUM_CYCLES) CODE PASSES.

Figure 18: Timing Relationship between ADC MUX and Compute Engine

Each CE program pass begins when the ADC0 conversion (slot 0, as defined by *SLOT0_SEL*) begins. Depending on the length of the CE program, it may continue running until the end of the last conversion. CE opcodes are constructed to ensure that all CE code passes consume exactly the same number of cycles. The result of each ADC conversion is inserted into the XRAM when the conversion is complete. The CE code is written to tolerate sudden changes in ADC data. The exact CK count when each ADC value is loaded into RAM is shown in Figure 18.

Figure 19 shows that the serial data stream, RTM, begins transmitting at the beginning of state S. RTM, consisting of 140 CK cycles, will always finish before the next code pass starts.

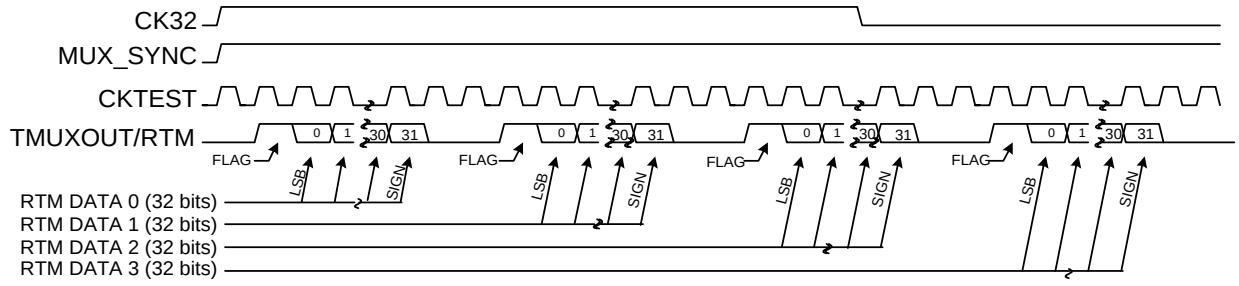


Figure 19: RTM Output Format

2.3 Battery Modes

Shortly after system power (V3P3SYS) is applied, the part will be in MISSION mode. MISSION mode means that the part is operating with system power and that the internal PLL is stable. This mode is the normal operation mode where the part is capable of measuring energy.

When system power is not available (i.e. when V1<VBIAS), the 71M6533 and 71M6534 will be in one of three battery modes: BROWNOUT, LCD, or SLEEP mode. Figure 20 shows a state diagram of the various operation modes, with the possible transitions between modes. For information on the timing of mode transitions refer to Figure 24 through Figure 26.

When V1 falls below VBIAS or the part wakes up under battery power, the part will automatically enter BROWNOUT mode (see Section 2.5 Wake Up Behavior). From BROWNOUT mode, the part may enter either LCD mode or SLEEP mode, as controlled by the MPU via the I/O RAM bits *LCD_ONLY* and *SLEEP*.

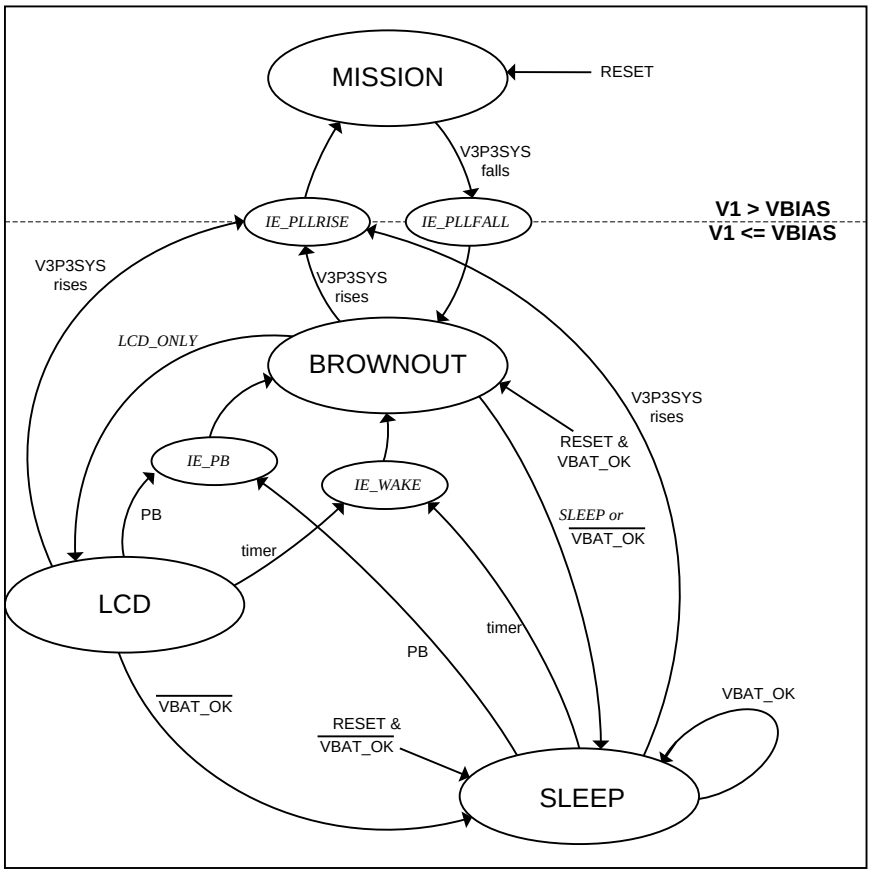


Figure 20: Operation Modes State Diagram

The transition from MISSION mode to BROWNOUT mode is signaled by the *IE_PLLFALL* interrupt flag (SFR 0xE8[7]). The transition in the other direction is signaled by the *IE_PLLRISE* interrupt flag (SFR 0xE8[6]), when the PLL becomes stable.

Transitions from both LCD and SLEEP mode are initiated by wake-up timer timeout conditions or push-button events. When the PB pin is pulled high (pushbutton is pressed), the *IE_PB* interrupt flag (SFR 0xE8[4]) is set, and when the wake-up timer times out, the *IE_WAKE* interrupt flag (SFR 0xE8[5]) is set.

In the absence of system power, if the voltage margin for the LDO regulator providing 2.5 V to the internal circuitry becomes too low to be safe, the part automatically enters sleep mode (BAT_OK false). The battery voltage must stay above 3 V to ensure that BAT_OK remains true. Under this condition, the 71M6533 and 71M6534 stays in SLEEP mode, even if the voltage margin for the LDO improves (BAT_OK true).
Table 45 shows the circuit functions available in each operating mode.

2.3.1 BROWNOUT Mode

In BROWNOUT mode, most non-metering digital functions are active (as shown in Table 45) including ICE, UART, EEPROM, LCD and RTC. In BROWNOUT mode, a low-bias current regulator will provide 2.5 Volts to V2P5 and V2P5NV. The regulator has an output called BAT_OK to indicate that it has sufficient overhead. When BAT_OK = 0, the part will enter SLEEP mode. From BROWNOUT mode, the processor can voluntarily enter LCD or SLEEP modes. When system power is restored, the part will automatically transition from any of the battery modes to MISSION mode, once the PLL has settled.

Table 45: Available Circuit Functions

Circuit Function	System Power	Battery Power (Nonvolatile Supply)		
	MISSION	BROWNOUT	LCD	SLEEP
CE	Yes	–	–	–
CE/MPU Data RAM	Yes	Yes	–	–
FIR	Yes	–	–	–
Analog circuits:	Yes	–	–	–
MPU clock rate	From PLL, as defined by *MPU_DIV*	28.672 kHz (7/8 of 32768 Hz)	–	–
MPU_DIV	Yes	–	–	–
ICE	Yes	Yes	–	–
DIO Pins	Yes	Yes	–	–
Watchdog Timer	Yes	Yes	–	–
LCD	Yes	Yes	Yes	–
EEPROM Interface (2-wire)	Yes	Yes (8 kb/s)	–	–
EEPROM Interface (3-wire)	Yes	Yes (16 kb/s)	–	–
UART	Yes	300 bd	–	–
Optical TX modulation	Yes	–	–	–
Flash Read	Yes	Yes	–	–
Flash Page Erase	Yes	Yes	–	–
Flash Write	Yes	–	–	–
XRAM Read and Write	Yes	Yes	–	–
Wakeup Timer	Yes	Yes	Yes	Yes
Oscillator and RTC	Yes	Yes	Yes	Yes
XRAM data preservation	Yes	Yes	–	–
V3P3D voltage output pin	Yes	Yes	–	–
GPO – GP7 registers	Yes	Yes	Yes	Yes

– indicates not active

The MPU will run at 7/8 of the crystal clock rate in BROWNOUT mode. This permits the UARTs to be operated at 300 bd. In this mode, the MPU clock has substantial short-term jitter.

The value of *MPU_DIV* will be remembered (not changed) as the part enters and exits BROWNOUT. *MPU_DIV* will be ignored during BROWNOUT.

While *PLL_OK* = 0, the I/O RAM bits *ADC_E* and *CE_E* are held in the zero state disabling both the ADC and the CE. When *PLL_OK* falls, the CE program counter is cleared immediately and all FIR processing halts.
Figure 21 shows the functional blocks active in BROWNOUT mode.

2.3.2 LCD Mode

In LCD mode, the data contained in the *LCD_SEG* registers is displayed. Up to four LCD segments connected to the pin SEG18 can be made to blink without the involvement of the MPU, which is disabled in LCD mode. To minimize power, only segments that might be used should be enabled.

LCD mode can be exited only by system power up, a timeout of the wake-up timer, or a push button.

When the IC exits LCD mode, the MPU can discover the event that caused the exit by reading the interrupt flags and interpret them as follows:

- *IE_WAKE* = 1 indicates that the wake timer has expired.
- *IE_PB* =1 indicates that the pushbutton input (PB) was activated.
- *COMPSTAT* = 0 indicates that a reset occurred but that main power is not yet available.
- If none of the above conditions applies, system power (V3P3SYS) must have been restored

After the transition from LCD mode to MISSION or BROWNOUT mode, the *PC* will be at 0x0000, the XRAM is in an undefined state, and the I/O RAM is only partially preserved (see the description of I/O RAM states in 4.2). *GP0[7:0]* through *GP7[7:0]* are preserved unless a hardware reset occurs (RESET pin is pulled high or power to the part is cycled without a battery being present). Figure 22 shows the functional blocks active in LCD mode.

2.3.3 SLEEP Mode

In SLEEP mode, the battery current is minimized and only the Oscillator and RTC functions are active. This mode can be exited only by system power-up, a timeout of the wake-up timer, or a push button event.

When the IC exits SLEEP mode, the MPU can discover the event that caused the exit by reading the interrupt flags and interpret them as follows:

- *IE_WAKE* = 1 indicates that the wake timer has expired.
- *IE_PB* =1 indicates that the pushbutton input (PB) was activated.
- *COMPSTAT* = 0 indicates that a reset occurred but that main power is not yet available.
- If none of the above conditions applies, system power (V3P3SYS) must have been restored

After the transition from SLEEP mode to MISSION or BROWNOUT mode the *PC* will be at 0x0000, the XRAM is in an undefined state, and the I/O RAM is only partially preserved (see the description of I/O RAM states in 4.2). *GP0[7:0]* through *GP7[7:0]* are preserved unless the a hardware reset occurs (RESET pin is pulled high or power to the part is cycled without a battery being present). Figure 23 shows the functional blocks active in SLEEP mode.

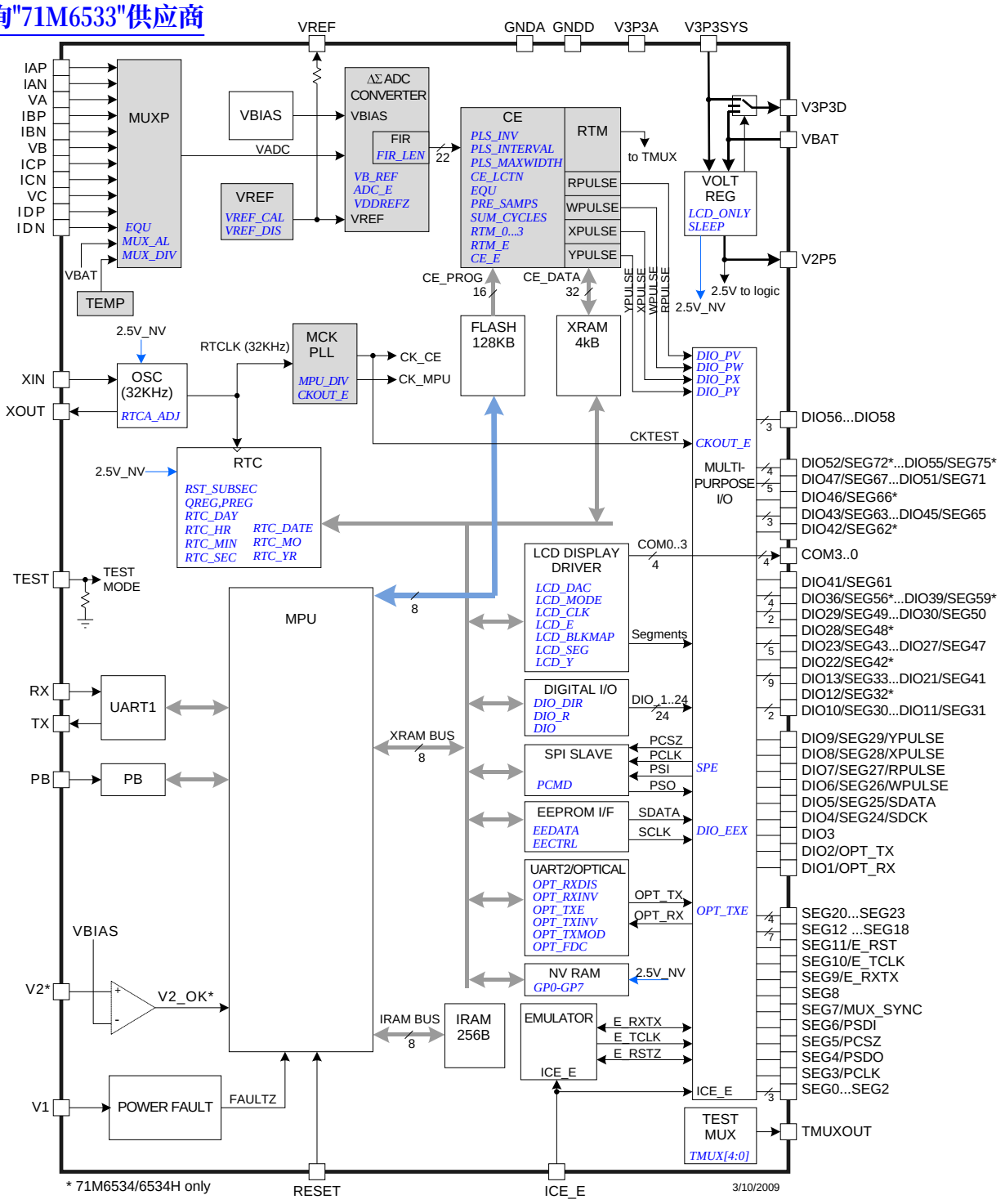


Figure 21: Functional Blocks in BROWNOUT Mode
(Inactive blocks in the figure are grayed out.)

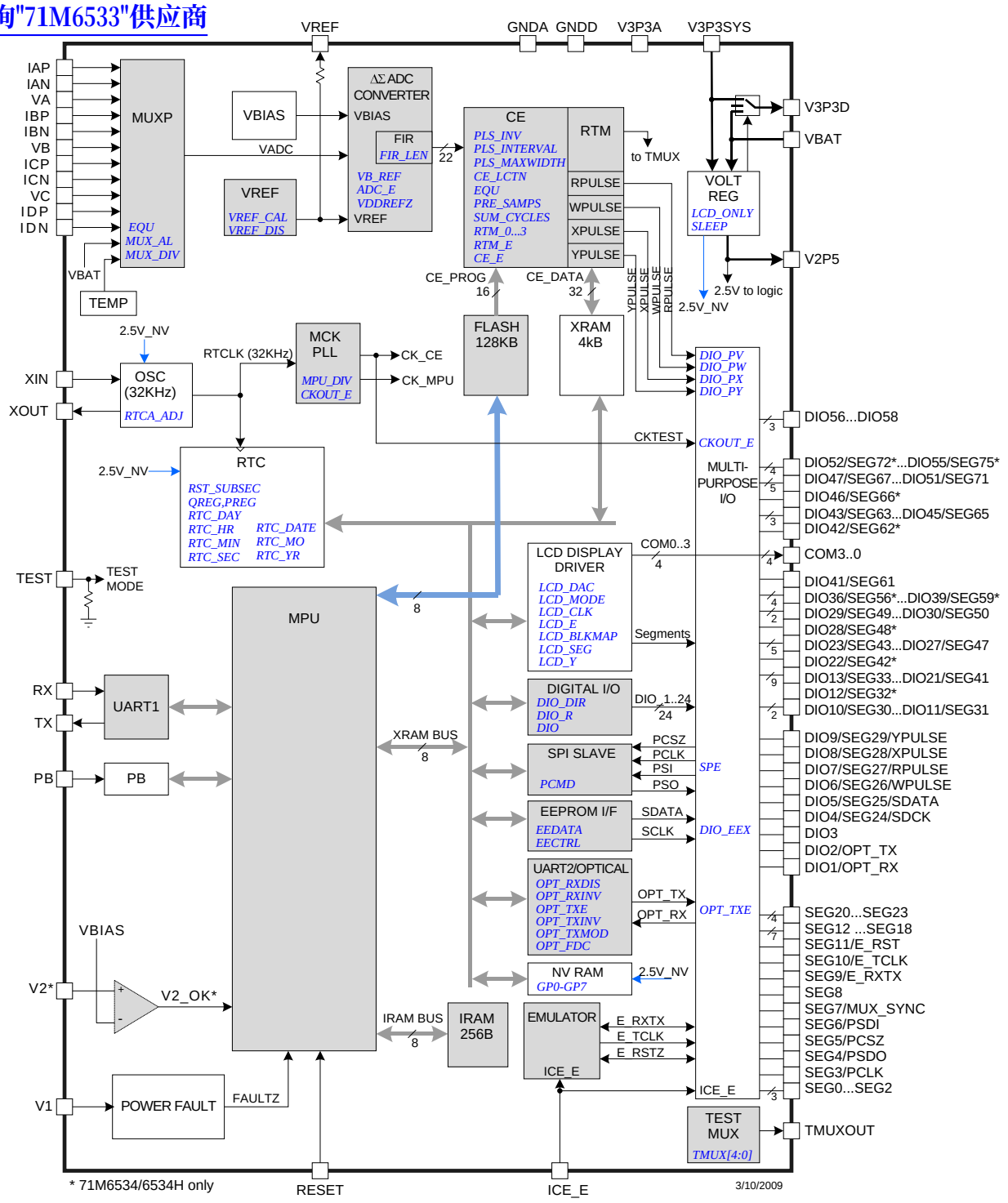


Figure 22: Functional Blocks in LCD Mode
(Inactive blocks in the figure are grayed out.)

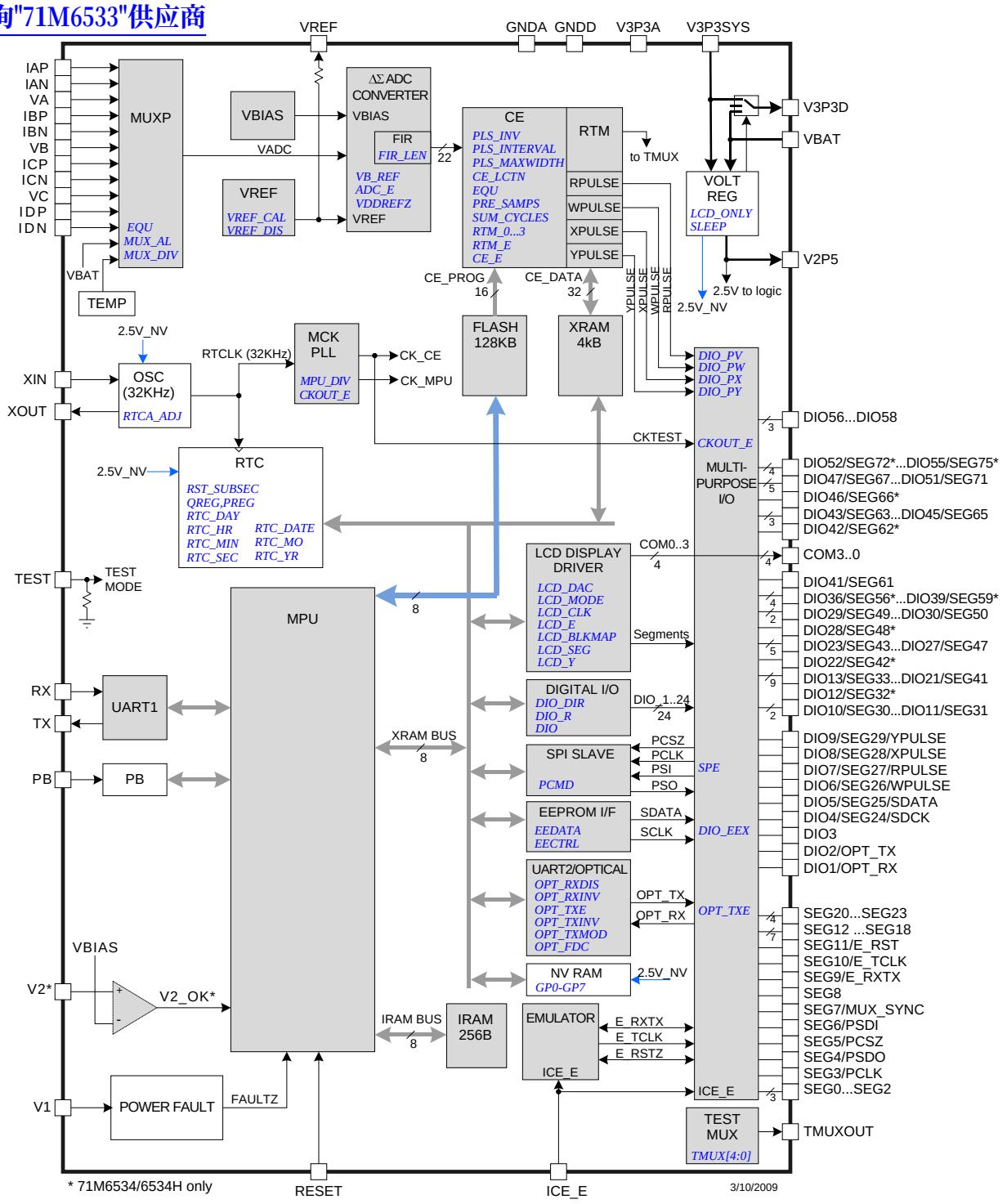


Figure 23: Functional Blocks in SLEEP Mode
(Inactive blocks in the figure are grayed out.)

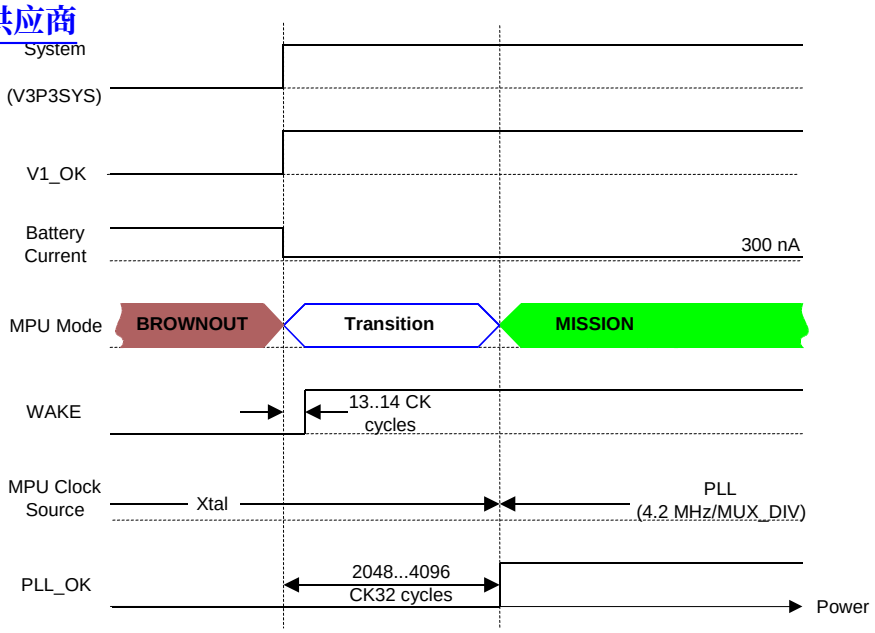


Figure 24: Transition from BROWNOUT to MISSION Mode when System Power Returns

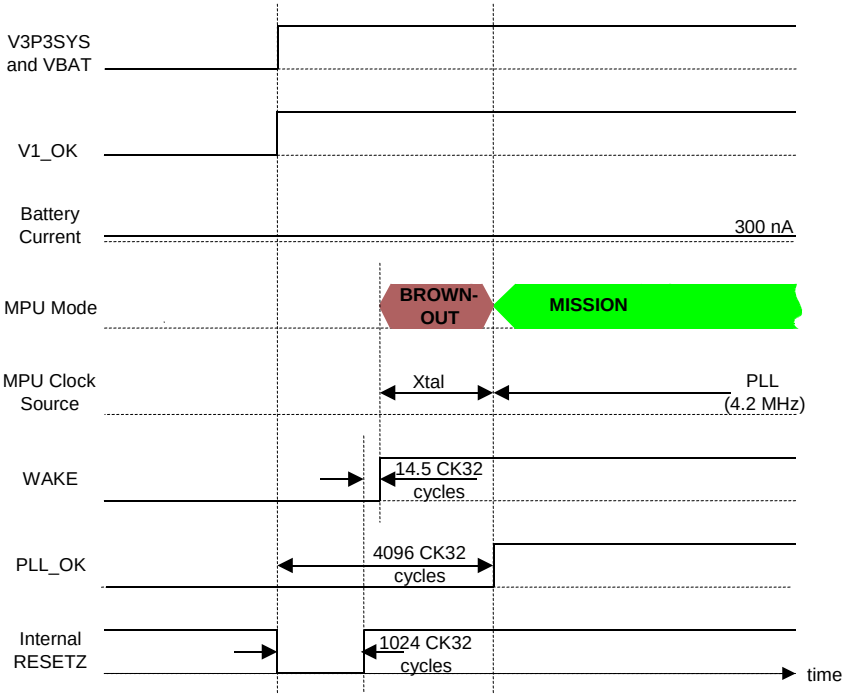


Figure 25: Power-Up Timing with V3P3SYS and VBAT tied together

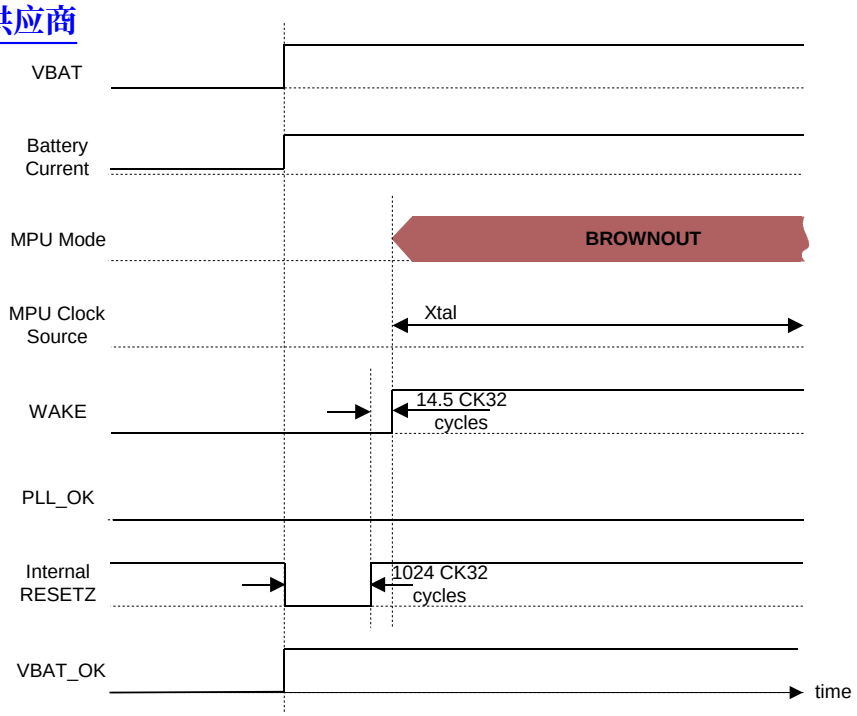


Figure 26: Power-Up Timing with VBAT only

2.4 Fault and Reset Behavior

2.4.1 Reset Mode

When the RESET pin is pulled high, all digital activity stops. The oscillator and RTC module continue to run. Additionally, all I/O RAM bits are set to their default states. As long as V1, the input voltage at the power fault block, is greater than VBIAS, the internal 2.5 V regulator will continue to provide power to the digital section.

Once initiated, the reset mode will persist until the reset timer times out, signified by WAKE rising. This will occur in 4100 cycles of the real time clock after RESET goes low, at which time the MPU will begin executing its pre-boot and boot sequences from address 00. See the description of Program Security in Section 1.4.5 for additional descriptions of pre-boot and boot.

If system power is not present, the reset timer duration will be 2 cycles of the crystal clock at which time the MPU will begin executing in BROWNOUT mode, starting at address 00.

2.4.2 Power Fault Circuit

The 71M6533 and 71M6534 includes a comparator to monitor system power fault conditions. When the output of the comparator falls (V1<VBIAS), the I/O RAM bits *PLL_OK* are zeroed and the part switches to BROWNOUT mode if a battery is present. Once system power returns, the MPU remains in reset and does not transition to MISSION mode until 2048 to 4096 CK32 clock cycles later, when PLL_OK rises. If a battery is not present, as indicated by BAT_OK=0, WAKE will fall and the part will enter SLEEP mode.

There are several conditions the device could be in as system power returns. If the part is in BROWNOUT mode, it will automatically switch to MISSION mode when PLL_OK rises. It will receive an interrupt indicating this. No configuration bits will be reset or reconfigured during this transition.

If the part is in LCD or SLEEP mode when system power returns, it will also switch to MISSION mode when PLL_OK rises. In this case, all configuration bits will be in the reset state due to WAKE having been zero. The RTC clock will not be disturbed, but the MPU RAM must be re-initialized. The hardware watchdog timer will become active when the part enters MISSION mode.

If there is no battery when system power returns, the part will switch to MISSION mode when PLL_OK rises. All configuration bits will be in reset state, and RTC and MPU RAM data will be unknown and must be initialized by the MPU.

2.5 Wake Up Behavior

As described above, the part will always wake up in MISSION mode when system power is restored. Additionally, the part will wake up in BROWNOUT mode when PB rises (push button is pressed) or when a timeout of the wake-up timer occurs.

2.5.1 Wake on PB

If the part is in SLEEP or LCD mode, it can be awakened by a rising edge on the PB pin. This pin is normally pulled to GND and can be pulled high by a push button depression. Before the PB signal rises, the MPU is in reset due to WAKE being low. When PB rises, WAKE rises and within three crystal cycles, the MPU begins to execute. The MPU can determine whether the PB signal woke it up by checking the *IE_PB* flag. Figure 27 shows the Wake Up timing.

For debouncing, the PB pin is monitored by a state machine operating from a 32 Hz clock. This circuit will reject between 31 ms and 62 ms of noise. Detection hardware will ignore all transitions after the initial rising edge. This will continue until the MPU clears the *IE_PB* bit.

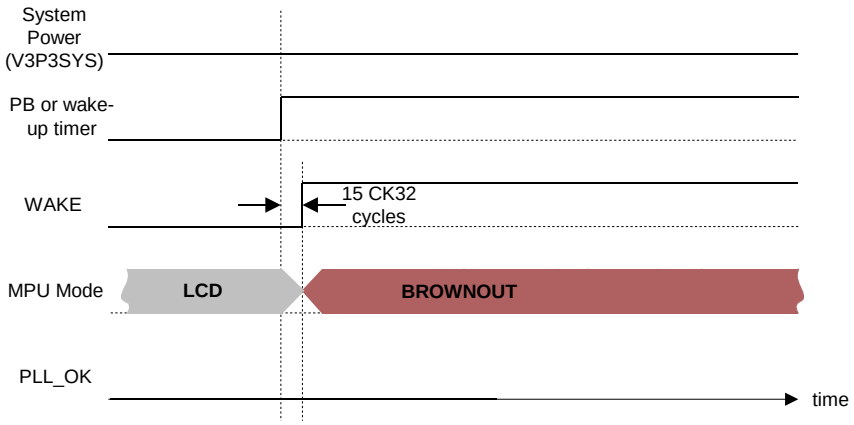


Figure 27: Wake Up Timing

2.5.2 Wake on Timer

The wake-up timer can wake up the part if it is in SLEEP or LCD mode. Until this timer times out, the MPU is in reset due to WAKE being low. When the wake-up timer times out, the WAKE signal rises and within three CK32 cycles, the MPU begins to execute. The MPU can determine whether the timer woke it by checking the *AUTOWAKE* interrupt flag (*IE_WAKE*).

The wake-up timer begins timing when the part enters LCD or SLEEP mode. Its duration is controlled by *WAKE_PRD[2:0]* and *WAKE_RES*. *WAKE_RES* selects a timer LSB of either 1 minute (*WAKE_RES* = 1) or 2.0 seconds (*WAKE_RES* = 0).

When *WAKE_RES* = 0, the first wake-timer LSB may be 1.5 or 2.5 seconds; subsequent LSBs will be 2.0 seconds. *WAKE_PRD[2:0]* selects a duration of from 1 to 7 LSBs. When *WAKE_RES* = 0, the wake-up timer duration will range from 1.5 + 2.0 *(*WAKE_PRD[2:0]* -1) seconds to 2.5 + 2.0 *(*WAKE_PRD[2:0]* -1) seconds.

When *WAKE_RES* = 1, the time will be (*WAKE_PRD[2:0]* +1) minutes.

The timer is armed by *WAKE_ARM* = 1. It must be armed at least 64 RTC cycles (64 CK32 cycles), or 2 ms, before *SLEEP* or *LCD_ONLY* is initiated to ensure that *WAKE_ARM* is valid before entering the SLEEP or LCD modes. Setting *WAKE_ARM* presets the timer with the values in *WAKE_RES* and *WAKE_PRD* and

readies the timer to start when the processor writes to the *SLEEP* or *LCD_ONLY* registers. The timer is reset and disarmed whenever the processor is awake. Thus, if it is desired to wake the MPU periodically (every 5 seconds, for example) the timer must be rearmed every time the part returns from SLEEP or LCD mode.

2.6 Data Flow

The data flow between the Compute Engine (CE) and the MPU is shown in Figure 28. In a typical application, the 32-bit CE sequentially processes the samples from the voltage inputs on pins IA, VA, IB, and VB, performing calculations to measure active power (Wh), reactive power (VARh), A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU. Figure 28 illustrates the CE/MPU data flow.

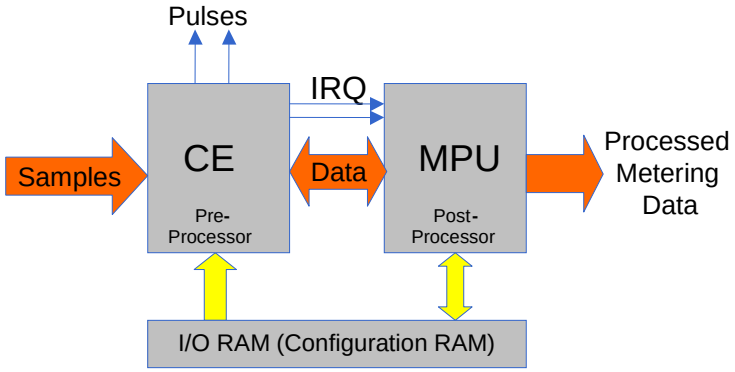


Figure 28: MPU/CE Data Flow

2.7 CE/MPU Communication

Figure 29 shows the functional relationships between the CE and the MPU. The CE is controlled by the MPU via shared registers in the I/O RAM and in RAM.

The CE outputs two interrupt signals to the MPU: CE_BUSY and XFER_BUSY, which are connected to the MPU interrupt service inputs as external interrupts. CE_BUSY indicates that the CE is actively processing data. This signal will occur once every multiplexer cycle. XFER_BUSY indicates that the CE is updating data to the output region of the RAM. This will occur whenever the CE has finished generating a sum by completing an accumulation interval determined by *SUM_CYCLES * PRE_SAMPS* samples. Interrupts to the MPU occur on the falling edges of the XFER_BUSY and CE_BUSY signals.

Refer to Section 4.3 CE Interface Description for additional information on setting up the device using the MPU firmware.

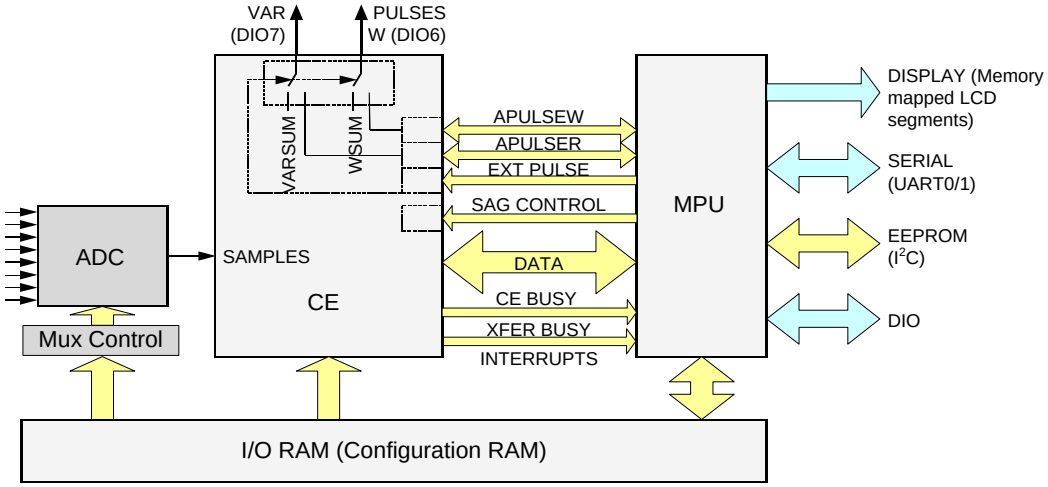


Figure 29: MPU/CE Communication

3 Application Information

3.1 Connection of Sensors (CT, Resistive Shunt)

Figure 30 through Figure 32 show how resistive dividers, current transformers, Rogowski coils and resistive shunts are connected to the voltage and current inputs of the 71M6533/71M6534.

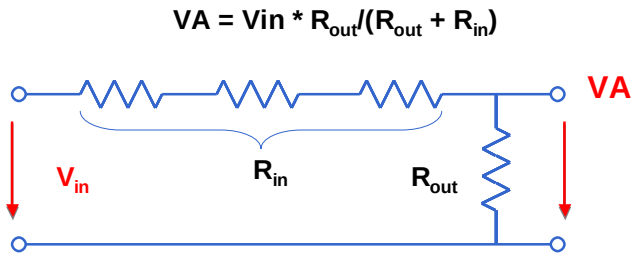


Figure 30: Resistive Voltage Divider

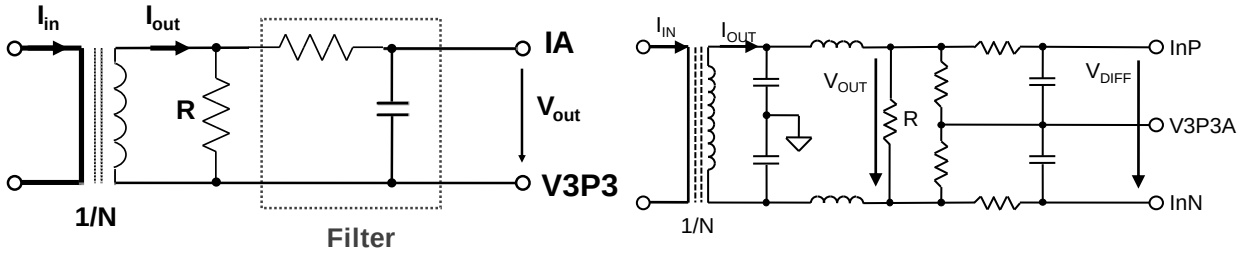


Figure 31: CT with Single Ended (Left) and Differential Input (Right) Connection

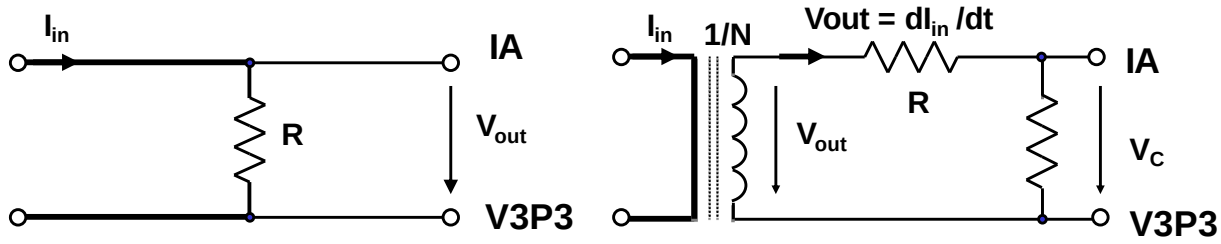


Figure 32: Resistive Shunt (Left), Rogowski Sensor (Right)

3.2 Distinction between 71M6533/71M6534 and 71M6533H/71M6534H Parts

The 71M6533H/71M6534H parts go through an additional process of characterization during production which makes them suitable to high-accuracy applications.

The first process, applied to both the 71M6533/71M6534 and the 71M6533H/71M6534H, is the trimming of the reference voltage to the target value of 1.195V.

The second process, which is applied only to the 71M6533H/71M6534H, is the characterization of the reference voltage over temperature. The coefficients for the reference voltage are stored in trim fuses (I/O RAM registers *TRIMBGA*, *TRIMBGB*, *TRIMM[2:0]*. The MPU can read these trim fuses and calculate the correction coefficients *PPM1* and *PPMC2* per the formulae given in Section 5.4.15 VREF. See Section 3.5 Temperature Compensation for additional details.

The fuse *TRIMBGB* is non-zero for the 71M6533H/71M6534H part and zero for the 71M6533/71M6533 part.

Only partial trim fuse information is available for non-H parts. The values for *PPMC* and *PPMC2* that are used by the CE to implement temperature compensation are calculated as follows:

- *PPMC* = TC1 * 22.46 = (52.46 - *TRIMT*) * 3.18 * 22.46 = (52.46 - *TRIMT*) * 71.423
- *PPMC2* = TC2 * 1150.1 = –0.444 * 1150.1 = -510.6

The factor *TRIMT* used to calculate *PPMC* is derived from the trim fuse *TRIMT*[7:0].

3.3 Connecting 5 V Devices

All digital input pins of the 71M6533/71M6534 are compatible with external 5 V devices. I/O pins configured as inputs do not require current-limiting resistors when they are connected to external 5 V devices.

3.4 Temperature Measurement

Measurement of absolute temperature uses the on-chip temperature sensor and applying the following formula:

$$T = \frac{(N(T) - N_n)}{S_n} + T_n$$

In the above formula T is the temperature in °C, $N(T)$ is the ADC count at temperature T, N_n is the ADC count at 25°C, S_n is the sensitivity in LSB/°C as stated in the Electrical Specifications, and T_n is +25 °C.

Example: At 25°C a temperature sensor value of 483,203,000 (N_n) is read by the ADC. At an unknown temperature T the value 449.648.000 is read at (N(T)). We determine the absolute temperature by dividing the difference of N_n and N(T) by 512 times the slope factor (-1180). After that, we add the 25C from the reference measurement:

$$T = \frac{449.648.000 - 483,203,000}{512 \cdot (-1180)} + 25C = 80.5C$$

The divisor 512 accounts for the 8-bit shift of the ADC value and for the factor of 2 introduced into the measurement by the CE which adds two consecutive temperature readings. It is recommended that temperature measurements be based on *TEMP_RAW_X* which is the sum of two consecutive temperature readings, thus being higher by a factor of two than the raw sensor readings.

3.5 Temperature Compensation

In a typical application, the CE compensates for the temperature dependency of the reference voltage (see Section 3.5.2). System-wide temperature correction over the entire meter is possible by involving the MPU. The thermal coefficients processed by the MPU may include the current sensors, the voltage sensors, and other influences.

3.5.1 Temperature Coefficients

For the 71M6533 and 71M6534, the temperature coefficient TC2 is given as a constant that represent typical component behavior (in µV/°C^2). TC1 can be calculated for the individual chip from the contents of the *TRIMT*[7:0] I/O RAM register. TC1 and TC2 allow compensation for variations of the reference voltage to within ±40 PPM/°C.

For the 71M6533H/71M6534H, individualized coefficients TC1 and TC2 can be retrieved from the on-chip fuses via *TRIMBGA*, *TRIMBGB*, *TRIMM[2:0]* (see Section 3.2 Distinction between 71M6533/71M6534 and 71M6533H/71M6534H Parts). For this part, TC1 and TC2 allow compensation for variations of the reference voltage to within ±15 PPM/°C

Since TC1 and TC2 are given in µV/°C and µV/°C^2, respectively, the value of the VREF voltage (1.195V) has to be taken into account when transitioning to PPM/°C and PPM/°C^2. This means that *PPMC* = 26.84*TC1/1.195 and *PPMC2* = 1374*TC2/1.195).

3.5.2 Temperature Compensation for VREF

The bandgap temperature is used to digitally compensate the power outputs for the temperature dependence of VREF, using the CE register *GAIN_ADJ* (internal temperature compensation). Since the band gap amplifier is chopper-stabilized via the *CHOP_E* bits, the most significant long-term drift mechanism in the voltage reference is removed.

In internal temperature compensation mode, the CE applies the following formula to determine the *GAIN_ADJ* value. In this formula *TEMP_X* is the deviation from nominal or calibration temperature expressed in multiples of 0.1 °C:

$$GAIN\_ADJ = 16385 + \frac{TEMP\_X \cdot PPMC}{2^{14}} + \frac{TEMP\_X^2 \cdot PPMC2}{2^{23}}$$

3.5.3 System Temperature Compensation

In a production electricity meter, the 71M6533 and 71M6534 is not the only component contributing to temperature dependency. A whole range of components (e.g. current transformers, resistor dividers, power sources, filter capacitors) will contribute temperature effects.

Since the output of the on-chip temperature sensor is accessible to the MPU, temperature compensation mechanisms with great flexibility are possible. MPU access to *GAIN_ADJ* permits a system-wide temperature correction over the entire meter rather than local to the chip.

3.5.4 Temperature Compensation for the RTC

In order to obtain accurate readings from the RTC, the following calibration procedures are recommended:

1. At the time of meter calibration, the crystal oscillator is calibrated using the *RTCA_ADJ* register in I/O RAM to be as close to 32768 Hz as possible. The recommended procedure is to connect a high-precision frequency counter to the TMUXOUT pin and select 0x11 for *TMUX[4:0]*. This will generate a 4-second pulse at TMUXOUT that can be used to trim *RTCA_ADJ* to the best value.
2. When the meter is in service, the MPU takes frequent temperature readings. If the temperature characteristics of the crystal are known, the temperature readings can be used to modify the settings for the I/O RAM registers *PREG[16:0]* and *QREG[1:0]* in order to keep the crystal frequency close to 32768 Hz.
3. After periods of operation under battery power, the temperature for the time the meter was not powered can be estimated by averaging the temperatures before and after battery operation. Based on this, the overall correction for the RTC time can be calculated and applied to the RTC after main power returns to the meter.

3.6 Connecting LCDs

The 71M6533 and 71M6534 has an on-chip LCD controller capable of controlling static or multiplexed LCDs. Figure 33 shows the basic connection for an LCD.

The following dedicated and multi-use pins can be assigned as LCD segments:

- 15 dedicated LCD segment pins: SEG0 to SEG2, SEG8, SEG12 to SEG18, SEG20 to SEG23.
- 9 dual-function pins: MUX_SYNC/SEG7, CKTEST/SEG19, E_RXTX/SEG9, E_TCLK/SEG10, E_RST/SEG11, SEG3/PCLK, SEG4/PSDO, SEG5/PCSZ, SEG6/PSDI.
- 5 additional dual-function pins in the 71M6534: SEG51/E_TBUS0, SEG52/E_TBUS1, SEG53/E_TBUS2, SEG54/E_TBUS3, SEG55/E_ISYNC
- 33 (71M6533) or 46 (71M6534) combined DIO and segment pins
  - 71M6533: SEG24/DIO4 to SEG31/DIO11, SEG33/DIO13 to SEG41/DIO21, SEG43/DIO23 to SEG47/DIO27, SEG49/DIO29, SEG50/DIO30, SEG61/DIO41, SEG63/DIO43 to SEG65/DIO45, and SEG67/DIO47 to SEG71/DIO51.
  - 71M6534: SEG24/DIO4 to SEG50/DIO30, SEG56/DIO36 to SEG59/DIO39, SEG61/DIO41 to SEG75/DIO55.

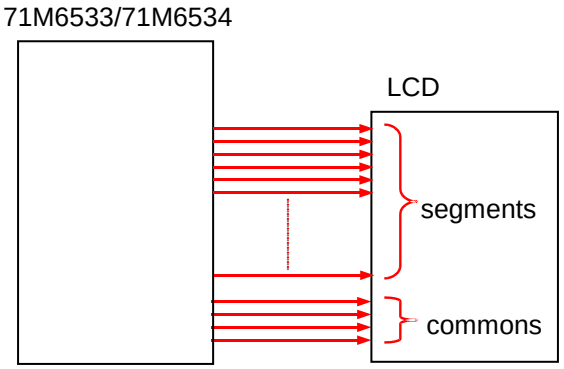


Figure 33: Connecting LCDs

3.7 Connecting I²C EEPROMs

I²C EEPROMs or other I²C compatible devices should be connected to the DIO pins DIO4 and DIO5, as shown in Figure 34.

Pull-up resistors of roughly 10 kΩ to V3P3D (to ensure operation in BROWNOUT mode) should be used for both SCL and SDA signals. The *DIO_EEX* register in I/O RAM must be set to 01 in order to convert the DIO pins DIO4 and DIO5 to I²C pins SCL and SDA.

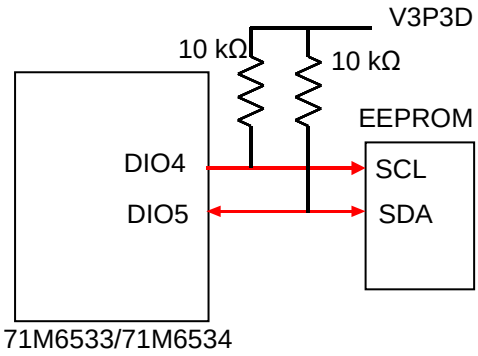


Figure 34: I²C EEPROM Connection

3.8 Connecting Three-Wire EEPROMs

µWire EEPROMs and other compatible devices should be connected to the DIO pins DIO4 and DIO5, as shown in Figure 35 and described below:

- DIO5 connects to both the DI and DO pins of the three-wire device.
- The CS pin must be connected to a vacant DIO pin of the 71M6533/71M6534.
- In order to prevent bus contention, a 10 kΩ to resistor is used to separate the DI and DO signals.
- The CS and CLK pins should be pulled down with a resistor to prevent operation of the three-wire device on power-up, before the 71M6533/71M6534 can establish a stable signal for CS and CLK.
- The *DIO_EEX* register in I/O RAM must be set to 2 (b10) in order to convert the DIO pins DIO4 and DIO5 to µWire pins.

The µ-Wire EEPROM interface is only functional when *MPU_DIV[2:0]* = 000.

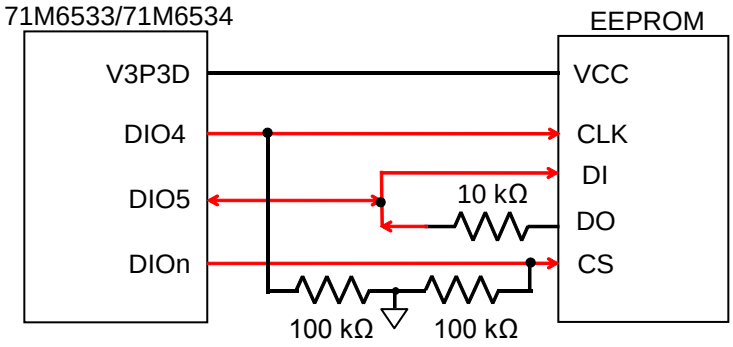


Figure 35: Three-Wire EEPROM Connection

3.9 UART0 (TX/RX)

The UART0 RX pin should be pulled down by a 10 kΩ resistor and additionally protected by a 100 pF ceramic capacitor, as shown in Figure 36.

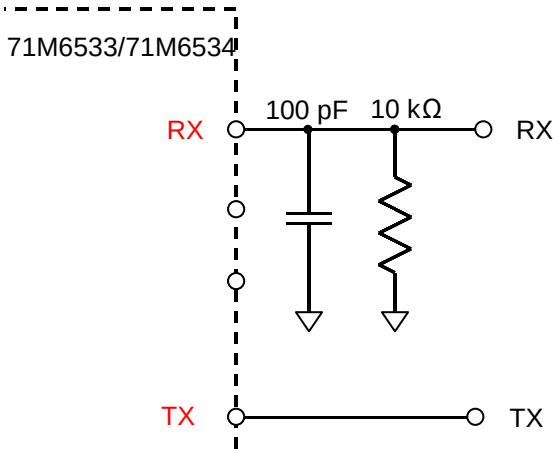


Figure 36: Connections for UART0

3.10 Optical Interface (UART1)

The OPT_TX and OPT_RX pins can be used for a regular serial interface (by connecting a RS_232 transceiver for example), or they can be used to directly operate optical components (for example, an infrared diode and phototransistor implementing a FLAG interface). Figure 37 shows the basic connections for UART1. The OPT_TX pin becomes active when the I/O RAM register *OPT_TXE* is set to 00.

The polarity of the OPT_TX and OPT_RX pins can be inverted with the configuration bits, *OPT_TXINV* and *OPT_RXINV*, respectively.

The OPT_TX output may be modulated at 38 kHz when system power is present. Modulation is not available in BROWNOUT mode. The *OPT_TXMOD* bit enables modulation. The duty cycle is controlled by *OPT_FDC[1:0]*, which can select 50%, 25%, 12.5%, and 6.25% duty cycle. A 6.25% duty cycle means OPT_TX is low for 6.25% of the period. The OPT_RX pin uses digital signal thresholds. It may need an analog filter when receiving modulated optical signals.

With modulation, an optical emitter can be operated at higher current than nominal, enabling it to increase the distance along the optical path.

If operation in BROWNOUT mode is desired, the external components should be connected to V3P3D.

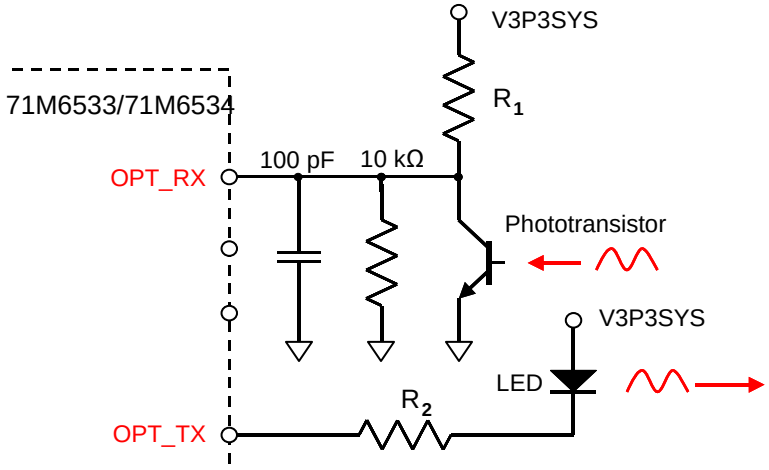


Figure 37: Connection for Optical Components

3.11 Connecting the V1 Pin

A voltage divider should be used to establish that V1 is in a safe range when the meter is in MISSION mode (see Figure 38). V1 must be lower than 2.9 V in all cases in order to keep the hardware watchdog timer enabled. The resistor divider ratio must be chosen so that V1 crosses the VBIAS threshold when V3P3 is near the minimum supply voltage (3.0 VDC). A series resistor (R3) provides additional hysteresis, and a capacitor to ground (C1) is added for enhanced EMC immunity.

The amount of hysteresis depends on the choice of R1 and R3: If V1 < VBIAS, approximately 1 µA will flow into the on-chip V1 comparator causing a voltage drop. If V1 ≥ VBIAS, almost no current will flow into the comparator. The voltage drop will require V3P3 to be slightly higher for V1 to cross the VBIAS threshold when V3P3 is rising as compared to when V3P3 is falling. Maintaining sufficient hysteresis helps to eliminate rapid mode changes which may occur in cases where the power supply is unstable with V1 close to the VBIAS threshold point.

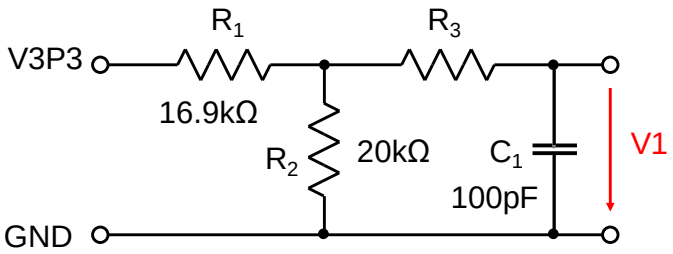


Figure 38: Voltage Divider for V1

3.12 Connecting the Reset Pin

Even though a functional meter will not necessarily need a reset switch, it is useful to have a reset push-button for prototyping as shown in Figure 39, left side. The RESET signal may be sourced from V3P3SYS (functional in MISSION mode only), V3P3D (MISSION and BROWNOUT modes), or VBAT (all modes, if a battery is present), or from a combination of these sources, depending on the application.

For a production meter, the RESET pin should be protected by the by the external components shown in Figure 39, right side. R1 should be in the range of 100Ω and mounted as closely as possible to the IC.

Since the 71M6533 and 71M6534 generates its own power-on reset, a reset button or circuitry, as shown in Figure 39, is only required for test units and prototypes.

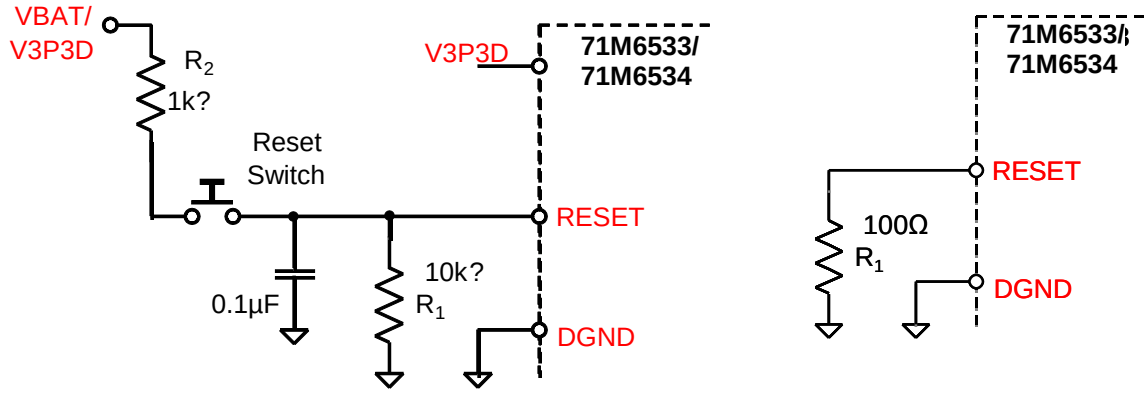


Figure 39: External Components for the RESET Pin: Push-Button (Left), Production Circuit (Right)

3.13 Connecting the Emulator Port Pins

Even when the emulator is not used, small shunt capacitors to ground (22 pF) should be used for protection from EMI as illustrated in Figure 40. Production boards should have the ICE_E pin connected to ground via a resistor of around 200 Ω.

The 71M6534 is capable of supporting a trace emulator. To connect this non-standard emulator, the pins E_TBUS0 (SEG51) – E_TBUS3 (SEG54) and E_ISYNC (SEG55) have to be brought out to the emulator interface.

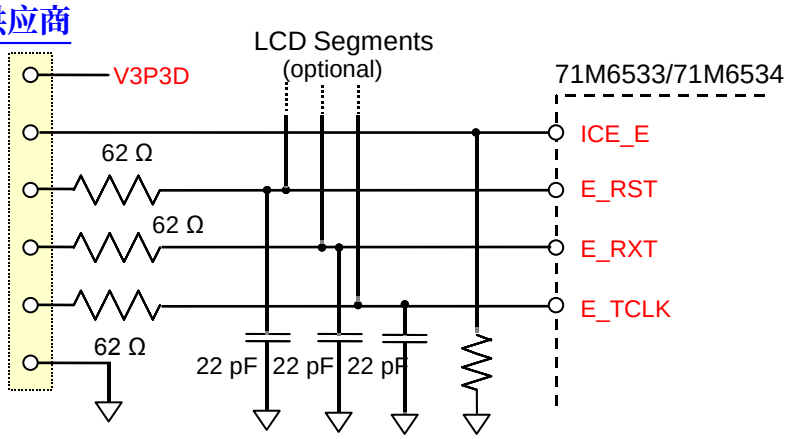


Figure 40: External Components for the Emulator Interface

3.14 Connecting a Battery

It is important that a valid voltage is connected to the VBAT pin at all times. For meters without a battery, VBAT should be connected directly to V3P3SYS. Designs for meters with batteries need to ensure that the meter functions even when the battery voltage decreases below the specified voltage for VBAT. This can be achieved by connecting a diode from V3P3SYS to VBAT. However, the battery test will yield inaccurate results if that technique is used, since the voltage at V3P3SYS will feed current to the VBAT pin. A better solution is shown in Figure 41: During the battery test, a DIO pin is activated as an output and applies a low voltage to the anode of the diode. This prevents the voltage at the power supply to influence the voltage at the VBAT pin.

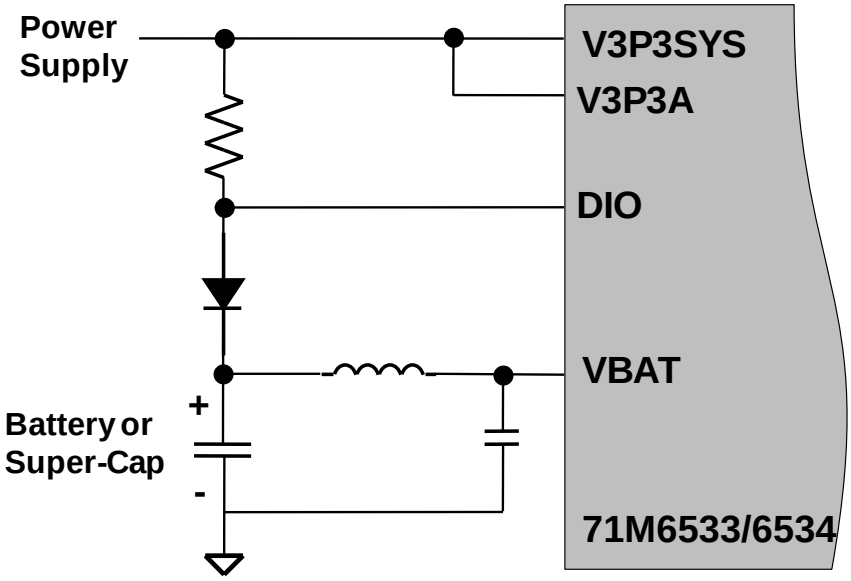


Figure 41: Connecting a Battery

Meters equipped with batteries need to contain code that transitions the chip to SLEEP mode as soon as the battery is attached in production. Otherwise, remaining in BROWNOUT mode would add unnecessary drain to the battery.

3.15 Flash Programming

Operational or test code can be programmed into the flash memory using either an in-circuit emulator or the Flash Programmer Module (TFP-2) available from Teridian. The flash programming procedure uses the E_RST, E_RXTX, and E_TCLK pins. The *FL_BANK* register has to be set to the value corresponding to the bank that is being programmed.

3.16 MPU Firmware Library

All application-specific MPU functions mentioned in Section 3 Application Information are available from Teridian as a standard ANSI C library and as ANSI C source code. The code is available as part of the Demonstration Kit for the 71M6533/71M6534. The Demonstration Kits come with the 71M6533/71M6534 preprogrammed with demo firmware and mounted on a functional sample meter Demo Board. The Demo Boards allow for quick and efficient evaluation of the IC without having to write firmware or having to supply an in-circuit emulator (ICE).

3.17 Crystal Oscillator

The oscillator of the 71M6533/71M6534 drives a standard 32.768 kHz watch crystal. The oscillator has been designed specifically to handle these crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to VBAT.

Board layouts with minimum capacitance from XIN to XOUT will require less battery current. Good layouts will have XIN and XOUT shielded from each other.

Since the oscillator is self-biasing, an external resistor must not be connected across the crystal.

3.18 Meter Calibration

Once the Teridian 71M6533 and 71M6534 energy meter device has been installed in a meter system, it must be calibrated. A complete calibration includes the following:

- Calibration of the metrology section, i.e. calibration for tolerances of the current sensors, voltage dividers and signal conditioning components as well as of the internal reference voltage (VREF).
- Establishment of the reference temperature (Section 3.2) for temperature measurement and temperature compensation (Section 3.5).
- Calibration of the battery voltage measurement (Section 1.4.9).
- Calibration of the oscillator frequency (Section 1.4.3) and temperature compensation for the RTC (Section 3.5.4).

The metrology section can be calibrated using the gain and phase adjustment factors accessible to the CE. The gain adjustment is used to compensate for tolerances of components used for signal conditioning, especially the resistive components. Phase adjustment is provided to compensate for phase shifts introduced by the current sensors or by the effects of reactive power supplies.

Due to the flexibility of the MPU firmware, any calibration method, such as calibration based on energy, or current and voltage can be implemented. It is also possible to implement segment-wise calibration (depending on current range).

The 71M6533 and 71M6534 supports common industry standard calibration techniques, such as single-point (energy-only), multi-point (energy, Vrms, Irms), and auto-calibration.

4 Firmware Interface

4.1 I/O RAM Map –Functional Order

Bits marked with an asterisk (e.g. *UMUX_E*)* apply to the 71M6534 only.

Table 46: I/O RAM Map – Functional Order

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	B
Configuration:								
CE0	2000	*EQU[2:0]*			*CE_E*	*CE10MHZ*		Not
CE1	2001	*PRE_SAMPS[1:0]*		*SUM_CYCLES[5:0]*				
CE2	2002	Not Used		*CHOP_E[1:0]*		*RTM_E*	*WD_OVF*	*EX*
COMP0	2003	Not Used	*PLL_OK*	Not Used	Not Used	Not Used	Not Used	Not
CONFIG0	2004	*VREF_CAL*	*PLS_INV*	Not Used	*CKOUT_E*	*VREF_DIS*		*MPU_*
CONFIG1	2005	Reserved (0)	Not Used	*ECK_DIS*	*M26MHZ*	*ADC_E*	*MUX_ALT*	Not
VERSION	2006	*VERSION[7:0]*						
CONFIG2	2007	*OPT_TXE[1:0]*		*EX_PLL*	*EX_FWCOL*	*FIR_LEN[1:0]*		
CE3	209D	Not Used	Not Used	Not Used	Not Used	*MUX_DIV[3:0*		
CE4	20A7	*BOOT_SIZE[7:0]*						
CE5	20A8	*CE_LCTN[7:0]*						
WAKE	20A9	*WAKE_ARM*	*SLEEP*	*LCD_ONLY*	Not Used	*WAKE_RES*		*WAKE_*
TMUX	20AA	Not Used	Not Used	Not Used	*TMUX[4:0]*			
ANACTRL	20AB	Reserved (0000)				*LCD_DAC*[2:0]		
CONFIG3	20AC	Not Used	Not Used	*SEL_IBN*	*CHOP_IB*	Not Used	Not Used	*SEL*
CONFIG4	20AD	Not Used	Not Used	*SEL_IDN*	*CHOP_ID*	Not Used	Not Used	*SEL*
Digital I/O:								
	20AF	Not Used	Not Used	Not Used	Not Used	Not Used		*DIO_F*
DIO0	2008	*DIO_EEX[1:0]*		*OPT_RXDIS*	*OPT_RXINV*	*DIO_PW*	*DIO_PV*	*OPT_*
DIO1	2009	Not Used	*DIO_R1[2:0]*			Not Used		*DI_R*
DIO2	200A	Not Used	*DIO_R3[2:0]*			Not Used		*DIO_*
DIO3	200B	Not Used	*DIO_R5[2:0]*			Not Used		*DIO_*
DIO4	200C	Not Used	*DIO_R7[2:0]*			Not Used		*DIO_*
DIO5	200D	Not Used	*DIO_R9[2:0]*			Not Used		*DIO_*

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	B
DIO6	200E	Not Used	*DIO_R11[2:0]*			Not Used		*DIO_*
	200F	Reserved (00)		Not Used	Not Used	*DIO_PX*	*DIO_PY*	Not
		*UMUX_E**	*UMUX_SEL**					
DIO7/ P0	SFR 80	*DIO_0[7:0]*(Port 0)						
DIO8	SFR A2	*DIO_DIR0[7:1]*						
DIO9 / P1 (Port 1)	SFR 90	*DIO_1[7:5]*			Not Used	*DIO_1[3:0]*		
					*DIO_1[4]**			
DIO10	SFR 91	*DIO_DIR1[7:5]*			Not Used	*DIO_DIR1[3:0*		
					*DIO_DIR[4]**			
DIO11/ P2 (Port 2)	SFR A0	*DIO_2[7]*	Not Used	*DIO_2[5:0]*				
			*DIO_2[6]**					
DIO12	SFR A1	*DIO_DIR2[7]*	Not Used	*DIO_DIR2[5:0]*				
			*DIO_DIR2[6]**					
P3	SFR B0	Not Used	*DIO3[6]*	*DIO3[5]*	Not Used	*DIO3[3]*	*DIO3[2]*	*DI*
					*DIO3[4]**			
Interrupts and WD Timer:								
INTBITS	SFR F8	*WD_RST*	*INT6*	*INT5*	*INT4*	*INT3*	*INT2*	*I*
IFLAGS	SFR E8	*IE_PLLFALL*	*IE_PLLRISE*	*IE_WAKE*	*IE_PB*	*IE_FWCOL1*	*IE_FWCOL0*	*IE_*
Flash:								
ERASE	SFR 94	*FLSH_ERASE[7:0]*						
FLSHCTL	SFR B2	*PREBOOT*	*SECURE*	*WRPROT_BT*	*WRPROT_CE*	Not Used	Not Used	*FLSH*
FL_BANK	SFR B6	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	
							FL_BA	
PGADR	SFR B7	*FLSH_PGADR[5:0]*						Not U
Real Time Clock:								
RTCCTRL	2010	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not
RTCA_ADJ	2011	Not Used	*RTCA_ADJ[6:0]*					
SUBSEC1	2014	*SUBSEC[7:0]*						
RTC0	2015	Not Used	Not Used	*RTC_SEC[5:0]*				
RTC1	2016	Not Used	Not Used	*RTC_MIN[5:0]*				
RTC2	2017	Not Used	Not Used	Not Used	*RTC_HR[4:0]*			
RTC3	2018	Not Used	Not Used	Not Used	Not Used	Not Used	*RTC_I*	
RTC4	2019	Not Used	Not Used	Not Used	*RTC_DATE[2:0]*			

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	B
RTC5	201A	Not Used	Not Used	Not Used	Not Used	*RTC_MO[3:0]*		
RTC6	201B	*RTC_YR[7:0]*						
RTCADJ_H	201C	Not Used	Not Used	Not Used	Not Used	Not Used	*PREC*	
RTCADJ_M	201D	*PREG[13:6]*						
RTCADJ_L	201E	*PREG[5:0]*						
WE	201F	RTC write protect register						
LCD Display Interface:								
LCDX	2020	*MUX_SYNC_E*	*BME*	Reserved (0)	Reserved (0)	Not Used	Not Used	Not
LCDY	2021	Not Used	*LCD_Y*	*LCD_E*	*LCD_MODE[2:0]*			
LCD_MAP0	2023	See the detailed description for *LCD_BITMAP[ ]* in Table 47: I/O RAM Description – Alphabetical						
…	…							
LCD_MAP5	2028							
*LCD_MAP6**	2029							
LCD0	2030	See the detailed description for *LCD_SEG[ ]* in Table 47: I/O RAM Description – Alphabetical						
…	…							
LCD41	2059							
LCD_BLNK	205A	*LCD_BLKMAP19[3:0]*				*LCD_BLKMAP18[*		
Area Reserved for Factory Test:								
RTM0H	2060	Not Used						
RTM0L	2061	*RTM0[7:0]*						
RTM1H	2062	Not Used						
RTM1L	2063	*RTM1[7:0]*						
RTM2H	2064	Not Used						
RTM2L	2065	*RTM2[7:0]*						
RTM3H	2066	Not Used						
RTM3L	2067	*RTM3[7:0]*						
SPI Interface:								
SPI…	2070	*SPE*	Not Used	Not Used	Not Used	Not Used	Not Used	Not
SP_CMD	2071	*SP_CMD[7:0]*						
SP_ADH	2072	*SP_ADDR[15:8]*						
SP_ADL	2073	*SP_ADDR[7:0]*						

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	B
Pulse Generator:								
PLS_W	2080	*PLS_MAXWIDTH[7:0]*						
PLS_I	2081	*PLS_INTERVAL[7:0]*						
ADC Mux:								
SLOT0	2090	*SLOT1_SEL*				*SLOT0_SEL*		
SLOT1	2091	*SLOT3_SEL*				*SLOT2_SEL*		
SLOT2	2092	*SLOT5_SEL*				*SLOT4_SEL*		
SLOT3	2093	*SLOT7_SEL*				*SLOT6_SEL*		
SLOT4	2094	*SLOT9_SEL*				*SLOT8_SEL*		
SLOT5	2096	*SLOT1_ALTSEL*				*SLOT0_ALTSE*		
SLOT6	2097	*SLOT3_ALTSEL*				*SLOT2_ALTSE*		
SLOT7	2098	*SLOT5_ALTSEL*				*SLOT4_ALTSE*		
SLOT8	2099	*SLOT7_ALTSEL*				*SLOT6_ALTSE*		
SLOT9	209A	*SLOT9_ALTSEL*				*SLOT8_ALTSE*		
SPI Interrupt:								
SPI0	20B0	Not Used	Not Used	Not Used	*IEN_SPI*	Not Used	Not Used	Not
SPI1	20B1	Not Used	Not Used	Not Used	*SPI_FLAG*	Not Used	Not Used	Not
General-Purpose and Non Volatile Registers:								
GP0 … *GP7*	20C0 … 20C7	*GP0[7:0]* … *GP7[7:0]*						
VERSION	20C8	*VERSION[7:0]*						
Serial EEPROM:								
EEDATA	SFR 9E	*EEDATA[7:0]*						
EECTRL	SFR 9F	*EECTRL[7:0]*						

4.2 I/O RAM Description – Alphabetical Order

The following conventions apply to the descriptions in this table:

- Bits with a W (write) direction are written by the MPU into configuration RAM. Typically, they are initially stored in flash the configuration RAM by the MPU. Some of the more frequently programmed bits are mapped to the MPU SFR mem ing bits are mapped to 2xxx.
- Bits with an R (read) direction can be read by the MPU.
- Columns labeled Reset and Wake describe the bit values upon reset and wake, respectively. "NV" in the Wake colum wered by the nonvolatile supply and is not initialized. LCD-related registers labeled "L" retain data upon transition from BROWNOUT mode and vice versa, but do not retain data in SLEEP mode. "–" means that the value is undefined.
- Write-only bits will return zero when they are read.
- Bits marked with an asterisk (e.g. *DIO_DIR1[4]**) are applicable to the 71M6534 only.

Table 47: I/O RAM Description – Alphabetical (by Bit Name)

Name	Location	Reset	Wake	Dir	Description
ADC_E	2005[3]	0	0	R/W	Enables ADC and VREF. When disabled, removes bias current
BME	2020[6]	0	–	R/W	Battery Measure Enable. When set, a load current is immediate tery and it is connected to the ADC to be measured on Alternati the *MUX_ALT* bit.
BOOT_SIZE[7:0]	20A7[7:0]	01	01	R/W	End of space reserved for boot program. The ending address o 1024**BOOT_SIZE*.
CE10MHZ	2000[3]	0	0	R/W	CE clock select. When set, the CE is clocked at 10 MHz. Othe frequency is 5 MHz.
CE_E	2000[4]	0	0	R/W	CE enable.
CE_LCTN[7:0]	20A8[7:0]	0x31	0x31	R/W	CE program location. The starting address for the CE program
CHOP_E[1:0]	2002[5:4]	00	00	R/W	Chop enable for the reference bandgap circuit. The value of CH rising edge of MUXSYNC according to the value in *CHOP_E*: 00 = toggle, except at the mux sync edge at the end of SUM MUX frame is automatically inserted at the end of each accu 01 = positive. 10 = reversed. 11 = toggle, no alternative MUX frame is inserted
CHOP_I_EN	20AB[0]	0	0	R/W	When *CHOP_I_EN* is set, chop mode for the analog current inp with the *CHOP_IA*, *CHOP_IB*, *CHOP_IC*, and *CHOP_ID* bits.
CHOP_IA *CHOP_IB* *CHOP_IC* *CHOP_ID*	20AC[0] 20AC[4] 20AD[0] 20AD[4]	0 0 0 0	0 0 0 0	R/W	When *CHOP_I_EN* is set, these bits enable chop mode for the r

CKOUT_E	2004[4]	0	0	R/W	Control bit for the SEG19/CKOUT pin: 0: The pin is the SEG19 LCD driver 1: The pin is the CK_FIR output (5 MHz in mission mode, 32 kH
COMPSTAT	2003[0]	--	--	R	Status bit for the V1 comparator (same as V1_OK, see TMUXO
DI_RPB[2:0] *DIO_R1[2:0]* *DIO_R2[2:0]* *DIO_R3[6:4]* *DIO_R4[2:0]* *DIO_R5[2:0]* *DIO_R6[2:0]* *DIO_R7[2:0]* *DIO_R8[2:0]* *DIO_R9[2:0]* *DIO_R10[2:0]* *DIO_R11[2:0]* *DIO_RRX[2:0]*	2009[2:0] 2009[6:4] 200A[2:0] 200A[6:4] 200B[2:0] 200B[6:4] 200C[2:0] 200C[6:4] 200D[2:0] 200D[6:4] 200E[2:0] 200E[6:4] 20AF[2:0]	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	R/W	Connects dedicated I/O pins DIO1 through DIO11 as well as inp resources. If more than one input is connected to the same res column in the table below specifies how they are combined. *DIO_RRX* applies to the RX pin.
DIO_DIR0[7:1]	SFR A2	0	–	R/W	Programs the direction of pins DIO7 through DIO1. Writing a 1 in is ignored if the corresponding pin is not configured as DIO. See for special options for DIO6 and DIO7. See *DIO_EEX* for special DIO5.
DIO_DIR1[7:5, 3:0], *DIO_DIR1[4]**	SFR 91	0	–	R/W	Programs the direction of pins DIO15 through DIO8. Writing a 1 A bit is ignored if the corresponding pin is not configured as DIO *DIO_PW* for special options for the DIO8 and DIO9 outputs. *DIO_DIR1[4]* controlling DIO12 is only applicable to the 71M653
DIO_DIR2[7,5:0] *DIO_DIR2[6]**	SFR A1	0	–	R/W	Programs the direction of pins DIO23 through DIO16. Writing a A bit is ignored if the corresponding pin is not configured as a D *DIO_DIR2[6]* controlling DIO22 is only applicable to the 71M653
DIO_56 *DIO_57* *DIO_58*	2052[4] 2053[4] 2054[4]	0 0 0	– – –	R/W	The value on DIO pins 56 through 58. The MPU writes data to the the data on these pins.
DIO_DIR56 *DIO_DIR57* *DIO_DIR58*	2052[7] 2053[7] 2054[7]	0 0 0	– – –	R/W	Programs the direction of DIO pins 56 through 58. Writing a 1 indi

DIO_Rx[2:0]	**Resource**	**Mul**
000	NONE	-
001	Reserved	C
010	T0 (Counter /Timer 0 clock or gate)	C
011	T1 (Counter /Timer 1 clock or gate)	C
100	High priority IO interrupt (int0 rising)	C
101	Low priority IO interrupt (int1 rising)	C
110	High priority IO interrupt (int0 falling)	C
111	Low priority IO interrupt (int1 falling)	C

DIO_0[7:0] *DIO_1[7:0]* *DIO_2[7:0]* *DIO_3[6:0]*	SFR 80 SFR 90 SFR A0 SFR B0	0 0 0 0	– – – –	R/W	The value on the DIO pins. Pins configured as LCD will read zero. these registers to change the data on pins configured as outputs. or input will ignore writes. *DIO_0[7:0]* corresponds to DIO7 through DIO1 and PB (PB *DIO_1[7:0]* corresponds to DIO15 through DIO8. (*DIO_1[4]* DIO12 is only applicable to the 71M6534) *DIO_2[7:0]* corresponds to DIO23 through DIO16. (*DIO_2[4* DIO22 is only applicable to the 71M6534) *DIO_3[6:0]* corresponds to DIO30 through DIO24. (*DIO_3[4* DIO28 is only applicable to the 71M6534)
DIO_EEX[1:0]	2008[7:6]	0	0	R/W	When set, converts DIO4 and DIO5 to interface with external EE comes SDCK and DIO5 becomes bi-directional SDATA. ***DIO_EEX[1:0]*** / **Function** 00 – Disable EEPROM interface 01 – 2-Wire EEPROM interface 10 – 3-Wire EEPROM interface 11 – --not used--
DIO_PV	2008[2]	0	0	R/W	Causes VARPULSE to be output on DIO7.
DIO_PW	2008[3]	0	0	R/W	Causes WPULSE to be output on DIO6.
DIO_PX	200F[3]	0	0	R/W	Causes XPULSE to be output on DIO8.
DIO_PY	200F[2]	0	0	R/W	Causes YPULSE to be output on DIO9.
EEDATA[7:0]	SFR 9E	0	0	R/W	Serial EEPROM interface data.
EECTRL[7:0]	SFR 9F	0	0	R/W	Serial EEPROM interface control.
ECK_DIS	2005[5]	0	0	R/W	Emulator clock disable. When *ECK_DIS* = 1, the emulator clock CAUTION If *ECK_DIS* is set, the emulator and programming devi erase or program the device.
EQU[2:0]	2000[7:5]	0	0	R/W	Specifies the power equation to be used by the CE.
EX_XFR *EX_RTC* *EX_FWCOL* *EX_PLL*	2002[0] 2002[1] 2007[4] 2007[5]	0 0 0 0	0 0 0 0	R/W	Interrupt enable bits. These bits enable the XFER_BUSY, the F WareCollision (FWCOL), and PLL interrupts. Note that if one of be enabled, its corresponding MPU EX enable must also be set Interrupts for details.

<table>
<tr><td>FIR_LEN[1:0]</td><td>2007[3:2]</td><td>1</td><td>1</td><td>R/W</td><td>FIR_LEN[1:0] controls the length of the ADC decimation FIR filte
<table>
<tr><th>[M40MHZ, M26MHZ]</th><th>FIR_LEN</th><th>Resulting FIR Filter Cycles</th><th>Resul ADC</th></tr>
<tr><td rowspan="3">[00], [10], or [11]</td><td>00</td><td>138</td><td>0.110</td></tr>
<tr><td>01</td><td>288</td><td>1.000</td></tr>
<tr><td>10</td><td>384</td><td>2.370</td></tr>
<tr><td rowspan="3">[01]</td><td>00</td><td>186</td><td>0.113</td></tr>
<tr><td>01</td><td>384</td><td>1.000</td></tr>
<tr><td>10</td><td>588</td><td>3.590</td></tr>
</table></td></tr>
<tr><td>FL_BANK[1:0]
FL_BANK[2:0]*</td><td>SFR B6[1:0]
SFR B6[2:0]</td><td>1</td><td>1</td><td>R/W</td><td>Flash bank selection register. Flash memory above 32 k is map
dress space from 0x8000 to 0xFFFF in 32 k banks. When MPU
address in flash is mapped to FL_BANK[1:0] or FL_BANK[2:0],
FL_BANK is reset by the erase cycle.</td></tr>
<tr><td>FLSH_ERASE [7:0]</td><td>SFR 94[7:0]</td><td>0</td><td>0</td><td>W</td><td>Flash Erase Initiate. (Default = 0x00). FLSH_ERASE is used to i
Mass Erase cycle or the Flash Page Erase cycle. Specific patte
FLSH_ERASE in order to initiate the appropriate Erase cycle.
0x55 = Initiate Flash Page Erase cycle. Must be proceeded
FLSH_PGADR @ SFR 0xB7.
0xAA = Initiate Flash Mass Erase cycle. Must be proceeded
FLSH_MEEN @ SFR 0xB2 and the debug (CC) port
Any other pattern written to FLSH_ERASE will have no effect. Th
completed until 0x00 is written to FLSH_ERASE.</td></tr>
<tr><td>FLSH_MEEN</td><td>SFR B2[1]</td><td>0</td><td>0</td><td>W</td><td>Mass Erase Enable.
0 = Mass Erase disabled (default).
1 = Mass Erase enabled.
Must be re-written for each new Mass Erase cycle.</td></tr>
<tr><td>FLSH_PGADR [5:0]</td><td>SFR B7 [7:2]</td><td>0</td><td>0</td><td>W</td><td>Flash Page Erase Address. (Default = 0x00)
FLSH_PGADR[5:0] with FL_BANK[2:0], sets the Flash Page Add
127) that will be erased during the Page Erase cycle.
Must be re-written for each new Page Erase cycle.</td></tr>
<tr><td>FLSH_PWE</td><td>SFR B2[0]</td><td>0</td><td>0</td><td>R/W</td><td>Program Write Enable. This bit must be cleared by the MPU aft
eration. Writes to this bit are inhibited when interrupts are enab
0 = MOVX commands refer to XRAM Space, normal operati
1 = MOVX @DPTR,A moves A to Program Space (Flash) @</td></tr>
<tr><td>FOVRIDE</td><td>20FD[4]</td><td>0</td><td>0</td><td>R/W</td><td>Permits the values written by the MPU to temporarily override th
register (reserved for production test).</td></tr>
</table>

GP0 ... *GP7*	20C0 … 20C7	0 … 0	NV … NV	R/W	Non-volatile general-purpose registers powered by the RTC sup maintain their value in all power modes, but will be cleared on re *GP0…GP7* will be undefined if VBAT drops below the minimum v
IE_FWCOL0 *IE_FWCOL1*	SFR E8[2] SFR E8[3]	0 0	0 0	R/W R/W	Interrupt flags for the Firmware Collision Interrupt. See the Flas details.
IE_PB	SFR E8[4]	0	–	R/W	PB flag. Indicates that a rising edge occurred on PB. Firmware this bit to clear it. The bit is also cleared when the MPU request mode. On bootup, the MPU can read this bit to determine if the the PB DIO0[0].
IE_PLLRISE	SFR E8[6]	0	0	R/W	Indicates that the MPU was woken or interrupted (INT4) by syst available, or more precisely, by PLL_OK rising. The firmware m bit to clear it.
IE_PLLFALL	SFR E8[7]	0	0	R/W	Indicates that the MPU has entered BROWNOUT mode becaus become unavailable (INT4), or more precisely, because PLL_O be set if the part wakes into BROWNOUT mode because of PB The firmware must write a zero to this bit to clear it.
IEN_SPI	20B0[4]			R/W	SPI interrupt enable.
IEN_WD_NROVF	20B0[0]	0	0	R/W	Active high watchdog near overflow interrupt enable.
IE_XFER *IE_RTC*	SFR E8[0] SFR E8[1]	0 0	0 0	R/W	Interrupt flags. These flags monitor the XFER_BUSY interrupt a interrupt. The flags are set by hardware and clear automatically
IE_WAKE	SFR E8[5]	0	–	R/W	Indicates that the MPU was awakened by the autowake timer. T by the MPU on bootup. The firmware must write a zero to this b
INTBITS	SFR F8[6:0]	–	–	R/W	Interrupt inputs. The MPU may read these bits to see the status INT0, INT1 up to INT6. These bits do not have any memory and for debug use.
LCD_BITMAP [31:24]	2023[7:0]	0	L	R/W	Configuration for DIO11/SEG31 through DIO4/SEG24. Unused bi 1 = LCD pin, 0 = DIO pin.
LCD_BITMAP [39:32]	2024[7:0]	0	L	R/W	Configuration for DIO19/SEG39 through DIO12/SEG32. *LCD_B* ponding to DIO12/SEG32 is only applicable to the 71M6534. U to zero. 1 = LCD pin, 0 = DIO pin.
LCD_BITMAP [47:40]	2025[7:0]	0	L	R/W	Configuration for DIO27/SEG47 through DIO20/SEG40. (*LCD_B* ponding to DIO22/SEG42 is only applicable to the 71M6534. Unus zero. 1 = LCD pin, 0 = DIO pin.

LCD_BITMAP [50:48]	2026[2:0]	0	L	R/W	Configuration for DIO30/SEG50 through DIO28/SEG48. *LCD_B* ing to DIO28/SEG48 is only applicable to the 71M6534. Unused b 1 = LCD pin, 0 = DIO pin.
*LCD_BITMAP [63:61], [59:56]**	2027[7:5,3:0]	0	L	R/W	Configuration for DIO43/SEG63 through DIO41/SEG61 and DIO DIO36/SEG56. *LCD_BITMAP[62]* corresponding to DIO42/SEG *LCD_BITMAP[59:56]* corresponding to DIO39/SEG59 through D applicable to the 71M6534. Unused bits should be set to zero. 1 = LCD pin, 0 = DIO pin.
LCD_BITMAP [71:64]	2028[7:0]	0	L	R/W	Configuration for DIO51/SEG71 through DIO44/SEG64. *LCD_B* ing to DIO46/SEG66 is only applicable to the 71M6534. Unused b 1 = LCD pin, 0 = DIO pin.
LCD_BLKMAP18 [3:0]	205A[3:0]	0	L	R/W	Identifies which segments connected to SEG18 should blink. 1 most significant bit corresponds to COM3, the least significant b
LCD_CLK[1:0]	2021[1:0]	0	L	R/W	Sets the LCD clock frequency for the COM/SEG pins (not the fr the following (f_w = 32768 Hz): 00 = f_w/512, 01 = f_w/256, 10 = f_w/128, 11 = f_w/64
LCD_DAC[2:0]	20AB[3:1]	0	L	R/W	LCD contrast control DAC. Adjusts the LCD voltage in steps of (mission mode) or VBAT (brownout/LCD modes).
LCD_E	2021[5]	0	L	R/W	Enables the LCD display. When disabled, VLC2, VLC1 and VL the COM and SEG outputs.

LCD_DAC[2:0]	**Resulting LCD Voltage**
000	V3P3 or VBAT
001	V3P3 or VBAT – 0.2V
010	V3P3 or VBAT – 0.4V
011	V3P3 or VBAT – 0.6V
100	V3P3 or VBAT – 0.8V
101	V3P3 or VBAT – 1.0V
110	V3P3 or VBAT – 1.2V
111	V3P3 or VBAT – 1.4V

LCD_MODE[2:0]	2021[4:2]	0	L	R/W	The LCD bias mode. Use the LCD DAC to reduce saturation. T the number of commons which are driven to multiplex the LCD. ***LCD_MODE[2:0]*** / **Function** / **Notes** 000 / 4 states, ⅓ bias / ⅓ bias modes can 001 / 3 states, ⅓ bias / 010 / 2 states, ½ bias / ½ bias and static m 011 / 3 states, ½ bias / both 3.3 V and 5 V 100 / static display /
LCD_ONLY	20A9[5]	0	0	W	Puts the 71M6533/71M6534 to sleep, but with the LCD display is ignored if system power is present. While in SLEEP mode, th on reset, when the autowake timer times out, when the push bu system power returns.
LCD_SEG0[3:0] … *LCD_SEG18[3:0]*	2030[3:0] … 2042[3:0]	0 … 0	L … L	R/W	LCD Segment Data. Each word contains information for 1 to 4 t segment.
LCD_SEG19[3:0] … *LCD_SEG31[3:0]*	2043[3:0] … 204F[3:0]	0 … 0	L … L	R/W	In each word, bit 0 corresponds to COM0, bit 1 to COM1, bit 2 t COM3 of the first segment. Bits 4 through 7 correspond to COM tively, of the second segment.
*LCD_SEG32[3:0]**	2050[3:0]	0	L	R/W	Care should be taken when writing to *LCD_SEG* locations since DIO pins.
LCD_SEG33[3:0] … *LCD_SEG41[3:0]*	2051[3:0] … 2059[3:0]	0 … 0	L … L	R/W	*LCD_SEG32*, *LCD_SEG42*, *LCD_SEG48*, *LCD_SEG51* through *LCI* *LCD_SEG66*, and *LCD_SEG72* through *LCD_SEG75* are only app
*LCD_SEG42[3:0]**	2030[7:4]	0	L	R/W	
LCD_SEG43[3:0] … *LCD_SEG47[3:0]*	2031[7:4] … 2035[7:4]	0 … 0	L … L	R/W	
*LCD_SEG48[3:0]**	2036[7:4]	0	L	R/W	
LCD_SEG49[3:0] *LCD_SEG50[3:0]*	2037[7:4] 2038[7:4]	0 0	L L	R/W R/W	
LCD_SEG51[3:0] … *LCD_SEG59[3:0]**	2039[7:4] … 2041[7:4]	0 … 0	L … L	R/W	
LCD_SEG61[3:0]	2043[7:4]	0	L	R/W	
*LCD_SEG62[3:0]**	2044[7:4]	0	L	R/W	

LCD_SEG63[3:0] … *LCD_SEG65[3:0]*	2045[7:4] … 2047[7:4]	0 … 0	L … L	R/W	
*LCD_SEG66[3:0]**	2048[7:4]	0	L	R/W	
LCD_SEG67[3:0] … *LCD_SEG71[3:0]*	2049[7:4] … 204D[7:4]	0 … 0	L … L	R/W	LCD Segment Data continued.
*LCD_SEG72[3:0]** … *LCD_SEG75[3:0]**	204E[7:4] … 2051[7:4]	0 … 0	L … L	R/W	
LCD_Y	2021[6]	0	L	R/W	LCD Blink Frequency (ignored if blink is disabled or if the segme 0 = 1 Hz (500 ms ON, 500 ms OFF) 1 = 0.5 Hz (1 s ON, 1 s OFF)
M26MHZ *M40MHZ*	2005[4] 2005[0]	0 0	0 0	R/W R/W	*M26MHZ* and *M40MHZ* set the master clock (MCK) frequency. T chip reset and may only be set. Attempts to write zeroes to *M4* ignored.
MPU_DIV[2:0]	2004[2:0]	0	0	R/W	The MPU clock divider (from MCK). These bits may be program risk of losing control.
MUX_ALT	2005[2]	0	0	R/W	The MPU asserts this bit when it wishes the MUX to perform AD alternate set of inputs. If *CHOP_E* is 00, *MUX_ALT* is automatically asserted once per s XFER_BUSY falls.

M40MHZ	*M26MHZ*	MCK Frequency
0	0	20 MHz
0	1	26.7 MHz
1	0	40 MHz
1	1	40 MHz

MPU_DIV[2:0]	Resulting Clock Frequency
000	MCK/4
001	MCK/8
010	MCK/16
011	MCK/32
100	MCK/64
101	MCK/128
110	MCK/265
111	MCK/265

MUX_DIV[3:0]	209D[3:0]	0	0	R/W	The number of states in the input multiplexer.
MUX_SYNC_E	2020[7]	0	0	R/W	When set, SEG7 outputs MUX_SYNC. Otherwise, SEG7 is an
OPT_FDC[1:0]	2007[1:0]	0	0	R/W	Selects the modulation duty cycle for OPT_TX. ***OPT_FDC*[1:0]** / **Function** 00 / 50% Low 01 / 25% Low 10 / 12.5% Low 11 / 6.25% Low
OPT_RXDIS	2008[5]	0	0	R/W	Configures OPT_RX to an analog input to the optical UART con input/output, DIO1. 0 = OPT_RX, 1 = DIO1.
OPT_RXINV	2008[4]	0	0	R/W	Inverts the result from the OPT_RX comparator when 1. Affects Has no effect when OPT_RX is used as a DIO input.
OPT_TXE[1:0]	2007[7:6]	00	00	R/W	Configures the OPT_TX output pin. ***OPT_TXE*[1:0]** / **Function** 00 / OPT_TX 01 / DIO2 10 / WPULSE 11 / RPULSE
OPT_TXINV	2008[0]	0	0	R/W	Inverts *OPT_TX* when 1. This inversion occurs before modulatio
OPT_TXMOD	2008[1]	0	0	R/W	Enables modulation of OPT_TX. When *OPT_TXMOD* is set, OP when it would otherwise have been zero. The modulation is ap sion caused by *OPT_TXINV*.
PLL_OK	2003[6]	0	0	R	Indicates that system power is present and the clock generation
PLS_MAXWIDTH [7:0]	2080[7:0]	FF	FF	R/W	Determines the maximum width of the pulse (low going pulse). The maximum pulse width is (2*PLS_MAXWIDTH + 1)*T_I. Whe If *PLS_INTERVAL* = 0, T_I is the sample time (397 µs). If set to 25 is disabled and pulses are output with a 50% duty cycle.
PLS_INTERVAL [7:0]	2081[7:0]	0	0	R/W	For PULSE_W and PULSE_V only, if the FIFO is used, *PLS_INT* 81. If *PLS_INTERVAL* = 0, the FIFO is not used and pulses are CE issues them.
PLS_INV	2004[6]	0	0	R/W	Inverts the polarity of the pulse outputs Normally, these pulses inverted, they become active high.
PREBOOT	SFRB2[7]	–	–	R	Indicates that the preboot sequence is active.

PREG[16:0]	201C[2:0] 201D[7:0] 201E[7:2]	4 0 0	4 0 0	R/W R/W R/W	RTC adjust. See Section 1.4.3 Real-Time Clock (RTC) for addi 0x0FFBF ≤ *PREG* ≤ 0x10040 *PREG*[16:0] and *QREG*[1:0] are separate in hardware but can be single number calculated by the MPU.
PRE_SAMPS[1:0]	2001[7:6]	0	0	R/W	The duration of the pre-summer, in samples. ***PRE_SAMPS*[1:0]** / **Pre-Summer Duration** 00 / 42 01 / 50 10 / 84 11 / 100
QREG[1:0]	201E[1:0]	0	0	R/W	RTC adjust. See Section 1.4.3 Real-Time Clock (RTC) for addi
RST_SUBSEC	2010[0]	0	0	R/W	The sub-second counter is restarted when a 1 is written to this b
RTCA_ADJ[6:0]	2011[6:0]	40	–	R/W	Analog RTC adjust. See Section 1.4.3 Real-Time Clock (RTC)
RTC_SEC[5:0 *RTC_MIN[5:0]* *RTC_HR[4:0]* *RTC_DAY[2:0]* *RTC_DATE[4:0]* *RTC_MO[3:0]* *RTC_YR[7:0]*	2015 2016 2017 2018 2019 201A 201B	* * * * * * *	NV NV NV NV NV NV NV	R/W	These are the year, month, day, hour, minute and second paran Writing to these registers sets the time. Each write to one of the preceded by a write to 0x201F (*WE*). Valid values for each para SEC: 00 to 59, MIN: 00 to 59, HR: 00 to 23 (00 = Midnight) DAY: 01 to 07 (01 = Sunday), DATE: 01 to 31, MO: 01 to 12 YR: 00 to 99 (00 and all others divisible by 4 are leap years) Values in the RTC registers are undefined when the IC powers are maintained through mission and battery modes when a suffi tained at the VBAT pin. Write operations to these registers are second. * no change of value at reset if voltage at VBAT is within specifi
RTM_E	2002[3]	0	0	R/W	Real Time Monitor enable (RTM). When 0, the RTM output is lo
RTM0[7:0] *RTM1[7:0]* *RTM2[7:0]* *RTM3[7:0]*	2060[9:8] 2061[7:0] 2062[9:8] 2063[7:0] 2064[9:8] 2064[7:0] 2065[9:8] 2066[7:0]	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	R/W	The four RTM probes. Before each CE code pass, the values o serially output on the RTM pin. The RTM registers are ignored
SECURE	SFRB2[6]	0	–	R/W	When set, enables security provisions that prevent external read and CE program RAM (zeros will be returned if the memory is re while PREBOOT is set. This bit is cleared when the flash is ma reset. The bit may only be set, attempts to write zero are ignore

SLEEP	20A9[6]	0	0	W	Puts the 71M6533/71M6534 into SLEEP mode. This bit is ignor present. The 71M6533 and 71M6534 will wake when the autow when the push button is pushed, when system power returns or high.
SEL_IAN *SEL_IBN* *SEL_ICN* *SEL_IDN*	20AC[1] 20AC[5] 20AD[1] 20AD[5]	0 0 0 0	0 0 0 0	R/W	When set to 1, selects differential mode for the corresponding c or ID). When 0, the input remains single-ended.
SLOT0_SEL[3:0] *SLOT1_SEL[3:0]* … *SLOT8_SEL[3:0]* *SLOT9_SEL[3:0]*	2090[3:0] 2090[7:4] 2094[3:0] 2094[7:4]	0 1 … 8 9	0 1 … 8 9	R/W	Primary multiplexer frame analog input selection. These bits ma 0-9 to the multiplexer state. The ADC output is always written to corresponding to the input, regardless of which multiplexer state (see Section 1.2 Analog Front End (AFE)).
SLOT0_ALTSEL [3:0] *SLOT1_ALTSEL [3:0]* *SLOT2_ALTSEL [3:0]* … *SLOT8_ALTSEL [3:0]* *SLOT9_ALTSEL [3:0]*	2096[3:0] 2096[7:4] 2097[3:0] … 209A[3:0] 209A[7:4]	10 1 11 … 8 9	10 1 11 … 8 9	R/W	Alternate multiplexer frame analog input selection. Maps the se the multiplexer state. The additional inputs, 10 and 11 in the alternate frame are: 10 = TEMP 11 = VBAT
SP_ADDR[15:8] *SP_ADDR[7:0]*	2072[7:0] 2073[7:0]	–	–	R R	SPI Address. 16-bit address from the bus master.
SP_CMD	2071	–	–	R	SPI command. 8-bit command from the bus master.
SPE	2070[7]	0	0	R/W	SPI port enable. Enables the SPI interface on pins SEG3 throu
SPI_FLAG	20B1[4]			R/W	SPI interrupt flag. The flag is set by the hardware and is cleared ing a 0. Firmware using this interrupt should clear the spurious ing initialization.
SUBSEC[7:0]	2014[7:0]	–	–	R	The remaining count, in terms of 1/256 RTC cycles, to the next *SUBSEC* may be read by the MPU after the one second interrupt the next one second boundary. Setting *RST_SUBSEC* will clear
SUM_CYCLES[5:0]	2001[5:0]	0	0	R/W	The number of pre-summer outputs summed in the final summe
TMUX[4:0]	20AA[4:0]	2	–	R/W	Selects one of 32 signals for TMUXOUT. For details, see Secti (TMUXOUT Pin).

<table>
<tr><td>TRIMSEL[3:0]</td><td>20FD[3:0]</td><td>0</td><td>0</td><td>R/W</td><td>Selects the temperature trim fuse to be read with the TRIM regis
<table>
<tr><th>TRIMSEL[3:0]</th><th>Trim Fuse</th><th>Purpose</th></tr>
<tr><td>1</td><td>TRIMT[7:0]</td><td>Trim for the magnitude</td></tr>
<tr><td>4</td><td>TRIMM[2:0]</td><td rowspan="3">Trim values related to pensation</td></tr>
<tr><td>5</td><td>TRIMBGA</td></tr>
<tr><td>6</td><td>TRIMBGB</td></tr>
</table></td></tr>
<tr><td>TRIM[7:0]</td><td>20FF</td><td>0</td><td>0</td><td>R/W</td><td>Contains TRIMBGA,TRIMBGB or TRIMM[2:0] depending on the TRIMSEL[3:0]. If TRIMBGB = 0, the device is a 71M6533/71M65 71M6533H/71M6534H.</td></tr>
<tr><td>UMUX_E*</td><td>200F[7]</td><td>0</td><td>0</td><td>R/W</td><td>Enables the optical UART multiplexer, selects the alternate func DIO8, DIO9.</td></tr>
<tr><td>UMUX_SEL*</td><td>S00F[6]</td><td>0</td><td>0</td><td>R/W</td><td>When UMUX_E = 1, selects between OPT_TX, OPT_RX and M UART I/O pins. 0 = OPT_TX, OPT_RX, 1 = MTX, MRX</td></tr>
<tr><td>VB_REF</td><td>2005[6]</td><td>0</td><td>0</td><td>R/W</td><td>Configures the ADC so that VB is the zero reference.</td></tr>
<tr><td>VDDREGZ</td><td>2005[7]</td><td>0</td><td>0</td><td>R/W</td><td>When zero, changes the input reference of the ADC to V3P3A f VB inputs. Otherwise, the reference is VBIAS.</td></tr>
<tr><td>VERSION[7:0]</td><td>2006
20C8</td><td>–
–</td><td>–
–</td><td>R
R</td><td>The device version index. This word may be read by the firmwa silicon version.
<table>
<tr><th>VERSION[7:0]</th><th>Silicon Version</th></tr>
<tr><td>0000 0101</td><td>A05</td></tr>
</table></td></tr>
<tr><td>VREF_CAL</td><td>2004[7]</td><td>0</td><td>0</td><td>R/W</td><td>Brings VREF to the VREF pad. This feature is disabled when V</td></tr>
<tr><td>VREF_DIS</td><td>2004[3]</td><td>0</td><td>0</td><td>R/W</td><td>Disables the internal voltage reference.</td></tr>
<tr><td>WAKE_ARM</td><td>20A9[7]</td><td>0</td><td>–</td><td>W</td><td>Writing a 1 to this bit arms the autowake timer and presets it wit in WAKE_PRD and WAKE_RES. The autowake timer is reset and the processor is in MISSION mode or BROWNOUT mode. The at least three RTC cycles before the SLEEP or LCD-ONLY mod</td></tr>
<tr><td>WAKE_PRD</td><td>20A9[2:0]</td><td>001</td><td>–</td><td>R/W</td><td>Sleep time. Time = WAKE_PRD[2:0]*WAKE_RES. The default = value is 7.</td></tr>
<tr><td>WAKE_RES</td><td>20A9[3]</td><td>0</td><td>–</td><td>R/W</td><td>Resolution of WAKE timer: 1 = 1 minute, 0 = 2.5 seconds.</td></tr>
<tr><td>WD_NROVF_FLAG</td><td>20B1[0]</td><td>–</td><td>0</td><td>R/W</td><td>This flag is set approximately 1 ms before the watchdog timer o by writing a 0 or on the falling edge of WAKE.</td></tr>
<tr><td>WD_RST</td><td>SFR F8[7]</td><td>0</td><td>0</td><td>W</td><td>WD timer bit. This bit must be accessed with byte operations. this bit are:
Write 0: Clears the flag.
Write 1: Resets the WDT.</td></tr>
</table>

WD_OVF	2002[2]	0	0	R/W	The WD overflow status bit. This bit is set when the WD timer o by the nonvolatile supply and at bootup will indicate if the part is overflow or a power fault. This bit should be cleared by the MPU automatically cleared when RESET is high.
WE	201F[7:0]			W	An 8-bit value has to be written to this address prior to accessing the
WRPROT_BT	SFR B2[5]	0	0		When set, this bit protects flash addresses from 0 to *BOOT_SIZE**102
WRPROT_CE	SFR B2[4]	0	0		When set, this bit protects flash addresses from *CE_LCTN**1024 from flash page erase.

4.3 CE Interface Description

4.3.1 CE Program

The CE performs the precision computations necessary to accurately measure power. These computations include offset cancellation, phase compensation, product smoothing, product summation, frequency detection, VAR calculation, sag detection and voltage phase measurement. All data computed by the CE is dependent on the selected meter equation as given by *EQU* (in I/O RAM). As a function of *EQU*, the element components V0 through I2 take on different meanings.

The CE program is supplied by Teridian as a data image that can be merged with the MPU operational code for meter applications. Typically, the CE program covers most applications and does not need to be modified. Other variations of CE code may be available from TERIDIAN. The description in this section applies to CE code revision CE34A02D, which functions for both the 71M6533 and the 71M6534. This version of the CE code does not process the ID current channel. CE codes capable of calculating and measuring the ID channel are available from Teridian.

4.3.2 CE Data Format

All CE words are 4 bytes. Unless specified otherwise, they are in 32-bit two's complement format (-1 = 0xFFFFFFFF). Calibration parameters are defined in flash memory (or external EEPROM) and must be copied to CE data memory by the MPU before enabling the CE. Internal variables are used in internal CE calculations. Input variables allow the MPU to control the behavior of the CE code. Output variables are outputs of the CE calculations. The corresponding MPU address for the most significant byte is given by 0x0000 + 4 x CE_address and by 0x0003 + 4 x CE_address for the least significant byte.

4.3.3 Constants

Constants used in the CE Data Memory tables are:

- Sampling Frequency: F_S = 32768 Hz/13 = 2520.62 Hz.
- F_0 is the fundamental frequency of the mains phases.
- *IMAX* is the external rms current corresponding to 250 mV pk at the inputs IA, IB and IC.
- *VMAX* is the external rms voltage corresponding to 250 mV pk at the VA, VB and VC inputs.
- NACC, the accumulation count for energy measurements is *PRE_SAMPS*SUM_CYCLES*. This value also resides in *SUM_PRE* (CE address 0x23) where it is used for phase angle measurement.
- The duration of the accumulation interval for energy measurements is *PRE_SAMPS*SUM_CYCLES*/F_S.
- In_8 is a gain constant of the current channel, n. Its value is 8 or 1 and is controlled by *In_SHUNT*.
- X is a gain constant of the pulse generators. Its value is determined by *PULSE_FAST* and *PULSE_SLOW*.
- Voltage LSB for sag detection = *VMAX* * 7.879810^{-9} V.

The system constants *IMAX* and *VMAX* are used by the MPU to convert internal digital quantities (as used by the CE) to external, i.e. metering quantities. Their values are determined by the scaling of the voltage and current sensors used in an actual meter. The LSB values used in this document relate digital quantities at the CE or MPU interface to external meter input quantities. For example, if a SAG threshold of 80 V peak is desired at the meter input, the digital value that should be programmed into *SAG_THR* would be 80 V/SAG_THR_{LSB}, where SAG_THR_{LSB} is the LSB value in the description of *SAG_THR*.

The parameters *EQU*, *CE_E*, *PRE_SAMPS*, and *SUM_CYCLES* essential to the function of the CE are stored in I/O RAM (see Section 4.2 I/O RAM Description – Alphabetical Order).

4.3.4 Environment

Before starting the CE using the *CE_E* bit, the MPU has to establish the proper environment for the CE by implementing the following steps:

- Load the CE data into RAM.
- Establish the equation to be applied in *EQU*.
- Establish the accumulation period and number of samples in *PRE_SAMPS* and *SUM_CYCLES*.
- Establish the number of cycles per ADC multiplexer frame (*MUX_DIV*).
- Apply proper values to *SLOTn_SEL* and *SLOTn_ALTSEL*.
- Initialize any MPU interrupts, such as CE_BUSY, XFER_BUSY, or a power failure detection interrupt.

Typically, there are thirteen 32768 Hz cycles per ADC multiplexer frame (see Figure 18 in the System Timing Summary section). This means that the product of the number of cycles per frame and the number of conversions per frame must be 12 (allowing for one settling cycle). The default configuration is *FIR_LEN* = 0 (two cycles per conversion) and *MUX_DIV* = 6 (6 conversions per mux cycle).

4.3.5 CE Calculations

Table 48: CE *EQU* Equations and Element Input Mapping

EQU	Watt & VAR Formula *(WSUM/VARSUM)*	*W0SUM/ VAR0SUM*	*W1SUM/ VAR1SUM*	*W2SUM/ VAR2SUM*	*I0SQ SUM*	*I1SQ SUM*	*I2SQ SUM*
0*	VA IA (1 element, 2W 1ϕ)	VA*IA	–	–	IA	–	–
1*	VA*(IA-IB)/2 (1 element, 3W 1ϕ)	VA*(IA-IB)/2	–	–	IA-IB	IB	–
2*	VA*IA + VB*IB (2 element, 3W 3ϕ Delta)	VA*IA	VB*IB	–	IA	IB	–
3*	VA*(IA-IB)/2 + VC*IC (2 element, 4W 3ϕ Delta)	VA*(IA-IB)/2	–	VC*IC	IA-IB	IB	IC
4*	VA*(IA-IB)/2 + VB*(IC-IB)/2 (2 element, 4W 3ϕ Wye)	VA*(IA-IB)/2	VB*(IC-IB)/2	–	IA-IB	IC-IB	IC
5	VA*IA + VB*IB + VC*IC (3 element, 4W 3ϕ Wye)	VA*IA	VB*IB	VC*IC	IA	IB	IC

* Only *EQU* = 5 is supported by CE code version CE34A02D.

4.3.6 CE Front End Data (Raw Data)

Access to the raw data provided by the AFE is possible by reading addresses 0 through B shown in Table 49.

Table 49: CE Raw Data Access Locations

Name	Address			Description
	CE	MPU	Type	
IA FIR data	0x00	0x00	Input	ADC Input data, valid at the end of the MUX frame. The address mapping of analog inputs to memory is hard-wired in the ADC converter circuit.
VA FIR data	0x01	0x04	Input	
IB FIR data	0x02	0x08	Input	
VB FIR data	0x03	0x0C	Input	
IC FIR data	0x04	0x10	Input	
VC FIR data	0x05	0x14	Input	
ID FIR data	0x06	0x18	Input	

Name	Address			Description
	CE	MPU	Type	
TEMP FIR data	0x0A	0x28	Input	
VBAT FIR data	0x0B	0x2C	Input	
…		…	Internal	…
Chip ID, Version bytes	0x0F	003C	Read Only	Upper 16 bits are zero. Lower 16 bits are *CHIP_ID*[15:8], *VERSION*[7:0]. This word is read only.
…		…	Internal	…
Last Address	0x3FF	0xFFC	Internal	Last Memory Location

4.3.7 CE Status and Control

The CE Status Word is useful for generating early warnings to the MPU (Table 50). It contains sag warnings for phase A, B, and C, as well as *F0*, the derived clock operating at the fundamental input frequency. The MPU can read the CE status word at every CE_BUSY interrupt. Since the CE_BUSY interrupt occurs at 2520.6 Hz, it is desirable to minimize the computation required in the interrupt handler of the MPU.

Table 50: *CESTATUS* Register

CE Address	Name	Description
0x80	*CESTATUS*	See description of *CESTATUS* bits in Table 51.

CESTATUS provides information about the status of voltage and input AC signal frequency, which are useful for generating an early power fail warning to initiate necessary data storage. *CESTATUS* represents the status flags for the preceding CE code pass (CE_BUSY interrupt). The significance of the bits in *CESTATUS* is shown in Table 51.

Table 51: *CESTATUS* Bit Definitions

CESTATUS [bit]	Name	Description
31:29	Not Used	These unused bits will always be zero.
28	*F0*	*F0* is a square wave at the exact fundamental input frequency.
27	*SAG_C*	Normally zero. Becomes one when |VC| remains below *SAG_THR* for *SAGCNT* samples. Will not return to zero until |VC| rises above *SAG_THR*.
26	*SAG_B*	Normally zero. Becomes one when VB remains below *SAG_THR* for *SAG_CNT* samples. Will not return to zero until VB rises above *SAG_THR*.
25	*SAG_A*	Normally zero. Becomes one when VA remains below *SAG_THR* for *SAG_CNT* samples. Will not return to zero until VA rises above *SAG_THR*.
24:0	Not Used	These unused bits will always be zero.

The CE is initialized by the MPU using *CECONFIG* (Table 52). This register contains in packed form *SAG_CNT*, *FREQSEL0*, *FREQSEL1*, *EXT_PULSE*, *I0_SHUNT*, *I1_SHUNT*, *PULSE_SLOW*, and *PULSE_FAST*. The *CECONFIG* bit definitions are given in Table 53.

Table 52: *CECONFIG* Register

CE Address	Name	Data	Description
0x20	*CECONFIG*	0x5020	See description of the *CECONFIG* bits in Table 53.

The *SAG_MASK*n bits enable sag detection for the respective phase when set to 1. When *SAG_INT* is set to 1, a sag event will generate a transition on the YPULSE output.

The *EXT_TEMP* bit enables temperature compensation by the MPU, when set to 1. When 0, internal (CE) temperature compensation is enabled.

I0_SHUNT, *I1_SHUNT* and *I2_SHUNT* can configure their respective current inputs to accept shunt resistor sensors. In this case the CE provides an additional gain of 8 to the selected current input. *WRATE* may need to be adjusted based on the values *In_SHUNT*.

The CE pulse generator can be controlled by either the MPU (external) or CE (internal) variables. Control is by the MPU if *EXT_PULSE* = 1. In this case, the MPU controls the pulse rate by placing values into *APULSEW* and *APULSER*. By setting *EXT_PULSE* = 0, the CE controls the pulse rate based on *WSUM* and *VARSUM*.

The 71M6533 Demo Code creep function halts both internal and external pulse generation.

Table 53: *CECONFIG* Bit Definitions

<table>
<tr><th>CECONFIG [bit]</th><th>Name</th><th>Default</th><th>Description</th></tr>
<tr><td>[20]</td><td>SAG_MASK2</td><td>0</td><td>When 1, enables sag interrupt based on phase C.</td></tr>
<tr><td>[19]</td><td>SAG_MASK1</td><td>0</td><td>When 1, enables sag interrupt based on phase B.</td></tr>
<tr><td>[18]</td><td>SAG_MASK0</td><td>0</td><td>When 1, enables sag interrupt based on phase A.</td></tr>
<tr><td>[17]</td><td>SAG_INT</td><td>0</td><td>When 1, activates YPULSE/DIO8 output when a sag is detected (see also 1.4.7).</td></tr>
<tr><td>[16]</td><td>EXT_TEMP</td><td>0</td><td>When 1, enables temperature compensation by the MPU. When 0, internal (CE) temperature compensation is enabled.</td></tr>
<tr><td>[15:8]</td><td>SAG_CNT</td><td>80 (0x50)</td><td>The number of consecutive voltage samples below SAG_THR before a sag alarm is declared. The maximum value is 255. SAG_THR is at address 0x24.</td></tr>
<tr><td>[7]</td><td>FREQSEL1</td><td>0</td><td rowspan="2">The combination of FREQSEL1 and FEQSEL2 selects the phase to be used for the frequency monitor, the phase-to-phase lag calculation and for the zero crossing counter (MAINEDGE_X).
<table>
<tr><th rowspan="2">FREQ SEL1</th><th rowspan="2">FREQ SEL0</th><th rowspan="2">Phase Selected</th><th colspan="2">Phases Used for Voltage Phase Lag Calculation</th></tr>
<tr><th>PH_AtoB_X</th><th>PH_AtoC_X</th></tr>
<tr><td>0</td><td>0</td><td>A</td><td>A-B</td><td>A-C</td></tr>
<tr><td>0</td><td>1</td><td>B</td><td>B-C</td><td>B-A</td></tr>
<tr><td>1</td><td>0</td><td>C</td><td>C-A</td><td>C-B</td></tr>
<tr><td>1</td><td>1</td><td colspan="3">Not allowed</td></tr>
</table></td></tr>
<tr><td>[6]</td><td>FREQSEL0</td><td>0</td></tr>
<tr><td>[5]</td><td>EXT_PULSE</td><td>1</td><td>When zero, causes the pulse generators to respond to internal data (WPULSE = WSUM_X, RPULSE = VARSUM_X, XPULSE = WSUM_X). Otherwise, the generators respond to values the MPU places in APULSEW and APULSER.</td></tr>
<tr><td>[4]</td><td>IC_SHUNT</td><td>0</td><td>When 1, the current gain of channel C is increased by 8. The gain factor controlled by In_SHUNT is referred to as In_8 throughout this document.</td></tr>
<tr><td>[3]</td><td>IB_SHUNT</td><td>0</td><td>When 1, the current gain of channel B is increased by 8.</td></tr>
<tr><td>[2]</td><td>IA_SHUNT</td><td>0</td><td>When 1, the current gain of channel A is increased by 8.</td></tr>
<tr><td>[1]</td><td>PULSE_FAST</td><td>0</td><td>When PULSE_FAST = 1, the pulse generator input is increased 16x. When PULSE_SLOW = 1, the pulse generator input is reduced by a factor of 64. These two parameters control the pulse gain factor X (see table below). Allowed values are ei-</td></tr>
</table>

[0]	*PULSE_SLOW*	0	ther 1 or 0. Default is 0 for both (X = 6).

PULSE_SLOW	*PULSE_FAST*	*X*
0	0	$1.5 * 2^2 = 6$
0	1	$1.5 * 2^6 = 96$
1	0	$1.5 * 2^{-4} = 0.09375$
1	1	Do not use

Table 54: Sag Threshold and Gain Adjust Control

CE Address	Name	Default	Description
0x24	*SAG_THR*	$2.39*10^7$	The voltage threshold for sag warnings. The default value is equivalent to 80 V RMS if *VMAX* = 600 V.
0x40	*GAIN_ADJ*	16384	This register scales all voltage and current channels. The default value is equivalent to unity gain (1.000).

4.3.8 CE Transfer Variables

When the MPU receives the XFER_BUSY interrupt, it knows that fresh data is available in the transfer variables. CE transfer variables are modified during the CE code pass that ends with an XFER_BUSY interrupt. They remain constant throughout each accumulation interval. In this data sheet, the names of CE transfer variables always end with _X. The transfer variables can be categorized as:

1. Fundamental energy measurement variables
2. Instantaneous (RMS) values
3. Other measurement parameters

Fundamental Energy Measurement Variables

Table 55 describes each transfer variable for fundamental energy measurement. All variables are signed 32-bit integers. Accumulated variables such as *WSUM* are internally scaled so they have at least 2x margin before overflow when the integration time is one second. Additionally, the hardware will not permit output values to fold back upon overflow.

Table 55: CE Transfer Variables

CE Address	Name	Description
0x85	*WSUM_X*	The signed sum: *W0SUM_X*+*W1SUM_X*+*W2SUM_X*.
0x86	*W0SUM_X*	The sum of Wh samples from each wattmeter element. LSB = $9.4045*10^{-13}$ *VMAX IMAX* / *In_8* Wh.
0x87	*W1SUM_X*	
0x88	*W2SUM_X*	
0x8A	*VARSUM_X*	The signed sum: *VAR0SUM_X*+*VAR1SUM_X*+*VAR2SUM_X*.
0x8B	*VAR0SUM_X*	The sum of VARh samples from each wattmeter element. LSB = $9.4045*10^{-13}$ *VMAX IMAX* / *In_8* VARh.
0x8C	*VAR1SUM_X*	
0x8D	*VAR2SUM_X*	

WxSUM_X and *VARSUM_X* are the signed sum of Phase-A, Phase-B and Phase-C Wh or VARh values according to the metering equation specified in the I/O RAM register *EQU*. *WxSUM_X* is the Wh value accumulated for phase x in the last accumulation interval and can be computed based on the specified LSB value.

For example, with *VMAX* = 600 V and *IMAX* = 208 A, the LSB for *WxSUM_X* is 0.1173 µWh.

Instantaneous Energy Measurement Variables

IxSQSUM_X and *VxSQSUM* are the squared current and voltage samples acquired during the last accumulation interval. *INSQSUM_X* can be used for computing the neutral current.

Table 56: CE Energy Measurement Variables

CE Address	Name	Description
0x8F	*I0SQSUM_X*	The sum of squared current samples from each element. $LSB_I = 9.4045*10^{-13}\ IMAX^2 / In\_8^2\ A^2h$
0x90	*I1SQSUM_X*	
0x91	*I2SQSUM_X*	
0x92	*INSQSUM_X*	The sum of squared current samples from the calculated neutral: $\sum (I_0 + I_1 + I_2)^2$ $LSB=9.4045*10^{-13}\ IMAX^2 / In\_8^2\ A^2h$
0x99	*I0SQRES_X*	Residual current measurements with double-precision accuracy. The exact current is: ISQn = *InSQSUM_X* + *InSQRES_X*
0x9A	*I1SQRES_X*	
0x9B	*I2SQRES_X*	
0x9C	*INSQRES_X*	
0x93	*V0SQSUM_X*	The sum of squared voltage samples from each element. $LSB_V = 9.4045*10^{-13}\ VMAX^2\ V^2h$
0x94	*V1SQSUM_X*	
0x95	*V2SQSUM_X*	

The RMS values can be computed by the MPU from the squared current and voltage samples as follows:

$$Ix_{RMS} = \sqrt{\frac{IxSQSUM \cdot LSB_I \cdot 3600 \cdot F_S}{N_{ACC}}} \qquad Vx_{RMS} = \sqrt{\frac{VxSQSUM \cdot LSB_V \cdot 3600 \cdot F_S}{N_{ACC}}}$$

Other Transfer variables include those available for frequency and phase measurement, and those reflecting the count of the zero-crossings of the mains voltage and the battery voltage. These transfer variables are listed in Table 57.

MAINEDGE_X reflects the number of half-cycles accounted for in the last accumulated interval for the AC signal of the phase specified in the *FREQSEL1* and *FREQSEL0* registers. *MAINEDGE_X* is useful for implementing a real-time clock based on the input AC signal.

Table 57: Other Transfer Variables

CE Address	Name	Description
0x82	*FREQ_X*	Fundamental frequency: LSB $\equiv \frac{F_S}{2^{32}} \approx 0.587 \cdot 10^{-6}\ Hz$
0x97	*PH_AtoB_X*	Voltage phase lag. The selection of the reference phase is based on *FREQSEL1* and *FREQSEL0* in the *CECONFIG* register: If *FREQSEL1/FREQSEL0* select phase A: Phase lag from A to B. If *FREQSEL1/FREQSEL0* select phase B: Phase lag from B to C. If *FREQSEL1/FREQSEL0* select phase C: Phase lag from C to A. The angle in degrees is (0 to 360): *PH_AtoB_X* * 360/N_{ACC} + 2.4

CE Address	Name	Description
0x98	*PH_AtoC_X*	If *FREQSEL1/FREQSEL0* select phase A: Phase lag from A to C. If *FREQSEL1/FREQSEL0* select phase B: Phase lag from B to A. If *FREQSEL1/FREQSEL0* select phase C: Phase lag from C to B. Angle in degrees is (0 to 360): *PH_AtoC_X* * 360/N_{ACC} + 4.8
0x83	*MAINEDGE_X*	The number of edge crossings of the selected voltage in the previous accumulation interval. Edge crossings are either direction and are de-bounced.

4.3.9 Other Measurement and Control Parameters

Temperature Measurement and Temperature Compensation

Table 58 describes the CE registers supporting temperature measurement and temperature compensation.

Table 58: CE Temperature Registers

CE Address	Name	Default	Description
0x81	*TEMP_RAW*	N/A	The filtered, unscaled reading from the temperature sensor.
0x9D	*TEMP_X*	N/A	This register contains the difference between the die temperature and the reference/calibration temperature as established in the *TEMP_NOM* register, measured in 0.1°C.
0x39	*DEGSCALE*	21755	Scale factor for the temperature calculation. . It is not necessary to use values other than the default value.
0x1F	*TEMP_NOM*	0	This register holds the reference or calibration temperature vale. At calibration time, the value read in *TEMP_RAW* must be written to *TEMP_NOM*.
0x3A	*PPMC*	0	Linear temperature correction factor.
0x3B	*PPMC2*	0	Quadratic temperature correction factor.

Pulse Generation

Table 59 describes the CE pulse generation parameters.

The combination of the *PULSE_SLOW* and *PULSE_FAST* parameters controls the speed of the pulse rate. The default values of 0 and 0 will maintain the original pulse rate given by the Kh equation.

WRATE controls the number of pulses that are generated per measured Wh and VARh quantities. The lower *WRATE* is the slower the pulse rate for measured energy quantity. The metering constant Kh is derived from *WRATE* as the amount of energy measured for each pulse. That is, if Kh = 1Wh/pulse, a power applied to the meter of 120 V and 30 A results in one pulse per second. If the load is 240 V at 150 A, ten pulses per second will be generated.

Control is transferred to the MPU for pulse generation if *EXT_PULSE* = 1. In this case, the pulse rate is determined by *APULSEW* and A*PULSER*. The MPU has to load the source for pulse generation in *APULSEW* and *APULSER* to generate pulses. Irrespective of the *EXT_PULSE* status, the output pulse rate controlled by *APULSEW* and *APULSER* is implemented by the CE only. By setting *EXT_PULSE* = 1, the MPU is providing the source for pulse generation. If *EXT_PULSE* is 1, *W0SUM_X* and *VAR0SUM_X* are the default pulse generation sources. In this case, creep cannot be controlled since it is an MPU function.

The maximum pulse rate is $3*F_S$ = 7.5 kHz.

PULSE_WIDTH allows adjustment of the pulse width for compatibility with calibration and other external equipment. The minimum pulse width possible is 66.16µs.

The maximum time jitter is1/6 of the MUX cycle period (nominally 67 µs) and is independent of the number of pulses measured. Thus, if the pulse generator is monitored for one second, the peak jitter is 67 ppm. After 10 seconds, the peak jitter is 6.7 ppm. The average jitter is always zero. If it is attempted to drive either pulse generator faster than its maximum rate, it will simply output at its maximum rate without exhibiting any rollover characteristics. The actual pulse rate, using *WSUM* as an example, is:

$$RATE = \frac{WRATE \cdot WSUM \cdot F_S \cdot X}{2^{46}} Hz,$$

where F_S = sampling frequency (2520.6 Hz), X = Pulse speed factor derived from the CE variables *PULSE_SLOW* and *PULSE_FAST*.

Table 59: CE Pulse Generation Parameters

CE Address	Name	Default	Description
0x21	*WRATE*	171	Kh = *VMAX***IMAX**66.1782 / (*In_8***WRATE**N_{ACC}*X) Wh/pulse.
0x22	*KVAR*	6448	Scale factor for VAR measurement.
0x23	*SUM_PRE*	2520	*PRE_SAMPS* * *SUM_CYCLES* (N_{ACC})
0x41	*APULSEW*	0	Wh pulse (WPULSE) generator input to be updated by the MPU when using external pulse generation. The output pulse rate is: *APULSEW* * F_S * 2^{-32} * *WRATE* * *X* * 2^{-14}. This input is buffered and can be updated by the MPU during a conversion interval. The change will take effect at the beginning of the next interval.
0x38	*PULSEWIDTH*	12	Register for pulse width control of XPULSE and YPULSE. The maximum pulse width is (2**PULSEWIDTH*+1)*(1/FS). The default value will generate pulses of 10 ms width at FS = 2520.62 Hz.
0x42	*APULSER*	0	VARh (RPULSE) pulse generator input.
0x43	*APULSEX*	0	Pulse generator input for XPULSE output.
0x44	*APULSEY*	0	Pulse generator input for YPULSE output.
0x45	*WSUM_ACCUM*	0	Roll-over accumulator for WPULSE.
0x46	*VSUM_ACCUM*	0	Roll-over accumulator for RPULSE.
0x47	*SUM2_ACCUM*	0	Roll-over accumulator for the XPULSE pulse output.
0x48	*SUM3_ACCUM*	0	Roll-over accumulator for the YPULSE pulse output.

Other CE Parameters

Table 60 shows the CE parameters used for suppression of noise due to scaling and truncation effects.

Table 60: CE Parameters for Noise Suppression and Code Version

CE Address	Name	Default	Description
0x26	*QUANTA*	0	These parameters are added in channel A to the Watt calculation to compensate for input noise and truncation. LSB = (*VMAX***IMAX* / *In_8*) *1.04173*10^{-9} W
0x27	*QUANTB*	0	
0x28	*QUANTC*	0	
0x2A	*QUANT_VARA*	0	These parameters are added to the VAR calculation for element A and B to compensate for input noise and truncation. LSB = (*VMAX***IMAX* / *In_8*) * 1.04173*10^{-9} W
0x2B	*QUANT_VARB*	0	
0x2C	*QUANT_VARC*	0	

0x2E	*QUANT_IA*	0	These parameters are added to compensate for input noise and truncation in their respective channels in the squaring calculations for I^2 and V^2. LSB=$VMAX^2$*5.08656*10^{-13} V^2 and LSB= ($IMAX^2$/*In_8*^{2})* 5.08656*10^{-13} A^2
0x2F	*QUANT_IB*	0	
0x30	*QUANT_IC*	0	
0x35	0x63653333		Text strings holding the CE version information as supplied by the CE data associated with the CE code. For example, the words 0x63653333 and 0x61303463 form the text string "ce33a04c". These locations are overwritten in operation.
0x36	0x61303463		
0x37	0x00000000		

4.3.10 CE Calibration Parameters

Table 61 lists the parameters that are typically entered to effect calibration of meter accuracy.

Table 61: CE Calibration Parameters

CE Address	Name	Default	Description
0x10	*CAL_IA*	16384	These constants control the gain of their respective channels. The nominal value for each parameter is 2^{14} = 16384. The gain of each channel is directly proportional to its CAL parameter. Thus, if the gain of a channel is 1% slow, CAL should be increased by 1%.
0x11	*CAL_VA*	16384	
0x12	*CAL_IB*	16384	
0x13	*CAL_VB*	16384	
0x14	*CAL_IC*	16384	
0x15	*CAL_VC*	16384	
0x18	*PHADJ_A*	0	These constants control the CT phase compensation. No compensation occurs when *PHADJ_X* = 0. As *PHADJ_X* is increased, more compensation (lag) is introduced. The range is $\pm 2^{15} - 1$. If it is desired to delay the current by the angle Φ, the equations are: $PHADJ\_X = 2^{20} \frac{0.02229 \cdot TAN\Phi}{0.1487 - 0.0131 \cdot TAN\Phi}$ at 60Hz $PHADJ\_X = 2^{20} \frac{0.0155 \cdot TAN\Phi}{0.1241 - 0.009695 \cdot TAN\Phi}$ at 50Hz
0x19	*PHADJ_B*	0	
0x1A	*PHADJ_C*	0	

4.3.11 CE Flow Diagrams

Figure 42 through Figure 44 show the data flow through the CE in simplified form. Functions not shown include delay compensation, sample interpolation, scaling and the processing of meter equations.

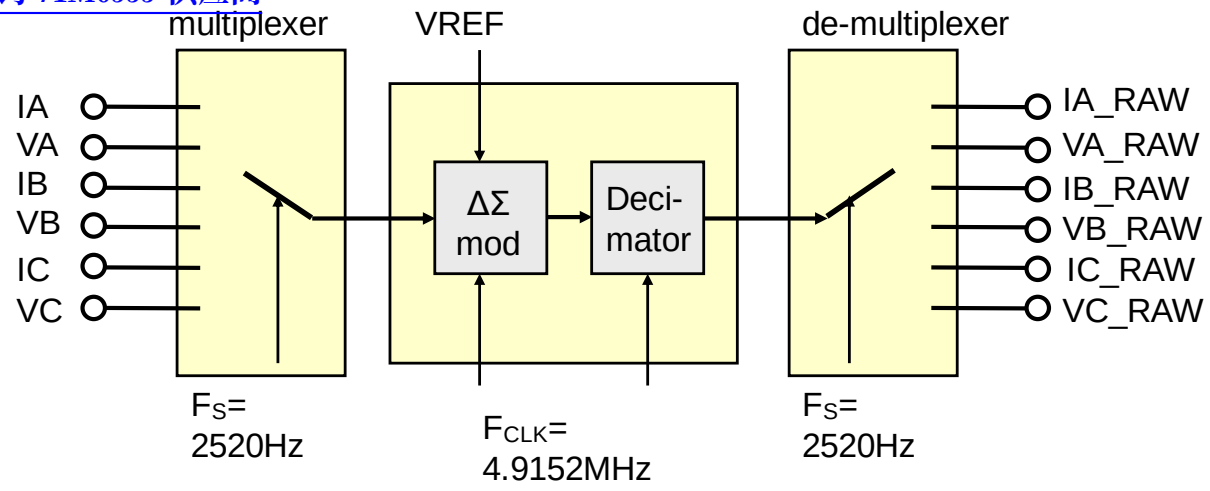


Figure 42: CE Data Flow: Multiplexer and ADC

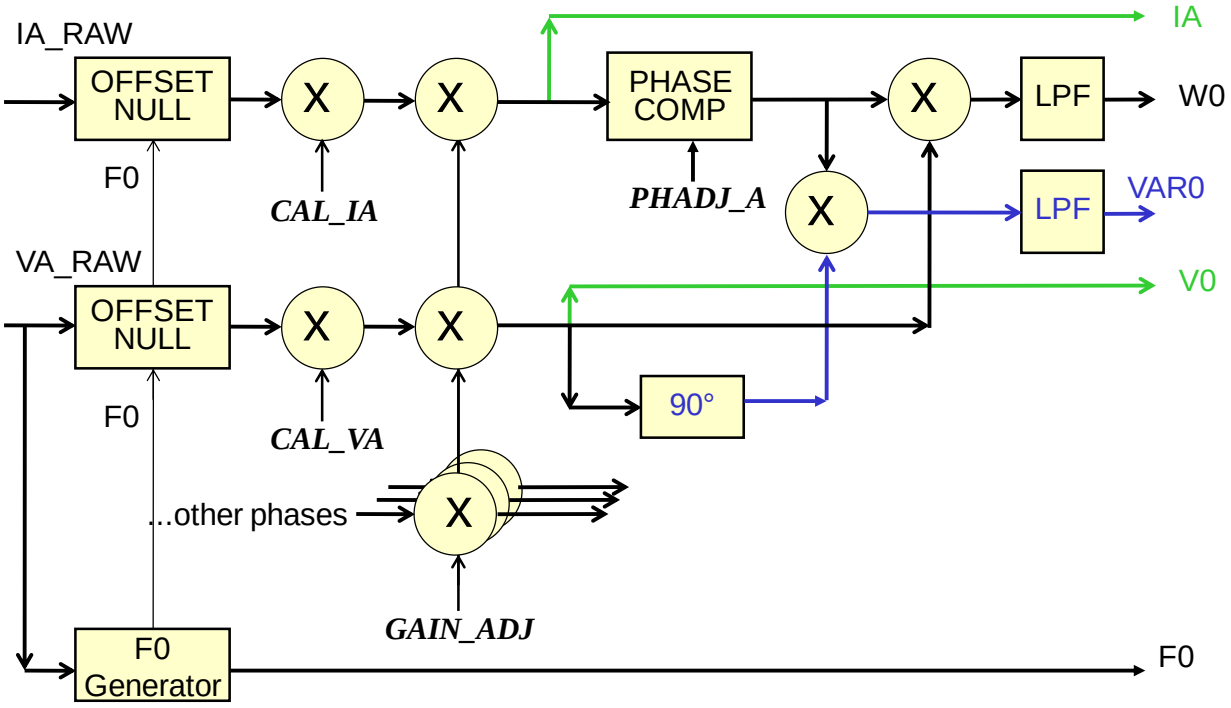


Figure 43: CE Data Flow: Scaling, Gain Control, Intermediate Variables

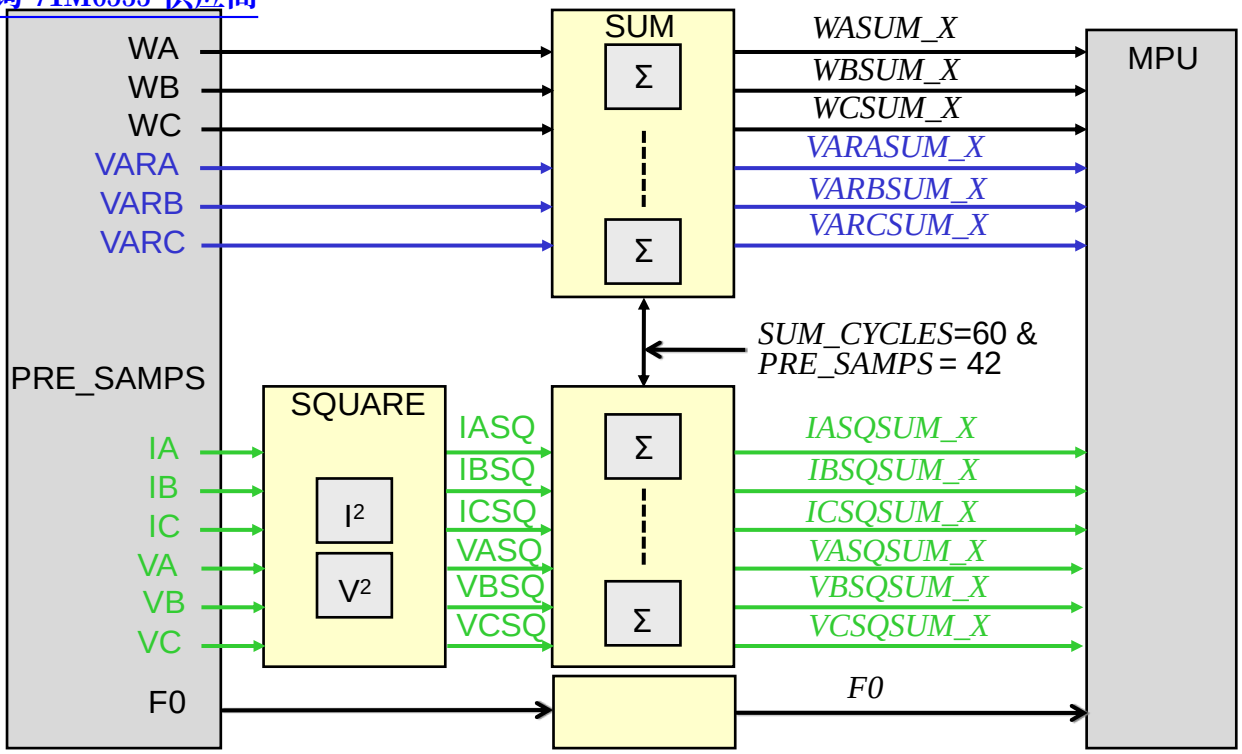


Figure 44: CE Data Flow: Squaring and Summation Stages

5 Specifications

5.1 Absolute Maximum Ratings

Table 62 shows the absolute maximum ranges for the device. Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under recommended operating conditions (Section 5.3) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

Table 62: Absolute Maximum Ratings

Voltage and Current	
Supplies and Ground Pins	
V3P3SYS, V3P3A	–0.5 V to 4.6 V
VBAT	-0.5 V to 4.6 V
GNDD	-0.5 V to +0.5 V
Analog Output Pins	
V3P3D	-10 mA to 10 mA, -0.5 V to 4.6 V
VREF	-10 mA to +10 mA, -0.5 V to V3P3A+0.5 V
V2P5	-10 mA to +10 mA, -0.5 V to 3.0 V
Analog Input Pins	
IA, VA, IB, VB, IC, VC, V1	-10 mA to +10 mA -0.5 V to V3P3A+0.5 V
XIN, XOUT	-10 mA to +10 mA -0.5 V to 3.0 V
All Other Pins	
Configured as SEG or COM drivers	-1 mA to +1 mA, -0.5 to V3P3D+0.5
Configured as Digital Inputs	-10 mA to +10 mA, -0.5 to 6 V
Configured as Digital Outputs	-15 mA to +15 mA, -0.5 V to V3P3D+0.5 V
All other pins	–0.5 V to V3P3D+0.5 V
Temperature and ESD Stress	
Operating junction temperature (peak, 100ms)	140 °C
Operating junction temperature (continuous)	125 °C
Storage temperature	–45 °C to +165 °C
Solder temperature – 10 second duration	250 °C
ESD stress on all pins	4 kV

5.2 Recommended External Components

Table 63: Recommended External Components

Name	From	To	Function	Value	Unit
C1	V3P3A	AGND	Bypass capacitor for 3.3 V supply	≥0.1 ±20% †	µF
C2	V3P3D	DGND	Bypass capacitor for 3.3 V output	≥0.1 ±20% †	µF
CSYS	V3P3SYS	DGND	Bypass capacitor for V3P3SYS	≥1.0 ±30%	µF
C2P5	V2P5	DGND	Bypass capacitor for V2P5	0.1 ±20%	µF
XTAL	XIN	XOUT	32.768 kHz crystal – electrically similar to ECS .327-12.5-17X or Vishay XT26T, load capacitance 12.5 pF	32.768	kHz
CXS	XIN	AGND	Load capacitor for crystal (depends on crystal specs and board parasitics).	33 ±10%	pF
CXL	XOUT	AGND	Load capacitor for crystal (depends on crystal specs and board parasitics).	15 ±10%	pF

Notes:
1. AGND and DGND should be connected together.
2. V3P3SYS and V3P3A should be connected together.
3. † For accuracy and EMI rejection, C1 + C2 should be 470 µF or higher.

5.3 Recommended Operating Conditions

Table 64: Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
V3P3SYS, V3P3A: 3.3 V Supply Voltage V3P3A and V3P3SYS must be at the same voltage	Normal Operation	3.0	3.3	3.6	V
	Battery Backup	0		3.6	V
VBAT	No Battery	Externally Connect to V3P3SYS			
	Battery Backup: BRN and LCD modes SLEEP mode	3.0 2.0		3.8 3.8	V V
Operating Temperature		-40		+85	ºC

5.4 Performance Specifications

5.4.1 Input Logic Levels

Table 65: Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage[a], V_{IH}		2			V
Digital low-level input voltage[a], V_{IL}				0.8	V
Input pull-up current, I_{IL}	VIN=0 V, ICE_E=1				
E_RXTX, E_ISYNC		10		100	µA
E_RST, CKTEST		10		100	µA
Other digital inputs		-1	0	1	µA
Input pull down current, I_{IH}	VIN = V3P3D				
ICE_E		10		100	µA
RESET		10		100	µA
PB		-1	0	1	µA
Other digital inputs		-1	0	1	µA

[a] In battery powered modes, digital inputs should be below 0.3 V or above 2.5 V to minimize battery current.

5.4.2 Output Logic Levels

Table 66: Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V3P3D–0.4			V
	I_{LOAD} = 15 mA	V3P3D-0.6			V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0		0.4	V
	I_{LOAD} = 15 mA			0.8	V
OPT_TX V_{OH} (V3P3D-OPT_TX)	I_{SOURCE}=1 mA			0.4	V
OPT_TX V_{OL}	I_{SINK}=20 mA			0.7	V

5.4.3 Power-Fault Comparator

Table 67: Power-fault Comparator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Offset Voltage: V1-VBIAS		-20		+15	mV
Hysteresis Current: V1	Vin = VBIAS – 100 mV	0.8		1.2	µA
Response Time: V1	±100 mV overdrive	10	37	100	µs
WDT Disable Threshold: V1-V3P3A		-400		-10	mV

5.4.4 V2 Comparator (71M6534 only)

Table 68: V2 Comparator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Offset Voltage: V2-VBIAS		-20		+15	mV
Hysteresis Current	Vin = VBIAS – 100 mV	0.8		1.2	µA
Response Time	±100 mV overdrive			1	µs

5.4.5 Battery Monitor

Table 69: Battery Monitor Performance Specifications (*BM_E*= 1)

Parameter		Condition	Min	Typ	Max	Unit
Load Resistor			27	45	63	kΩ
LSB Value	[*M40MHZ*, *M26MHZ*] = [00], [10], or [11]	*FIR_LEN*=0 (L=138) *FIR_LEN*=1 (L=288) *FIR_LEN*=2 (L=384)	(-10%)	-48.7 -5.35 -2.26	(+10%)	µV µV µV
	[*M40MHZ*, *M26MHZ*] = [01]	*FIR_LEN*=0 (L=186) *FIR_LEN*=1 (L=384) *FIR_LEN*=2 (L=588)	(-10%)	-19.8 -2.26 -0.63	(+10%)	µV µV µV
Offset Error			-200	0	+100	mV

5.4.6 Supply Current

Table 70: Supply Current Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
V3P3SYS current (CE off)	Normal Operation, V3P3A = V3P3SYS = 3.3 V CKMPU = 614 kHz No Flash Memory write *RTM_E*=0, *ECK_DIS*=1, *ADC_E*=1, *ICE_E*=0		4.2	5.3	mA
V3P3SYS current (CE on)			8.4	9.6	mA
V3P3A current			3.5	3.8	mA
VBAT current		-400		+400	nA
V3P3SYS current, Write Flash	Normal Operation as above, except write Flash at maximum rate, *CE_E* = 0, *ADC_ E* = 0		10	12	mA
VBAT current	VBAT=3.6V BROWNOUT mode 71M6533/6533H 71M6534H LCD Mode LCD DAC off LCD DAC on SLEEP Mode		 82 112 11 21 0.7	 250 250 40 46 1.5	 µA µA µA µA µA

5.4.7 V3P3D Switch

Table 71: V3P3D Switch Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
On resistance – V3P3SYS to V3P3D	$\lvert I_{V3P3D} \rvert \leq 1$ mA		9	15	Ω
On resistance – VBAT to V3P3D	$\lvert I_{V3P3D} \rvert \leq 1$ mA		32	45	Ω

5.4.8 2.5 V Voltage Regulator

Unless otherwise specified, the load = 5 mA.

Table 72: 2.5 V Voltage Regulator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
V2P5	Iload = 0	2.3	2.5	2.7	V
V2P5 load regulation	Iload = 0 mA to 5 mA			40	mV
Voltage overhead V3P3SYS-V2P5	Iload = 5 mA, reduce V3P3 until V2P5 drops 200 mV	460			mV
PSSR ΔV2P5/ΔV3P3	RESET=0, iload=0	-2		+2	mV/V

5.4.9 Low-Power Voltage Regulator

Unless otherwise specified, V3P3SYS = V3P3A = 0, PB=GND (BROWNOUT).

Table 73: Low-Power Voltage Regulator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
V2P5	I_{LOAD} = 0	2.3	2.5	2.7	V
V2P5 load regulation	I_{LOAD} = 0 mA to 1 mA			30	mV
VBAT voltage requirement	I_{LOAD} = 1 mA, reduce VBAT until REG_LP_OK = 0			3.0	V
PSRR ΔV2P5/ΔVBAT	I_{LOAD} = 0	-50		50	mV/V

5.4.10 Crystal Oscillator

Table 74: Crystal Oscillator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Maximum Output Power to Crystal [4]	Crystal connected			1	µW
XIN to XOUT Capacitance [1]				3	pF
Capacitance to DGND [1] XIN XOUT	*RTCA_ADJ* = 0			 5 5	 pF pF

5.4.11 Optical Interface

Table 75: Optical Interface Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
OPT_TX V_{OH} (V3P3D-OPT_TX)	I_{SOURCE} =1 mA			0.4	V
OPT_TX V_{OL}	I_{SINK} = 20 mA			0.7	V

5.4.12 LCD DAC

Table 76: LCD DAC Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
VLCD Voltage $V_{LCD} = V3P3 \cdot (1 - 0.059 \cdot LCD\_DAC) - 0.019V$	$1 \le LCD\_DAC \le 7$	-10		+10	%

5.4.13 LCD Drivers

The information in Table 77 applies to all COM and SEG pins with *LCD_DAC*[2:0] = 000.

Table 77: LCD Driver Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
VLC2 Voltage	With respect to VLCD[a]	-0.1		+0.1	V
VLC1 Voltage†, ⅓ bias ½ bias ½ bias, minimum output level	 With respect to 2*VLC2/3 With respect to VLC2/2	 -3 -3		 +2 +2 1.0	 % VLC2 % VLC2 V
VLC0 Voltage†, ⅓ bias	 With respect to VLC2/3	 -4		 +1	 %
VLC1 Impedance	ΔILOAD = 100 µA (Isink)		9	15	kΩ
	ΔILOAD = -100 µA (Isource)		9	15	
VLC0 Impedance	ΔILOAD = 100 µA (Isink)		9	15	kΩ
	ΔILOAD = -100 µA (Isource)		9	15	

[a]VLCD is V3P3SYS in MISSION mode and VBAT in BROWNOUT and LCD modes.
† Specified as percentage of VLC2, the maximum LCD voltage.

5.4.14 Temperature Sensor

Table 78 shows the performance for the temperature sensor. The LSB values do not include the 8-bit left shift at CE input.

Table 78: Temperature Sensor Performance Specifications

Parameter		Condition	Min	Typ	Max	Unit
Nominal relationship: $N(T) = S_n*(T-T_n) + N_n$, T_n = 25ºC						
Nominal Sensitivity (S_n)[4] $S_n = -0.00109 \cdot \left(\frac{L}{3}\right)^3$	[*M40MHZ, M26MH*] = [00], [10], or [11]	*FIR_LEN*=0 (L=138) *FIR_LEN*=1 (L=288) *FIR_LEN*=2 (L=384)		-106 -964 -2286		LSB/ºC
	[*M40MHZ*, *M26MHZ*] = [01]	*FIR_LEN*=0 (L=186) *FIR_LEN*=1 (L=384) *FIR_LEN*=2 (L=588)		-260 -2286 -8207		
Nominal Offset (N_n) [4] $N_n = 0.508 \cdot \left(\frac{L}{3}\right)^3$	[*M40MHZ*, *M26MHZ*] = [00], [10], or [11]	*FIR_LEN*=0 (L=138) *FIR_LEN*=1 (L=288) *FIR_LEN*=2 (L=384)		49447 449446 1065353		LSB
	[*M40MHZ*, *M26MHZ*] = [01]	*FIR_LEN*=0 (L=186) *FIR_LEN*=1 (L=384) *FIR_LEN*=2 (L=588)		121071 1065353 3825004		
Temperature Error [1†] $ERR = T - \left\{\frac{(N(T) - N_n)}{S_n}\right\}$		T_n = 25°C, T = -40ºC to +85ºC	-10		+10	ºC

† Temperature error is calculated with the value N_n, which is measured at T_n during meter calibration and stored in MPU or CE for use in temperature calculations.

5.4.15 VREF and VBIAS

Table 79 shows the performance specifications for VREF and VBIAS. Unless otherwise specified, *VREF_DIS* = 0.

Table 79: VREF Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
VREF output voltage, VREF(22)	Ta = 22ºC	1.193	1.195	1.197	V
VREF chop step				40	mV
VREF power supply sensitivity ΔVREF / ΔV3P3A	V3P3A = 3.0 to 3.6 V	-1.5		1.5	mV/V
VREF input impedance	*VREF_DIS* = 1, VREF = 1.3 to 1.7 V	100			kΩ
VREF output impedance	CAL =1, ILOAD = 10 µA, -10 µA			2.5	kΩ
VNOM definition[a]	$VNOM(T) = VREF(22) + (T-22)TC1 \cdot 10^{-6} + (T-22)^2 TC2 \cdot 10^{-6}$				V
If *TRIMBGA* and *TRIMBGB* are available (71M6533H/71M6534H)					
Definitions	$\gamma = 0.1 \cdot TRIMBGB - 0.143 \cdot (TRIMM + 0.5)$, $\xi = \frac{TEMP_{22} - 500 \cdot TRIMBGA - 370000}{900}$, $\eta = (56.2 - TRIMT) \cdot 0.55$				
VNOM temperature coefficients [b] TC1 TC2	$\eta + 19\gamma - 0.065\gamma\xi + 0.34\xi + 8.0$ $0.015\gamma - 0.0013\xi - 0.35$				µV/ºC µV/ºC^2
VREF(T) deviation from VNOM(T) $\frac{VREF(T) - VNOM(T)}{VNOM(T)} \frac{10^6}{\max(\lvert T-22\rvert, 40)}$		-15		+15	PPM/ºC
If *TRIMBGA* and *TRIMBGB* are not available (71M6533/71M6534)					
VNOM temperature coefficients: TC1 TC2	$3.18 \cdot (52.46 - TRIMT)$ -0.444				µV/ºC µV/°C^2
VREF(T) deviation from VNOM(T) $\frac{VREF(T) - VNOM(T)}{VNOM(T)} \frac{10^6}{\max(\lvert T-22\rvert, 40)}$		-40		+40	PPM/ºC
VREF aging			±25		PPM/ year
VBIAS Voltage	Ta = 25 °C Ta = -40 °C to 85 °C	(-1%) (-4%)	1.6 1.6	(+1%) (+4%)	V V

[a] This relationship describes the nominal behavior of VREF at different temperatures.

[b] $TEMP_{22}$ is the value read from the temperature sensor at 22°C.

5.4.16 ADC Converter, V3P3A Referenced

Table 80 shows the performance specifications for the ADC converter, V3P3A referenced. For this data, *FIR_LEN*=2, [*M40MHZ, M26MHZ*]=[00], unless stated otherwise, *VREF_DIS*=0. LSB values do not include the 8-bit left shift at the CE input.

Table 80: ADC Converter Performance Specifications

Parameter		Condition	Min	Typ	Max	Unit
Recommended Input Range (Vin-V3P3A)			-250		250	mV peak
Voltage to Current Crosstalk $\frac{10^6 * Vcrosstalk}{Vin}\cos(\angle Vin - \angle Vcrosstalk)$		*Vin* = 200 mV peak, 65 Hz, on VA. *Vcrosstalk* = largest measurement on IA or IB	-10		10	µV/V
THD (First 10 harmonics): [1] 250 mV-pk 20 mV-pk		Vin=65 Hz, 64 kpts FFT, Blackman-Harris window			 -75 -90	 dB dB
Input Impedance		At 65 Hz	40		90	kΩ
Temperature coefficient of Input Impedance		At 65 Hz		1.7		Ω/°C
LSB size $V_{LSB} = V_{REF} \cdot \frac{1.25}{4.75} \cdot \left(\frac{3}{L}\right)^3$ *L* = FIR length	[*M40MHZ*, *M26MHZ*] = [00], [10], or [11]	FIR_LEN=0 FIR_LEN=1 FIR_LEN=2		3231 355 150		nV/LSB
	[*M40MHZ*, *M26MHZ*] = [01]	FIR_LEN=0 FIR_LEN=1 FIR_LEN=2		1319 150 42		nV/LSB
Digital Full Scale $\left(\frac{L}{3}\right)^3$ *L* = FIR length	[*M40MHZ*, *M26MHZ*] = [00], [10], or [11]	FIR_LEN=0 FIR_LEN=1 FIR_LEN=2		± 97336 ± 884736 ± 2097152		LSB
	[M40MHZ, M26MHZ] = [01]	FIR_LEN=0 FIR_LEN=1 FIR_LEN=2		± 238328 ± 2097152 ± 7529536		LSB
ADC Gain Error vs %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\, 357nV/V_{IN}}{100 \Delta V3P3A/3.3}$		Vin=200 mV pk, 65 Hz V3P3A=3.0 V, 3.6 V			50	PPM / %
Input Offset (Vin-V3P3A)			-10		10	mV

5.5 Timing Specifications

5.5.1 Flash Memory

Table 81: Flash Memory Timing Specifications

Parameter	Condition	Min	Typ	Max	Unit
Flash Read Pulse Width	V3P3A = V3P3SYS = 0 (BROWNOUT Mode)	30		100	ns
Flash write cycles	-40°C to +85°C	20,000			Cycles
Flash data retention	25°C	100			Years
Flash data retention	85°C	10			Years
Flash byte writes between page or mass erase operations				2	Cycles
Write Time per Byte				42	µs
Page Erase (1024 bytes)				20	ms
Mass Erase				200	ms

5.5.2 EEPROM Interface

Table 82: EEPROM Interface Timing

Parameter	Condition	Min	Typ	Max	Unit
Write Clock frequency (I^2C)	CKMPU = 4.9 MHz, Using interrupts		78		kHz
	CKMPU = 4.9 MHz, bit-banging DIO4/5		150		kHz
Write Clock frequency (3-wire)	CKMPU=4.9 MHz		500		kHz

5.5.3 RESET

Table 83: RESET Timing

Parameter	Condition	Min	Typ	Max	Unit
Reset pulse width		5			µs
Reset pulse fall time				1	µs

5.5.4 RTC

Table 84: RTC Range for Date

Parameter	Condition	Min	Typ	Max	Unit
Range for date		2000	-	2255	year

5.5.5 SPI Slave Port (MISSION Mode)

Table 85: SPI Slave Port (MISSION Mode) Timing

Parameter		Condition	Min	Typ	Max	Unit
t_{SPIcyc}	PCLK cycle time		1			µs
$t_{SPILead}$	Enable lead time		15			ns
t_{SPILag}	Enable lag time		0			ns
t_{SPIW}	PCLK pulse width: High Low		 40 40			 ns ns
t_{SPISCK}	PCSZ to first PCLK fall	Ignore if PCLK is low when PCSZ falls.	2			ns
t_{SPIDIS}	Disable time		0			ns
t_{SPIEV}	PCLK to Data Out				15	ns
t_{SPISU}	Data input setup time		10			ns
t_{SPIH}	Data input hold time		5			ns

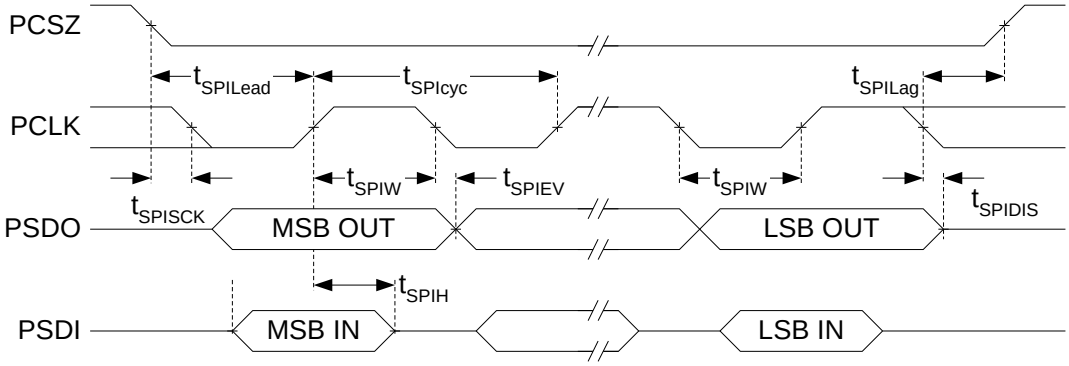


Figure 45: SPI Slave Port (MISSION Mode) Timing

5.5.5.1 Electrical Specification Footnotes

1. This spec will be guaranteed and verified in production samples, but will not be measured in production.
2. This spec will be guaranteed and verified in production samples, but will be measured in production only at DC.
3. This spec will be measured in production at the limits of the specified operating temperature.
4. This spec defines a nominal relationship rather than a measured parameter. Correct circuit operation will be verified with other specs that use this nominal relationship as a reference.

5.6 Typical Performance Data

5.6.1 Accuracy over Current

Figure 46 shows meter accuracy over current for various line frequencies. Figure 47 shows meter accuracy over current at various load angles.

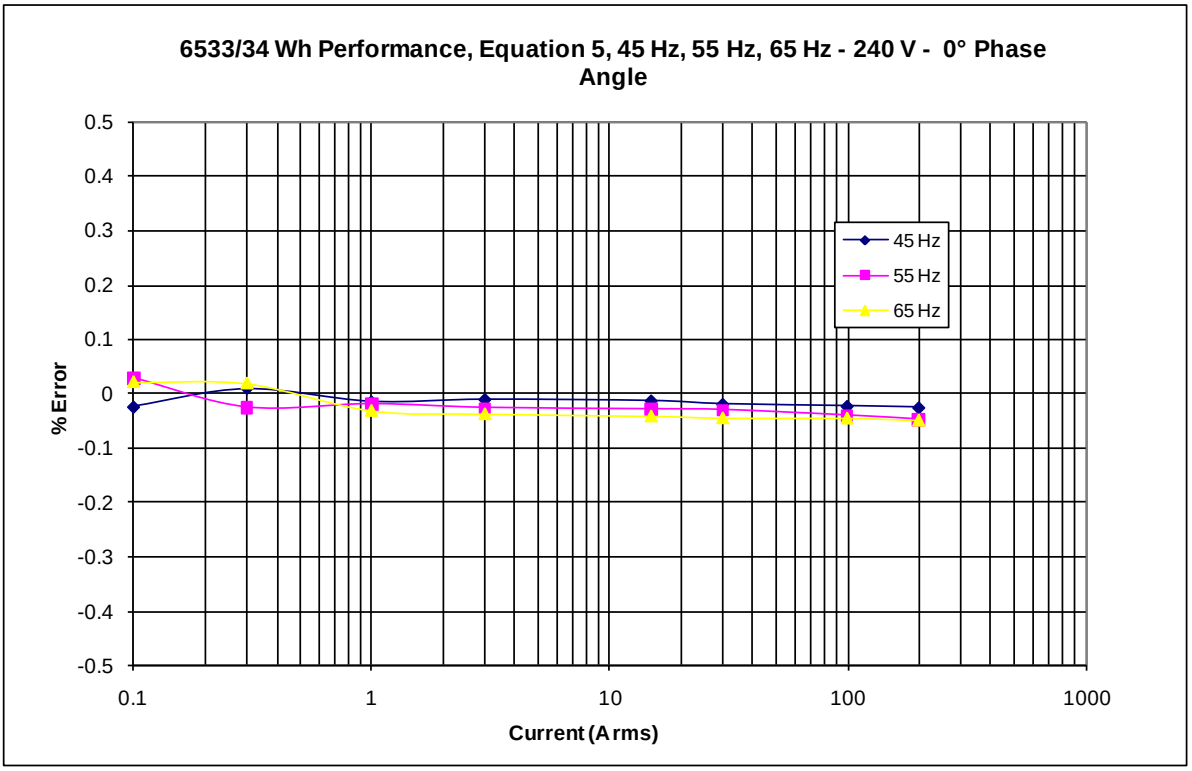


Figure 46: Wh Accuracy (0.1 A - 200 A, 240 V, Room Temperature) at Various Frequencies (Differential Mode, CTs)

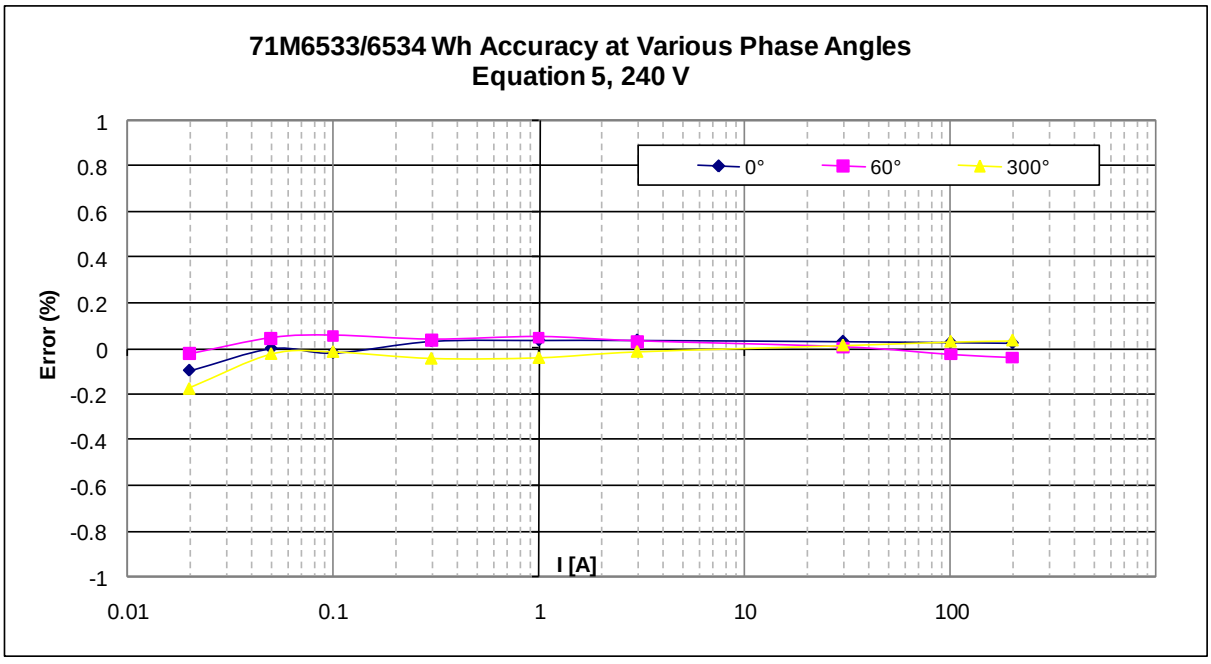


Figure 47: Typical Wh Accuracy (0.02 A - 200 A, 240 V, Room Temperature), Various Load Angles (Differential Mode, CTs)

5.6.2 Accuracy over Temperature

With digital temperature compensation enabled, the temperature characteristics of the reference voltage (VREF) are compensated to within ±40 PPM/°C for the 71M6533/71M6534 and within ±15 PPM/°C for the 71M6533H/71M6534H.

5.7 Package Outline Drawings

5.7.1 71M6533 (100 Pin LQFP)

Controlling dimensions are in mm.

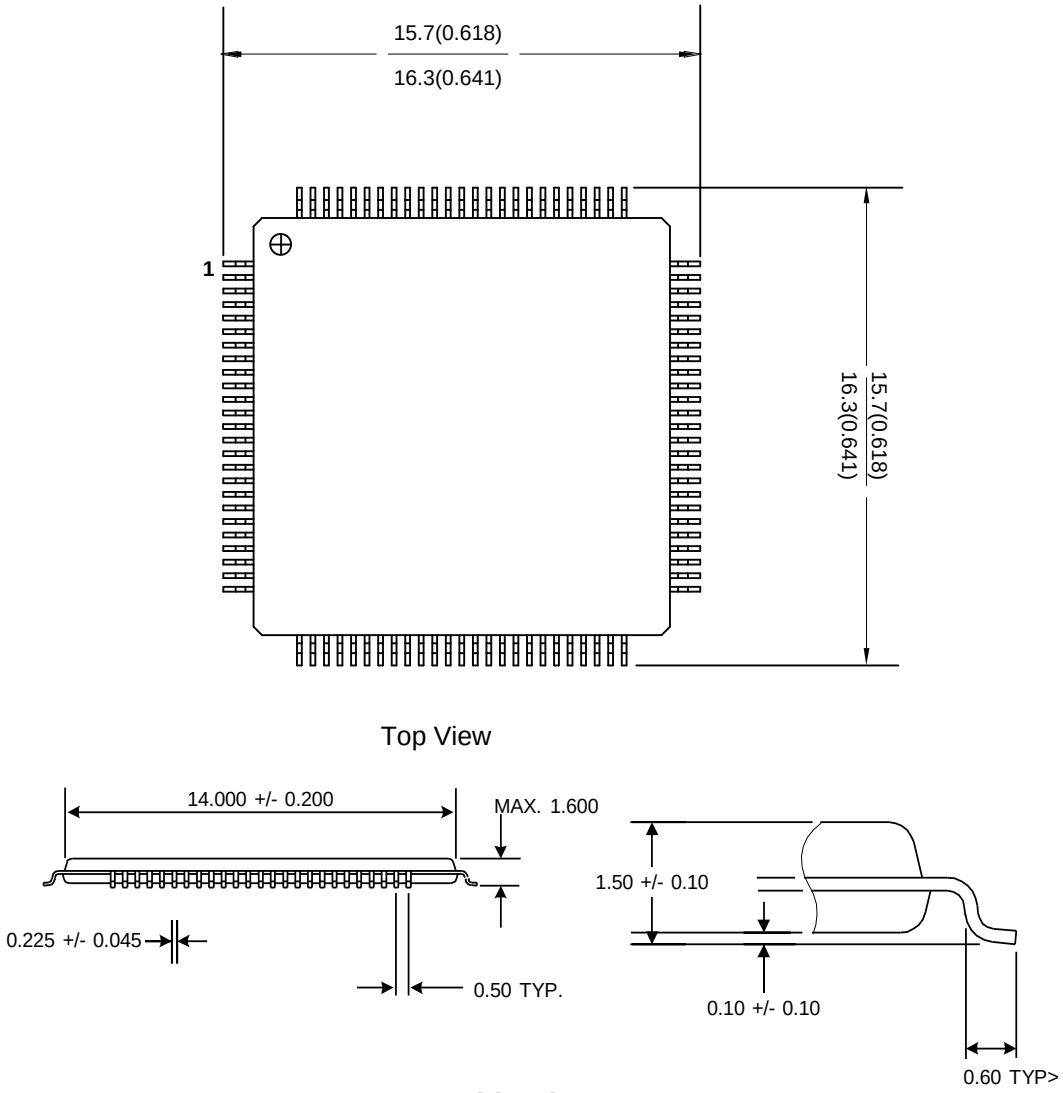


Figure 48: 71M6533/6533H 100-pin LQFP Package Outline

5.7.2 71M6534/6534H (120 Pin LQFP)

Controlling dimensions are in mm.

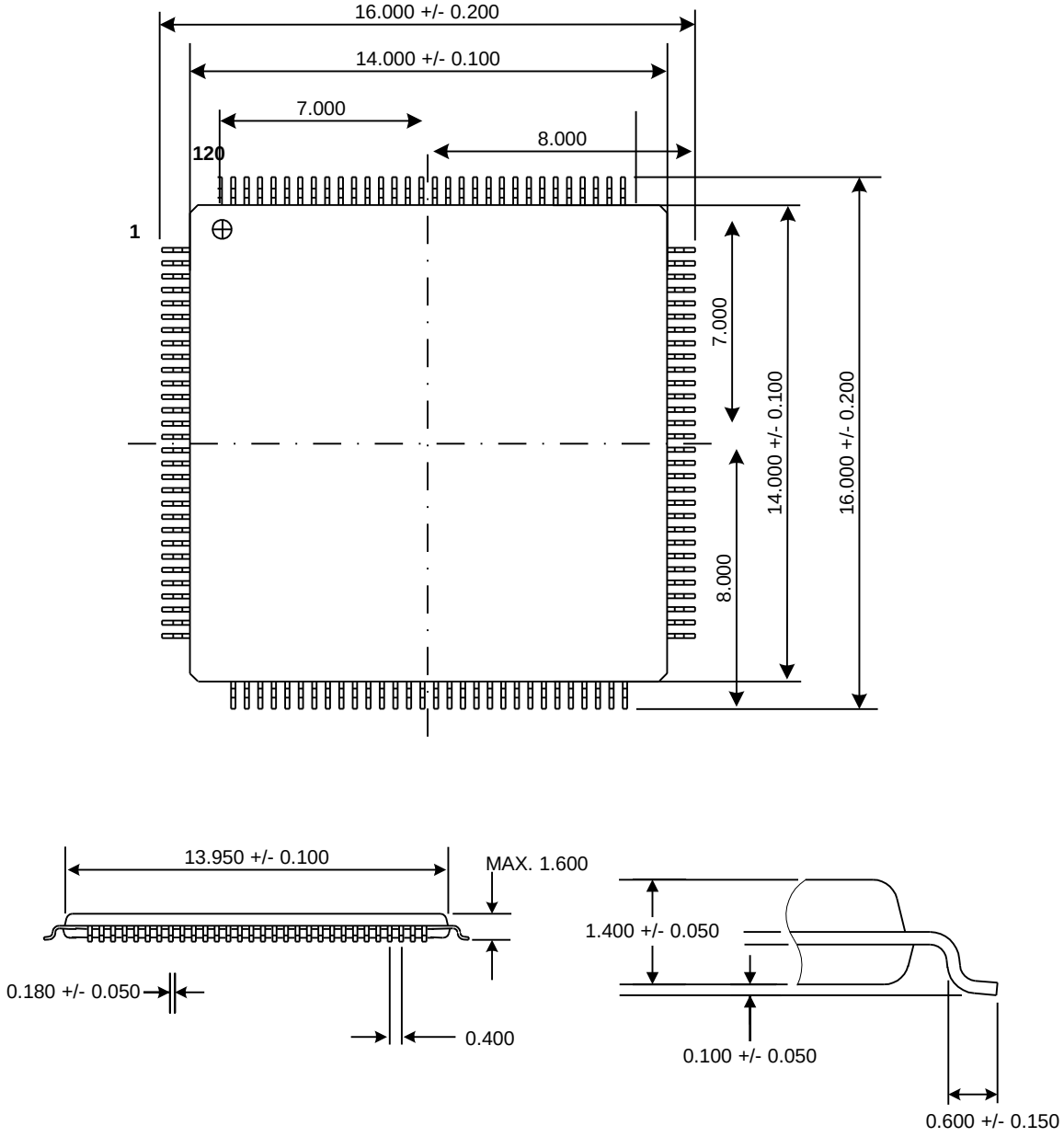


Figure 49: 71M6534/6534H 120-pin LQFP Package Outline

5.8 Pinout

5.8.1 71M6533/71M6533H Pinout (100 Pin LQFP)

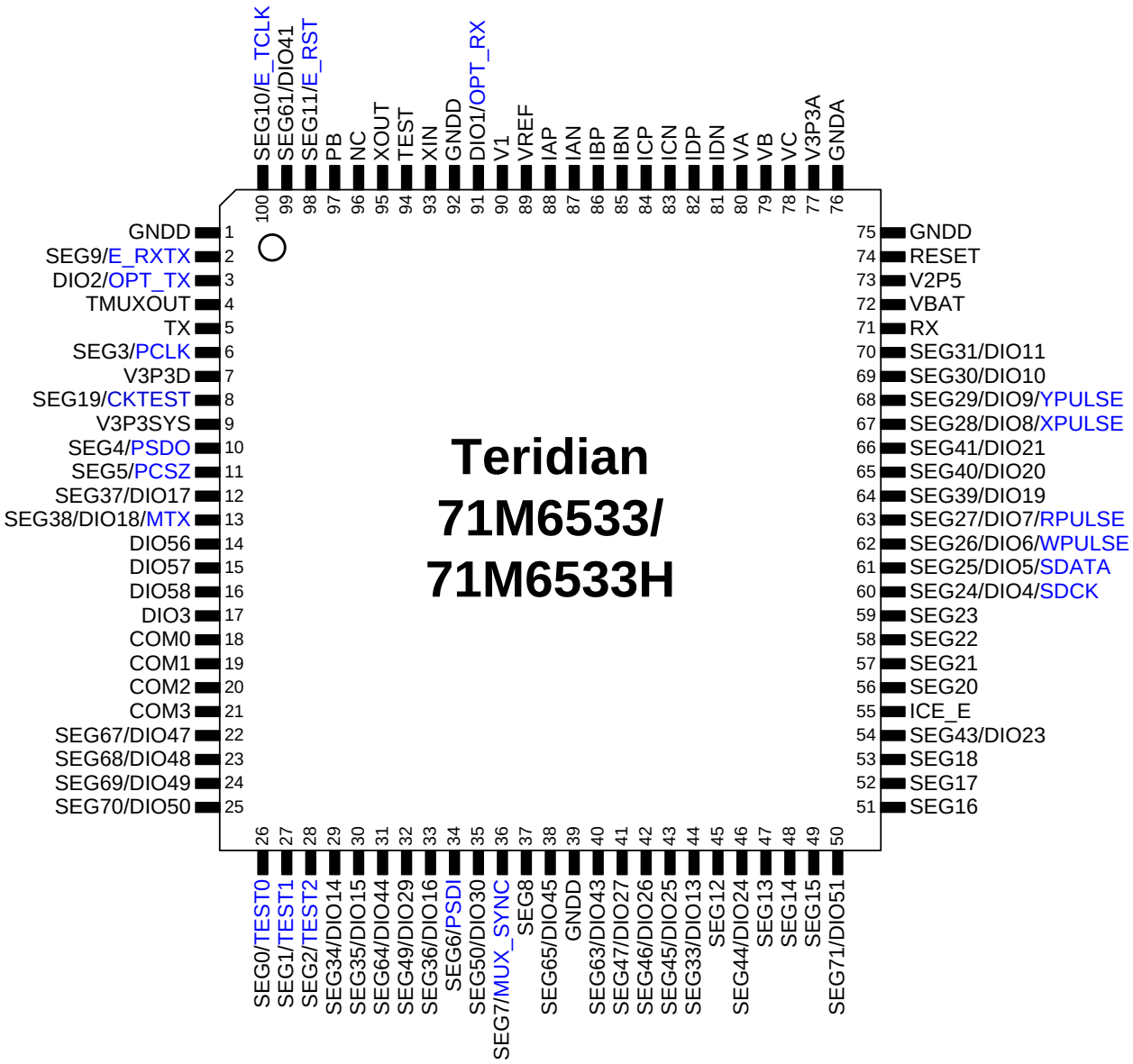


Figure 50: Pinout for 71M6533/71M6533H LQFP-100 Package

5.8.2 71M6534/71M6534H Pinout (120 Pin LQFP)

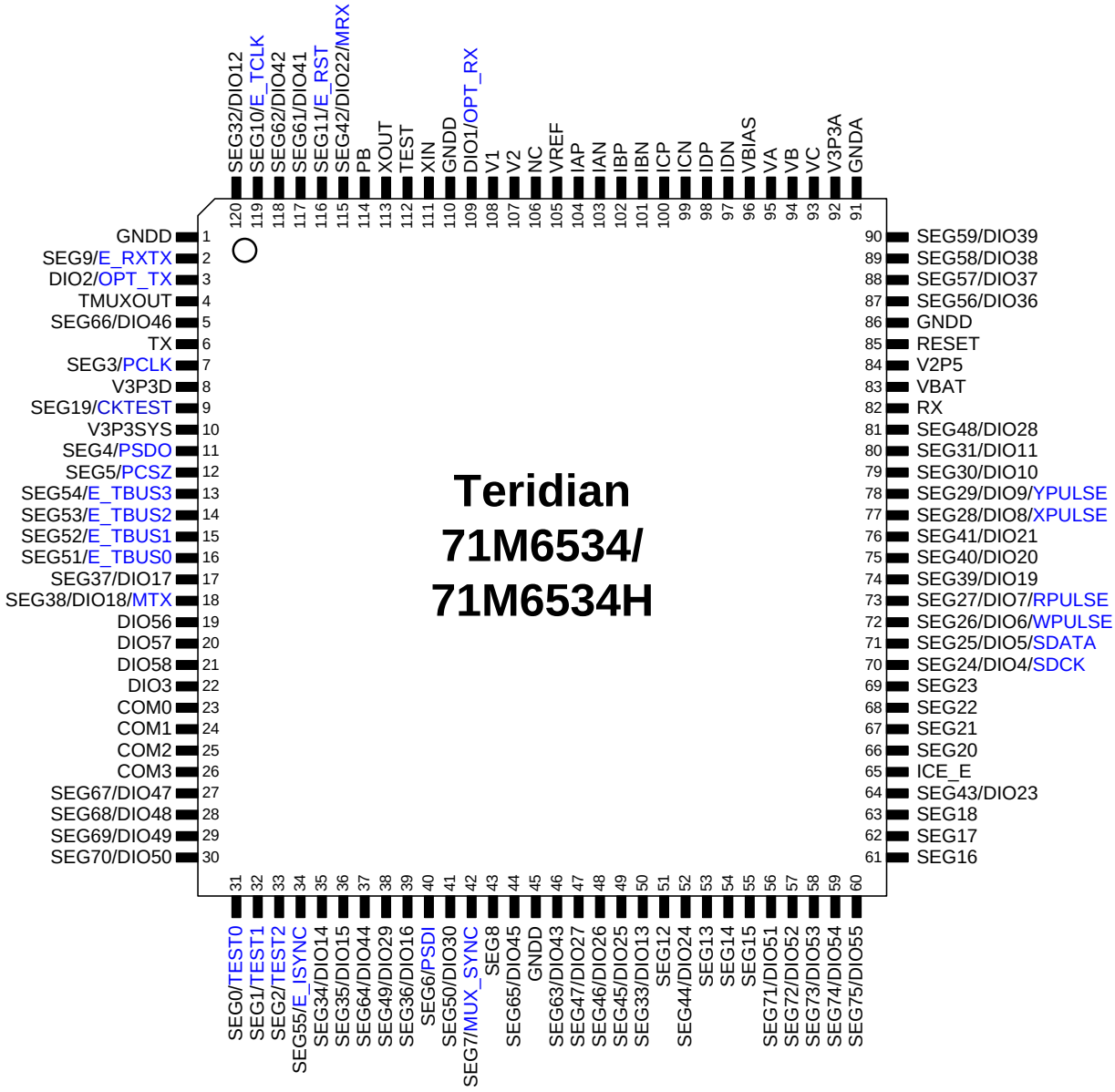


Figure 51: Pinout for 71M6534/71M6534H LQFP-120 Package

5.9 Pin Descriptions

Pins marked with an asterisk (e.g. V2*) are only available on the 71M6534.

5.9.1 Power and Ground Pins

Table 86: Power and Ground Pins

Name	Type	Circuit	Description
GNDA	P	–	Analog ground: This pin should be connected directly to the ground plane.
GNDD	P	–	Digital ground: This pin should be connected directly to the ground plane.
V3P3A	P	–	Analog power supply: A 3.3 V power supply should be connected to this pin, must be the same voltage as V3P3SYS.
V3P3SYS	P	–	System 3.3 V supply. This pin should be connected to a 3.3 V power supply.
V3P3D	O	13	Auxiliary voltage output of the chip. In mission mode, this pin is connected to V3P3SYS by the internal selection switch. In BROWNOUT mode, it is internally connected to VBAT. V3P3D is floating in LCD and sleep mode. A bypass capacitor to ground should not exceed 0.1 µF.
VBAT	P	12	Battery backup and oscillator power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3SYS.
V2P5	O	10	Output of the internal 2.5 V regulator. A 0.1 µF capacitor to GNDA should be connected to this pin.

5.9.2 Analog Pins

Table 87: Analog Pins

Name	Type	Circuit	Description
IAP/IAN, IBP/IBN, ICP/ICN IDP/IDN	I	6	Differential or single-ended Line Current Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of current sensors. **Unused pins must be tied to V3P3A**.
VA, VB, VC	I	6	Line Voltage Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of resistor dividers. **Unused pins must be tied to V3P3A.**
V1	I	7	Comparator Input: This pin is a voltage input to the internal comparator. The voltage applied to the pin is compared to the internal BIAS voltage (1.6 V). If the input voltage is above VBIAS, the comparator output will be high (1). If the comparator output is low, a voltage fault will occur. A series 5 kΩ resistor should be connected from V1 to the resistor divider.
V2*	I	7	Comparator Input (71M6534 only): This pin is a voltage input to an internal comparator. The voltage applied to this pin is compared to an internal reference voltage (VBIAS). If the input voltage is above VBIAS, the comparator output will be high (1).
VBIAS*	O	9	Low-impedance output for use in biasing current sensors and voltage dividers.
VREF	O	9	Voltage Reference for the ADC. This pin should be left unconnected (floating).
XIN XOUT	I	8	Crystal Inputs: A 32 kHz crystal should be connected across these pins. Typically, a 33 pF capacitor is also connected from XIN to GNDA and a 15 pF capacitor is connected from XOUT to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer datasheet for details. If an external clock is used, a 150 mV (p-p) clock signal should be applied to XIN, and XOUT should be left unconnected.

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified under Section 5.9.4 I/O Equivalent Circuits.

5.9.3 Digital Pins

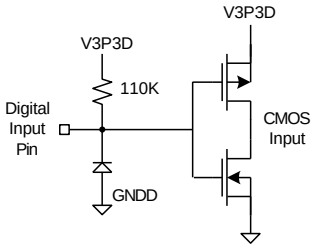
Table 88: Digital Pins

Name	Type	Circuit	Description
COM3,COM2, COM1,COM0	O	5	LCD Common Outputs: These 4 pins provide the select signals for the LCD display.
SEG0…SEG2, SEG8, SEG12…SEG18, SEG20…SEG23	O	5	Dedicated LCD Segment Output pins.
SEG24/DIO4 … SEG31/DIO11, SEG32/DIO12* SEG33/DIO13 … SEG41/DIO21, SEG42/DIO22* SEG43/DIO23 … SEG47/DIO27, SEG48/DIO28* SEG49/DIO29, SEG50/DIO30, SEG56/DIO36* … SEG59/DIO39* SEG61/DIO41, SEG62/DIO42* SEG63/DIO43 … SEG65/DIO45, SEG66/DIO45* SEG67/DIO47 … SEG71/DIO51 SEG72/DIO52* … SEG75/DIO55*	I/O	3, 4, 5	Multi-use pins, configurable as either LCD SEG driver or DIO. (DIO4 = SCK, DIO5 = SDA when configured as EEPROM interface; WPULSE = DIO6, VARPULSE = DIO7, DIO8 = XPULSE, DIO9 = YPULSE when configured as pulse outputs). **Unused pins must be configured as outputs or terminated to V3P3/GNDD.** SEG32/DIO12, SEG42/DIO22, SEG48/DIO28, SEG56/DIO36 through SEG59/DIO39, SEG62/DIO42, SEG66/DIO45, SEG72/DIO52 through SEG75/DIO55 are only available in the 71M6534. SEG38/DIO18 and SEG42/DIO22 can be assigned to the multiplexed UART outputs/inputs MTX and MRX (71M6534 only). This function is controlled by the I/O RAM registers *UMUX_E* and *UMUX_SEL*.
SEG51/E_TBUS0* SEG52/E_TBUS1* SEG53/E_TBUS2* SEG54/E_TBUS3* SEG55/E_ISYNC_BRKRQ*	I/O	5	Multiuse pins, configurable as either LCD SEG driver or emulator trace bus or handshake (71M6534 only).
SEG3/PCLK SEG4/PSDO SEG5/PCSZ SEG6/PSDI	I/O	3, 4, 5	Multi-use pins, configurable as either LCD SEG driver or SPI PORT.
DIO3, DIO56, DIO57, DIO58	I/O	3	Dedicated DIO Pins.

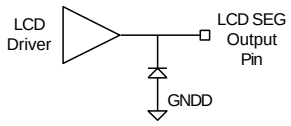
Name	Type	Cicuit	Description
E_RXTX/SEG9	I/O	1, 4, 5	Multi-use pins, configurable as either emulator port pins (when ICE_E pulled high) or LCD SEG drivers (when ICE_E tied to GND).
E_RST/SEG11	I/O	1, 4, 5	
E_TCLK/SEG10	O	4, 5	
ICE_E	I	2	ICE enable. When zero, E_RST, E_TCLK, and E_RXTX become SEG9, SEG10, and SEG11 respectively. For production units, this pin should be pulled to GND to disable the emulator port.
CKTEST/SEG19, MUXSYNC/SEG7	O	4, 5	Multi-use pins, configurable as either multiplexer/clock output or LCD segment driver using the I/O RAM registers *CKOUT_E* or *MUX_SYNC_E*.
TMUXOUT	O	4	Pin connected to the output test multiplexer. Controlled by *TMUX[3:0].*
OPT_RX/DIO1	I/O	3, 4	Multi-use pin, configurable as Optical Receive Input or general DIO. When configured as OPT_RX, this pin is a regular UART RX pin. **If this pin is unused it must be configured as an output or terminated to V3P3D or GNDD.**
OPT_TX/DIO2	I/O	3, 4	Multi-use pin, configurable as either Optical LED Transmit Output or general DIO. When configured as OPT_TX, this pin is capable of directly driving an LED for transmitting data in an IR serial interface.
RESET	I	2	Chip reset: This input pin is used to reset the chip into a known state. For normal operation, this pin is pulled low. To reset the chip, this pin should be pulled high. This pin has an internal 30 µA (nominal) current source pull-down. No external reset circuitry is necessary.
RX	I	3	UART input. **If this pin is unused it must be terminated to V3P3D or GNDD.**
TX	O	4	UART output.
TEST	I	7	Enables Production Test. **This pin must be grounded in normal operation.**
PB	I	3	Push button input. This pin must be at GNDD when not active or unused. A rising edge sets the *IE_PB* flag. It also causes the part to wake up if it is in SLEEP or LCD mode. PB does not have an internal pull-up or pull-down resistor.

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output.
The circuit number denotes the equivalent circuit, as specified in Section 5.9.4.

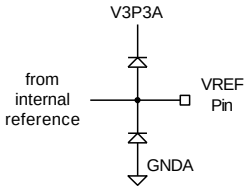
5.9.4 I/O Equivalent Circuits



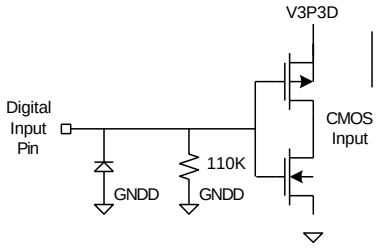
Digital Input Equivalent Circuit
Type 1:
Standard Digital Input or
pin configured as DIO Input
with Internal Pull-Up



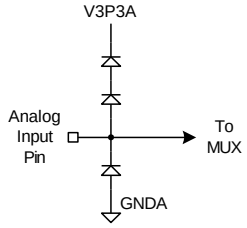
LCD Output Equivalent Circuit
Type 5:
LCD SEG or
pin configured as LCD SEG



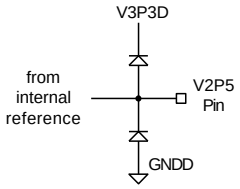
VREF Equivalent Circuit
Type 9:
VREF



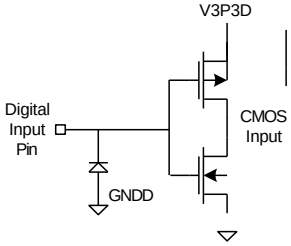
Digital Input
Type 2:
Pin configured as DIO Input
with Internal Pull-Down



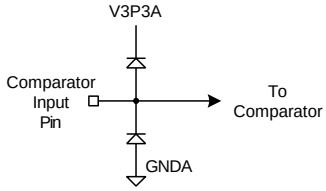
Analog Input Equivalent Circuit
Type 6:
ADC Input



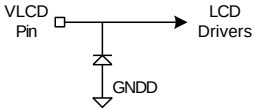
V2P5 Equivalent Circuit
Type 10:
V2P5



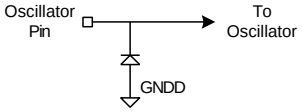
Digital Input Type 3:
Standard Digital Input or
pin configured as DIO Input



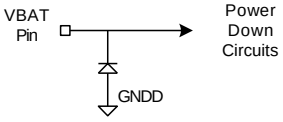
Comparator Input Equivalent
Circuit Type 7:
Comparator Input



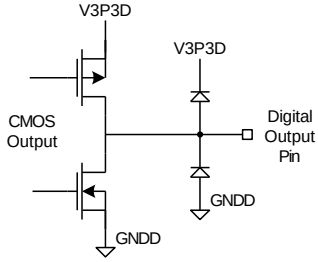
VLCD Equivalent Circuit
Type 11:
VLCD Power



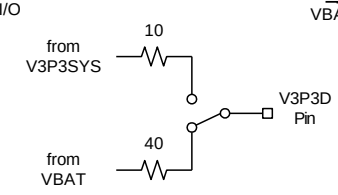
Oscillator Equivalent Circuit
Type 8:
Oscillator I/O



VBAT Equivalent Circuit
Type 12:
VBAT Power



Digital Output Equivalent Circuit
Type 4:
Standard Digital Output or
pin configured as DIO Output



V3P3D Equivalent Circuit
Type 13:
V3P3D

6 Ordering Information

Part	Part Description (Package, accuracy)	Flash Size	Packaging	Order Number	Package Marking
71M6533	100-pin LQFP Lead Free, 0.5%	128 KB	bulk	71M6533-IGT/F	71M6533-IGT
71M6533H	100-pin LQFP Lead Free, 0.1%	128 KB	bulk	71M6533H-IGT/F	71M6533H-IGT
71M6533	100-pin LQFP Lead Free, 0.5%	128 KB	tape and reel	71M6533-IGTR/F	71M6533-IGT
71M6533H	100-pin LQFP Lead Free, 0.1%	128 KB	tape and reel	71M6533H-IGTR/F	71M6533H-IGT
71M6534	120-pin LQFP Lead Free, 0.5%	128 KB	bulk	71M6534-IGT/F	71M6534-IGT
71M6534H	120-pin LQFP Lead Free, 0.1%	256 KB	bulk	71M6534H-IGT/F	71M6534H-IGT
71M6534	120-pin LQFP Lead Free, 0.5%	128 KB	tape and reel	71M6534-IGTR/F	71M6534-IGT
71M6534H	120-pin LQFP Lead Free, 0.1%	256 KB	tape and reel	71M6534H-IGTR/F	71M6534H-IGT

7 Related Information

The following documents related to the 71M6533 and 71M6534 are available from Teridian Semiconductor Corporation:

71M6533/71M6534 Data Sheet (this document)
71M653X Software User's Guide (SUG)

8 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the *71M6533/33H* and *71M6534/34H*, contact us at:

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FAX: (714) 508-8878
Email: meter.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.

Appendix A: Acronyms

AFE	Analog Front End
AMR	Automatic Meter Reading
ANSI	American National Standards Institute
CE	Compute Engine
DIO	Digital I /O
DSP	Digital Signal Processor
FIR	Finite Impulse Response
ICE	In-Circuit Emulator
IEC	International Electrotechnical Commission
MPU	Microprocessor Unit (CPU)
PLL	Phase-locked loop
RMS	Root Mean Square
SFR	Special Function Register
SOC	System on Chip
TOU	Time of Use
UART	Universal Asynchronous Receiver/Transmitter

Appendix B: Revision History

Revision	Date	Description
1.0	March 6, 2009	First publication with changes with respect to the preliminary data sheet (PDS) as follows: 1) Corrected reversed labels for Timer/Counter 1 and 2 in Table 22. 2) Updated Figure 7 (Interrupt structure). 3) Updated range for *RTC_A* from 1.9 PPM to 3.8 PPM. 4) Changed sleep mode current at 25°C to 0.7 µV and deleted entry for typical sleep mode current over temperature. 5) Corrected bit enumeration for *FLSH_PGADR[7:2]*. 6) Corrected various typographical errors (*TRIMMT* etc.). 7) Corrected entries under "Wk." Column for *GP0-GP7* in alphabetical I/O RAM table. 8) Added explanation for hysteresis at the V1 pin in Applications section. 9) Replaced graph showing system performance specification over temperature with specification on accuracy of VREF compensation. 10) Changed accuracy of VREF compensation over temperature to ±15 PPM/°C 11) Changed LSB values provided for temperature sensor. 12) Added minimum output level for VLC1 LCD voltage. 13) Removed access to I/O RAM from SPI Port description. 14) Updated numerous parameters in Electrical Specification (temperature sensor, supply current for mission and battery modes). 15) Corrected number of pre-boot cycles in Flash Memory Section. 16) Updated entries in I/O RAM table under "Wake" column. 17) Updated CE register tables.
1.1	November 9, 2009	Changes and corrections: 1) Stated < 0.1% for accuracy for both H and non-H parts over 2000:1 range on title page. 2) Added *STOP* and *IDLE* bits in description of *PCOM* SFR. 3) Consolidated spelling of *RTCA_ADJ*. 4) Added explanation for Figure 18. 5) Completely revised section 2.5.2 (Wake on Timer). 6) Improved description of hysteresis in Application Section (3.11). 7) Corrected bit range for *CE_LCTN* to *CE_LCTN[7:0]*. 8) Corrected bit assignment for control of DIO56 – DIO58 (*DIO_56[4]* and *DIO_DIR56[7]*. 9) Added *LCD_SEG19[ ]* to Table 47. 10) Added text in Table 47 stating that registers *RTC_SEC* to *RTC_YR* do not change at reset. 11) Specified Voltage LSB in CE Interface Description (for sag detection). 12) Corrected formulae for RMS calculation below Table 56. 13) Updated package outline drawing. 14) Added text describing connection of a trace emulator to the 71M6534 in section 3.13. 15) Clarified write delay that applies to the *RTC_SEC* and other RTC registers in section 1.4.3 and Table 47. 16) Added note describing firmware measures to be applied when using UART1 in full-duplex mode.

