Philips Semiconductors-Signetics

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Status	Product Specification
FAST Products	

FAST 74F112
Flip-Flop

Dual J-K Negative Edge-triggered Flip-Flop

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F112	100MHz	15mA

FEATURE

- **Industrial temperature range available (-40°C to +85°C)**

DESCRIPTION

The 74F112, Dual Negative Edge-Triggered JK-Type Flip-Flop, features individual J, K, Clock ($\overline{CP}_n$), Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, true (Q_n) and complementary ($\overline{Q}_n$) outputs.

The $\overline{S}_D$ and $\overline{R}_D$ inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the level at the other inputs.

A High level on the clock ($\overline{CP}_n$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}_n$ is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the $\overline{CP}_n$.

ORDERING INFORMATION

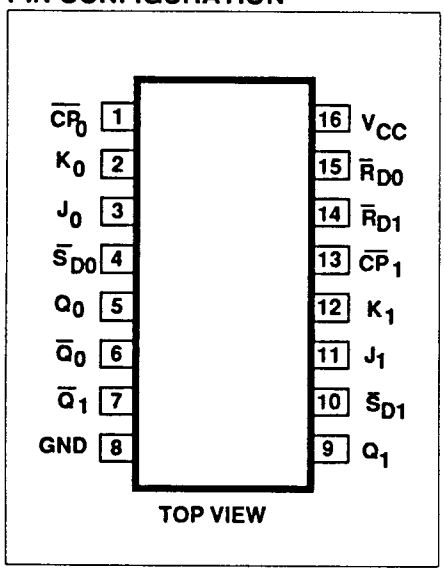
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
16-Pin Plastic DIP	N74F112N	I74F112N
16-Pin Plastic SO	N74F112D	I74F112D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20µA/0.6mA
K_0, K_1	K inputs	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{CP}_0$, $\overline{CP}_1$	Clock Pulse input (active falling edge)	1.0/4.0	20µA/2.4mA
Q_0,$\overline{Q}_0$; Q_1,$\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

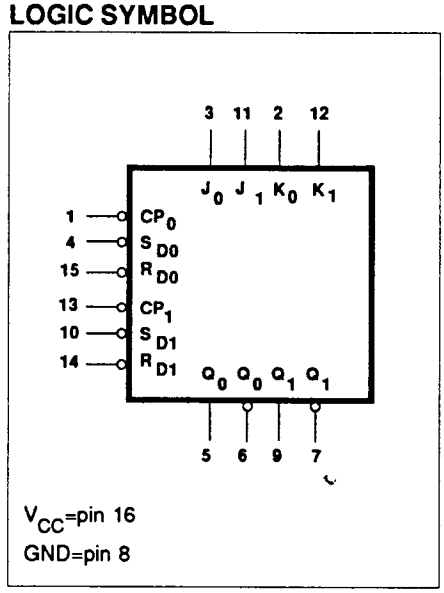
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



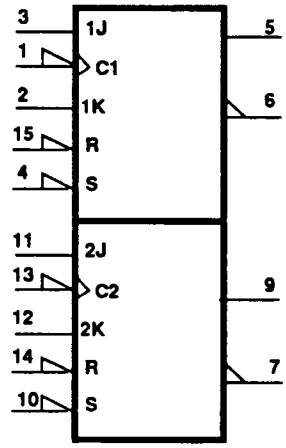
TOP VIEW

LOGIC SYMBOL

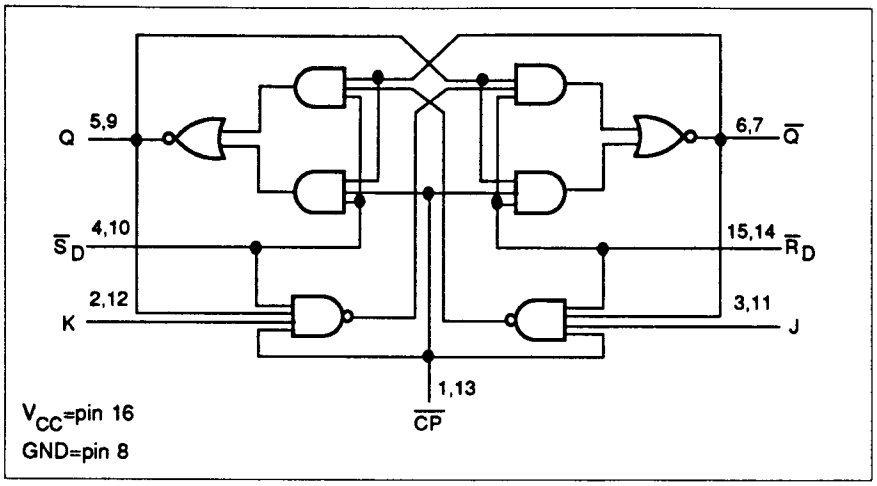


V_{CC}=pin 16
GND=pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronmous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined *
H	H	↓	h	h	$\overline{q}$	q	Toggle
H	H	↓	l	h	L	H	Load "0"(Reset)
H	H	↓	h	l	H	L	Load "1" (Set)
H	H	↓	l	l	q	$\overline{q}$	Hold "no change"
H	H	H	X	X	Q	$\overline{Q}$	Hold "no change"

H = High voltage level
h = High voltage level one setup time prior to High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to High-to-Low clock transition
q=Lower case letters indicate the state of the referenced output prior to the High-to-Low clock transition
X = Don't care
↓= High-to-Low clock transition
* =Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_A	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	-40		85	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	J_n, K_n	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CP}_n$					-2.4	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					-3.0	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.

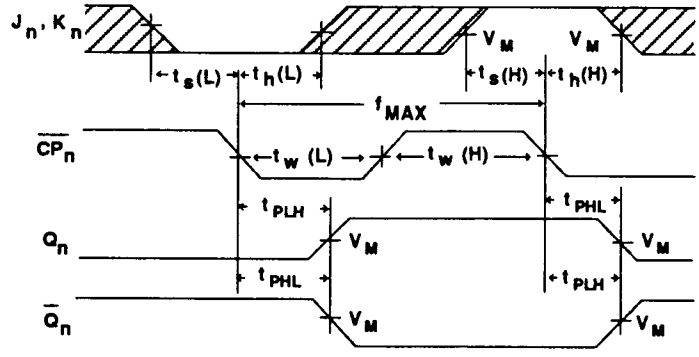
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		T_A = -40°C to +85°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		80		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	5.0 5.0	6.5 6.5	2.0 2.0	7.5 7.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_D$ to Q_n or $\overline{Q}_n$	Waveform 2,3	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	1.5 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		T_A = -40°C to +85°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, K_n to $\overline{CP}$	Waveform 1	4.0 3.5			5.0 4.0		5.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, K_n to $\overline{CP}$	Waveform 1	0.0 0.0			0.0 0.0		0.0 0.0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width High or Low	Waveform 1	4.5 4.5			5.0 5.0		5.0 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$, $\overline{R}_D$ Pulse width Low	Waveform 2,3	4.5			5.0		5.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$, $\overline{R}_D$ to $\overline{CP}$	Waveform 2,3	4.5			5.0		5.0		ns

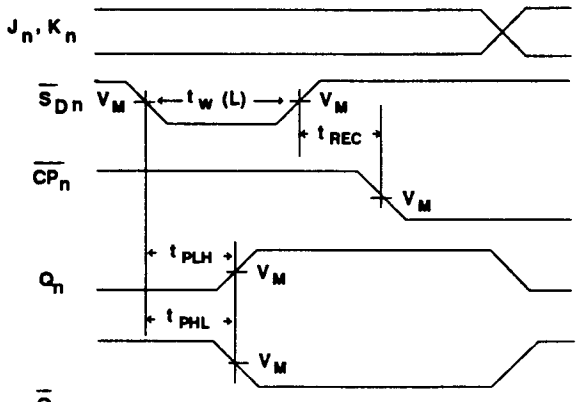
AC WAVEFORMS



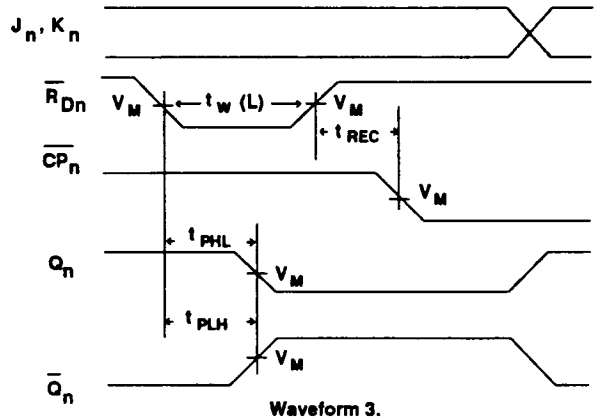
Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock pulse width

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS



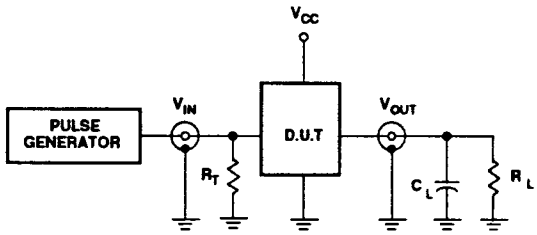
Waveform 2.
Propagation Delay for Set to Output, Set
Pulse Width, and Recovery Time for Set to Clock



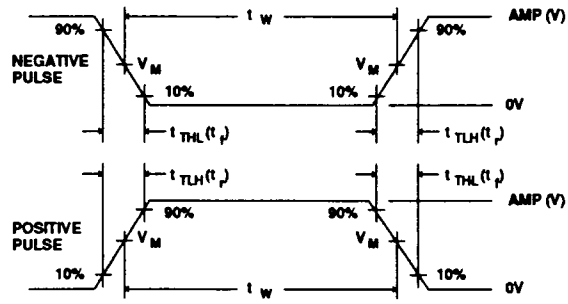
Waveform 3.
Propagation Delay for Reset to Output, Reset
Pulse Width, and Recovery Time for Reset to Clock

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

VI. COMMERCIAL PRODUCT SPECIAL PROCESSING T-90-20

SUPR II LEVEL B

Signetics Upgraded Product Reliability (SUPR) program is designed to provide customers whose systems require an infant mortality level less than that of our non-burned-in products (which is typically below 1000 PPM).

DEVICE AVAILABILITY

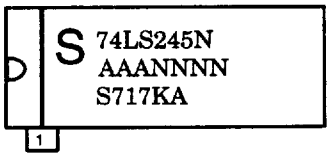
Products available for Level B processing are identified in the Price Book with a "B" suffix to the basic part number.

SUPR II LEVEL B PRICING ADDERS

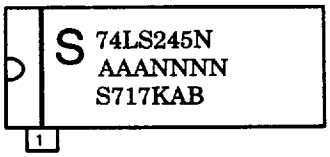
PRODUCT FAMILY	SUGGESTED RESALE ADDERS 1–99	100–999	OVER 1000
LIN	.14	.14	.11
LOG (TTL)			
(SSI)	.12	.10	.08
(MSI)	.16	.14	.11
(OCT)	.16	.14	.11
(CTM)	.16	.14	.11
LOG (ECL)			
(SSI)	.25	.23	.20
(MSI)	.25	.23	.20
LOG (LSI) (RAM) MIC (8X)	Consult Factory for Pricing		
PLD	Consult Factory for Pricing		
MCG	Consult Factory for Pricing		
DAT MIC	Not Available		

MARKING FORMAT EXAMPLES

Standard (no Burn-In) Products (Dual-in-line)



SUPR II (Burned-In) Products (Dual-in-line)



NOTE: The "B" in the 7th position on the 3rd line, when present, is the SUPR II Burn-In indicator.

TAPE AND REEL PACKAGING

SPECIFICATIONS

Tape and Reel specifications conform to Electronic Industries Association (EIA) Proposed Specification #EIA-481-A using 13 inch reels. Current incremental quantities reflect the quantities per reel. As more customers are able to handle a larger quantity per reel, this quantity will be increased.

DEVICE AVAILABILITY

Products available in tape and reel packaging are identified in the Price Book with a "T" suffix to the basic part number and are only offered as a product for sale by the reel. Return of product is limited to full reels with unbroken quality seals.

TAPE AND REEL PRICING ADDERS

PRODUCT FAMILY	SUGGESTED RESALE ADDER
MCG	.07
LIN	.07
LOG	.07
DAT MIC	PACKAGE A28 = .20 A44 = .25 A52 = .30 A68 = .40 A84 = .45 D24 = .17

VII. PACKING QUANTITY INFORMATION

T-90-20

CERAMIC DUAL IN-LINE (CERDIP)

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TUBE	DEVICES PER BOX
F/FE, BPA, PA	8-pin (300-mil)	48	1920
F, BCA, CA	14-pin (300-mil)	25	1000
F, BEA, EA	16-pin (300-mil)	25	1000
F, BVA, MVA	18-pin (300-mil)	21	840
F/FA, BRA, RA	20-pin (300-mil)	20	800
F, BWA, WA	22-pin (400-mil)	17	544
F/FA/F6, BJA, JA	24-pin (600-mil)	15	360
F/FA/F3/F24, BLA, LA	24-pin (300-mil)	15	600
F, BXA, XA	24-pin (400-mil)	15	480
F/FA/F28, BXA, XA	28-pin (600-mil)	13	312
FA	32-pin (600-mil)	11	264
F/FA/F40, BQA, MQA, QA	40-pin (600-mil)	9	216

CERPAC

PACKAGE CODE	PIN COUNT	QUANTITIES
		DEVICES PER TUBE
BDA/DA/W	14-pin	145
BFA/FA/W	16-pin	145
BXA/BYA/W	18-pin	100
BSA/SA/W/WB	20-pin	100
BKA/KA/W	24-pin	120
BYA/YA/W	28-pin	50

CERQUAD

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TRAY	DEVICES PER BOX
KA/K44	44-pin	6	6
KA/K68	68-pin	4	4
KA	84-pin	42	210

LEADLESS CHIP CARRIER

PACKAGE CODE	PIN COUNT	QUANTITIES
		DEVICES PER TUBE
B2A/2A/GA	20-pin	55
B3A/3A/GA/GC1	28-pin	43
YA/YA/GC2	32-pin	35
BUA/MXA/MUA/UA/XA/GA/GC	44-pin	27
BZA/BUA/UA/ZA/GA/GC	68-pin	19

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.

VII. PACKING QUANTITY INFORMATION

T-90-20

PLASTIC DUAL IN-LINE

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TUBE	DEVICES PER BOX
N/N8	8-pin (300-mil)	50	2000
N/N14/N16	14- 16-pin (300-mil)	25	1000
N	18-pin (300-mil)	20	800
N/N20	20-pin (300-mil)	18	720
N	22-pin (400-mil)	17	544
N/N6	24-pin (600-mil)	15	360
N/N3/N24	24-pin (300-mil)	15	600
N/N24	24-pin (400-mil)	15	480
N/N28	28-pin (600-mil)	13	312
N/N3	28-pin (300-mil)	13	520
N	32-pin (600-mil)	11	264
N/N40	40-pin (600-mil)	9	216
NB (Shrink)	42-pin (600-mil)	12	288
N/N48	48-pin (600-mil)	7	168
N	50-pin (900-mil)	7	112
N/N64	64-pin (900-mil)	5	80

PLASTIC LEADED CHIP CARRIER (PLCC)

PACKAGE CODE	PIN COUNT	QUANTITIES		
		DEVICES PER TUBE	DEVICES PER BOX	DEVICES PER REEL
A	20-pin	46	3680	1000
A/A28	28-pin	37	2368	750
A	32-pin	31	2232	750
A/A44	44-pin	26	1248	500
A/A52	52-pin	23	1012	500
A/A68	68-pin	18	648	250
A/A84	84-pin	15	420	250

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.

VII. PACKING QUANTITY INFORMATION

T-90-20

PLASTIC SMALL OUTLINE (SO)

PACKAGE CODE	PIN COUNT	QUANTITIES		
		DEVICES PER TUBE	DEVICES PER BOX	DEVICES PER REEL
D/D8	8-pin (150-mil)	100	10000	2500
D	8-pin (300-mil)	64	2560	1000 – 13" 700 – 7"
D/D14	14-pin (150-mil)	57	5700	2500
D	16-pin (150-mil)	50	5000	2500
D	16-pin (300-mil)	48	1920	1000
DK(SSOP)	20-pin (170-mil)	75	6750	2500
D	20-pin (300-mil)	38	1520	1000
D/D24	24-pin (300-mil)	32	1280	1000
D	28-pin (300-mil)	27	1080	1000
D	40-pin (VSO-40)	31	1240	1000 – 13" 300 – 7"
D	56-pin (VSO-56)	22	616	1000

QUAD FLAT PACK*

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TRAY	DEVICES PER BOX
B/B44	44-pin	50	500
B/B44	44-pin	96	480
B	52-pin	119	595
B	80-pin	66	330
B	100-pin	50	250
B	120-pin	24	120
B	120-pin (Philips source)	30	150

* Quad Flat Pack parts require dry pack handling according to EIA Standard - 583.
These parts are identified in part list section with DRY PACK in the Cross Ref Part No field.

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.