National Semiconductor

查询"NMC6518N-5"供应商

NMC6518 1024-Bit (1024 × 1) Static RAM

General Description

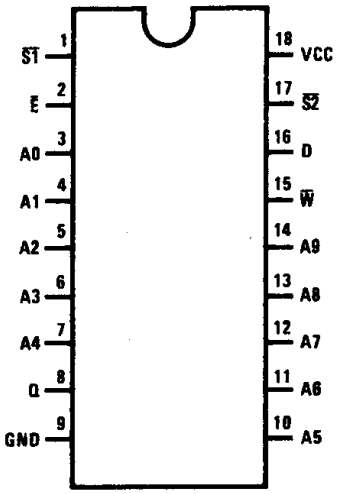
The NMC6518 is a static CMOS random access read/write memory organized as 1024 words of 1 bit each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by the on-chip latches for the address inputs and data output. The ENABLE input serves as the device strobe controlling the latching functions. The TRI-STATE® output, in conjunction with the ENABLE input, allow easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- 18 pin — high density packaging
- Output data latches

Connection Diagram

Dual-In-Line Package

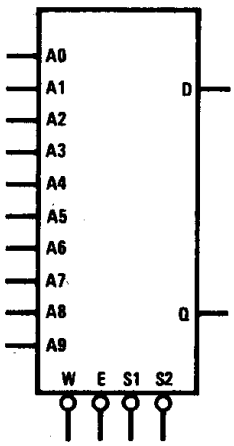


TOP VIEW

Order Number NMC6518J-2, NMC6518J-9 or NMC6518J-5
See NS Package J16A

Order Number NMC6518N-5
See NS Package N16A

Logic Symbol



Pin Names

A0–A9	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
$\overline{S1}$, $\overline{S2}$	Chip Selects

Functional Description

An NMC6518 memory cycle is initiated by the falling edge of the ENABLE input, which latches the address information into the on-chip registers. Data output is enabled when the WRITE ($\overline{W}$) input is high and the ENABLE, SELECT 1 ($\overline{S1}$) and SELECT 2 ($\overline{S2}$) inputs are LOW.

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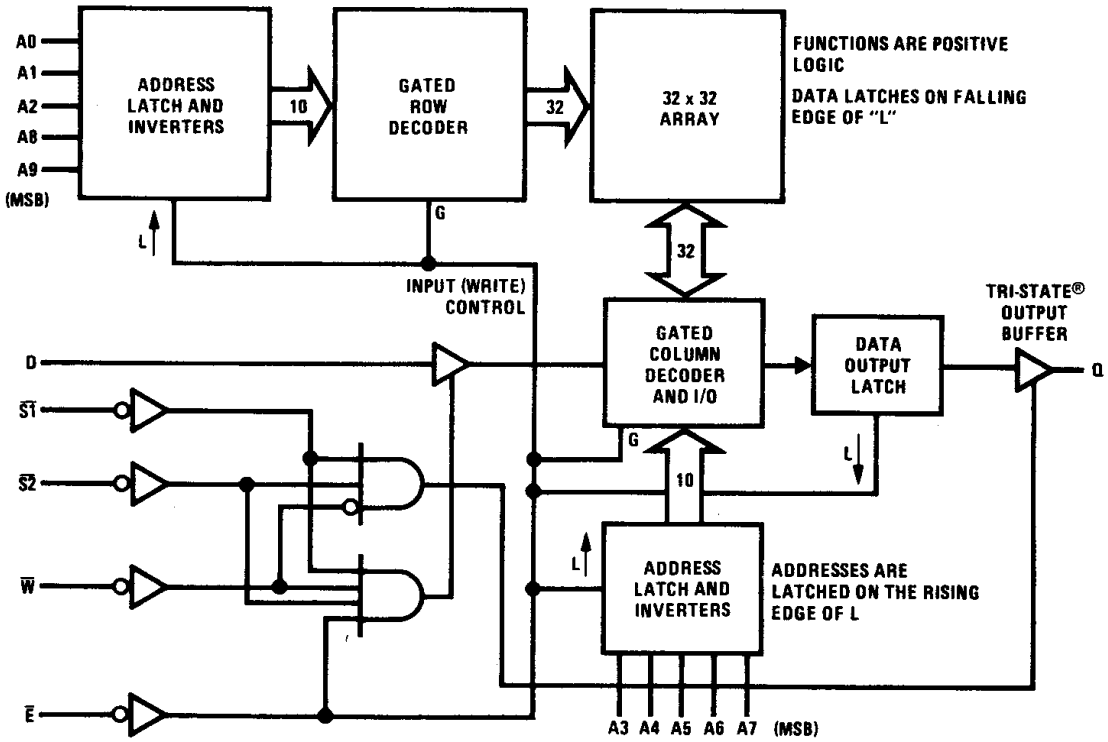
When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum ENABLE LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle.

When performing a write cycle, the minimum ENABLE LOW time is required to enter new data. The write pulse is created by the coincident LOW of the WRITE, ENABLE and both SELECT inputs. The input data set-up and hold times are referenced to the rising edge of the WRITE, ENABLE, SELECT 1 or SELECT 2 inputs, whichever occurs first.

Block Diagram



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Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6518B-9	4.5V	5.5V
NMC6518B-2	4.5V	5.5V
NMC6518-9	4.5V	5.5V
NMC6518-2	4.5V	5.5V
NMC6518-5	4.75V	5.25V
Temperature		
NMC6518B-9	−40°C	85°C
NMC6518B-2	−55°C	125°C
NMC6518-9	−40°C	85°C
NMC6518-2	−55°C	125°C
NMC6518-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

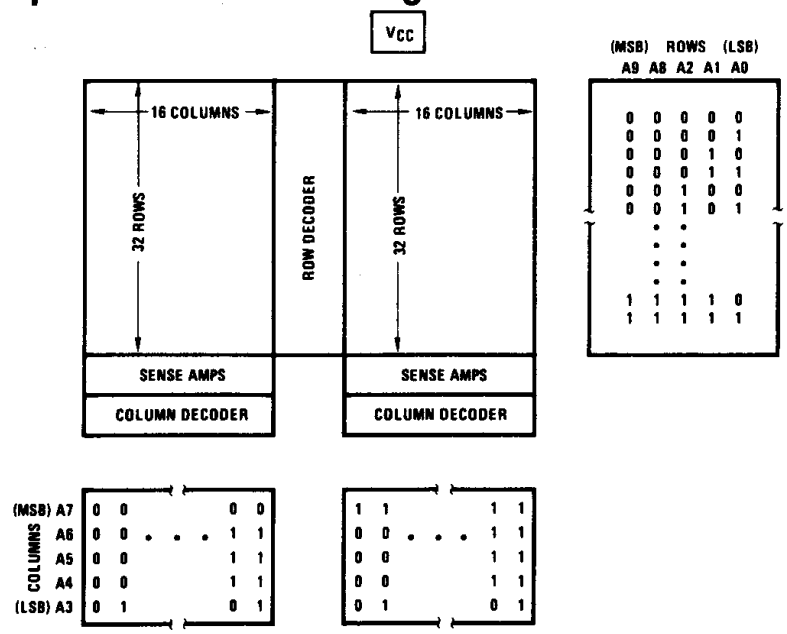
Symbol	Parameter	Conditions	NMC6518B-9, NMC6518B-2 NMC6518-9, NMC6518-2		NMC6518-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC −2.0	VCC +0.3	VCC −2	VCC +0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

AC Test Conditions

Input Rise and Fall Times: ≤20 ns
All Timing Reference Levels: 1/2 VCC
Output Load: 1 TTL Load, 50 pF

NMC6518 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

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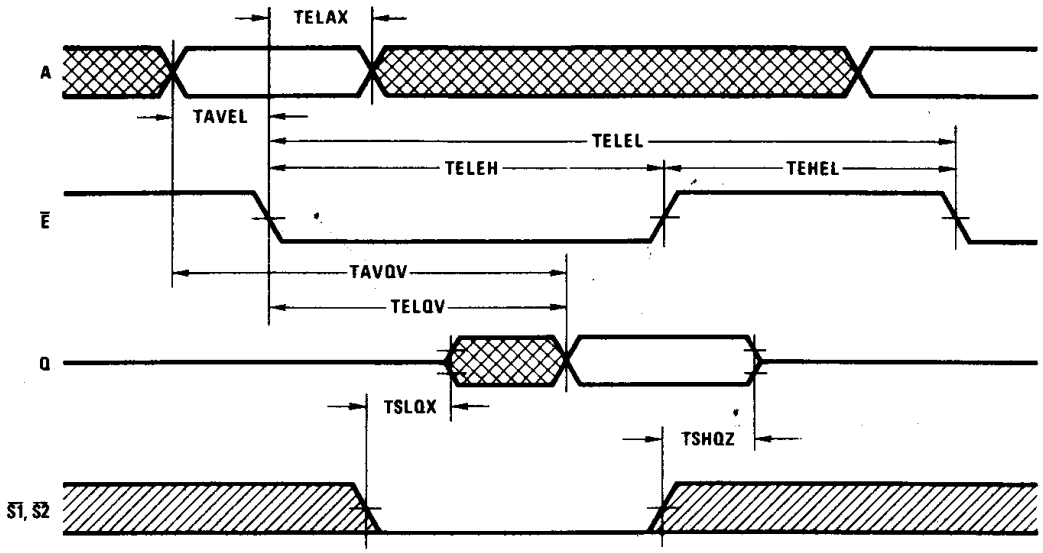
Symbol	Parameter	NMC6518B-9 NMC6518B-2		NMC6518-9 NMC6518-2		NMC6518-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		50		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	180		250		300		ns
TELEL	Read or Write Cycle Time	280		350		450		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	100		100		150		ns
TSHQX	Chip Select Output Disable Time		120		160		200	ns
TSLQX	Chip Select Output Enable Time		120		160		200	ns

Read Cycle Waveforms

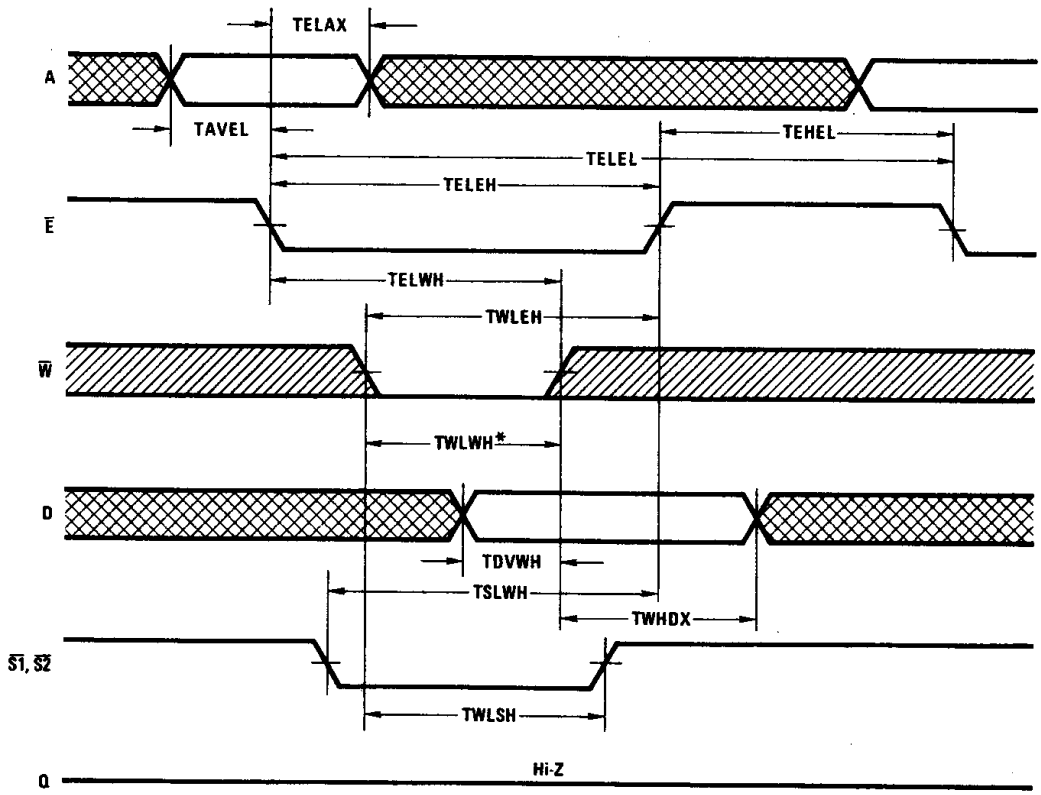


查询"NMC6518N-5"供应商

Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6518B-9 NMC6518B-2		NMC6518-9 NMC6518-2		NMC6518-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		50		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	100		130		160		ns
TELEL	Read or Write Cycle Time	280		350		450		ns
TWLSH	Chip Select Write Pulse Set-up Time	100		130		160		ns
TWLEH	Chip Enable Write Pulse Set-up Time	100		130		160		ns
TSLWH	Chip Select Write Pulse Hold Time	100		130		160		ns
TWHDX	Data Hold Time	0		0		0		ns
TDVWH	Data Set-up Time	80		110		130		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	180		250		300		ns
TELWH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	100		130		160		ns

Write Cycle Waveforms



* TWLWH, the write pulse, is coincidence low of $\overline{E}$, $\overline{W}$, $\overline{S1}$, and $\overline{S2}$ inputs

Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

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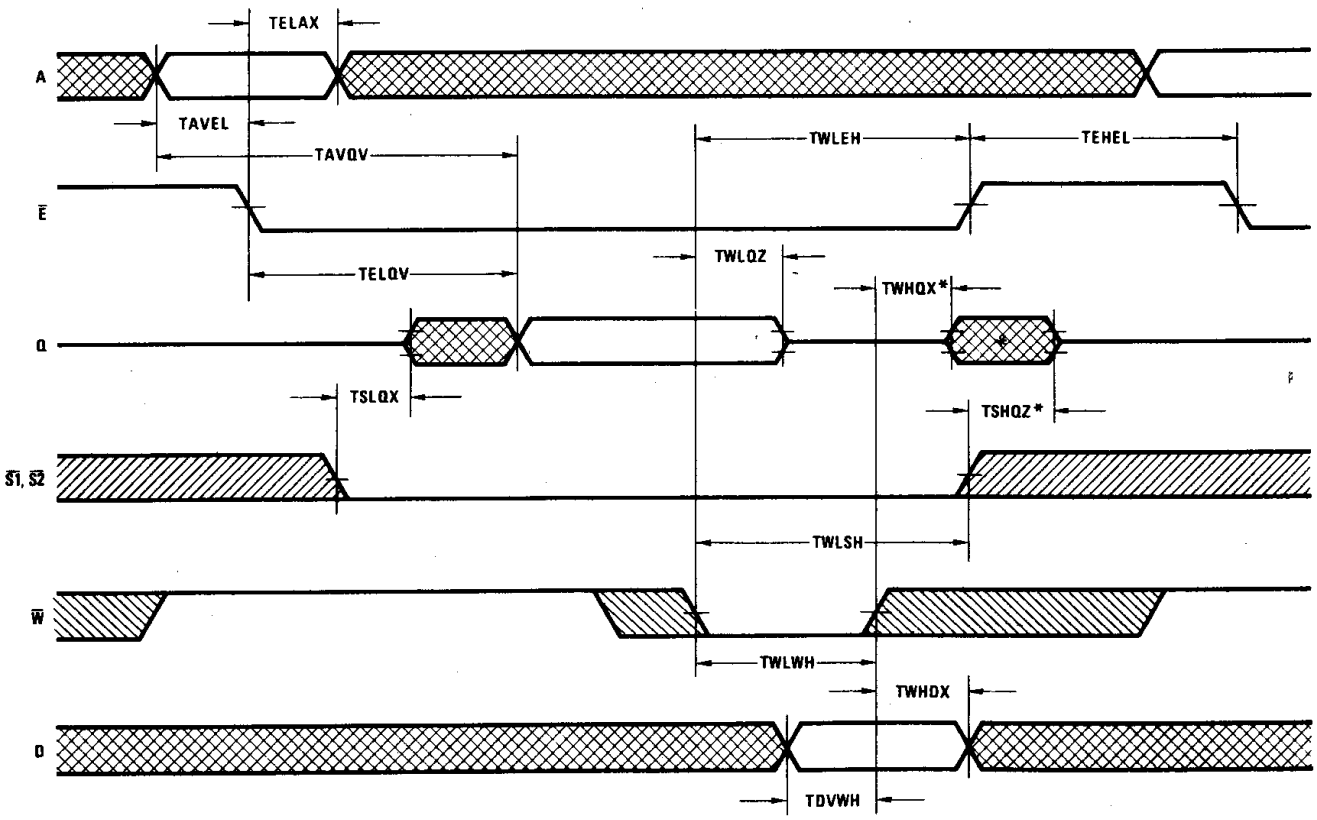
Symbol	Parameter	NMC6518B-9 NMC6518B-2		NMC6518-9 NMC6518-2		NMC6518-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		50		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TSHQX	Chip Select Output Disable Time		120		160		200	ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	100		130		160		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TWLSH	Chip Select Write Pulse Set-up Time	100		130		160		ns
TWLEH	Chip Enable Write Pulse Set-up Time	100		130		160		ns
TSLQX	Chip Select Output Enable Time		120		160		200	ns
TWHDX	Data Hold Time	0		0		0		ns
TDVWH	Data Set-up Time	80		110		130		ns
TWHQX	Output Enable from Write ($\overline{W}$)		120		160		200	ns
TWLQZ	Output Disable from Write ($\overline{W}$)		120		160		200	ns

Read-Modify-Write Cycle Waveforms



* Precede $\overline{W}$ rising edge with $\overline{E}$ rising edge to avoid unwanted output enabling