PN512

Transmission Module

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Product data sheet
PUBLIC

1. Introduction

This Product data sheet document describes the functionality of the transceiver IC PN512. It includes functional and electrical specifications.

2. General description

The PN512 is a highly integrated transceiver IC for contactless communication at 13.56 MHz. This transceiver IC utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz.

The PN512 transceiver ICs support 4 different operating modes

- Reader/Writer mode supporting ISO/IEC 14443A/MIFARE and FeliCa scheme
- Reader/Writer mode supporting ISO/IEC 14443B
- Card Operation mode supporting ISO/IEC 14443A/MIFARE and FeliCa scheme
- NFCIP-1 mode

Enabled in Reader/Writer mode for ISO/IEC 14443A/MIFARE, the PN512's internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A/ MIFARE cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC 14443A/MIFARE compatible cards and transponders. The digital part handles the complete ISO/IEC 14443A framing and error detection (Parity & CRC).

The PN512 supports MIFARE 1 KB or MIFARE 4 KB emulation products. The PN512 supports contactless communication using MIFARE higher transfer speeds up to 424 kbit/s in both directions.

Enabled in Reader/Writer mode for FeliCa, the PN512 transceiver IC supports the FeliCa communication scheme. The receiver part provides a robust and efficient implementation of the demodulation and decoding circuitry for FeliCa coded signals. The digital part handles the FeliCa framing and error detection like CRC. The PN512 supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

The PN512 supports all layers of the ISO/IEC 14443B reader/writer communication scheme, given correct implementation of additional components, like oscillator, power supply, coil etc. and provided that standardized protocols, e.g. like ISO/IEC 14443-4 and/or ISO/IEC 14443B anticollision are correctly implemented.

In Card Operation mode, the PN512 transceiver IC is able to answer to a reader/writer command either according to the FeliCa or ISO/IEC 14443A/MIFARE card interface scheme. The PN512 generates the digital load modulated signals and in addition with an external circuit the answer can be sent back to the reader/writer. A complete card functionality is only possible in combination with a secure IC using the S^2C interface.

Additionally, the PN512 transceiver IC offers the possibility to communicate directly to an NFCIP-1 device in the NFCIP-1 mode. The NFCIP-1 mode offers different communication mode and transfer speeds up to 424 kbit/s according to the Ecma 340 and ISO/IEC 18092 NFCIP-1 Standard. The digital part handles the complete NFCIP-1 framing and error detection.

Various host controller interfaces are implemented:

- 8-bit parallel interface[1]
- SPI interface
- serial UART (similar to RS232 with voltage levels according pad voltage supply)
- I^2C interface.

A purchaser of this NXP IC has to take care for appropriate third party patent licenses.

1. 8-bit parallel Interface only available in HVQFN40 package.

3. Features

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF Level detector
- Integrated data mode detector
- ISO/IEC 14443A/MIFARE support
- ISO/IEC 14443B reader/writer functionality
- Typical operating distance in Reader/Writer mode for communication to a ISO/IEC 14443A/ MIFARE or FeliCa card up to 50 mm depending on the antenna size, tuning and power supply
- Typical operating distance in NFCIP-1 mode up to 50 mm depending on the antenna size and tuning and power supply
- Typical operating distance in ISO/IEC 14443A/MIFARE card or FeliCa Card Operation mode of about 100 mm depending on the antenna size and tuning and the external field strength
- Supports MIFARE 1 KB or MIFARE 4 KB emulation encryption in Reader/Writer mode
- ISO/IEC 14443A higher transfer speed communication at 212 kbit/s and 424 kbit/s
- Contactless communication according to the FeliCa scheme at 212 kbit/s and 424 kbit/s
- Integrated RF interface for NFCIP-1 up to 424 kbit/s
- S^2C interface
- Additional power supply to directly supply the smart card IC connected via S^2C
- Supported host controller interfaces
  - SPI interface up to 10 Mbit/s
  - I^2C interface up to 400 kbit/s in Fast mode, up to 3400 kbit/s in High-speed mode
  - serial UART in different transfer speeds up to 1228.8 kbit/s, framing according to the RS232 interface with voltage levels according pad voltage supply
  - 8-bit parallel interface with and without Address Latch Enable
- Comfortable 64 byte send and receive FIFO-buffer
- Flexible interrupt modes
- Hard reset with low power function
- Power-down mode per software
- Programmable timer
- Internal oscillator to connect 27.12 MHz quartz
- 2.5-3.6 V power supply
- CRC Co-processor
- Free programmable I/O pins
- Internal self test

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AV_{DD}	Supply Voltage	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V,	[1][2]	2.5	-	3.6	V
DV_{DD}		$PV_{DD} \leq AV_{DD} = DV_{DD} = TV_{DD}$	[1][2]				
TV_{DD}			[1][2]				
PV_{DD}	Pad power supply	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V, $PV_{DD} \leq AV_{DD} = DV_{DD} = TV_{DD}$	[3]	1.6	-	3.6	V
SV_{DD}	S^2C Pad Power Supply	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V,		1.6	-	3.6	V
I_{HPD}	Hard Power-down Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, N_{RESET} = LOW	[7]	-	-	5	µA
I_{SPD}	Soft Power-down Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, RF level detector on	[7]	-	-	10	µA
I_{DVDD}	Digital Supply Current	$DV_{DD} = 3$ V		-	6.5	9	mA
I_{AVDD}	Analog Supply Current	$AV_{DD} = 3$ V, bit RCVOff = 0		-	7	10	mA
$I_{AVDD,RCVOFF}$	Analog Supply Current, receiver switched off	$AV_{DD} = 3$ V, bit RCVOff = 1		-	3	5	mA
I_{PVDD}	Pad Supply Current		[5]	-	-	40	mA
I_{TVDD}	Transmitter Supply Current	Continuous Wave	[4][6][8]	-	60	100	mA
T_{amb}	operating ambient temperature			-30		+85	°C

[1] Supply voltage below 3 V reduces the performance (e.g. the achievable operating distance).

[2] AV_{DD}, DV_{DD} and TV_{DD} shall always be on the same voltage level.

[3] PV_{DD} shall always be on the same or lower voltage level than DV_{DD}.

[4] I_{TVDD} depends on TV_{DD} and the external circuitry connected to Tx1 and Tx2

[5] I_{PVDD} depends on the overall load at the digital pins.

[6] During operation with a typical circuitry the overall current is below 100 mA.

[7] I_{SPD} and I_{HPD} are the total currents over all supplies.

[8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between TX1 and TX2 at 13.56 MHz

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5120A0HN1/C1	HVQFN32	Plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617
PN5120A0HN/C1	HVQFN40	Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6× 6× 0.85 mm	SOT618

6. Block diagram

The Analog interface handles the modulation and demodulation of the analog signals according to the Card Receiving mode, Reader/Writer mode and NFCIP-1 mode communication scheme.

The RF level detector detects the presence of an external RF-field delivered by the antenna to the RX pin.

The Data mode detector detects a MIFARE, FeliCa or NFCIP-1 mode in order to prepare the internal receiver to demodulate signals, which are sent to the PN512.

The communication (S^2C) interface provides digital signals to support communication for transfer speeds above 424 kbit/s and digital signals to communicate to a secure IC.

The contactless UART handles the protocol requirements for the communication schemes in co-operation with the host controller. The comfortable FIFO-buffer allows a fast and convenient data transfer from the host controller to the contactless UART and vice versa.

Various host controller interfaces are implemented to fulfill different customer requirements.

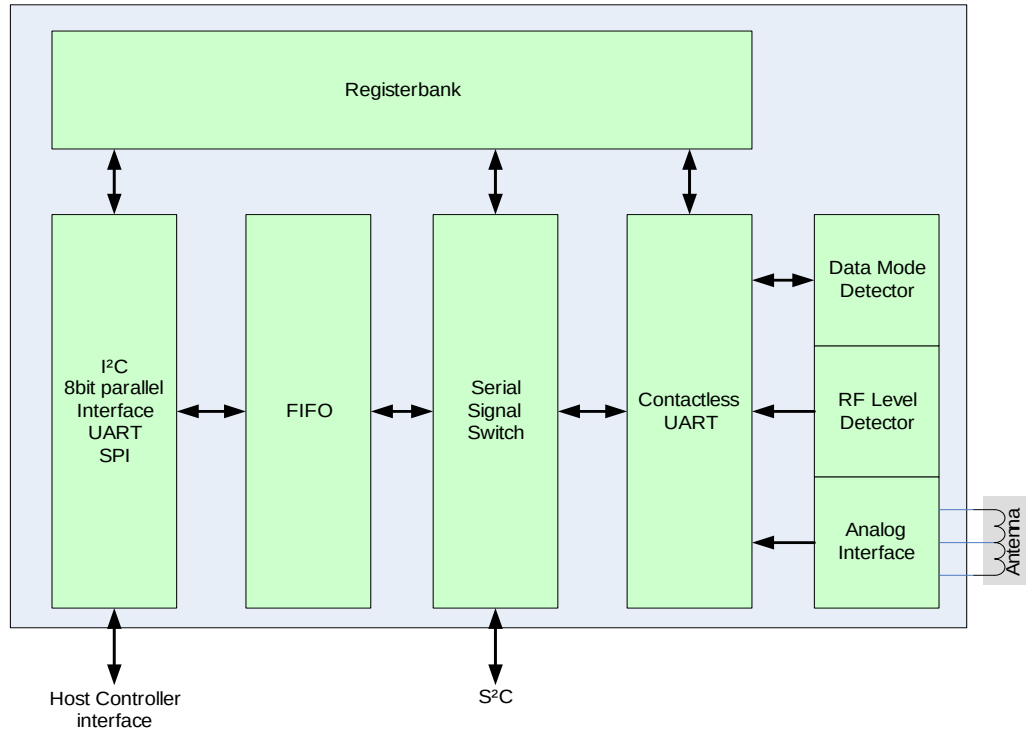


Fig 1. Simplified PN512 Block diagram

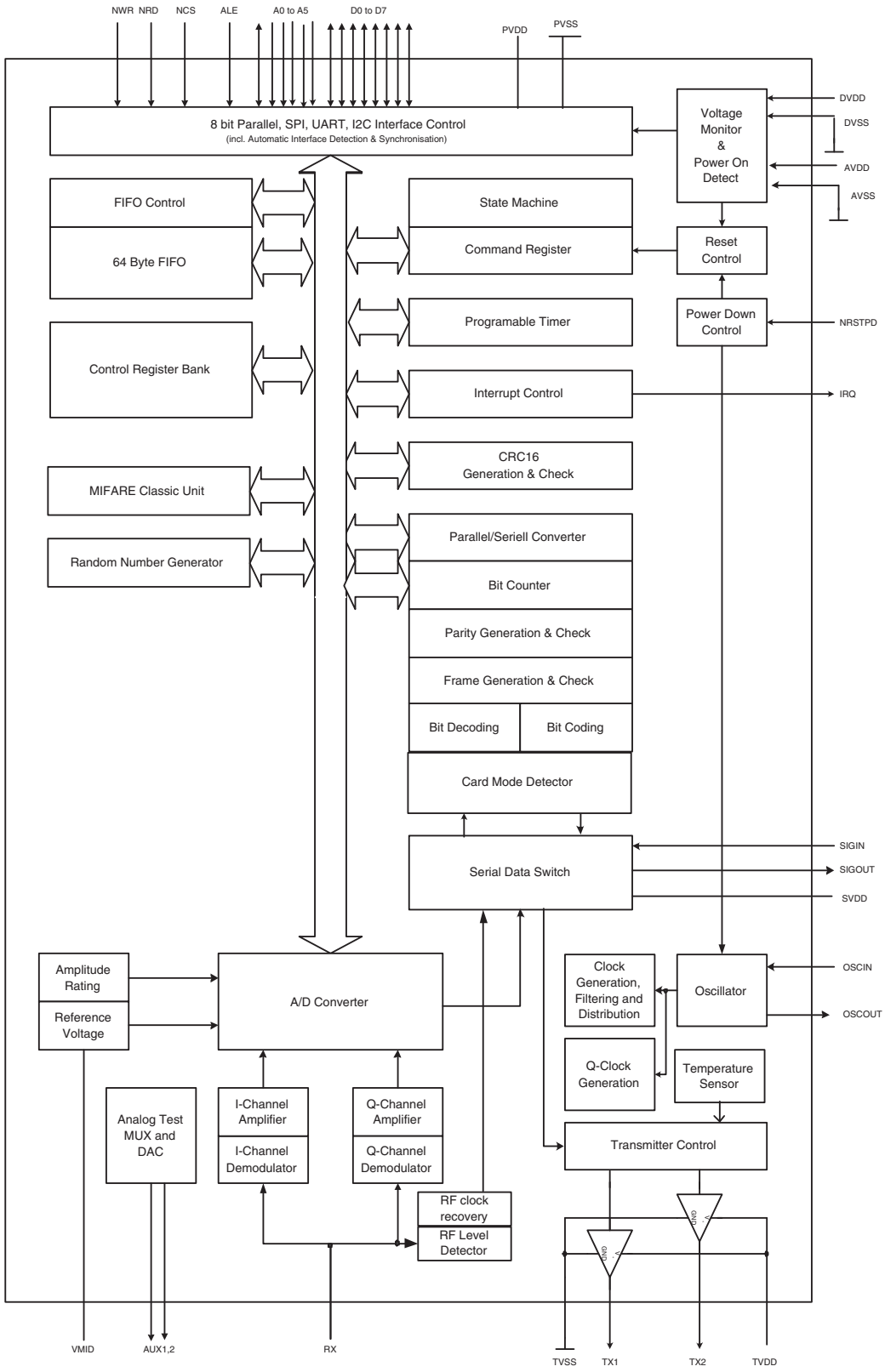


Fig 2. PN512 Block diagram

7. Pinning information

7.1 Pinning

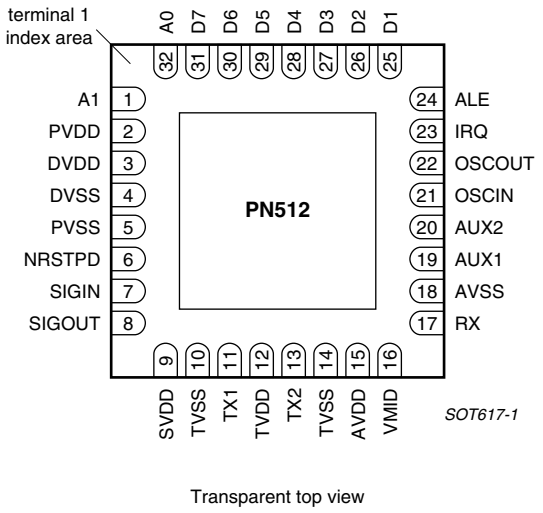


Fig 3. Pinning configuration HVQFN32 (SOT617-1)

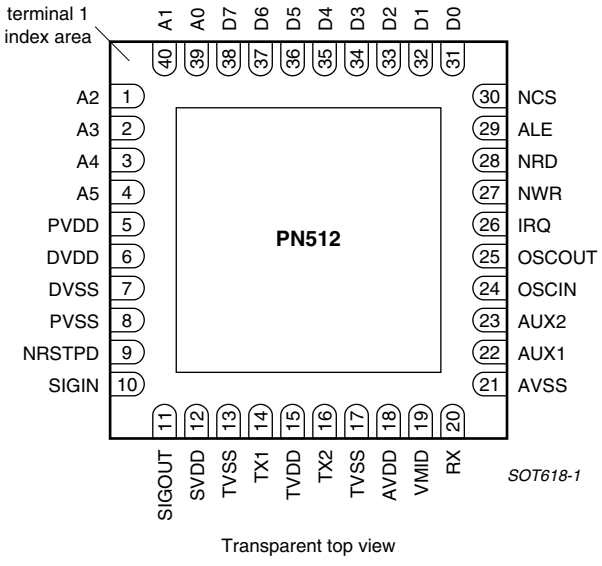


Fig 4. Pinning configuration HVQFN40 (SOT618)

7.2 Pin description

Table 3. Pin description HVQFN32

Symbol	Pin	Type	Description
A1	1	I	**Address Line**
PVDD	2	PWR	**Pad power supply**
DVDD	3	PWR	**Digital Power Supply**
DVSS	4	PWR	**Digital Ground**
PVSS	5	PWR	**Pad power supply ground**
NRSTPD	6	I	**Not Reset and Power Down:** When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
SIGIN	7	I	**Communication Interface Input:** accepts a digital, serial data stream
SIGOUT	8	O	**Communication Interface Output**: delivers a serial data stream
SVDD	9	PWR	**S^{2}C Pad Power Supply:** provides power to the S^{2}C pads
TVSS	10	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
TX1	11	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
TVDD	12	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
TX2	13	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
TVSS	14	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
AVDD	15	PWR	**Analog Power Supply**
VMID	16	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage.
RX	17	I	**Receiver Input**
AVSS	18	PWR	**Analog Ground**
AUX1	19	O	**Auxiliary Outputs:** These pins are used for testing.
AUX2	20	O	
OSCIN	21	I	**Crystal Oscillator Input:** input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (f_{osc} = 27.12 MHz).
OSCOUT	22	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator.
IRQ	23	O	**Interrupt Request:** output to signal an interrupt event
ALE	24	I	**Address Latch Enable:** signal to latch AD0 to AD5 into the internal address latch when HIGH.
D1 to D7	25 to 31	I/O	**8-bit Bi-directional Data Bus.** **Remark:** An 8-bit parallel interface is not available. **Remark:** If the host controller selects I^{2}C as digital host controller interface, these pins can be used to define the I^{2}C address. **Remark:** For serial interfaces this pins can be used for test signals or I/Os.
A0	32	I	**Address Line**

Table 4. Pin description HVQFN40

Symbol	Pin	Type	Description
A2 to A5	1 to 4	I	**Address Line**
PVDD	5	PWR	**Pad power supply**
DVDD	6	PWR	**Digital Power Supply**
DVSS	7	PWR	**Digital Ground**
PVSS	8	PWR	**Pad power supply ground**
NRSTPD	9	I	**Not Reset and Power Down:** When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
SIGIN	10	I	**Communication Interface Input:** accepts a digital, serial data stream
SIGOUT	11	O	**Communication Interface Output**: delivers a serial data stream
SVDD	12	PWR	**S^2C Pad Power Supply:** provides power to the S^2C pads
TVSS	13	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
TX1	14	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
TVDD	15	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
TX2	16	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
TVSS	17	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
AVDD	18	PWR	**Analog Power Supply**
VMID	19	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage.
RX	20	I	**Receiver Input**
AVSS	21	PWR	**Analog Ground**
AUX1	22	O	**Auxiliary Outputs:** These pins are used for testing.
AUX2	23	O	
OSCIN	24	I	**Crystal Oscillator Input:** input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (f_{osc} = 27.12 MHz).
OSCOUT	25	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator.
IRQ	26	O	**Interrupt Request:** output to signal an interrupt event
NWR	27	I	**Not Write:** strobe to write data (applied on D0 to D7) into the PN512 register
NRD	28	I	**Not Read:** strobe to read data from the PN512 register (applied on D0 to D7)
ALE	29	I	**Address Latch Enable:** signal to latch AD0 to AD5 into the internal address latch when HIGH.
NCS	30	I	**Not Chip Select:** selects and activates the host controller interface of the PN512
D0 to D7	31 to 38	I/O	**8-bit Bi-directional Data Bus.** **Remark:** For serial interfaces this pins can be used for test signals or I/Os. **Remark:** If the host controller selects I^2C as digital host controller interface, these pins can be used to define the I^2C address.
A0 to1 A1	39 to 40	I	**Address Line**

8. PN512 register SET

8.1 PN512 registers overview

Table 5. PN512 registers overview

Addr (hex)	Register Name	Function
Page 0: Command and Status		
0	PageReg	Selects the register page
1	CommandReg	Starts and stops command execution
2	ComlEnReg	Controls bits to enable and disable the passing of Interrupt Requests
3	DivlEnReg	Controls bits to enable and disable the passing of Interrupt Requests
4	ComIrqReg	Contains Interrupt Request bits
5	DivIrqReg	Contains Interrupt Request bits
6	ErrorReg	Error bits showing the error status of the last command executed
7	Status1Reg	Contains status bits for communication
8	Status2Reg	Contains status bits of the receiver and transmitter
9	FIFODataReg	In- and output of 64 byte FIFO-buffer
A	FIFOLevelReg	Indicates the number of bytes stored in the FIFO
B	WaterLevelReg	Defines the level for FIFO under- and overflow warning
C	ControlReg	Contains miscellaneous Control Registers
D	BitFramingReg	Adjustments for bit oriented frames
E	CollReg	Bit position of the first bit collision detected on the RF-interface
F	RFU	Reserved for future use
Page 1: Command		
0	PageReg	Selects the register page
1	ModeReg	Defines general modes for transmitting and receiving
2	TxModeReg	Defines the data rate and framing during transmission
3	RxModeReg	Defines the data rate and framing during receiving
4	TxControlReg	Controls the logical behavior of the antenna driver pins TX1 and TX2
5	TxAutoReg	Controls the setting of the antenna drivers
6	TxSelReg	Selects the internal sources for the antenna driver
7	RxSelReg	Selects internal receiver settings
8	RxThresholdReg	Selects thresholds for the bit decoder
9	DemodReg	Defines demodulator settings
A	FelNFC1Reg	Defines the length of the valid range for the receive package
B	FelNFC2Reg	Defines the length of the valid range for the receive package
C	MifNFCReg	Controls the communication in ISO/IEC 14443/MIFARE and NFC target mode at 106 kbit
D	ManualRCVReg	Allows manual fine tuning of the internal receiver
E	TypeBReg	Configure the ISO/IEC 14443 type B
F	SerialSpeedReg	Selects the speed of the serial UART interface
Page 2: CFG		

Table 5. PN512 registers overview *...continued*

Addr (hex)	Register Name	Function
0	PageReg	Selects the register page
1	CRCResultReg	Shows the actual MSB and LSB values of the CRC calculation
2		
3	GsNOffReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation, when the driver is switched off
4	ModWidthReg	Controls the setting of the ModWidth
5	TxBitPhaseReg	Adjust the TX bit phase at 106 kbit
6	RFCfgReg	Configures the receiver gain and RF level
7	GsNOnReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation when the drivers are switched on
8	CWGsPReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation during times of no modulation
9	ModGsPReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation during modulation
A	TModeReg TPrescalerReg	Defines settings for the internal timer
B		
C	TReloadReg	Describes the 16-bit timer reload value
D		
E	TCounterValReg	Shows the 16-bit actual timer value
F		
Page 3: TestRegister		
0	PageReg	selects the register page
1	TestSel1Reg	General test signal configuration
2	TestSel2Reg	General test signal configuration and PRBS control
3	TestPinEnReg	Enables pin output driver on 8-bit parallel bus (Note: For serial interfaces only)
4	TestPin ValueReg	Defines the values for the 8-bit parallel bus when it is used as I/O bus
5	TestBusReg	Shows the status of the internal testbus
6	AutoTestReg	Controls the digital selftest
7	VersionReg	Shows the version
8	AnalogTestReg	Controls the pins AUX1 and AUX2
9	TestDAC1Reg	Defines the test value for the TestDAC1
A	TestDAC2Reg	Defines the test value for the TestDAC2
B	TestADCReg	Shows the actual value of ADC I and Q
C-F	RFT	Reserved for production tests

8.1.1 Register bit behavior

Depending on the functionality of a register, the access conditions to the register can vary. In principle bits with same behavior are grouped in common registers. In Table 6 the access conditions are described.

Table 6. Behavior of register bits and its designation

Abbreviation	Behavior	Description
r/w	read and write	These bits can be written and read by the μ-Controller. Since they are used only for control means, there content is not influenced by internal state machines, e.g. the PageSelect-Register may be written and read by the μ-Controller. It will also be read by internal state machines, but never changed by them.
dy	dynamic	These bits can be written and read by the μ-Controller. Nevertheless, they may also be written automatically by internal state machines, e.g. the Command-Register changes its value automatically after the execution of the actual command.
r	read only	These registers hold bits, which value is determined by internal states only, e.g. the CRCReady bit can not be written from external but shows internal states.
w	write only	Reading these registers returns always ZERO.
RFU	-	These registers are reserved for future use. In case of a PN512 Version V1.0 (VersionReg=80h) a read access to these registers returns always the value “0”. Nevertheless this is not guaranteed for future chips versions where the value is undefined. In case of a write access, it is recommended to write always the value “0”.
RFT	-	These registers are reserved for production tests and shall not be changed.

8.2 Register description

8.2.1 Page 0: Command and status

8.2.1.1 PageReg

Selects the register page.

Table 7. PageReg register (address 00h); reset value: 00h, 0000000b

	7	6	5	4	3	2	1	0
	UsePage Select	0	0	0	0	0	PageSelect	
Access Rights	r/w	RFU	RFU	RFU	RFU	RFU	r/w	r/w

Table 8. Description of PageReg bits

Bit	Symbol	Description
7	UsePageSelect	Set to logic 1, the value of PageSelect is used as register address A5 and A4. The LSB-bits of the register address are defined by the address pins or the internal address latch, respectively. Set to logic 0, the whole content of the internal address latch defines the register address. The address pins are used as described in Section 10.1 “Automatic host controller interface type detection”.
6 to 2	-	Reserved for future use.
1 to 0	PageSelect	The value of PageSelect is used only if UsePageSelect is set to logic 1. In this case it specifies the register page (which is A5 and A4 of the register address).

8.2.1.2 CommandReg

Starts and stops command execution.

Table 9. CommandReg register (address 01h); reset value: 20h, 00100000b

	7	6	5	4	3	2	1	0
	0	0	RcvOff	Power Down	Command			
Access Rights	RFU	RFU	r/w	dy	dy	dy	dy	dy

Table 10. Description of CommandReg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5	RcvOff	Set to logic 1, the analog part of the receiver is switched off.
4	PowerDown	Set to logic 1, Soft Power-down mode is entered. Set to logic 0, the PN512 starts the wake up procedure. During this procedure this bit still shows a 1. A 0 indicates that the PN512 is ready for operations; see Section 16.2 “Soft Power-down”. Note: The bit Power Down cannot be set, when the command SoftReset has been activated.
3 to 0	Command	Activates a command according to the Command Code. Reading this register shows, which command is actually executed (see Section 18.3 “PN512 Commands overview”).

8.2.1.3 CommIEnReg

Control bits to enable and disable the passing of interrupt requests.

Table 11. CommIEnReg register (address 02h); reset value: 80h, 10000000b

	7	6	5	4	3	2	1	0
	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 12. Description of CommIEnReg bits

Bit	Symbol	Description
7	IRqInv	Set to logic 1, the signal on pin IRQ is inverted with respect to bit IRq in the register Status1Reg. Set to logic 0, the signal on pin IRQ is equal to bit IRq. In combination with bit IRqPushPull in register DivIEnReg, the default value of 1 ensures, that the output level on pin IRQ is 3-state.
6	TxIEn	Allows the transmitter interrupt request (indicated by bit TxIRq) to be propagated to pin IRQ.
5	RxIEn	Allows the receiver interrupt request (indicated by bit RxIRq) to be propagated to pin IRQ.
4	IdleIEn	Allows the idle interrupt request (indicated by bit IdleIRq) to be propagated to pin IRQ.
3	HiAlertIEn	Allows the high alert interrupt request (indicated by bit HiAlertIRq) to be propagated to pin IRQ.
2	LoAlertIEn	Allows the low alert interrupt request (indicated by bit LoAlertIRq) to be propagated to pin IRQ.
1	ErrIEn	Allows the error interrupt request (indicated by bit ErrIRq) to be propagated to pin IRQ.
0	TimerIEn	Allows the timer interrupt request (indicated by bit TimerIRq) to be propagated to pin IRQ.

8.2.1.4 DivIEnReg

Control bits to enable and disable the passing of interrupt requests.

Table 13. DivIEnReg register (address 03h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	IRQPushPull	0	0	SiginActIEn	ModeIEn	CRCIEn	RFOnIEn	RFOffIEn
Access Rights	r/w	RFU	RFU	r/w	r/w	r/w	r/w	r/w

Table 14. Description of DivIEnReg bits

Bit	Symbol	Description
7	IRQPushPull	Set to logic 1, the pin IRQ works as standard CMOS output pad. Set to logic 0, the pin IRQ works as open drain output pad.
6 to 5	-	Reserved for future use.
4	SiginActIEn	Allows the SIGIN active interrupt request to be propagated to pin IRQ.
3	ModeIEn	Allows the mode interrupt request (indicated by bit ModeIRq) to be propagated to pin IRQ.
2	CRCIEn	Allows the CRC interrupt request (indicated by bit CRCIRq) to be propagated to pin IRQ.
1	RfOnIEn	Allows the RF field on interrupt request (indicated by bit RfOnIRq) to be propagated to pin IRQ.
0	RfOffIEn	Allows the RF field off interrupt request (indicated by bit RfOffIRq) to be propagated to pin IRQ.

8.2.1.5 CommIRqReg

Contains Interrupt Request bits.

Table 15. CommIRqReg register (address 04h); reset value: 14h, 00010100b

	7	6	5	4	3	2	1	0
	Set1	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Access Rights	w	dy	dy	dy	dy	dy	dy	dy

Table 16. Description of CommIRqReg bits

All bits in the register CommIRqReg shall be cleared by software.

Bit	Symbol	Description
7	Set1	Set to logic 1, Set1 defines that the marked bits in the register CommIRqReg are set. Set to logic 0, Set1 defines, that the marked bits in the register CommIRqReg are cleared.
6	TxIRq	Set to logic 1 immediately after the last bit of the transmitted data was sent out.
5	RxIRq	Set to logic 1 when the receiver detects the end of a valid datastream. If the bit RxNoErr in register RxModeReg is set to logic 1, bit RxIRq is only set to logic 1 when data bytes are available in the FIFO.
4	IdleIRq	Set to logic 1, when a command terminates by itself e.g. when the CommandReg changes its value from any command to the Idle Command. If an unknown command is started, the CommandReg changes its content to the idle state and the bit IdleIRq is set. Starting the Idle Command by the μ-Controller does not set bit IdleIRq.
3	HiAlertIRq	Set to logic 1, when bit HiAlert in register Status1Reg is set. In opposition to HiAlert, HiAlertIRq stores this event and can only be reset as indicated by bit Set1.
2	LoAlertIRq	Set to logic 1, when bit LoAlert in register Status1Reg is set. In opposition to LoAlert, LoAlertIRq stores this event and can only be reset as indicated by bit Set1.
1	ErrIRq	Set to logic 1 if any error bit in the Error Register is set.
0	TimerIRq	Set to logic 1 when the timer decrements the TimerValue Register to zero.

8.2.1.6 DivIRqReg

Contains Interrupt Request bits

Table 17. DivIRqReg register (address 05h); reset value: XXh, 000X00XXb

	7	6	5	4	3	2	1	0
	Set2	0	0	SiginActIRq	ModeIRq	CRCIRq	RFOnIRq	RFOffIRq
Access Rights	w	RFU	RFU	dy	dy	dy	dy	dy

Table 18. Description of DivIRqReg bits

All bits in the register DivIRqReg shall be cleared by software.

Bit	Symbol	Description
7	Set2	Set to logic 1, Set2 defines that the marked bits in the register DivIRqReg are set. Set to logic 0, Set2 defines, that the marked bits in the register DivIRqReg are cleared
6 to 5	-	Reserved for future use.
4	SiginActIRq	Set to logic 1, when SIGIN is active. See Section 11.6 “S^{2}C interface support”. This interrupt is set when either a rising or falling signal edge is detected.
3	ModeIRq	Set to logic 1, when the mode has been detected by the Data mode detector. Note: The Data mode detector can only be activated by the AutoColl command and is terminated automatically having detected the Communication mode. Note: The Data mode detector is automatically restarted after each RF Reset.
2	CRCIRq	Set to logic 1, when the CRC command is active and all data are processed.
1	RFOnIRq	Set to logic 1, when an external RF field is detected.
0	RFOffIRq	Set to logic 1, when a present external RF field is switched off.

8.2.1.7 ErrorReg

Error bit register showing the error status of the last command executed.

Table 19. ErrorReg register (address 06h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	WrErr	TempErr	RFErr	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access Rights	r	r	r	r	r	r	r	r

Table 20. Description of ErrorReg bits

Bit	Symbol	Description
7	WrErr	Set to logic 1, when data is written into FIFO by the host controller during the AutoColl command or MFAuthent command or if data is written into FIFO by the host controller during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface.
6	TempErr[1]	Set to logic 1, if the internal temperature sensor detects overheating. In this case, the antenna drivers are switched off automatically.
5	RFErr	Set to logic 1, if in Active Communication mode the counterpart does not switch on the RF field in time as defined in NFCIP-1 standard. Note: RFErr is only used in Active Communication mode. The bits RxFraming or the bits TxFraming has to be set to 01 to enable this functionality.
4	BufferOvfl	Set to logic 1, if the host controller or a PN512's internal state machine (e.g. receiver) tries to write data into the FIFO-bufferFIFO-buffer although the FIFO-buffer is already full.
3	CollErr	Set to logic 1, if a bit-collision is detected. It is cleared automatically at receiver start-up phase. This bit is only valid during the bitwise anticollision at 106 kbit. During communication schemes at 212 and 424 kbit this bit is always set to logic 1.
2	CRCErr	Set to logic 1, if bit RxCRCEn in register RxModeReg is set and the CRC calculation fails. It is cleared to 0 automatically at receiver start-up phase.
1	ParityErr	Set to logic 1, if the parity check has failed. It is cleared automatically at receiver start-up phase. Only valid for ISO/IEC 14443A/MIFARE or NFCIP-1 communication at 106 kbit.
0	ProtocolErr	Set to logic 1, if one out of the following cases occur: • Set to logic 1 if the SOF is incorrect. It is cleared automatically at receiver start-up phase. The bit is only valid for 106 kbit in Active and Passive Communication mode. • If bit DetectSync in register ModeReg is set to logic 1 during FeliCa communication or active communication with transfer speeds higher than 106 kbit, the bit ProtocolErr is set to logic 1 in case of a byte length violation. • During the AutoColl command, bit ProtocolErr is set to logic 1, if the bit Initiator in register ControlReg is set to logic 1. • During the MFAuthent Command, bit ProtocolErr is set to logic 1, if the number of bytes received in one data stream is incorrect. • Set to logic 1, if the Miller Decoder detects 2 pulses below the minimum time according to the ISO/IEC 14443A definitions.

[1] Command execution will clear all error bits except for bit TempErr. A setting by software is impossible.

8.2.1.8 Status1Reg

Contains status bits of the CRC, Interrupt and FIFO-buffer.

Table 21. Status1Reg register (address 07h); reset value: XXh, X100X01Xb

	7	6	5	4	3	2	1	0
	RFFreqOK	CRCOk	CRCReady	IRq	TRunning	RFOn	HiAlert	LoAlert
Access Rights	r	r	r	r	r	r	r	r

Table 22. Description of Status1Reg bits

Bit	Symbol	Description
7	RFFreqOK	Indicates if the frequency detected at the RX pin is in the range of 13.56 MHz. Set to logic 1, if the frequency at the RX pin is in the range 12 MHz < RX pin frequency < 15 MHz. Note: The value of RFFreqOK is not defined if the external RF frequency is in the range from 9 to 12 MHz or in the range from 15 to 19 MHz.
6	CRCOk	Set to logic 1, if the CRC Result is zero. For data transmission and reception the bit CRCOk is undefined (use CRCErr in register ErrorReg). CRCOk indicates the status of the CRC co-processor, during calculation the value changes to ZERO, when the calculation is done correctly, the value changes to ONE.
5	CRCReady	Set to logic 1, when the CRC calculation has finished. This bit is only valid for the CRC co-processor calculation using the command CalcCRC.
4	IRq	This bit shows, if any interrupt source requests attention (with respect to the setting of the interrupt enable bits, see register CommIEnReg and DivIEnReg).
3	TRunning	Set to logic 1, if the PN512's timer unit is running, e.g. the timer will decrement the TCounterValReg with the next timer clock. Note: In the gated mode the bit TRunning is set to logic 1, when the timer is enabled by the register bits. This bit is not influenced by the gated signal.
2	RFOn	Set to logic 1, if an external RF field is detected. This bit does not store the state of the RF field.
1	HiAlert	Set to logic 1, when the number of bytes stored in the FIFO-buffer fulfills the following equation: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ Example: FIFOLength = 60, WaterLevel = 4 → HiAlert = 1 FIFOLength = 59, WaterLevel = 4 → HiAlert = 0
0	LoAlert	Set to logic 1, when the number of bytes stored in the FIFO-buffer fulfills the following equation: $LoAlert = FIFOLength \leq WaterLevel$ Example: FIFOLength = 4, WaterLevel = 4 → LoAlert = 1 FIFOLength = 5, WaterLevel = 4 → LoAlert = 0

8.2.1.9 Status2Reg

Contains status bits of the Receiver, Transmitter and Data mode detector.

Table 23. Status2Reg register (address 08h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TempSensClear	I²CForceHS	0	TargetActivated	MFCrypto1On	Modem State		
Access Rights	r/w	r/w	RFU	dy	dy	r	r	r

Table 24. Description of Status2Reg bits

Bit	Symbol	Description
7	TempSensClear	Set to logic 1, this bit clears the temperature error, if the temperature is below the alarm limit of 125 °C.
6	I²CForceHS	I²C input filter settings. Set to logic 1, the I²C input filter is set to the High-speed mode independent of the I²C protocol. Set to logic 0, the I²C input filter is set to the used I²C protocol.
5	-	Reserved for future use.
4	TargetActivated	Set to logic 1 if the Select command or if the Polling command was answered. Note: This bit can only be set during the AutoColl command in Passive Communication mode. Note: This bit is cleared automatically by switching off the external RF field.
3	MFCrypto1On	This bit indicates that the MIFARE Crypto1 unit is switched on and therefore all data communication with the card is encrypted. This bit can only be set to logic 1 by a successful execution of the MFAuthent Command. This bit is only valid in Reader/Writer mode for MIFARE cards. This bit shall be cleared by software.
2 to 0	Modem State	ModemState shows the state of the transmitter and receiver state machines.

Value	Description
000	IDLE
001	Wait for StartSend in register BitFramingReg
010	TxWait: Wait until RF field is present, if the bit TxWaitRF is set to logic 1. The minimum time for TxWait is defined by the TxWaitReg register.
011	Sending
100	RxWait: Wait until RF field is present, if the bit RxWaitRF is set to logic 1. The minimum time for RxWait is defined by the RxWaitReg register.
101	Wait for data
110	Receiving

8.2.1.10 FIFODataReg

In- and output of 64 byte FIFO-buffer.

Table 25. FIFODataReg register (address 09h); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	FIFOData							
Access Rights	dy	dy	dy	dy	dy	dy	dy	dy

Table 26. Description of FIFODataReg bits

Bit	Symbol	Description
7 to 0	FIFOData	Data input and output port for the internal 64 byte FIFO-buffer. The FIFO-buffer acts as parallel in/parallel out converter for all serial data stream in- and outputs.

8.2.1.11 FIFOLevelReg

Indicates the number of bytes stored in the FIFO.

Table 27. FIFOLevelReg register (address 0Ah); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	FlushBuffer	FIFOLevel						
Access Rights	w	r	r	r	r	r	r	r

Table 28. Description of FIFOLevelReg bits

Bit	Symbol	Description
7	FlushBuffer	Set to logic 1, this bit clears the internal FIFO-buffer's read- and write-pointer and the bit BufferOvfl in the register ErrReg immediately. Reading this bit will always return 0.
6 to 0	FIFOLevel	Indicates the number of bytes stored in the FIFO-buffer. Writing to the FIFODataReg increments, reading decrements the FIFOLevel.

8.2.1.12 WaterLevelReg

Defines the level for FIFO under- and overflow warning.

Table 29. WaterLevelReg register (address 0Bh); reset value: 08h, 00001000b

	7	6	5	4	3	2	1	0
	0	0	WaterLevel					
Access Rights	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table 30. Description of WaterLevelReg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5 to 0	WaterLevel	This register defines a warning level to indicate a FIFO-buffer over- or underflow: The bit HiAlert in Status1Reg is set to logic 1, if the remaining number of bytes in the FIFO-buffer space is equal or less than the defined number of WaterLevel bytes. The bit LoAlert in Status1Reg is set to logic 1, if equal or less than WaterLevel bytes are in the FIFO. Note: For the calculation of HiAlert and LoAlert see Table 21

8.2.1.13 ControlReg

Miscellaneous control bits.

Table 31. ControlReg register (address 0Ch); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TStopNow	TStartNow	WrNFCIDtoFIFO	Initiator	0	RxLastBits		
Access Rights	w	w	dy	r/w	RFU	r	r	r

Table 32. Description of ControlReg bits

Bit	Symbol	Description
7	TStopNow	Set to logic 1, the timer stops immediately. Reading this bit will always return 0.
6	TStartNow	Set to logic 1 starts the timer immediately. Reading this bit will always return 0.
5	WrNFCIDtoFIFO	Set to logic 1, the internal stored NFCID (10 bytes) is copied into the FIFO. Afterwards the bit is cleared automatically
4	Initiator	Set to logic 1, the PN512 acts as initiator, otherwise it acts as target
3	-	Reserved for future use.
2 to 0	RxLastBits	Shows the number of valid bits in the last received byte. If zero, the whole byte is valid.

8.2.1.14 BitFramingReg

Adjustments for bit oriented frames.

Table 33. BitFramingReg register (address 0Dh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	StartSend		RxAlign		0		TxLastBits	
Access Rights	w	r/w	r/w	r/w	RFU	r/w	r/w	r/w

Table 34. Description of BitFramingReg bits

Bit	Symbol	Description
7	StartSend	Set to logic 1, the transmission of data starts. This bit is only valid in combination with the Transceive command.
6 to 4	RxAlign	Used for reception of bit oriented frames: RxAlign defines the bit position for the first bit received to be stored in the FIFO. Further received bits are stored at the following bit positions. Example: RxAlign = 0: the LSB of the received bit is stored at bit 0, the second received bit is stored at bit position 1. RxAlign = 1: the LSB of the received bit is stored at bit 1, the second received bit is stored at bit position 2. RxAlign = 7: the LSB of the received bit is stored at bit 7, the second received bit is stored in the following byte at bit position 0. This bit shall only be used for bitwise anticollision at 106 kbit/s in Passive Communication mode. In all other modes it shall be set to logic 0.
3	-	Reserved for future use.
2 to 0	TxLastBits	Used for transmission of bit oriented frames: TxLastBits defines the number of bits of the last byte that shall be transmitted. A 000 indicates that all bits of the last byte shall be transmitted.

8.2.1.15 CollReg

Defines the first bit collision detected on the RF interface.

Table 35. CollReg register (address 0Eh); reset value: XXh, 101XXXXXb

	7	6	5	4	3	2	1	0
	Values AfterColl	0	CollPos NotValid			CollPos		
Access Rights	r/w	RFU	r	r	r	r	r	r

Table 36. Description of CollReg bits

Bit	Symbol	Description
7	ValuesAfterColl	If this bit is set to logic 0, all receiving bits will be cleared after a collision. This bit shall only be used during bitwise anticollision at 106 kbit, otherwise it shall be set to logic 1.
6	-	Reserved for future use.
5	CollPosNotValid	Set to logic 1, if no Collision is detected or the Position of the Collision is out of the range of bits CollPos. This bit shall only be interpreted in Passive Communication mode at 106 kbit or ISO/IEC 14443A/MIFARE Reader/Writer mode.
4 to 0	CollPos	These bits show the bit position of the first detected collision in a received frame, only data bits are interpreted.
		Example: 00h indicates a bit collision in the 32th bit 01h indicates a bit collision in the 1st bit 08h indicates a bit collision in the 8th bit
		These bits shall only be interpreted in Passive Communication mode at 106 kbit or ISO/IEC 14443A/MIFARE Reader/Writer mode if bit CollPosNotValid is set to logic 0.

8.2.2 Page 1: Communication

8.2.2.1 PageReg

Selects the register page.

Table 37. PageReg register (address 10h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	UsePage Select	0	0	0	0	0	PageSelect	
Access Rights	r/w	RFU	RFU	RFU	RFU	RFU	r/w	r/w

Table 38. Description of PageReg bits

Bit	Symbol	Description
7	UsePage Select	Set to logic 1, the value of PageSelect is used as register address A5 and A4. The LSB-bits of the register address are defined by the address pins or the internal address latch, respectively. Set to logic 0, the whole content of the internal address latch defines the register address. The address pins are used as described in Section 10.1 “Automatic host controller interface type detection”.
6 to 2	-	Reserved for future use.
1 to 0	PageSelect	The value of PageSelect is used only, if UsePageSelect is set to logic 1. In this case it specifies the register page (which is A5 and A4 of the register address).

8.2.2.2 ModeReg

Defines general mode settings for transmitting and receiving.

Table 39. ModeReg register (address 11h); reset value: 3Bh, 00111011b

	7	6	5	4	3	2	1	0
	MSBFirst	Detect Sync	TxWaitRF	RxWaitRF	PolSigin	ModeDetOff	CRCPreset	
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 40. Description of ModeReg bits

Bit	Symbol	Description
7	MSBFirst	Set to logic 1, the CRC co-processor calculates the CRC with MSB first and the CRCResultMSB and the CRCResultLSB in the CRCResultReg register are bit reversed. Note: During RF communication this bit is ignored.
6	Detect Sync	If set to logic 1, the contactless UART waits for the value F0h before the receiver is activated and F0h is added as a Sync-byte for transmission. This bit is only valid for 106 kbit during NFCIP-1 data exchange protocol. In all other modes it shall be set to logic 0.
5	TxWaitRF	Set to logic 1 the transmitter in reader/writer or initiator mode for NFCIP-1 can only be started, if an RF field is generated.
4	RxWaitRF	Set to logic 1, the counter for RxWait starts only if an external RF field is detected in Target mode for NFCIP-1 or in Card Communication mode.
3	PolSigin	PolSigin defines the polarity of the SIGIN pin. Set to logic 1, the polarity of SIGIN pin is active high. Set to logic 0 the polarity of SIGIN pin is active low. Note: The internal envelope signal is coded active low. Note: Changing this bit will generate a SiginActIRq event.
2	ModeDetOff	Set to logic 1, the internal mode detector is switched off. Note: The mode detector is only active during the AutoColl command.
1 to 0	CRCPreset	Defines the preset value for the CRC co-processor for the command CalCRC. Note: During any communication, the preset values is selected automatically according to the definition in the bits RxMode and TxMode. **Value** **Description** 00 0000 01 6363 10 A671 11 FFFF

8.2.2.3 TxModeReg

Defines the data rate and framing during transmission.

Table 41. TxModeReg register (address 12h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TxCRCEn		TxSpeed		InvMod	TxMix	TxFraming	
Access Rights	r/w	dy	dy	dy	r/w	r/w	dy	dy

Table 42. Description of TxModeReg bits

Bit	Symbol	Description	
7	TxCRCEn	Set to logic 1, this bit enables the CRC generation during data transmission. Note: This bit shall only be set to logic 0 at 106 kbit.	
6 to 4	TxSpeed	Defines the bit rate while data transmission.	
		Value	**Description**
		000	106 kbit
		001	212 kbit
		010	424 kbit
		011	848 kbit
		100	1696 kbit
		101	3392 kbit
		110	Reserved
		111	Reserved
		Note: The bit coding for transfer speeds above 424 kbit is equivalent to the bit coding of Active Communication mode 424 kbit (Ecma 340).	
3	InvMod	Set to logic 1, the modulation for transmitting data is inverted.	
2	TxMix	Set to logic 1, the signal at pin SIGIN is mixed with the internal coder (see Section 11.6 “S^{2}C interface support”).	
1 to 0	TxFraming	Defines the framing used for data transmission.	
		Value	**Description**
		00	ISO/IEC 14443A/MIFARE and Passive Communication mode 106 kbit
		01	Active Communication mode
		10	FeliCa and Passive communication mode 212 and 424 kbit
		11	ISO/IEC 14443B

8.2.2.4 RxModeReg

Defines the data rate and framing during reception.

Table 43. RxModeReg register (address 13h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	RxCRCEn		RxSpeed		RxNoErr	RxMultiple	RxFraming	
Access Rights	r/w	dy	dy	dy	r/w	r/w	dy	dy

Table 44. Description of RxModeReg bits

Bit	Symbol	Description
7	RxCRCEn	Set to logic 1, this bit enables the CRC calculation during reception. Note: This bit shall only be set to logic 0 at 106 kbit.
6 to 4	RxSpeed	Defines the bit rate while data transmission. The PN512's analog part handles only transfer speeds up to 424 kbit internally, the digital UART handles the higher transfer speeds as well. **Value** – **Description** 000 – 106 kbit 001 – 212 kbit 010 – 424 kbit 011 – 848 kbit 100 – 1696 kbit 101 – 3392 kbit 110 – Reserved 111 – Reserved Note: The bit coding for transfer speeds above 424 kbit is equivalent to the bit coding of Active Communication mode 424 kbit (Ecma 340).
3	RxNoErr	If set to logic 1, a not valid received data stream (less than 4 bits received) will be ignored. The receiver will remain active.
2	RxMultiple	Set to logic 0, the receiver is deactivated after receiving a data frame. Set to logic 1, it is possible to receive more than one data frame. This bit is only valid for 212 and 424 kbit to handle the Polling command. Having set this bit, the receive and transceive commands will not terminate automatically. In this case the multiple receiving can only be deactivated by writing any command (except the Receive command) to the CommandReg register or by clearing the bit by the host controller. If set to logic 1, at the end of a received data stream an error byte is added to the FIFO. The error byte is a copy of the ErrorReg register.
1 to 0	RxFraming	Defines the expected framing for data reception. **Value** – **Description** 00 – ISO/IEC 14443A/MIFARE and Passive Communication mode 106 kbit 01 – Active Communication mode 10 – FeliCa and Passive Communication mode 212 and 424 kbit 11 – ISO/IEC 14443B

8.2.2.5 TxControlReg

Controls the logical behavior of the antenna driver pins Tx1 and Tx2.

Table 45. TxControlReg register (address 14h); reset value: 80h, 10000000b

	7	6	5	4	3	2	1	0
	InvTx2RFOn	InvTx1RFOn	InvTx2RFOff	InvTx1RFOff	Tx2CW	CheckRF	Tx2RFEn	Tx1RFEn
Access Rights	r/w	r/w	r/w	r/w	r/w	w	r/w	r/w

Table 46. Description of TxControlReg bits

Bit	Symbol	Description
7	InvTx2RFOn	Set to logic 1, the output signal at pin TX2 will be inverted, if driver TX2 is enabled.
6	InvTx1RFOn	Set to logic 1, the output signal at pin TX1 will be inverted, if driver TX1 is enabled.
5	InvTx2RFOff	Set to logic 1, the output signal at pin TX2 will be inverted, if driver TX2 is disabled.
4	InvTx1RFOff	Set to logic 1, the output signal at pin TX1 will be inverted, if driver TX1 is disabled.
3	Tx2CW	Set to logic 1, the output signal on pin TX2 will deliver continuously the un-modulated 13.56 MHz energy carrier. Set to logic 0, Tx2CW is enabled to modulate the 13.56 MHz energy carrier.
2	CheckRF	Set to logic 1, Tx2RFEn and Tx1RFEn can not be set if an external RF field is detected. Only valid when using in combination with bit Tx2RFEn or Tx1RFEn
1	Tx2RFEn	Set to logic 1, the output signal on pin TX2 will deliver the 13.56 MHz energy carrier modulated by the transmission data.
0	Tx1RFEn	Set to logic 1, the output signal on pin TX1 will deliver the 13.56 MHz energy carrier modulated by the transmission data.

8.2.2.6 TxAutoReg

Controls the settings of the antenna driver.

Table 47. TxAutoReg register (address 15h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	AutoRF OFF	Force100 ASK	Auto WakeUp	0	CAOn	InitialRF On	Tx2RFAut oEn	Tx1RFAuto En
Access Rights	r/w	r/w	r/w	RFU	r/w	r/w	r/w	r/w

Table 48. Description of TxAutoReg bits

Bit	Symbol	Description
7	AutoRFOFF	Set to logic 1, all active antenna drivers are switched off after the last data bit has been transmitted as defined in the NFCIP-1.
6	Force100ASK	Set to logic 1, Force100ASK forces a 100% ASK modulation independent of the setting in register ModGsPReg.
5	AutoWakeUp	Set to logic 1, the PN512 in soft Power-down mode will be started by the RF level detector.
4	-	Reserved for future use.
3	CAOn	Set to logic 1, the collision avoidance is activated and internally the value n is set in accordance to the NFCIP-1 Standard.
2	InitialRFOn	Set to logic 1, the initial RF collision avoidance is performed and the bit InitialRFOn is cleared automatically, if the RF is switched on. Note: The driver, which should be switched on, has to be enabled by bit Tx2RFAutoEn or bit Tx1RFAutoEn.
1	Tx2RFAutoEn	Set to logic 1, the driver Tx2 is switched on after the external RF field is switched off according to the time TADT. If the bits InitialRFOn and Tx2RFAutoEn are set to logic 1, Tx2 is switched on if no external RF field is detected during the time TIDT. Note: The times TADT and TIDT are defined in the NFC IP-1 standard (ISO/IEC 18092).
0	Tx1RFAutoEn	Set to logic 1, the driver Tx1 is switched on after the external RF field is switched off according to the time TADT. If the bit InitialRFOn and Tx1RFAutoEn are set to logic 1, Tx1 is switched on if no external RF field is detected during the time TIDT. Note: The times TADT and TIDT are defined in the NFC IP-1 standard (ISO/IEC 18092).

8.2.2.7 TxSelReg

Selects the sources for the analog part.

Table 49. TxSelReg register (address 16h); reset value: 10h, 00010000b

	7	6	5	4	3	2	1	0
	0	0	DriverSel			SigOutSel		
Access Rights	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table 50. Description of TxSelReg bits

Bit	Symbol	Description	
7 to 6	-	Reserved for future use.	
5 to 4	DriverSel	Selects the input of driver Tx1 and Tx2.	
		Value	**Description**
		00	Tristate
			Note: In soft power down the drivers are only in Tristate mode if DriverSel is set to Tristate mode.
		01	Modulation signal (envelope) from the internal coder
		10	Modulation signal (envelope) from SIGIN
		11	HIGH
			Note: The HIGH level depends on the setting of InvTx1RFOn/ InvTx1RFOff and InvTx2RFOn/InvTx2RFOff.

Table 50. Description of TxSelReg bits *…continued*

Bit	Symbol	Description	
3 to 0	SigOutSel	Selects the input for the SIGOUT Pin.	
		Value	**Description**
		0000	Tristate
		0001	Low
		0010	High
		0011	TestBus signal as defined by bit TestBusBitSel in register TestSel1Reg.
		0100	Modulation signal (envelope) from the internal coder
		0101	Serial data stream to be transmitted
		0110	Output signal of the receiver circuit (card modulation signal regenerated and delayed). This signal is used as data output signal for SAM interface connection using 3 lines. Note: To have a valid signal the PN512 has to be set to the receiving mode by either the Transceive or Receive command. The bit RxMultiple can be used to keep the PN512 in receiving mode. Note: Do not use this setting in MIFARE mode. Manchester coding as data collisions will not be transmitted on the SIGOUT line.
		0111	Serial data stream received. Note: Do not use this setting in MIFARE mode. Miller coding parameters as the bitlength can vary.
		1000-1011	FeliCa Sam modulation 1000 RX* 1001 TX 1010 Demodulator comparator output 1011 RFU Note: * To have a valid signal the PN512 has to be set to the receiving mode by either the Transceive or Receive command. The bit RxMultiple can be used to keep the PN512 in receiving mode.
		1100-1111	MIFARE Sam modulation 1100 RX* with RF carrier 1101 TX with RF carrier 1110 RX with RF carrier un-filtered 1111 RX envelope un-filtered Note: *To have a valid signal the PN512 has to be set to the receiving mode by either the Transceive or Receive command. The bit RxMultiple can be used to keep the PN512 in receiving mode.

8.2.2.8 RxSelReg

Selects internal receiver settings.

Table 51. RxSelReg register (address 17h); reset value: 84h, 10000100b

	7	6	5	4	3	2	1	0
	UartSel				RxWait			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 52. Description of RxSelReg bits

Bit	Symbol	Description	
7 to 6	UartSel	Selects the input of the contactless UART	
		Value	**Description**
		00	Constant Low
		01	Envelope signal at SIGIN
		10	Modulation signal from the internal analog part
		11	Modulation signal from SIGIN pin. Only valid for transfer speeds above 424 kbit
5 to 0	RxWait	After data transmission, the activation of the receiver is delayed for RxWait bit-clocks. During this 'frame guard time' any signal at pin RX is ignored. This parameter is ignored by the Receive command. All other commands (e.g. Transceive, Autocoll, MFAuthent) use this parameter. Depending on the mode of the PN512, the counter starts different. In Passive Communication mode the counter starts with the last modulation pulse of the transmitted data stream. In Active Communication mode the counter starts immediately after the external RF field is switched on.	

8.2.2.9 RxThresholdReg

Selects thresholds for the bit decoder.

Table 53. RxThresholdReg register (address 18h); reset value: 84h, 10000100b

	7	6	5	4	3	2	1	0
	MinLevel				0	CollLevel		
Access Rights	r/w	r/w	r/w	r/w	RFU	r/w	r/w	r/w

Table 54. Description of RxThresholdReg bits

Bit	Symbol	Description
7 to 4	MinLevel	Defines the minimum signal strength at the decoder input that shall be accepted. If the signal strength is below this level, it is not evaluated.
3	-	Reserved for future use.
2 to 0	CollLevel	Defines the minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester-coded signal to generate a bit-collision relatively to the amplitude of the stronger half-bit.

8.2.2.10 DemodReg

Defines demodulator settings.

Table 55. DemodReg register (address 19h); reset value: 4Dh, 01001101b

	7	6	5	4	3	2	1	0
	AddIQ		FixIQ	0	TauRcv		TauSync	
Access Rights	r/w	r/w	r/w	RFU	r/w	r/w	r/w	r/w

Table 56. Description of DemodReg bits

Bit	Symbol	Description
7 to 6	AddIQ	Defines the use of I and Q channel during reception Note: FixIQ has to be set to logic 0 to enable the following settings. **Value** **Description** 00 Select the stronger channel 01 Select the stronger and freeze the selected during communication 10 combines the I and Q channel 11 Reserved
4	FixIQ	If set to logic 1 and the bits of AddIQ are set to X0, the reception is fixed to I channel. If set to logic 1 and the bits of AddIQ are set to X1, the reception is fixed to Q channel.
4	-	Reserved for future use.
3 to 2	TauRcv	Changes the time constant of the internal PLL during data reception. Note: If set to 00, the PLL is frozen during data reception.
1 to 0	TauSync	Changes the time constant of the internal PLL during burst.

8.2.2.11 FelNFC1Reg

Defines the length of the FeliCa Sync bytes and the minimum length of the received packet.

Table 57. FelNFC1Reg register (address 1Ah); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	FelSyncLen				DataLenMin			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 58. Description of FelNFC1Reg bits

Bit	Symbol	Description	
7 to 6	FelSyncLen	Defines the length of the Sync bytes.	
		Value	**Sync- bytes in hex**
		00	B2 4D
		01	00 B2 4D
		10	00 00 B2 4D
		11	00 00 00 B2 4D
5 to 0	DataLenMin	These bits define the minimum length of the accepted packet length: DataLenMin*4 ≤ data packet length This parameter is ignored at 106 kbit if the bit DetectSync in register ModeReg is set to logic 0. If a received data packet is shorter than the defined DataLenMin value, the data packet will be ignored.	

8.2.2.12 FelNFC2Reg

Defines the maximum length of the received packet.

Table 59. FelNFC2Reg register (address1Bh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	WaitForSelected	ShortTimeSlot			DataLenMax			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 60. Description of FelNFC2Reg bits

Bit	Symbol	Description
7	WaitForSelected	Set to logic 1, the AutoColl command is only terminated automatically when: 1. A valid command has been received after performing a valid Select procedure according ISO/IEC 14443A. 2. A valid command has been received after performing a valid Polling procedure according to the FeliCa specification. Note: If this bit is set, no active communication is possible. Note: Setting this bit reduces the host controller interaction in case of a communication to another device in the same RF field during Passive Communication mode.
6	ShortTimeSlot	Defines the time slot length for Passive Communication mode at 424 kbit. Set to logic 1 a short time slot is used (half of the timeslot at 212 kbit). Set to logic 0 a long timeslot is used (equal to the timeslot for 212 kbit).
5 to 0	DataLenMax	These bits define the maximum length of the accepted packet length: DataLenMax*4 ≥ data packet length Note: If set to logic 0 the maximum data length is 256 bytes. This parameter is ignored at 106 kbit if the bit DetectSync in register ModeReg is set to logic 0. If a received packet is larger than the defined DataLenMax value, the packet will be ignored.

8.2.2.13 MifNFCReg

Defines ISO/IEC 14443A/MIFARE/NFC specific settings in target or Card Operating mode.

Table 61. MifNFCReg register (address 1Ch); reset value: 62h, 01100010b

	7	6	5	4	3	2	1	0
	SensMiller			TauMiller		MFHalted	TxWait	
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 62. Description of MifNFCReg bits

Bit	Symbol	Description
7 to 5	SensMiller	These bits define the sensitivity of the Miller decoder.
4 to 3	TauMiller	These bits define the time constant of the Miller decoder.
2	MFHalted	Set to logic 1, this bit indicates that the PN512 is set to HALT mode in Card Operation mode at 106 kbit. This bit is either set by the host controller or by the internal state machine and indicates that only the code 52h is accepted as a request command. This bit is cleared automatically by a RF reset.
1 to 0	TxWait	These bits define the additional response time for the target at 106 kbit in Passive Communication mode and during the AutoColl command. Per default 7 bits are added to the value of the register bit.

8.2.2.14 ManualRCVReg

Allows manual fine tuning of the internal receiver.

Remark: For standard applications it is not recommended to change this register settings.

Table 63. ManualRCVReg register (address 1Dh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	0	FastFilt MF_SO	Delay MF_SO	Parity Disable	LargeBW PLL	Manual HPCF	HPFC	
Access Rights	RFU	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 64. Description of ManualRCVReg bits

Bit	Symbol	Description
7	-	Reserved for future use.
6	FastFilt MF_SO	If this bit is set to logic 1, the internal filter for the Miller-Delay Circuit is set to Fast mode. Note: This bit should only set to logic 1, if Millerpulses of less than 400 ns Pulse length are expected. At 106 kBaud the typical value is 3 us.
5	Delay MF_SO	If this bit is set to logic 1, the Signal at SIGOUT-pin is delayed, so that in SAM mode the Signal at SIGIN must be 128/fc faster compared to the ISO/IEC 14443A, to reach the ISO/IEC 14443A restrictions on the RF-Field. Note: This delay shall only be activated for setting bits SigOutSel to (1110b) or (1111b) in register TxSelReg.
4	Parity Disable	If this bit is set to logic 1, the generation of the Parity bit for transmission and the Parity-Check for receiving is switched off. The received Parity bit is handled like a data bit.
3	LargeBWPLL	Set to logic 1, the bandwidth of the internal PLL used for clock recovery is extended.
2	ManualHPCF	Set to logic 0, the HPCF bits are ignored and the HPCF settings are adapted automatically to the receiving mode. Set to logic 1, values of HPCF are valid.
1 to 0	HPFC	Selects the High Pass Corner Frequency (HPCF) of the filter in the internal receiver chain 00 For signals with frequency spectrum down to 106 kHz. 01 For signals with frequency spectrum down to 212 kHz. 10 For signals with frequency spectrum down to 424 kHz. 11 For signals with frequency spectrum down to 848 kHz

8.2.2.15 TypeBReg

Table 65. TypeBReg register (address 1Eh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	RxSOF Req	RxEOF Req	0	EOFSO FWidth	NoTxSOF	NoTxEOF	TxEGT	
Access Rights	r/w	r/w	RFU	r/w	r/w	r/w	r/w	r/w

Table 66. Description of TypeBReg bits

Bit	Symbol	Description
7	RxSOFReq	If this bit is set to logic 1, the SOF is required. A datastream starting without SOF is ignored. If this bit is cleared, a datastream with and without SOF is accepted. The SOF will be removed and not written into the FIFO.
6	RxEOFReq	If this bit is set to logic 1, the EOF is required. A datastream ending without EOF will generate a Protocol-Error. If this bit is cleared, a datastream with and without EOF is accepted. The EOF will be removed and not written into the FIFO.
5	-	Reserved for future use.
4	EOFSOFWidth	If this bit is set to logic 1, the SOF and EOF will have the maximum length defined in ISO/IEC 14443B. If this bit is cleared, the SOF and EOF will have the minimum length defined in ISO/IEC 14443B.
3	NoTxSOF	If this bit is set to logic 1, the generation of the SOF is suppressed.
2	NoTxEOF	If this bit is set to logic 1, the generation of the EOF is suppressed.
1 to 0	TxEGT	These bits define the length of the EGT. Value Description 00 0 bit 01 1 bit 10 2 bits 11 3 bits

8.2.2.16 SerialSpeedReg

Selects the speed of the serial UART interface.

Table 67. SerialSpeedReg register (address 1Fh); reset value: EBh, 11101011b

	7	6	5	4	3	2	1	0
	BR_T0					BR_T1		
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 68. Description of SerialSpeedReg bits

Bit	Symbol	Description
7 to 5	BR_T0	Factor BR_T0 to adjust the transfer speed, for description see Section 10.3.2 “Selection of the transfer speeds”.
3 to 0	BR_T1	Factor BR_T1 to adjust the transfer speed, for description see Section 10.3.2 “Selection of the transfer speeds”.

8.2.3 Page 2: Configuration

8.2.3.1 PageReg

Selects the register page.

Table 69. PageReg register (address 20h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	UsePageSelect	0	0	0	0	0	PageSelect	
Access Rights	r/w	RFU	RFU	RFU	RFU	RFU	r/w	r/w

Table 70. Description of PageReg bits

Bit	Symbol	Description
7	UsePageSelect	Set to logic 1, the value of PageSelect is used as register address A5 and A4. The LSB-bits of the register address are defined by the address pins or the internal address latch, respectively. Set to logic 0, the whole content of the internal address latch defines the register address. The address pins are used as described in Section 10.1 “Automatic host controller interface type detection”.
6 to 2	-	Reserved for future use.
1 to 0	PageSelect	The value of PageSelect is used only if UsePageSelect is set to logic 1. In this case, it specifies the register page (which is A5 and A4of the register address).

8.2.3.2 CRCResultReg

Shows the actual MSB and LSB values of the CRC calculation.

Note: The CRC is split into two 8-bit register.

Note: Setting the bit MSBFirst in ModeReg register reverses the bit order, the byte order is not changed.

Table 71. CRCResultReg register (address 21h); reset value: FFh, 11111111b

	7	6	5	4	3	2	1	0
	CRCResultMSB							
Access Rights	r	r	r	r	r	r	r	r

Table 72. Description of CRCResultReg bits

Bit	Symbol	Description
7 to 0	CRCResultMSB	This register shows the actual value of the most significant byte of the CRCResultReg register. It is valid only if bit CRCReady in register Status1Reg is set to logic 1.

Table 73. CRCResultReg register (address 22h); reset value: FFh, 11111111b

	7	6	5	4	3	2	1	0
	CRCResultLSB							
Access Rights	r	r	r	r	r	r	r	r

Table 74. Description of CRCResultReg bits

Bit	Symbol	Description
7 to 0	CRCResultLSB	This register shows the actual value of the least significant byte of the CRCResult register. It is valid only if bit CRCReady in register Status1Reg is set to logic 1.

8.2.3.3 GsNOffReg

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2 when the driver is switched off.

Table 75. GsNOffReg register (address 23h); reset value: 88h, 10001000b

	7	6	5	4	3	2	1	0
	CWGsNOff				ModGsNOff			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 76. Description of GsNOffReg bits

Bit	Symbol	Description
7 to 4	CWGsNOff	The value of this register defines the conductance of the output N-driver during times of no modulation. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1. Note: The value of the register is only used if the driver is switched off. Otherwise the bit value CWGsNOn of register GsNOnReg is used. Note: This value is used for LoadModulation.
3 to 0	ModGsNOff	The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1. Note: The value of the register is only used if the driver is switched off. Otherwise the bit value ModGsNOn of register GsNOnReg is used Note: This value is used for LoadModulation.

8.2.3.4 ModWidthReg

Controls the modulation width settings.

Table 77. ModWidthReg register (address 24h); reset value: 26h, 00100110b

	7	6	5	4	3	2	1	0
	ModWidth							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 78. Description of ModWidthReg bits

Bit	Symbol	Description
7 to 0	ModWidth	These bits define the width of the Miller modulation as initiator in Active and Passive Communication mode as multiples of the carrier frequency (ModWidth +1/fc). The maximum value is half the bit period. Acting as a target in Passive Communication mode at 106 kbit or in Card Operating mode for ISO/IEC 14443A/MIFARE these bits are used to change the duty cycle of the subcarrier frequency. The resulting number of carrier periods are calculated according to the following formulas: LOW value: #clocksLOW=(ModWidth modulo 8)+1. HIGH value: #clocksHIGH=16-#clocksLOW.

8.2.3.5 TxBitPhaseReg

Adjust the bitphase at 106 kbit during transmission.

Table 79. TxBitPhaseReg register (address 25h); reset value: 87h, 10000111b

	7	6	5	4	3	2	1	0
	RcvClkChange	TxBitPhase						
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 80. Description of TxBitPhaseReg bits

Bit	Symbol	Description
7	RcvClkChange	Set to logic 1, the demodulator's clock is derived by the external RF field.
6 to 0	TxBitPhase	These bits are representing the number of carrier frequency clock cycles, which are added to the waiting period before transmitting data in all communication modes. TXBitPhase is used to adjust the TX bit synchronization during passive NFCIP-1 communication mode at 106 kbit and in ISO/IEC 14443A/MIFARE card mode.

8.2.3.6 RFCfgReg

Configures the receiver gain and RF level detector sensitivity.

Table 81. RFCfgReg register (address 26h); reset value: 48h, 01001000b

	7	6	5	4	3	2	1	0
	RFLevelAmp		RxGain				RFLevel	
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 82. Description of RFCfgReg bits

Bit	Symbol	Description	
7	RFLevelAmp	Set to logic 1, this bit activates the RF level detectors' amplifier.	
6 to 4	RxGain	This register defines the receivers signal voltage gain factor:	
		Value	**Description**
		000	18 dB
		001	23 dB
		010	18 dB
		011	23 dB
		100	33 dB
		101	38 dB
		110	43 dB
		111	48 dB
3 to 0	RFLevel	Defines the sensitivity of the RF level detector, for description see Section 11.3 "RF level detector".	

8.2.3.7 GsNOnReg

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2 when the driver is switched on.

Table 83. GsNOnReg register (address 27h); reset value: 88h, 10001000b

	7	6	5	4	3	2	1	0
	CWGsNOn				ModGsNOn			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 84. Description of GsNOnReg bits

Bit	Symbol	Description
7 to 4	CWGsNOn	The value of this register defines the conductance of the output N-driver during times of no modulation. This may be used to regulate the output power and subsequently current consumption and operating distance. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1. Note: This value is only used if the driver TX1 or TX2 are switched on. Otherwise the value of the bits CWGsNOff of register GsNOffReg is used.
3 to 0	ModGsNOn	The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1. Note: This value is only used if the driver TX1 or Tx2 are switched on. Otherwise the value of the bits ModsNOff of register GsNOffReg is used.

8.2.3.8 CWGsPReg

Defines the conductance of the P-driver during times of no modulation

Table 85. CWGsPReg register (address 28h); reset value: 20h, 00100000b

	7	6	5	4	3	2	1	0
	0	0	CWGsP					
Access Rights	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table 86. Description of CWGsPReg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5 to 0	CWGsP	The value of this register defines the conductance of the output P-driver. This may be used to regulate the output power and subsequently current consumption and operating distance. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1.

8.2.3.9 ModGsPReg

Defines the driver P-output conductance during modulation.

Table 87. ModGsPReg register (address 29h); reset value: 20h, 00100000b

	7	6	5	4	3	2	1	0
	0	0	ModGsP					
Access Rights	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table 88. Description of ModGsPReg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5 to 0	ModGsP [1]	The value of this register defines the conductance of the output P-driver for the time of modulation. This may be used to regulate the modulation index. Note: The conductance value is binary weighted. Note: During soft Power-down mode the highest bit is forced to 1.

[1] If Force100ASK is set to logic 1, the value of ModGsP has no effect.

8.2.3.10 TMode Register, TPrescaler Register

Defines settings for the timer.

Note: The Prescaler value is split into two 8-bit registers

Table 89. TModeReg register (address 2Ah); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TAuto	TGated		TAutoRestart	TPrescaler_Hi			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 90. Description of TModeReg bits

Bit	Symbol	Description
7	TAuto	Set to logic 1, the timer starts automatically at the end of the transmission in all communication modes at all speeds or when bit InitialRFOn is set to logic 1 and the RF field is switched on. In mode MIFARE and ISO14443-B 106kbit/s the timer stops after the 5th bit (1 startbit, 4 databits) if the bit RxMultiple in the register RxModeReg is not set. In all other modes, the timer stops after the 4th bit if the bit RxMultiple the register RxModeReg is not set. If RxMultiple is set to logic 1, the timer never stops. In this case the timer can be stopped by setting the bit TStopNow in register ControlReg to 1. Set to logic 0 indicates, that the timer is not influenced by the protocol.

Table 90. Description of TModeReg bits *...continued*

Bit	Symbol	Description
6 to 5	TGated	The internal timer is running in gated mode. Note: In the gated mode, the bit TRunning is 1 when the timer is enabled by the register bits. This bit does not influence the gating signal.
		Value **Description** 00 Non gated mode 01 Gated by SIGIN 10 Gated by AUX1 11 Gated by A3
4	TAutoRestart	Set to logic 1, the timer automatically restart its count-down from TReloadValue, instead of counting down to zero. Set to logic 0 the timer decrements to ZERO and the bit TimerIRq is set to logic 1.
3 to 0	TPrescaler_Hi	Defines higher 4 bits for TPrescaler. The following formula is used to calculate f_{Timer}: f_{Timer} = 13.56 MHz/(2*TPreScaler+1). Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) For detailed description see Section 13 “Timer unit”.

Table 91. TPrescalerReg register (address 2Bh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TPrescaler_Lo							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 92. Description of TPrescalerReg bits

Bit	Symbol	Description
7 to 0	TPrescaler_Lo	Defines lower 8 bits for TPrescaler. The following formula is used to calculate f_{Timer}: f_{Timer} = 13.56 MHz/(2*TPreScaler+1). Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) For detailed description see Section 13 “Timer unit”.

8.2.3.11 TReloadReg

Describes the 16-bit long timer reload value.

Note: The Reload value is split into two 8-bit registers.

Table 93. TReloadReg (Higher bits) register (address 2Ch); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TReloadVal_Hi							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 94. Description of the higher TReloadReg bits

Bit	Symbol	Description
7 to 0	TReloadVal_Hi	Defines the higher 8 bits for the TReloadReg. With a start event the timer loads the TReloadVal. Changing this register affects the timer only at the next start event.

Table 95. TReloadReg (Lower bits) register (address 2Dh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TReloadVal_Lo							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 96. Description of lower TReloadReg bits

Bit	Symbol	Description
7 to 0	TReloadVal_Lo	Defines the lower 8 bits for the TReloadReg. With a start event the timer loads the TReloadVal. Changing this register affects the timer only at the next start event.

8.2.3.12 TCounterValReg

Contains the current value of the timer.

Note: The Counter value is split into two 8-bit register.

Table 97. TCounterValReg (Higher bits) register (address 2Eh); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	TCounterVal_Hi							
Access Rights	r	r	r	r	r	r	r	r

Table 98. Description of the higher TCounterValReg bits

Bit	Symbol	Description
7 to 0	TCounterVal_Hi	Current value of the timer, higher 8 bits.

Table 99. TCounterValReg (Lower bits) register (address 2Fh); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	TCounterVal_Lo							
Access Rights	r	r	r	r	r	r	r	r

Table 100. Description of lower TCounterValReg bits

Bit	Symbol	Description
7 to 0	TCounterVal_Lo	Current value of the timer, lower 8 bits.

8.2.4 Page 3: Test

8.2.4.1 PageReg

Selects the register page.

Table 101. PageReg register (address 30h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	UsePageSelect	0	0	0	0	0	PageSelect	
Access Rights	r/w	RFU	RFU	RFU	RFU	RFU	r/w	r/w

Table 102. Description of PageReg bits

Bit	Symbol	Description
7	UsePageSelect	Set to logic 1, the value of PageSelect is used as register address A5 and A4. The LSB-bits of the register address are defined by the address pins or the internal address latch, respectively. Set to logic 0, the whole content of the internal address latch defines the register address. The address pins are used as described in Section 10.1 “Automatic host controller interface type detection”.
6 to 2	-	Reserved for future use.
1 to 0	PageSelect	The value of PageSelect is used only if UsePageSelect is set to logic 1. In this case, it specifies the register page (which is A5 and A4 of the register address).

8.2.4.2 TestSel1Reg

General test signal configuration.

Table 103. TestSel1Reg register (address 31h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	-	-	SAMClockSel		SAMClkD1		TstBusBitSel	
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 104. Description of TestSel1Reg bits

Bit	Symbol	Description	
7 to 6	-	Reserved for future use.	
5 to 4	SAMClockSel	Defines the source for the 13.56 MHz SAM clock	
		Value	**Description**
		00	GND- Sam Clock switched off
		01	clock derived by the internal oscillator
		10	internal UART clock
		11	clock derived by the RF field
3	SAMClkD1	Set to logic 1, the SAM clock is delivered to D1. Note: Only possible if the 8bit parallel interface is not used.	
2 to 0	TstBusBitSel	Select the TestBus bit from the testbus to be propagated to SIGOUT.	

8.2.4.3 TestSel2Reg

General test signal configuration and PRBS control

Table 105. TestSel2Reg register (address 32h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	TstBusFlip	PRBS9	PRBS15			TestBusSel		
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 106. Description of TestSel2Reg bits

Bit	Symbol	Description
7	TstBusFlip	If set to logic 1, the testbus is mapped to the parallel port by the following order: D4, D3, D2, D6, D5, D0, D1. See Section 19 “Testsignals”.
6	PRBS9	Starts and enables the PRBS9 sequence according ITU-TO150. Note: All relevant registers to transmit data have to be configured before entering PRBS9 mode. Note: The data transmission of the defined sequence is started by the send command.
5	PRBS15	Starts and enables the PRBS15 sequence according ITU-TO150. Note: All relevant registers to transmit data have to be configured before entering PRBS15 mode. Note: The data transmission of the defined sequence is started by the send command.
4 to 0	TestBusSel	Selects the testbus. See Section 19 “Testsignals”

8.2.4.4 TestPinEnReg

Enables the pin output driver on the 8-bit parallel bus.

Table 107. TestPinEnReg register (address 33h); reset value: 80h, 10000000b

	7	6	5	4	3	2	1	0
	RS232LineEn				TestPinEn			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 108. Description of TestPinEnReg bits

Bit	Symbol	Description
7	RS232LineEn	Set to logic 0, the lines MX and DTRQ for the serial UART are disabled.
6 to 0	TestPinEn	Enables the pin output driver on the 8-bit parallel interface. **Example:** Setting bit 0 to 1 enables D0 Setting bit 5 to 1 enables D5 Note: Only valid if one of serial interfaces is used. If the SPI interface is used only D0 to D4 can be used. If the serial UART interface is used and RS232LineEn is set to logic 1 only D0 to D4 can be used.

8.2.4.5 TestPinValueReg

Defines the values for the 7-bit parallel port when it is used as I/O.

Table 109. TestPinValueReg register (address 34h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	UseIO				TestPinValue			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 110. Description of TestPinValueReg bits

Bit	Symbol	Description
7	UseIO	Set to logic 1, this bit enables the I/O functionality for the 7-bit parallel port in case one of the serial interfaces is used. The input /output behavior is defined by TestPinEn in register TestPinEnReg. The value for the output behavior is defined in the bits TestPinVal. Note: If SAMClkD1 is set to logic 1, D1 can not be used as I/O.
6 to 0	TestPinValue	Defines the value of the 7-bit parallel port, when it is used as I/O. Each output has to be enabled by the TestPinEn bits in register TestPinEnReg. Note: Reading the register indicates the actual status of the pins D6 - D0 if UseIO is set to logic 1. If UseIO is set to logic 0, the value of the register TestPinValueReg is read back.

8.2.4.6 TestBusReg

Shows the status of the internal testbus.

Table 111. TestBusReg register (address 35h); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	TestBus							
Access Rights	r	r	r	r	r	r	r	r

Table 112. Description of TestBusReg bits

Bit	Symbol	Description
7 to 0	TestBus	Shows the status of the internal testbus. The testbus is selected by the register TestSel2Reg. See Section 19 “Testsignals”.

8.2.4.7 AutoTestReg

Controls the digital selftest.

Table 113. AutoTestReg register (address 36h); reset value: 40h, 01000000b

	7	6	5	4	3	2	1	0
	0	AmpRcv	0	0	SelfTest			
Access Rights	RFT	r/w	RFU	RFU	r/w	r/w	r/w	r/w

Table 114. Description of bits

Bit	Symbol	Description
7	-	Reserved for production tests.
6	AmpRcv	If set to logic 1, the internal signal processing in the receiver chain is performed non-linear. This increases the operating distance in communication modes at 106 kbit. Note: Due to the non linearity the effect of the bits MinLevel and CollLevel in the register RxThreshholdReg are as well non linear.
5 to 4	-	Reserved for future use.
3 to 0	SelfTest	Enables the digital self test. The selftest can be started by the selftest command in the command register. The selftest is enabled by 1001. Note: For default operation the selftest has to be disabled by 0000.

8.2.4.8 VersionReg

Shows the version.

Table 115. VersionReg register (address 37h); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	Version							
Access Rights	r	r	r	r	r	r	r	r

Table 116. Description of VersionReg bits

Bit	Symbol	Description
7 to 0	Version	80h indicates PN512 Version V1.0.

8.2.4.9 AnalogTestReg

Controls the pins AUX1 and AUX2

Table 117. AnalogTestReg register (address 38h); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	AnalogSelAux1					AnalogSelAux2		
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 118. Description of AnalogTestReg bits

Bit	Symbol	Description	
7 to 4	AnalogSelAux1	Controls the AUX pin.	
3 to 0	AnalogSelAux2	Note: All test signals are described in Section 19 “Testsignals”.	
		Value	**Description**
		0000	Tristate
		0001	Output of TestDAC1 (AUX1), output of TESTDAC2 (AUX2) Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0010	Testsignal Corr1 Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0011	Testsignal Corr2 Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0100	Testsignal MinLevel Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0101	Testsignal ADC channel I Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0110	Testsignal ADC channel Q Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0111	Testsignal ADC channel I combined with Q Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		1000	Testsignal for production test Note: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		1001	SAM clock (13.56 MHz)
		1010	HIGH
		1011	LOW
		1100	TxActive At 106 kbit: HIGH during Startbit, Data bit, Parity and CRC. At 212 and 424 kbit: High during Preamble, Sync, Data and CRC.
		1101	RxActive At 106 kbit: High during databit, Parity and CRC. At 212 and 424 kbit: High during data and CRC.
		1110	Subcarrier detected 106 kbit: not applicable 212 and 424 kbit: High during last part of Preamble, Sync data and CRC
		1111	TestBus-Bit as defined by the TstBusBitSel in register TestSel1Reg.

8.2.4.10 TestDAC1Reg

Defines the testvalues for TestDAC1.

Table 119. TestDAC1Reg register (address 39h); reset value: XXh, 00XXXXXXb

	7	6	5	4	3	2	1	0
	0	0	TestDAC1					
Access Rights	RFT	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table 120. Description of TestDAC1Reg bits

Bit	Symbol	Description
7	-	Reserved for production tests.
6	-	Reserved for future use.
5 to 0	TestDAC1	Defines the testvalue for TestDAC1. The output of the DAC1 can be switched to AUX1 by setting AnalogSelAux1 to 0001 in register AnalogTestReg.

8.2.4.11 TestDAC2Reg

Defines the testvalue for TestDAC2.

Table 121. TestDAC2Reg register (address 3Ah); reset value: XXh, 00XXXXXXb

	7	6	5	4	3	2	1	0
	0	0	TestDAC2					
Access Rights	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table 122. Description ofTestDAC2Reg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5 to 0	TestDAC2	Defines the testvalue for TestDAC2. The output of the DAC2 can be switched to AUX2 by setting AnalogSelAux2 to 0001 in register AnalogTestReg.

8.2.4.12 TestADCReg

Shows the actual value of ADC I and Q channel.

Table 123. TestADCReg register (address 3Bh); reset value: XXh, XXXXXXXXb

	7	6	5	4	3	2	1	0
	ADC_I				ADC_Q			
Access Rights								

Table 124. Description of TestADCReg bits

Bit	Symbol	Description
7 to 4	ADC_I	Shows the actual value of ADC I channel.
3 to 0	ADC_Q	Shows the actual value of ADC Q channel.

8.2.4.13 RFTReg

Table 125. RFTReg register (address 3Ch); reset value: FFh, 11111111b

	7	6	5	4	3	2	1	0
	1	1	1	1	1	1	1	1
Access Rights	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT

Table 126. Description of RFTReg bits

Bit	Symbol	Description
7 to 0	-	Reserved for production tests.

Table 127. RFTReg register (address 3Dh, 3Fh); reset value: 00h, 00000000b

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0
Access Rights	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT

Table 128. Description of RFTReg bits

Bit	Symbol	Description
7 to 0	-	Reserved for production tests.

Table 129. RFTReg register (address 3Eh); reset value: 03h, 00000011b

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	1	1
Access Rights	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT

Table 130. Description of RFTReg bits

Bit	Symbol	Description
7 to 0	-	Reserved for production tests.

9. Operating modes

PN512 transceiver IC supports the following operating modes:

- Reader/Writer mode supporting ISO/IEC 14443A/MIFARE and FeliCa scheme
- Card Operation mode supporting ISO/IEC 14443A/MIFARE and FeliCa scheme
- NFCIP-1 mode

The modes support different transfer speeds and modulation schemes. The following chapters will explain the different modes in detail.

Note: All indicated modulation indices and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

9.1 Reader/Writer mode

Generally 3 Reader/Writer modes are supported. The PN512 can act as a reader/writer for ISO/IEC 14443A/MIFARE, ISO/IEC 14443B or FeliCa cards.

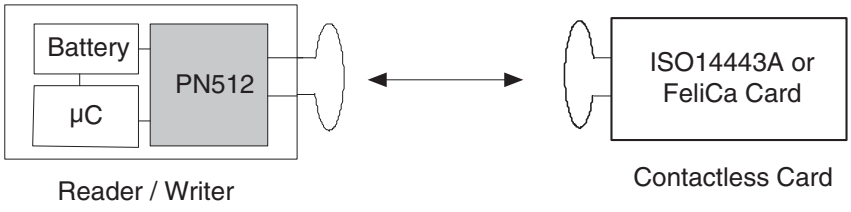


Fig 5. Reader/Writer mode

In the Reader/Writer mode the PN512 enables the communication to a contactless ISO/IEC 14443A/MIFARE, ISO/IEC 14443B or FeliCa card.

9.1.1 ISO/IEC 14443A/MIFARE reader/writer functionality

The ISO/IEC 14443A/MIFARE Reader/Writer mode is the general reader to card communication scheme according to the ISO/IEC 14443A/MIFARE specification. The following diagram describes the communication on a physical level, the communication table describes the physical parameters.

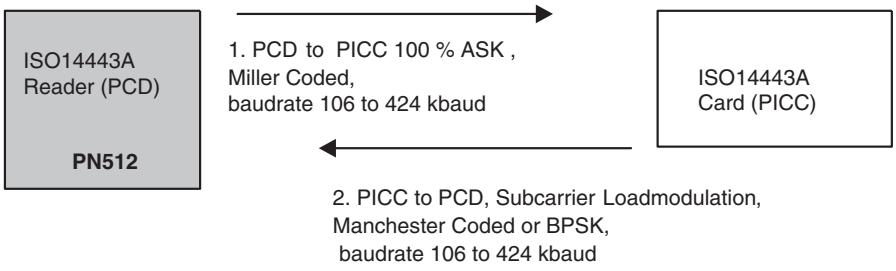


Fig 6. ISO/IEC 14443A/MIFARE Reader/Writer mode communication diagram

Table 131. Communication overview for ISO/IEC 14443A/MIFARE reader/writer

Communication direction		ISO/IEC 14443A/ MIFARE	MIFARE Higher transfer speeds	
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
PN512 → PICC (send data from the PN512 to a card)	Modulation on reader side	100% ASK	100% ASK	100% ASK
	bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
	Bitlength	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PICC → PN512 (receive data from a card)	modulation on card side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester coding	BPSK	BPSK

The contactless UART of PN512 and a dedicated external host controller are required to handle the complete MIFARE/ISO/IEC 14443A/MIFARE protocol.

9.1.1.1 Data coding and framing according to ISO/IEC 14443A/MIFARE

The internal CRC co-processor calculates the CRC value according to the definitions given in the ISO/IEC 14443A part 3 and handles parity generation internally according to the transfer speed.

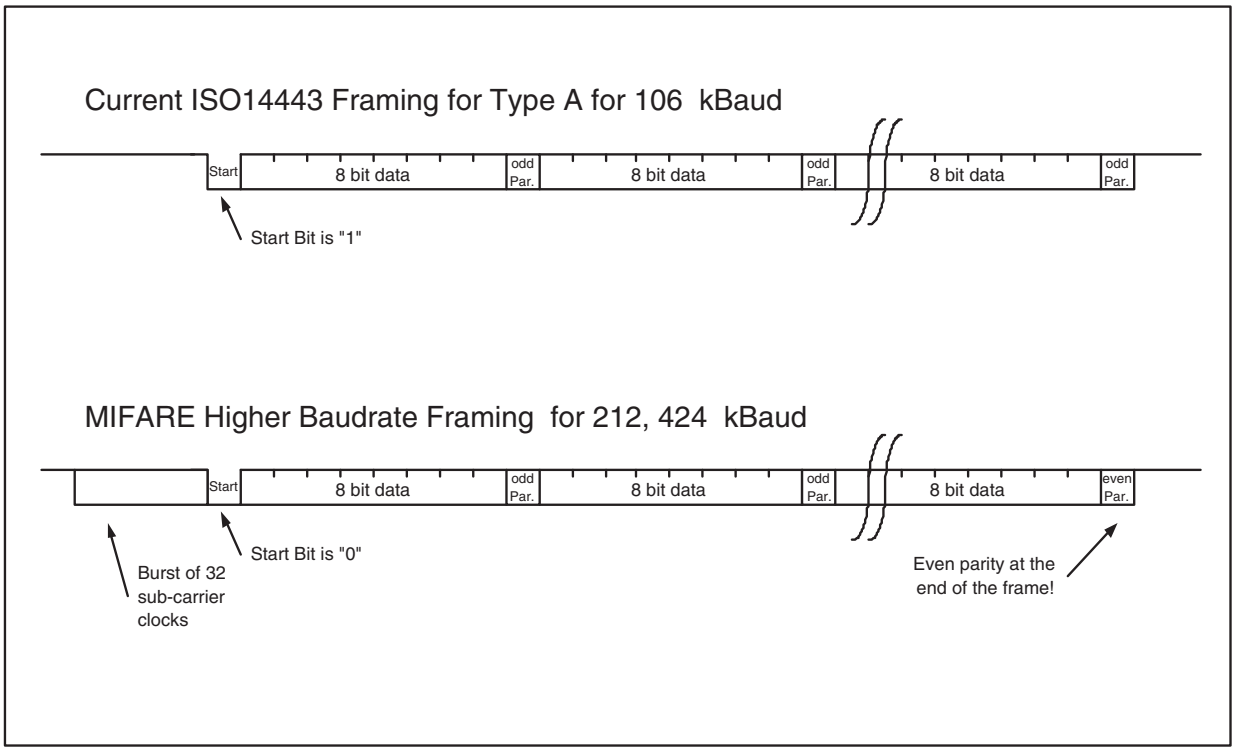


Fig 7. Data coding and framing according to ISO/IEC 14443A

9.1.2 FeliCa reader/writer functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The following diagram describes the communication on a physical level, the communication overview describes the physical parameters.

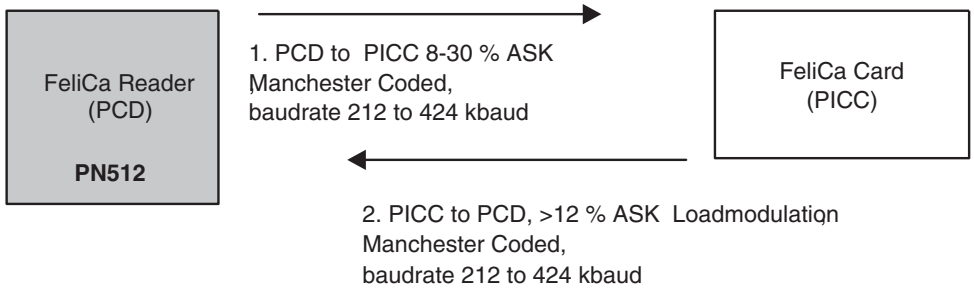


Fig 8. FeliCa reader/writer communication diagram

Table 132. Communication overview for FeliCa reader/writer

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
PN512 → card	Modulation on reader side	8-30% ASK	8-30% ASK
	bit coding	Manchester Coding	Manchester Coding
	Bitlength	(64/13.56) µs	(32/13.56) µs
card → PN512	Loadmodulation on card side	>12% ASK	>12% ASK
	bit coding	Manchester coding	Manchester coding

The contactless UART of PN512 and a dedicated external host controller are required to handle the complete FeliCa protocol.

9.1.2.1 FeliCa framing and coding

Table 133. FeliCa framing and coding

Preamble						Sync		Len	n-Data				CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh							

To enable the FeliCa communication a 6 byte preamble (00h, 00h, 00h, 00h, 00h, 00h) and 2 bytes Sync bytes (B2h, 4Dh) are sent to synchronize the receiver.

The following Len byte indicates the length of the sent data bytes plus the LEN byte itself. The CRC calculation is done according to the FeliCa definitions with the MSB first.

To transmit data on the RF interface, the host controller has to send the Len- and data-bytes to the PN512's FIFO-buffer. The preamble and the sync bytes are generated by the PN512 automatically and must not be written to the FIFO by the host controller. The PN512 performs internally the CRC calculation and adds the result to the data frame.

Example for FeliCa CRC Calculation:

Table 134. Start value for the CRC Polynomial: (00h), (00h)

Preamble						Sync		Len	2 Data Bytes		CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh	03h	ABh	CDh	90h	35h

9.1.3 ISO/IEC 14443B reader/writer functionality

The international standard ISO/IEC 14443 covers 2 communication schemes: the ISO/IEC 14443A and the ISO/IEC 14443B.

The PN512 reader IC fully supports the ISO/IEC 14443.

The following registers and bits cover the ISO/IEC 14443B communication scheme:

As a reference documentation the international standard ISO/IEC 14443 'Identification cards- Contactless integrated circuit(s) cards- Proximity cards, part 1-4' can be taken.

Note: NXP Semiconductors does not offer a software library to design in the ISO/IEC 14443B protocol.

9.2 NFCIP-1 mode

The NFCIP-1 communication differentiates between an active and a Passive Communication mode.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data.
- Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.
- Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

In order to fully support the NFCIP-1 standard the PN512 supports the Active and Passive Communication mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

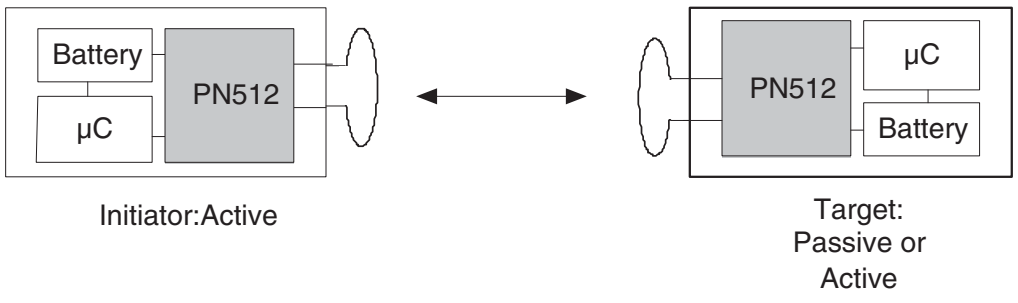


Fig 9. NFCIP-1 mode

9.2.1 Active communication mode

Active communication mode means both the initiator and the target are using their own RF field to transmit data.

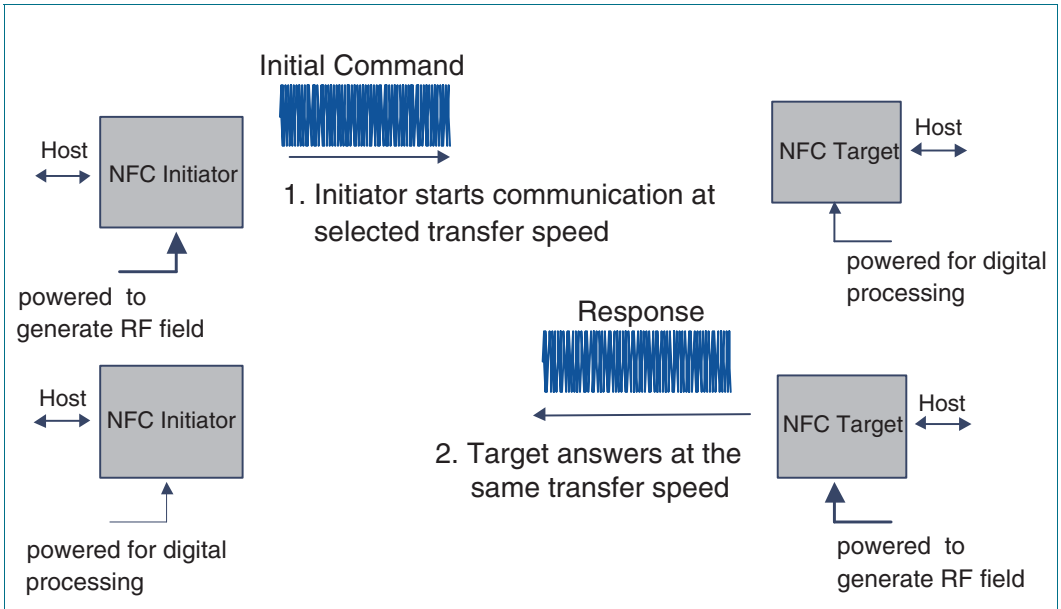


Fig 10. Active communication mode

Table 135. Communication overview for Active communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s	1.69 Mbit/s, 3.39 Mbit/s
Initiator → Target	According to ISO/IEC 14443A 100% ASK, Modified Miller Coded	According to FeliCa, 8-30% ASK Manchester Coded		digital capability to handle this communication	
Target → Initiator					

The contactless UART of PN512 and a dedicated host controller are required to handle the NFCIP-1 protocol.

Note: Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard. The PN512 supports these transfer speeds only with dedicated external circuits.

9.2.2 Passive communication mode

Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active meaning generating the RF field.

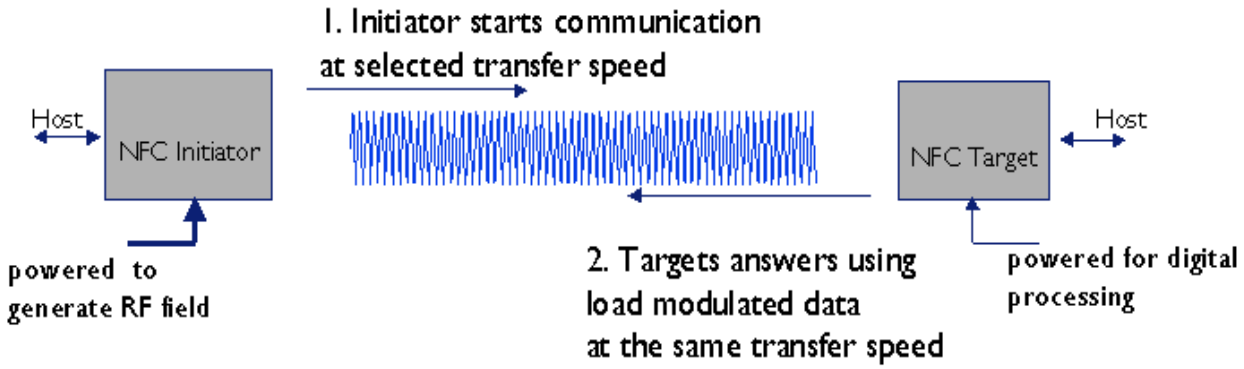


Fig 11. Passive communication mode

Table 136. Communication overview for Passive communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s	1.69 Mbit/s, 3.39 Mbit/s
Initiator → Target	According to ISO/IEC 14443A 100% ASK, Modified Miller Coded	According to FeliCa, 8-30% ASK Manchester Coded		digital capability to handle this communication	
Target → Initiator	According to ISO/IEC 14443A subcarrier load modulation, Manchester Coded	According to FeliCa, >12% ASK Manchester Coded			

The contactless UART of PN512 and a dedicated host controller are required to handle the NFCIP-1 protocol.

Note: Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard. The PN512 supports these transfer speeds only with dedicated external circuits.

9.2.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive Communication mode is defined in the NFCIP-1 standard.

Table 137. Framing and coding overview

Transfer speed	Framing and Coding
106 kbit/s	According to the ISO/IEC 14443A/MIFARE scheme
212 kbit/s	According to the FeliCa scheme
424 kbit/s	According to the FeliCa scheme

9.2.4 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol refer to the NFCIP-1 standard. However the datalink layer is according to the following policy:

- Speed shall not be changed while continuum data exchange in a transaction.
- Transaction includes initialization and anticollision methods and data exchange (in continuous way, meaning no interruption by another transaction).

In order not to disturb current infrastructure based on 13.56 MHz general rules to start NFCIP-1 communication are defined in the following way.

1. Per default NFCIP-1 device is in Target mode meaning its RF field is switched off.
2. The RF level detector is active.
3. Only if application requires the NFCIP-1 device shall switch to Initiator mode.
4. Initiator shall only switch on its RF field if no external RF field is detected by RF Level detector during a time of TIDT.
5. The initiator performs initialization according to the selected mode.

9.3 Card operation mode

The PN512 can be addressed like a FeliCa or ISO/IEC 14443A/MIFARE card. This means that the PN512 can generate an answer in a load modulation scheme according to the ISO/IEC 14443A/MIFARE or FeliCa interface description.

Note: The PN512 does not support a complete card protocol. This has to be handled by a dedicated card SAM or a host controller. The card-SAM is optional.

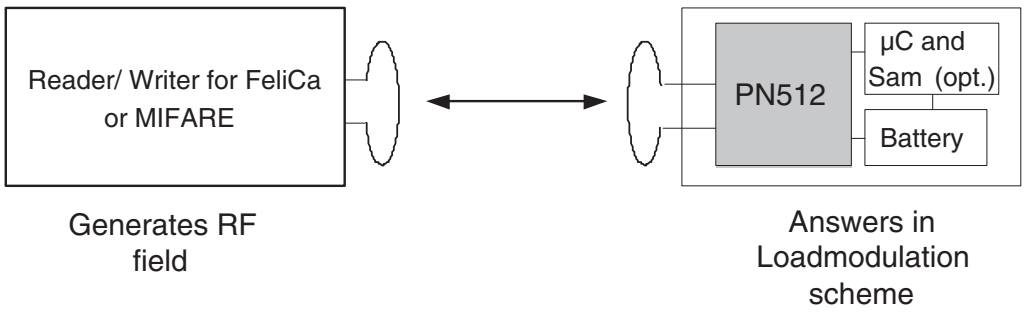


Fig 12. Card operation mode

9.3.1 MIFARE Card operation mode

Table 138. MIFARE Card operation mode

Communication direction		ISO/IEC 14443A/ MIFARE	MIFARE Higher transfer speeds	
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
reader / writer → PN512	Modulation on reader side	100% ASK	100% ASK	100% ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller
	Bitlength	(128/13.56) μs	(64/13.56) μs	(32/13.56) μs
PN512 → reader/ writer	Modulation on PN512 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester coding	BPSK	BPSK

9.3.2 FeliCa Card operation mode

FeliCa Card operation mode

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
reader/writer → PN512	Modulation on reader side	8-30% ASK	8-30% ASK
	bit coding	Manchester Coding	Manchester Coding
	Bitlength	(64/13.56) μs	(32/13.56) μs
PN512 → reader/ writer	Load modulation on PN512 side	>12% ASK load modulation	>12% ASK load modulation
	bit coding	Manchester coding	Manchester coding

10. Digital interfaces

10.1 Automatic host controller interface type detection

The PN512 supports direct interfacing of various host controllers as the 8-bit parallel, SPI, I^2C and serial UART interface type. The PN512 resets its interface and checks the current host controller interface type automatically having performed a Power-On or Hard Reset. The PN512 identifies the host controller interface by the means of the logic levels on the control pins after the Reset Phase. This is done by a combination of fixed pin connections. The following table shows the different configurations:

Table 139. Connection scheme for detecting the different interface types

PN512	Parallel Interface Type				Serial Interface Types		
	Separated Read/Write Strobe		Common Read/Write Strobe				
Pin	Dedicated Address Bus	Multiplexed Address Bus	Dedicated Address Bus	Multiplexed Address Bus	UART	SPI	I^2C
ALE	1	ALE	1	AS	RX	NSS	SDA
A5[1]	A5	0	A5	0	0	0	0
A4[1]	A4	0	A4	0	0	0	0
A3[2]	A3	0	A3	0	0	0	0
A2[2]	A2	1	A2	1	0	0	0
A1	A1	1	A1	1	0	0	1
A0	A0	1	A0	0	0	1	EA
NRD[2]	NRD	NRD	NDS	NDS	1	1	1
NWR[2]	NWR	NWR	RD/NWR	RD/NWR	1	1	1
NCS[2]	NCS	NCS	NCS	NCS	NCS	NCS	NCS
D7	D7	D7	D7	D7	TX	MISO	SCL
D6	D6	D6	D6	D6	MX	MOSI	ADR_0
D5	D5	AD5	D5	AD5	DTRQ	SCK	ADR_1
D4	D4	AD4	D4	AD4	-	-	ADR_2
D3	D3	AD3	D3	AD3	-	-	ADR_3
D2	D2	AD2	D2	AD2	-	-	ADR_4
D1	D1	AD1	D1	AD1	-	-	ADR_5
D0	D0	AD0	D0	AD0	-	-	ADR_6
Remark: Overview on the pin behavior							
Pin behavior	Input		Output	In/Out			

[1] only available in HVQFN 40.

[2] not available in HVQFN 32.

10.2 SPI compatible interface

A serial peripheral interface (SPI compatible) is supported to enable high speed communication to the host controller. In the communication with a host controller PN512 acts as a slave receiving data from the external host controller for register settings and to send and receive data relevant for the communication on the RF interface.

10.2.1 General

An interface compatible to an SPI interface enables a high-speed serial communication between the PN512 and a µ-Controller up to 5 Mbit in order to handle the requirements for the NFCIP-1 communication. The implemented SPI compatible interface is according to a standard SPI interface.

For timing specification refer to Section 24.8 “Timing for the SPI compatible interface”.

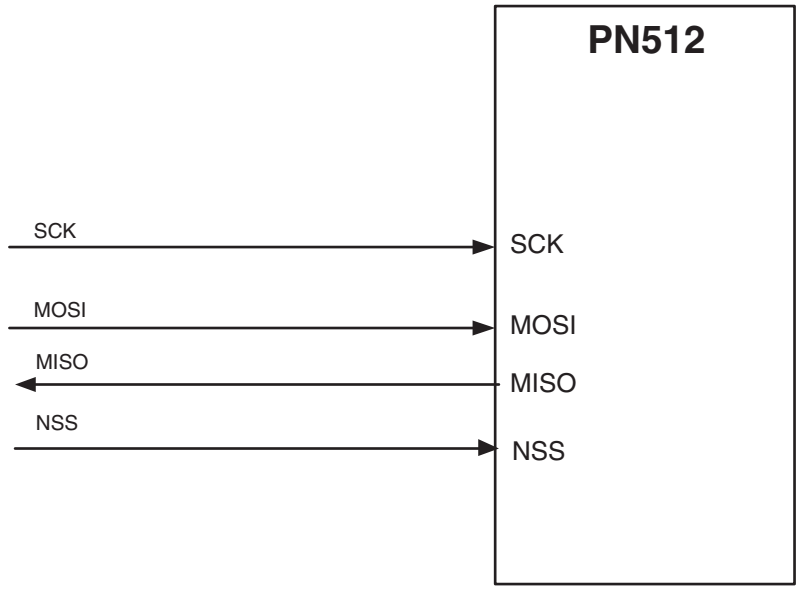


Fig 13. Connection to host controller with SPI

The PN512 acts as a slave during the SPI communication. The SPI clock SCK has to be generated by the master. Data communication from the master to the slave uses the Line MOSI. Line MISO is used to send data back from the PN512 to the master.

On both lines (MOSI, MISO) each data byte is sent by MSB first. Data on MOSI line should be stable on rising edge of the clock line and can changed on falling edge. The same is valid for the MISO line. Data is provided by the PN512 on falling edge and is stable during rising edge.

Read data:

To read out data using the SPI compatible interface the following byte order has to be used. It is possible to read out up to n-data bytes.

The first sent byte defines both, the mode itself and the address byte.

Table 140. Byte Order for MOSI and MISO

	byte 0	byte 1	byte 2	to	byte n	byte n+1
MOSI	adr 0	adr 1	adr 2	……..	adr n	00
MISO	X	data 0	data 1	……..	data n-1	data n

Remark: The most significant bit (MSB) has to be send first.

Write data:

To write data to the PN512 using the SPI interface the following byte order has to be used. It is possible to write out up to n-data bytes by only sending one's address byte.

The first send byte defines both, the mode itself and the address byte.

Note: The most significant bit (MSB) has to be send first.

Table 141. Byte order for MOSI and MISO

	byte 0	byte 1	byte 2	to	byte n	byte n+1
MOSI	adr	data 0	data 1	……..	data n-1	data n
MISO	X	X	X	……..	x	x

Address byte:

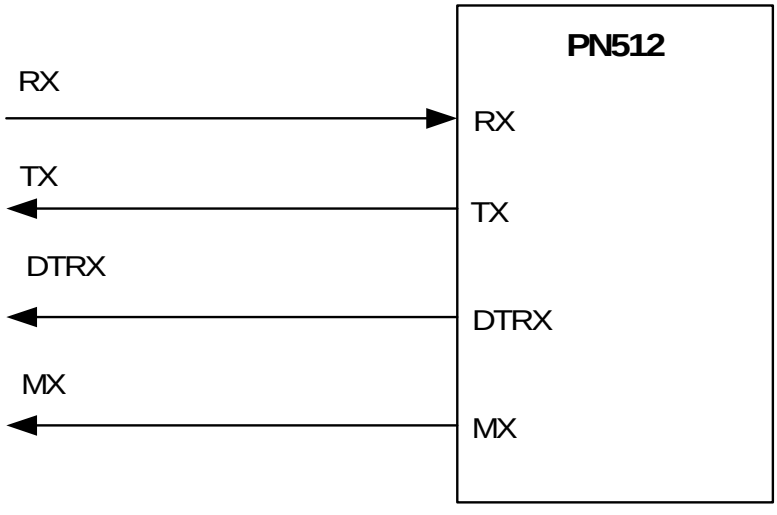
The address byte has to fulfill the following format. The MSB bit of the first byte defines the used mode. To read data from the PN512 the MSB bit is set to logic 1. To write data to the PN512 the MSB bit has to be set to logic 0. The bits 6 to 1 define the address and the last bit shall be set to logic 0.

Table 142. Address byte 0 register; address MOSI

7	6	5	4	3	2	1	0
1 (read) 0 (write)	address						RFU
MSB							LSB

10.3 UART interface

10.3.1 Connection to a host controller



Remark: DTRX and MX can be disabled by clearing the bit RS232LineEn in register TestPinEnReg.

Fig 14. Connection to host controller with UART

10.3.2 Selection of the transfer speeds

The internal UART interface is compatible to an RS232 serial interface.

Table 144 “Selectable transfer speeds” describes examples for different transfer speeds and relevant register settings.

The resulting transfer speed error is less than 1.5% for all described transfer speeds.

The default transfer speed is 9.6 kbit.

To change the transfer speed, the host controller has to write a value for the new transfer speed to the register SerialSpeedReg. The bits BR_T0 and BR_T1 define factors to set the transfer speed in the SerialSpeedReg.

Table 143 “Settings of BR_T0 and BR_T1” describes the settings of BR_T0 and BR_T1.

Table 143. Settings of BR_T0 and BR_T1

BR_T0	0	1	2	3	4	5	6	7
factor BR_T0	1	1	2	4	8	16	32	64
range BR_T1	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

Table 144. Selectable transfer speeds

Transfer Speed [bit/s]	SerialSpeedReg		Transfer Speed Accuracy
	decimal	heximal	
7.2 k	250	FA	-0.25%
9.6 k	235	EB	0.32%
14.4 k	218	DA	-0.25%
19.2 k	203	CB	0.32%
38.4 k	171	AB	0.32%
57.6 k	154	9A	-0.25%
115.2 k	122	7A	-0.25%
128 k	116	74	-0.06%
230.4 k	90	5A	-0.25%
460.8 k	58	3A	-0.25%
921.6 k	28	1C	1.45%
1228.8 k	21	15	0.32%

The selectable transfer speeds as shown in Table 144 “Selectable transfer speeds” are calculated according to the following formulas:

if BR_T0=0: transfer speed = 27.12 MHz/(BR_T1+1)

if BR_T0>0: transfer speed = 27.12 MHz/(BR_T1 +33)/2^(BR_T0 -1)

Remark: transfer speeds above 1228.8 k are not supported.

10.3.3 Framing

Table 145. UART Framing

	Length	Value
Start bit	1-bit	0
Data bits	8 bits	Data
Stop bit	1-bit	1

For data and address bytes the LSB bit has to be sent first.

Note: No parity bit is used during transmission.

Read data:

To read out data using the UART interface the flow described below has to be used. The first send byte defines both the mode itself and the address.

Table 146. Schematic diagram to read data

	byte 0	byte 1
RX	adr	
TX		data 0

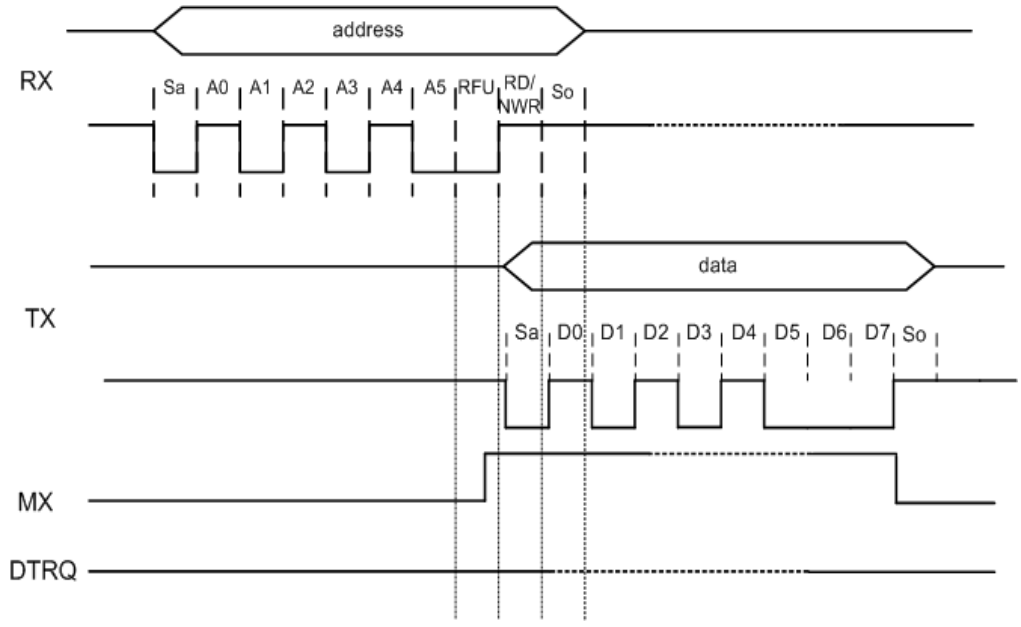


Fig 15. Schematic diagram to read data

Write data:

To write data to the PN512 using the UART interface the following structure has to be used.

The first send byte defines both, the mode itself and the address.

Table 147. Byte order to write data

	byte 0	byte 1
RX	adr 0	data 0
TX		adr 0

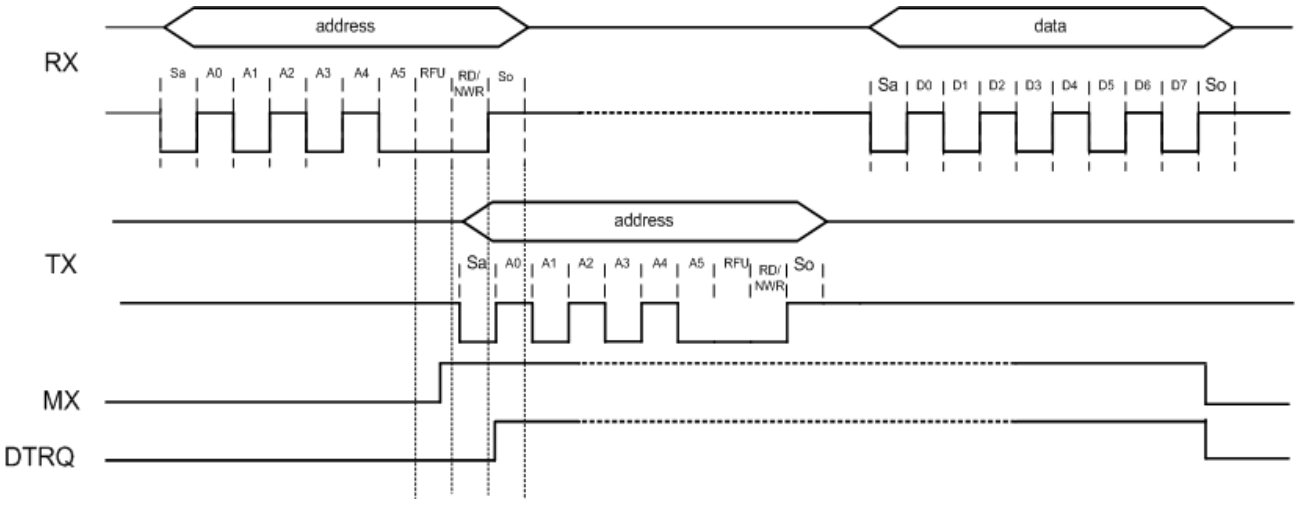


Fig 16. Schematic Diagram to Write Data

Remark: The data byte can be send directly after the address byte on RX.

Address byte:

The address byte has to fulfill the following format. The MSB of the first byte sets the used mode. To read data from the PN512 the MSB is set to logic 1. To write data to the PN512 the MSB has to be set to logic 0. The bit 6 is RFU and the bits 5 to 0 define the address.

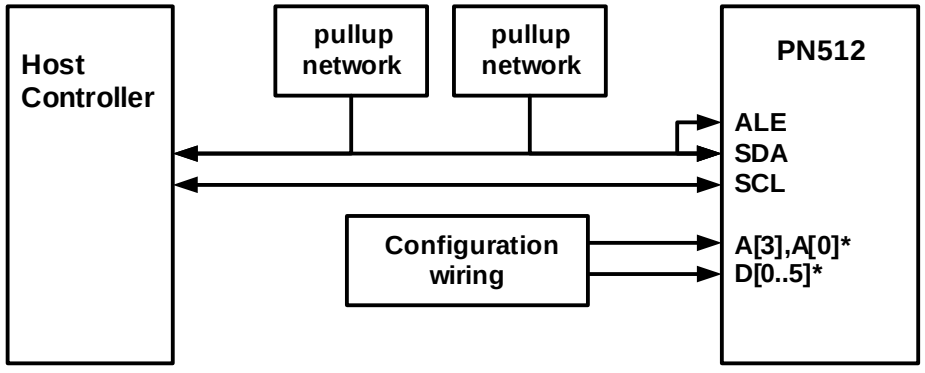
Table 148. Address byte 0 register; address MOSI

7	6	5	4	3	2	1	0
1 (read) 0 (write)	RFU	address					
MSB							LSB

10.4 I²C bus interface

An Inter IC (I²C) bus interface is supported to enable a low cost, low pin count serial bus interface to the host controller.

The implemented I²C interface is implemented according the NXP Semiconductors I²C interface specification, rev. 2.1, January 2000. The implemented interface can only act in Slave mode. Therefore no clock generation and access arbitration is implemented in the PN512.



Remark: *depending on the package type.

Fig 17. I²C interface

10.4.1 General

The implemented interface is conforming to the I²C-bus specification version 2.1, January 2000. The PN512 can act as a slave receiver or slave transmitter in standard, Fast mode and High-speed mode.

SDA is a bi-directional one, connected to a positive supply voltage via a current-source or a pull-up resistor. Both lines, SDA and SCL are set to HIGH level if no data is transmitted. The PN512 has a 3-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kbit in Standard mode, up to 400 kbit in the Fast mode or up to 3.4 Mbit in the High-speed mode.

If the I²C interface is selected, a spike suppression according to the I²C interface specification on SCL and SDA is activated.

For timing requirements refer to Section 24.9 “I²C timing”

10.4.2 Data validity

Data on the SDA line shall be stable during the HIGH period of the clock. The HIGH or LOW state of the data line shall only change when the clock signal on SCL is LOW.

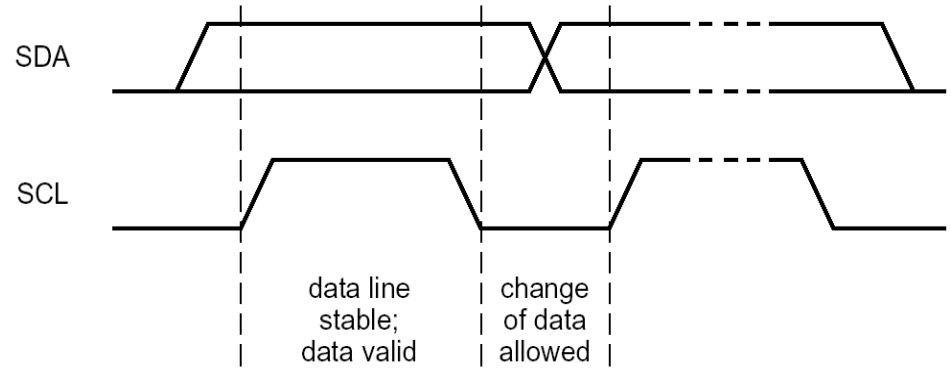


Fig 18. Bit transfer on the I²C-bus

10.4.3 START and STOP conditions

To handle the data transfer on the I²C-bus, unique START (S) and STOP (P) conditions are defined.

A START condition is defined with a HIGH to LOW transition on the SDA line while SCL is HIGH.

A STOP condition is defined with a LOW to HIGH transition on the SDA line while SCL is HIGH.

The master always generates the START and STOP conditions. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical.

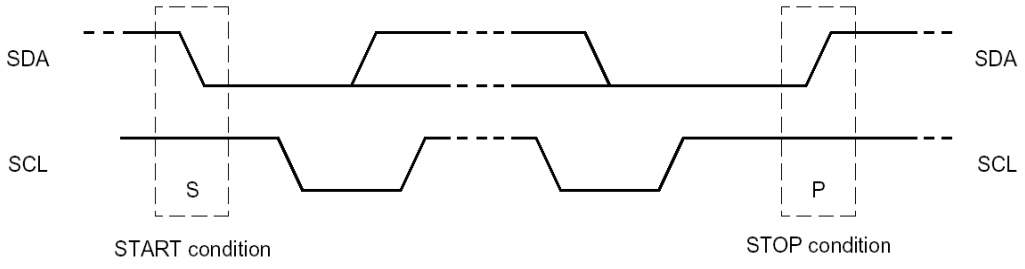


Fig 19. START and STOP conditions

10.4.4 Byte format

Each byte has to be followed by an acknowledge bit. Data is transferred with the MSB first, see Figure 22. The number of transmitted bytes during one data transfer is unrestricted but shall fulfill the read/write cycle format.

10.4.5 Acknowledge

An acknowledge at the end of one data byte is mandatory. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver shall pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer, or a repeated START (Sr) condition to start a new transfer.

A master-receiver shall indicate the end of data to the slave- transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter shall release the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

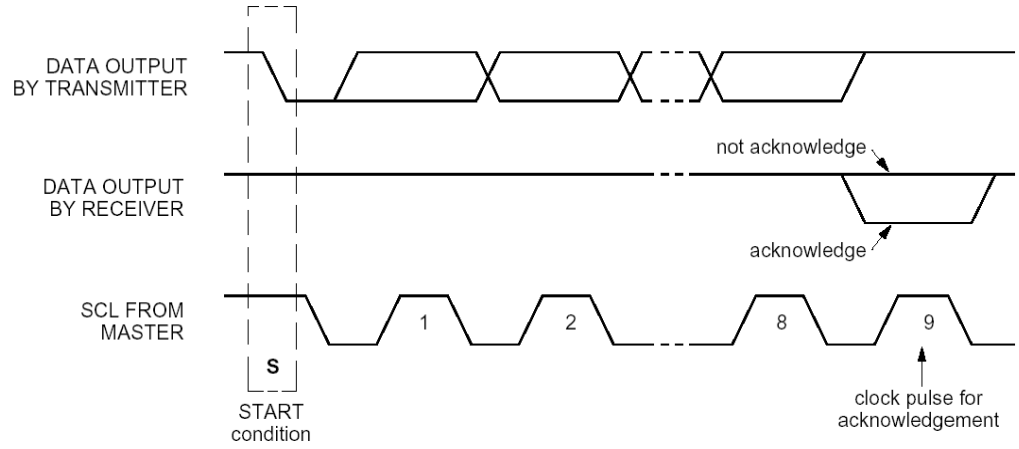


Fig 20. Acknowledge on the I²C- bus

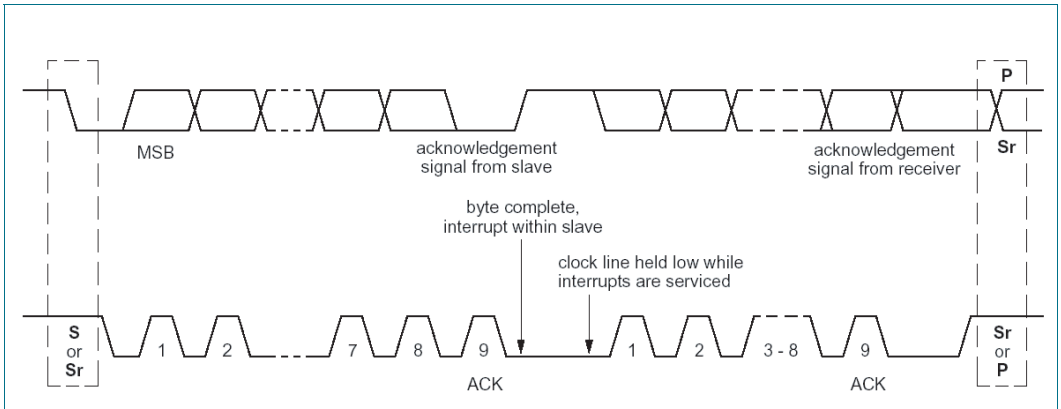


Fig 21. Data transfer on the I²C-bus

10.4.6 7-bit addressing

During the I²C-bus addressing procedure the first byte after the START condition is used to determine which slave will be selected by the master.

During device configuration, the designer has to ensure, that no collision with these reserved addresses is possible. Check the corresponding I²C specification for a complete list of reserved addresses.

For all PN512devices the upper 4 bits of the device bus address are reserved by NXP and set to 0101(bin). The remaining 3 bits of the Slave Address can be freely configured in order to prevent collisions with other I²C devices used.

Immediately after releasing the reset pin or after power on reset, the device defines the I²C address according EA (pin A0). In case of a LOW at EA, the NXP reserved address is taken for the upper 4 bits of the address. The lower 3 bits of the address are determined by the logic levels on the pins D6 to D4. In case of a HIGH at EA, the address can be completely specified at the external pins according to Table 139 “Connection scheme for detecting the different interface types”. In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins D6-D4 are not taken into consideration. Depending on the external wiring, the I²C address pins could be used for the output of test signals.

Remark: The PN512 in HVQFN32 package does not have a D0. In case of EA set to HIGH, the I²C address bit 6 is fixed to 0.

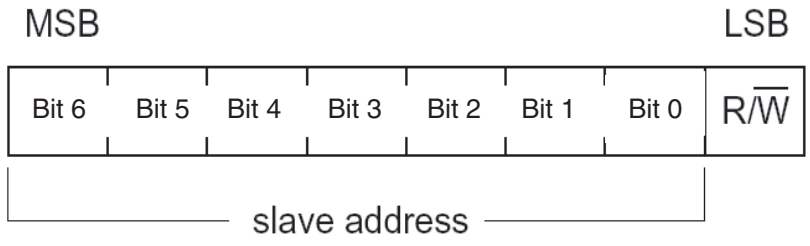


Fig 22. First byte following the START procedure

10.4.7 Register write access

To write data from the host controller via I²C to a specific register of the PN512 the following frame format shall be used.

The first byte of a frame indicates the device address according to the I²C rules. The second byte indicates the register address followed by up to n-data bytes. In one frame all n-data bytes are written to the same register address. This enables for example a fast FIFO access.

The read/write bit shall be set to logic 0.

10.4.8 Register read access

To read out data from a specific register address of the PN512 the host controller shall use the procedure:

First a write access to the specific register address has to be performed as indicated in the following frame.

The first byte of a frame indicates the device address according to the I^2C rules. The second byte indicates the register address. No data bytes are added.

The read/write bit shall be 0.

Having performed this write access, the read access can start. The host controller has to send the device address of the PN512. As an answer to this the PN512 responds with the content of this register. In one frame all n-data bytes could be read from the same register address. This enables for example a fast FIFO access or register polling.

The read/write bit shall be set to logic 1.

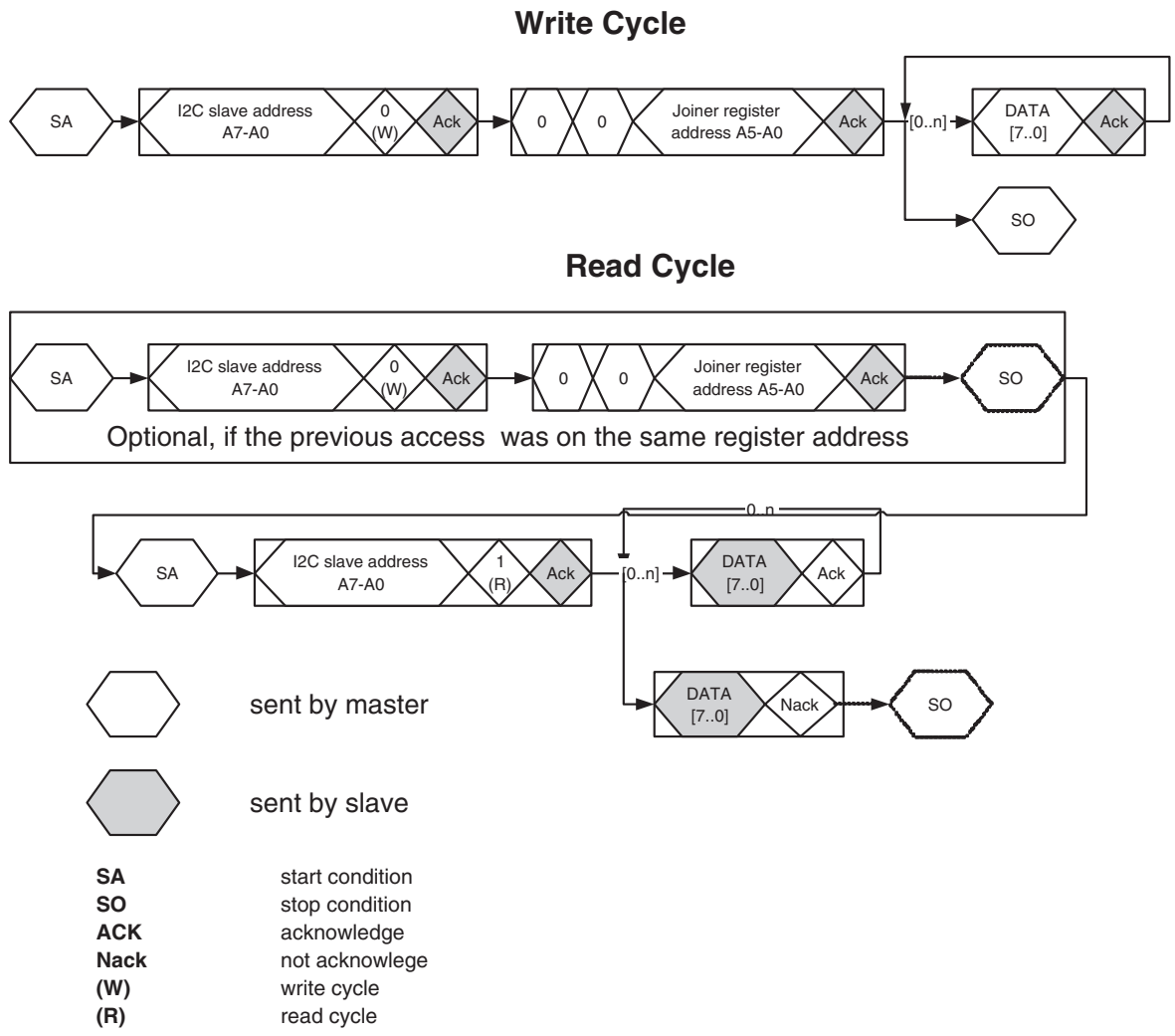


Fig 23. Register read and write access

10.4.9 HS mode

In High-speed mode (HS mode) the device can transfer information at data rates of up to 3.4 Mbit, it remains fully downward compatible with Fast- or Standard mode (F/S mode) for bi-directional communication in a mixed-speed bus system.

10.4.10 High speed transfer

To achieve a data rates of up to 3.4 Mbit the following improvements have been made to the regular I^2C-bus behavior.

- The inputs of the device in HS mode incorporates spike suppression and a Schmitt-trigger at the SDA and SCL inputs with different timing constants compared to F/S mode.
- The output buffers of the device in HS mode incorporates slope control of the falling edges of the SDA and SCL signals with different fall time compared to F/S mode.

10.4.11 Serial data transfer format in HS mode

Serial data transfer format in HS mode meets the Standard mode I^2C-bus specification. HS mode can only commence after the following conditions (all of which are in F/S mode):

1. START condition (S)
2. 8-bit master code (00001XXX)
3. Not-acknowledge bit (A)

The active master then sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address, and receives an acknowledge bit (A) from the selected PN512.

Data transfer continues in HS mode after the next repeated START (Sr), and only switches back to F/S mode after a STOP condition (P). To reduce overhead in the master code, it is possible that a master links a number of HS mode transfers, separated by repeated START conditions (Sr).

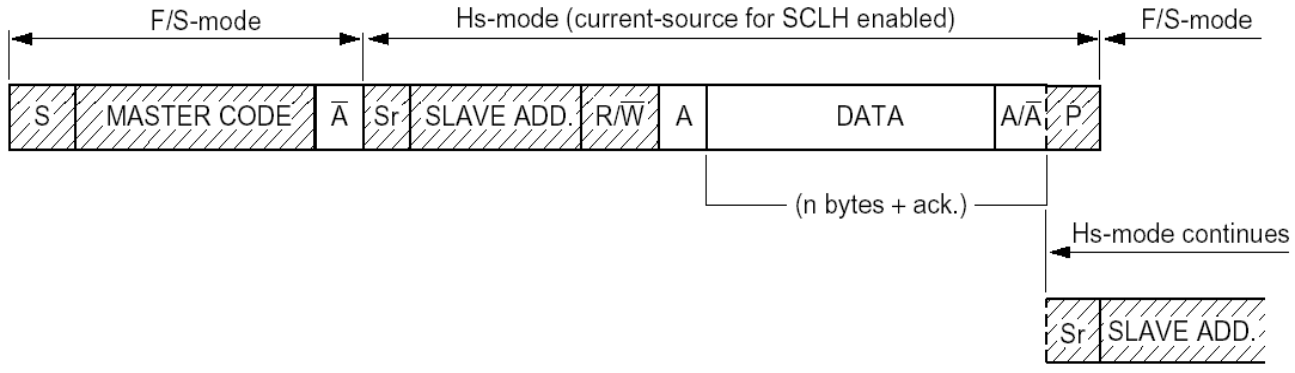


Fig 24. I^2C HS mode protocol switch

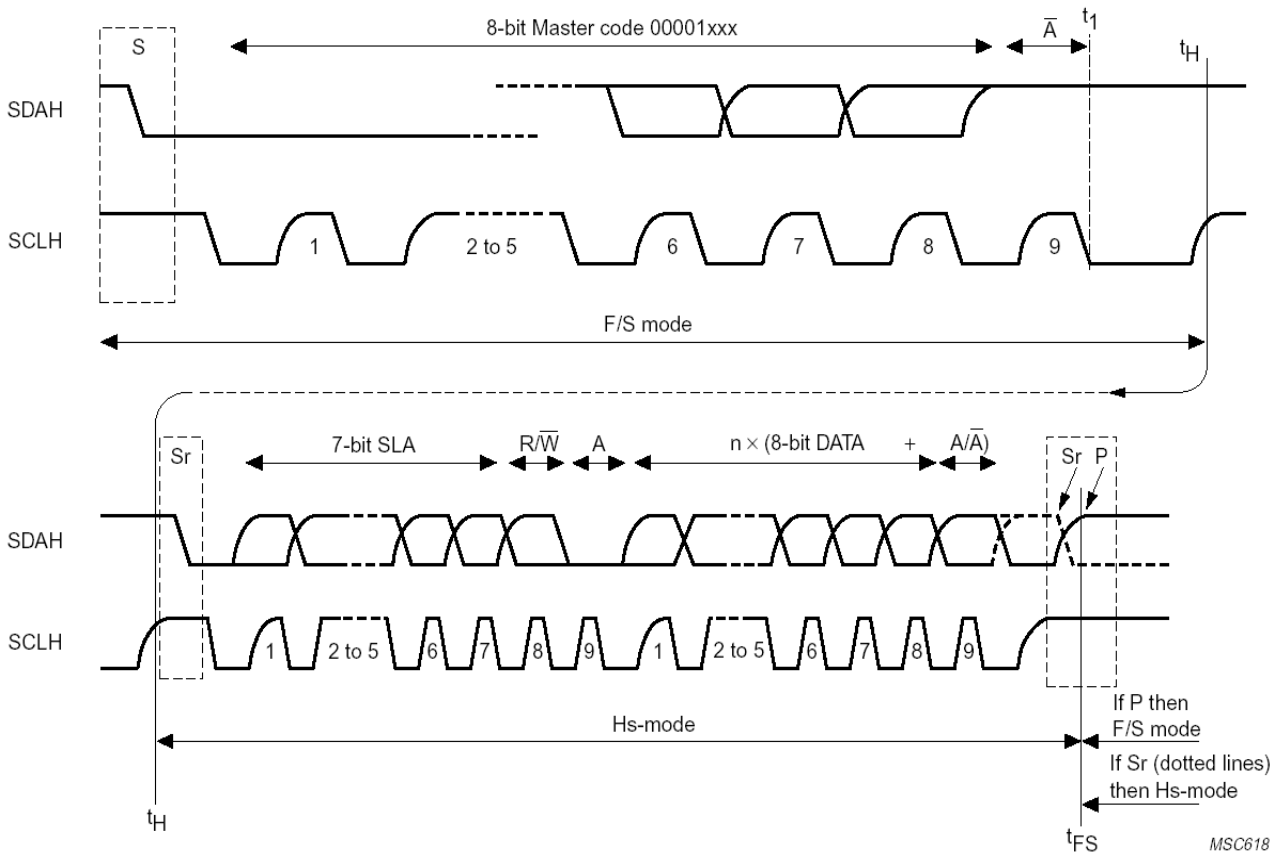


Fig 25. I²C HS mode protocol frame

10.4.12 Switching from F/S to HS mode and Vice Versa

After reset and initialization, the PN512 is in Fast mode (which is in effect F/S mode as Fast mode is downward compatible to Standard mode). The connected PN512 recognizes the “S 00001XXX A” sequence and switches its internal circuitry from the Fast mode setting to the HS mode setting.

Following actions are taken:

1. Adapt the SDA and SCL input filters according to the spike suppression requirement in HS mode.
2. Adapt the slope control of the SDA output stages.

System configurations having no other I²C devices involved in the communication an additional possibility to switch to HS mode exists. By setting the bit I²CForceHS in register Status2Reg to 1, the HS mode is entered. Setting this bit to 1 changes the HS mode permanent meaning that sending the master code is no longer necessary. This is not according the specification and should only be used when no other devices are on the bus. Spikes on the I²C lines shall be avoided because of the reduced spike suppression.

10.4.13 PN512 at lower speed modes

PN512 is fully downwards compatible, and can be connected to an F/S mode I^2C-bus system. As no master code will be transmitted in such a configuration, the device stays in F/S mode and communicates at F/S mode speeds.

10.5 8-bit parallel interface

The PN512 supports two different types of 8-bit parallel interfaces, Intel and Motorola compatible modes.

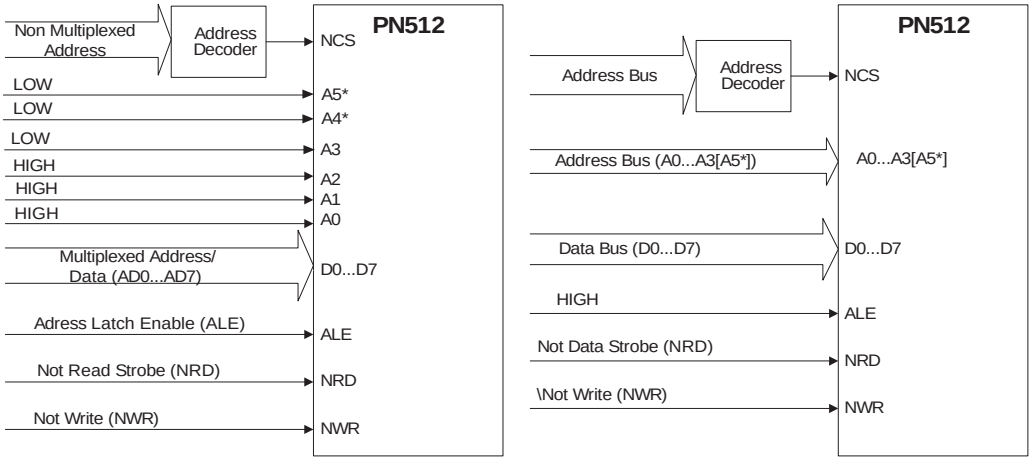
10.5.1 Overview of supported host controller interfaces

The PN512 supports direct interfacing to various µ-Controllers. The following table shows the parallel interface types supported by the PN512.

Table 149. Supported interface types

Supported interface types	Bus	Separated Address and Data Bus	Multiplexed Address and Data Bus
Separated Read and Write Strobes (INTEL compatible)	control	NRD, NWR, NCS	NRD, NWR, NCS, ALE
	address	A0 … A3 [..A5*]	AD0 … AD7
	data	D0 … D7	AD0 … AD7
Multiplexed Read and Write Strobe (Motorola compatible)	control	R/NW, NDS, NCS	R/NW, NDS, NCS, AS
	address	A0 … A3 [..A5*]	AD0 … AD7
	data	D0 … D7	AD0 … AD7

10.5.2 Separated Read/Write strobe

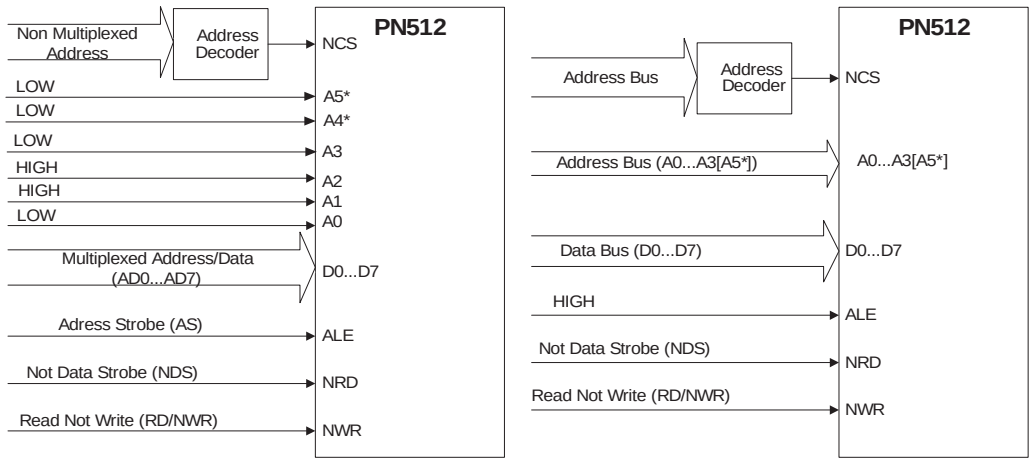


Remark: *depending on the package type.

Fig 26. Connection to host controller with separated Read/Write strobes

For timing requirements refer to Section 24.10 “8-bit parallel interface timing”.

10.5.3 Common Read/Write strobe



Remark: *depending on the package type.

Fig 27. Connection to host controller with common Read/Write strobes

For timing requirements refer to Section 24.10 “8-bit parallel interface timing”

11. AnaLog interface and contactless UART

11.1 General

The PN512 supports different Contactless Communication modes. The integrated contactless UART supports the external µ-Controller online with framing and error checking of the protocol requirements for the different selected communication schemes as Card Operation mode, Reader/Writer Operating mode or NFIP-1 mode up to 424 kbit.

Higher transfer speeds up to 3.39 Mbit can be handled by the digital part of the contactless UART. To modulate and demodulate the data an external circuit has to be connected to the communication interface pins SIGIN/SIGOUT.

The contactless UART handles the protocol requirements for the communication schemes in co-operation with the host controller. The protocol handling itself generates bit- and byte-oriented framing and handles error detection like Parity and CRC according to the different contactless communication schemes.

Remark: The size and tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

11.2 TX driver

The signal delivered on pin TX1 and pin TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly, using a few passive components for matching and filtering, see Section 20 “Application design-in information”. The signal on TX1 and TX2 can be configured by the register TxControlReg, see Section 8.2.2.5 “TxControlReg”.

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured by the registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured by the register GsNOnReg and GsNOffReg. Furthermore, the modulation index depends on the antenna design and tuning.

Note: It is recommended to use a modulation index in the range of 8% for the FeliCa and NFC IP-1 communication scheme at 212 and 424 kbit.

The register TxModeReg and TxAutoSelReg control the data rate and framing during transmission and the setting of the antenna driver to support the different requirements at the different modes and transfer speeds.

Table 150. Settings for TX1

TX1RFEn	Force 100ASK	InvTx1 RFON	InvTx1 RFOFF	Envelope	TX1	GSPMos	GSNMos	Remarks
0	X	x	0	0	0		nModOff	If TX1RFEN=0, the pin TX1 is set to logic 0 or 1 depending on InvTx1. The bit Force 100ASK has no effect, envelope modulates GS values
				1	0		nCWOff	
		x	1	0	1	pMod		
				1	1	pCW		
1	0	0	x	0	RF	pMod	nModOn	100% ASK: TX1 pulled to 0, independent of InvTx1RFOff
				1	RF	pCW	nCWOn	
	0	1	X	0	RF_n	pMod	nModOn	
				1	RF_n	pCW	nCWOn	
	1	1	x	0	0	pMod	nModOn	
				1	RF_n	pCW	nCWOn	

Table 151. Settings for TX2

TX2RFEn	Force 100ASK	TX2CW	InvTx2 RFON	InvTx2 RFOFF	Envelope	TX2	GSPMos	GSNMos	Remarks
0	X	0	x	0	0	0		nModOff	If TX2RFEN=0, the pin TX2 is set to logic 0 or 1 depending on InvTx2RF. The bit Force 100ASK has no effect, envelope modulates GS values
					1	0		nCWOff	
			x	1	0	1	pMod		
					1	1	pCW		
		1	x	0	0	0		nCWOff	TX2CW: always GsCw values
					1	0		nCWOff	
			x	1	0	1	pCW		
					1	1	pCW		
1	0	0	0	x	0	RF	pMod	nModOn	Gs always CW for TX2CW
					1	RF	pCW	nCWOn	
			1	X	0	RF_n	pMod	nModOn	
					1	RF_n	pCW	nCWOn	
		1	0	x	X	RF	pCW	nCWOn	
			1	x	X	RF_n	pCW	nCWOn	
	1	0	0	x	0	0	pMod	nModOn	100%ASK:Tx2 pulled to 0 (independent of InvTx2RFOn/ InvTI2RFOff)
					1	RF	pCW	nCWOn	
			1	x	0	0	pMod	nModOn	
					1	RF_n	pCW	nCWOn	
		1	0	x	X	RF	pCW	nCWOn	
			1	x	X	RF_n	pCW	nCWOn	

The following abbreviations are used:

- RF: 13.56 MHz clock derived from 27.12 MHz quartz divided by 2
- RF_n: inverted 13.56 MHz clock
- gspmos: Conductance, configuration of the PMOS array
- gspmos: Conductance, configuration of the NMOS array
- pCW: PMOS conductance value for continuous wave defined by CWGsP register
- pMod: PMOS conductance value for modulation defined by ModGsP register
- nCW: NMOS conductance value for continuous wave defined by CWGsN register
- nMod: NMOS conductance value for modulation defined by ModGsN register
- nCWOn: NMOS conductance value for continuous wave defined by CWGsNOn register
- nModOn: NMOS conductance value for modulation defined by ModGsNOn register
- nCWOff: NMOS conductance value for continuous wave defined by CWGsNOff register
- nModOff: NMOS conductance value for modulation defined by ModGsNOff register

Remark: If only 1 driver is switched on, the values for ModGsOn and CWGsOn are used for both drivers.

11.3 RF level detector

The RF level detector is integrated to fulfill NFCIP1 protocol requirements (e.g. RF collision avoidance). Furthermore the RF level detector can be used to wake up the PN512 and to generate an interrupt.

The sensitivity of the RF level detector is adjustable in a 4-bit range using the bits RFLevel in register RFCfgReg. The sensitivity itself depends on the antenna configuration and tuning.

Possible sensitivity levels at the RX pin are listed in the Table 152.

Table 152. Setting of the bits RFlevel in register RFCfgReg (RFLevel amplifier deactivated)

VRx [Vpp]	RFLevel
~2	1111
~1.4	1110
~0.99	1101
~0.69	1100
~0.49	1011
~0.35	1010
~0.24	1001
~0.17	1000
~0.12	0111
~0.083	0110
~0.058	0101
~0.041	0100
~0.029	0011
~0.020	0010
~0.014	0001
~0.010	0000

To increase the sensitivity of the RF level detector an amplifier can be activated by setting the bit RFLevelAmp in register RFCfgReg to 1.

Remark: During soft Power-down mode the RF level detector amplifier is automatically switched off to ensure that the power consumption is less than 10 μA at 3 V.

Remark: With typical antennas lower sensitivity levels can provoke misleading results because of intrinsic noise in the environment.

Note: It is recommended to use the bit RFLevelAmp only with higher RF level settings.

11.4 Data mode detector

The Data mode detector gives the possibility to detect received signals according to the ISO/IEC 14443A/MIFARE, FeliCa or NFCIP-1 schemes at the standard transfer speeds for 106 kbit, 212 kbit and 424 kbit in order to prepare the internal receiver in a fast and convenient way for further data processing.

The Data mode detector can only be activated by the AutoColl command. The mode detector resets, when no external RF field is detected by the RF level detector. The Data mode detector could be switched off during the AutoColl command by setting bit ModeDetOff in register ModeReg to 1.

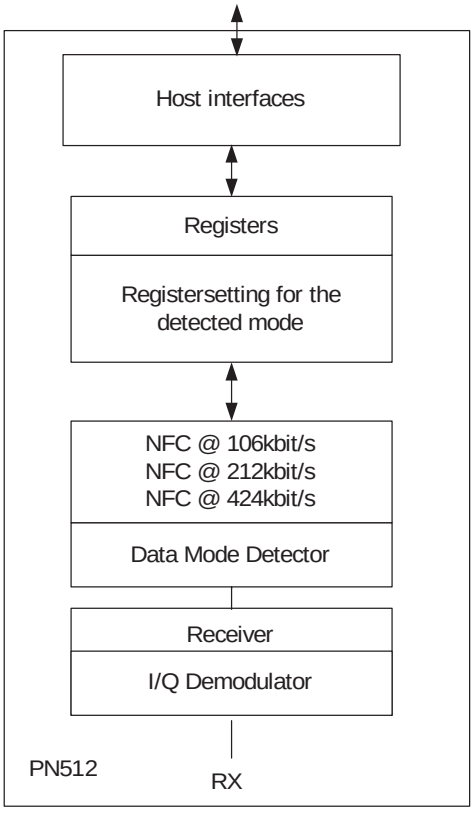


Fig 28. Data mode detector

11.5 Serial data switch

Two main blocks are implemented in the PN512. A digital circuitry, comprising state machines, coder and decoder logic and an analog circuitry with the modulator and antenna drivers, receiver and amplification circuitry. The interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins SIGIN and SIGOUT. SIGIN is capable of processing digital NFC signals on transfer speeds above 424 kbit. The SIGOUT pin can provide a digital signal that can be used with an additional external circuit to generate transfer speeds above 424 kbit (including 106, 212 and 424 kbit). Furthermore SIGOUT and SIGIN can be used to enable the S^2C interface in the card SAM mode to emulate a card functionality with the PN512 and a secure IC. A secure IC can be the Smart*MX* smart card controller IC.

The serial signal switch is controlled by the register TxSelReg and RxSelReg.

11.5.1 Serial data switch for driver

The following figure shows the serial data switch for pins TX1 and TX2.

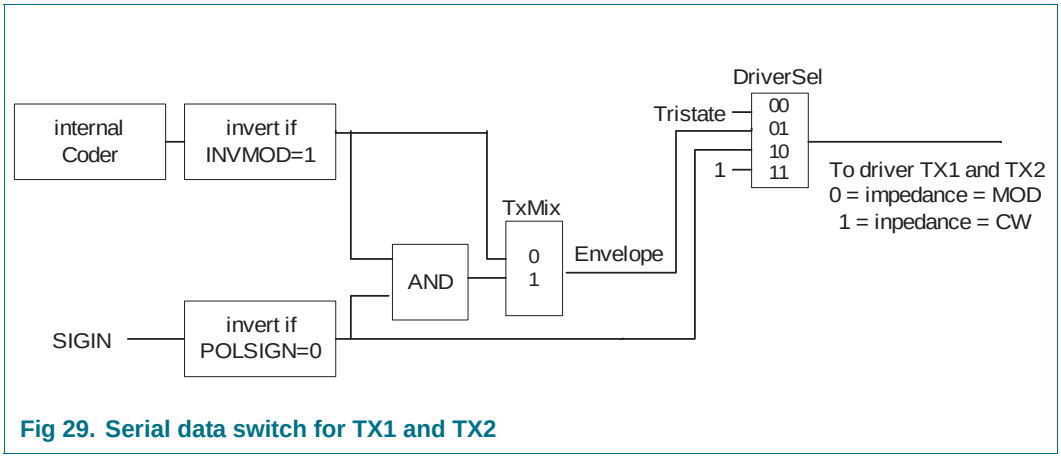


Fig 29. Serial data switch for TX1 and TX2

Pin SIGIN is in general only used for SAM communication. If TxMix is set to logic 1, the driver pins are simultaneously controlled by SIGIN and the internal coder.

11.6 S^2C interface support

The S^2C provides the possibility to directly connect a secure IC to the PN512 in order act as a contactless smart card IC via the PN512. The interfacing signals can be routed to the pins SIGIN and SIGOUT. SIGIN can receive either a digital FeliCa or digitized ISO/IEC 14443A signal sent by the secure IC. The SIGOUT pin can provide a digital signal and a clock to communicate to the secure IC. A secure IC can be the smart card IC provided by NXP Semiconductors.

The PN512 has an extra supply pin (SVDD and PVSS as Ground line) for the SIGIN and SIGOUT pads.

Figure 30 outlines possible ways of communications via the PN512 to the secure IC.

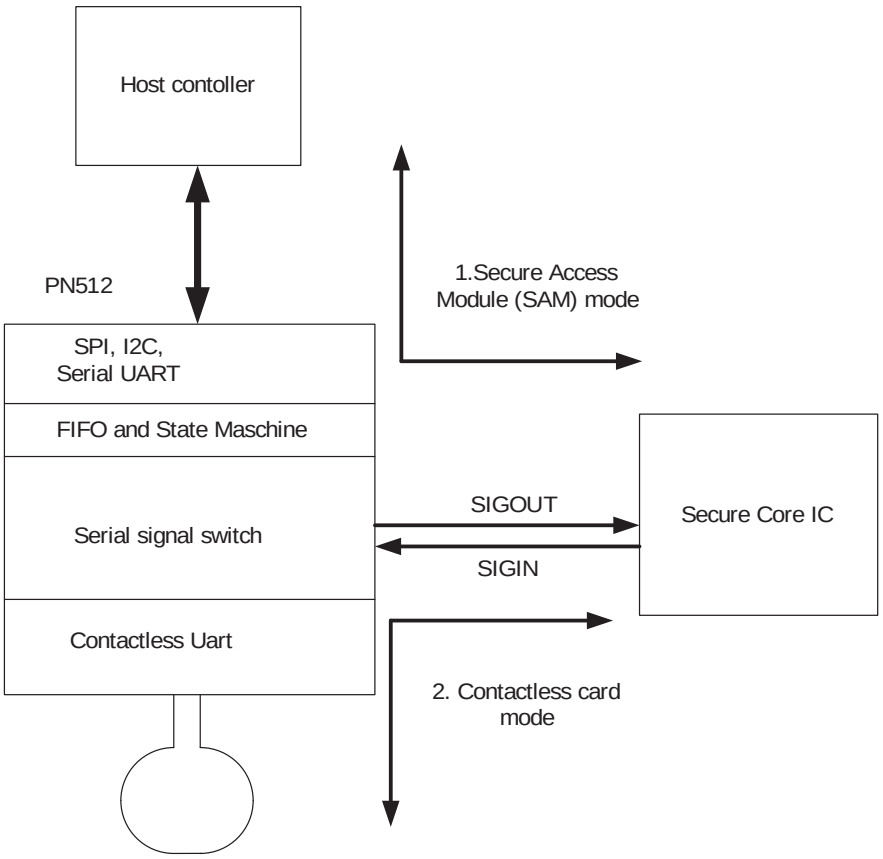


Fig 30. Communication flows using the S²C interface

Configured in the Secure Access Mode the host controller can directly communicate to the Secure IC via SIGIN/SIGOUT. In this mode the PN512 generates the RF clock and performs the communication on the SIGOUT line. To enable the Secure Access module mode the clock has to be derived by the internal oscillator of the PN512, see bits SAMClockSel in register TestSel1Reg.

Configured in Contactless Card mode the secure IC can act as contactless smart card IC via the PN512. In this mode the signal on the SIGOUT line is provided by the external RF field of the external reader/writer. To enable the Contactless Card mode the clock derived by the external RF field has to be used.

The configuration of the S²C interface differs for the FeliCa and MIFARE scheme as outlined in the following chapters.

11.6.1 Signal shape for Felica S²C interface support

The FeliCa secure IC is connected to the PN512 via the pins SIGOUT and SIGIN.

The signal at SIGOUT contains the information of the 13.56 MHz clock and the digitized demodulated signal. The clock and the demodulated signal is combined by using the logical function exclusive or.

To ensure that this signal is free of spikes, the demodulated signal is digitally filtered first. The time delay for that digital filtering is in the range of one bit length. The demodulated signal changes only at a positive edge of the clock.

The register TxSelReg controls the setting at SIGOUT.

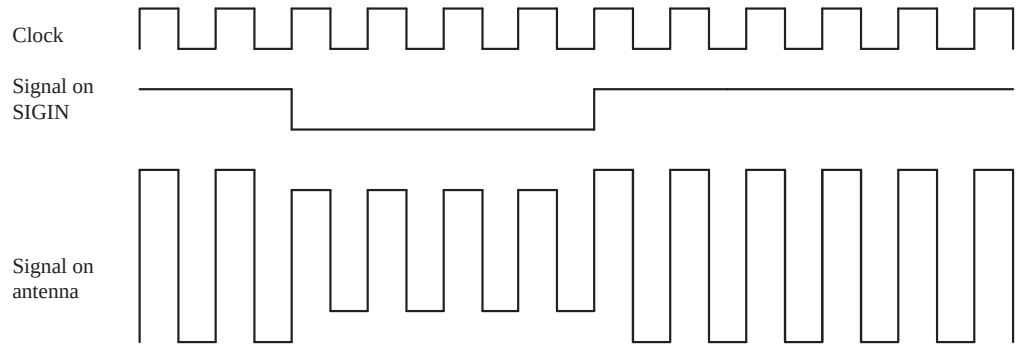


Fig 31. Signal shape for SIGOUT in FeliCa card SAM mode

The answer of the FeliCa SAM is transferred from SIGIN directly to the antenna driver. The modulation is done according to the register settings of the antenna drivers.

The clock is switched to AUX1 or AUX2 (see AnalogSelAux).

Note: A HIGH signal on AUX1 and AUX2 has the same level as AVDD. A HIGH signal at SIGOUT has the same level as SVDD. Alternatively it is possible to use pin D0 as clock output if a serial interface is used. The HIGH level at D0 is the same as PVDD.

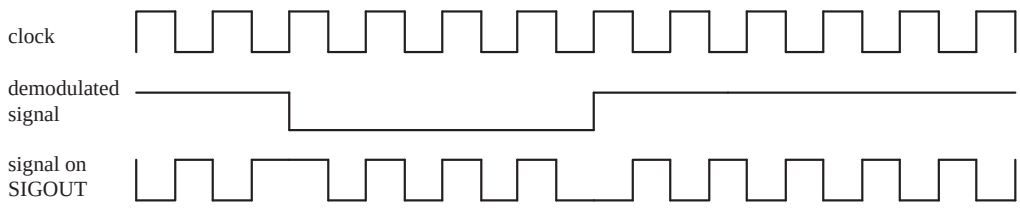


Fig 32. Signal shape for SIGIN in SAM mode

Note: The signal on the antenna is shown in principle only. In reality the waveform is sinusoidal.

11.6.2 Waveform shape for ISO/IEC 14443A and MIFARE S²C support

The secure IC, e.g. the Smart*MX* is connected to the PN512 via the pins SIGOUT and SIGIN.

The waveform shape at SIGOUT is a digital 13.56 MHz Miller coded signal with levels between PVSS and PVDD derived out of the external 13.56 MHz carrier signal in case of the Contactless Card mode or internally generated in terms of Secure Access mode.

The register TxSelReg controls the setting at SIGOUT.

Note: The clock settings for the Secure Access mode and the Contactless Card mode differ, refer to the description of the bits SAMClockSel in register TestSel1Reg.

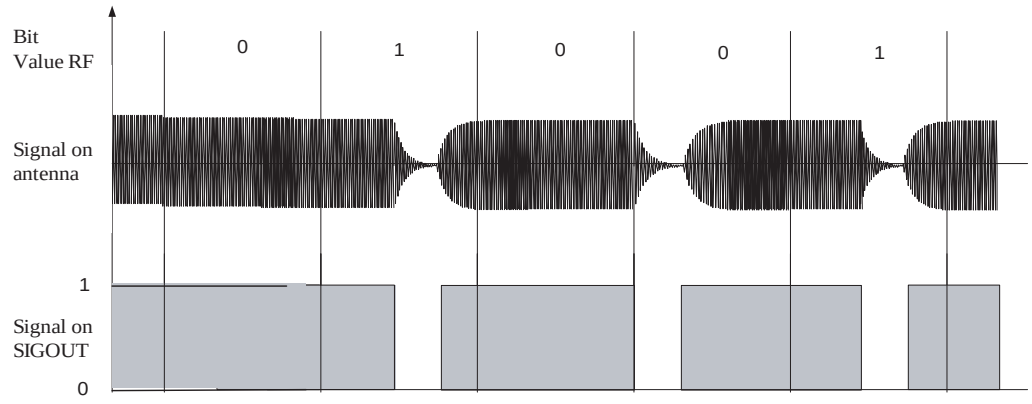


Fig 33. Signal shape for SIGOUT in MIFARE Card SAM mode

The signal at SIGIN is a digital Manchester coded signal according to the requirements of the ISO/IEC 14443A with the subcarrier frequency of 847.5 kHz generated by the secure IC.

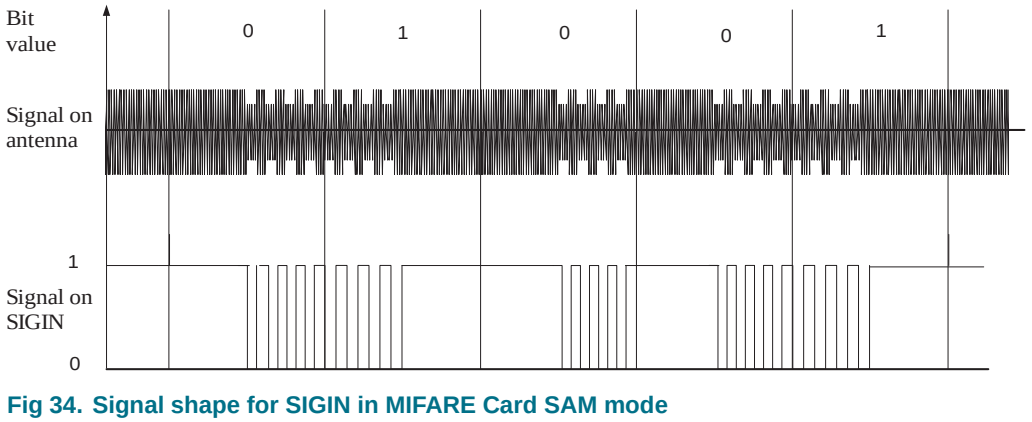


Fig 34. Signal shape for SIGIN in MIFARE Card SAM mode

11.7 Hardware support for FeliCa and NFC polling

11.7.1 Polling sequence functionality for initiator

1. Timer: The PN512 has a timer, which can be programmed in a way that it generates an interrupt at the end of each timeslot, or if required an interrupt is generated at the end of the last timeslot.
2. The receiver can be configured in a way to receive continuously. In this mode it can receive any number of packets. The receiver is ready to receive the next packet directly after the last packet has been received. This mode is active by setting the bit RxMultiple in register RxModeReg to 1 and has to be stopped by software.
3. The internal UART adds one byte to the end of every received packet, before it is transferred into the FIFO-buffer. This byte indicates if the received byte packet is correct (see register ErrReg). The first byte of each packet contains the length byte of the packet.
4. The length of one packet is 18 or 20 bytes (+ 1 byte Error-Info). The FIFO has a length of 64 bytes. This means three packets can be stored in the FIFO at the same time. If more than three packets are expected, the host controller has to empty the FIFO, before the FIFO is filled completely. In case of a FIFO-overflow data is lost (See bit BufferOvfl in register ErrorReg).

11.7.2 Polling sequence functionality for target

1. The host controller has to configure the PN512 with the correct polling response parameters for the polling command.
2. To activate the automatic polling in Target mode, the AutoColl Command has to be activated.
3. The PN512 receives the polling command send out by an initiator and answers with the polling response. The timeslot is selected automatically (The timeslot itself is randomly generated, but in the range 0 to TSN, which is defined by the Polling command). The PN512 compares the system code, stored in byte 17 and 18 of the Config Command with the system code received by the polling command of an initiator. If the system code is equal, the PN512 answers according to the configured polling response. The system code FF (hex) acts as a wildcard for the system code bytes, i.e. a target of a system code 1234 (hex) answers to the polling command with one of the following system codes 1234 (hex), 12FF (hex), FF34 (hex) or FFFF (hex). If the system code does not match no answer is sent back by the PN512.

   If a valid command is received by the PN512, which is not a Polling command, no answer is sent back and the command AutoColl is stopped. The received packet is stored in the FIFO.

11.7.3 Additional hardware support for FeliCa and NFC

Additionally to the polling sequence support for the Felica mode, the PN512 supports the check of the Len-byte.

The received Len-byte in accordance to the registers FelNFC1Reg and FelNFC2Reg:

DataLenMin in register FelNFC1Reg defines the minimum length of the accepted packet length. This register is six bit long. Each bit represents a length of four bytes.

DataLenMax in register FelNFC2Reg defines the maximum length of the accepted package. This register is six bit long. Each bit represents a length of four bytes. If set to logic 1 this limit is ignored. If the length is not in the supposed range, the packet is not transferred to the FIFO and receiving is kept active.

Example 1:

- DataLenMin = 4
  - The length shall be greater or equal 16.
- DataLenMax = 5
  - The length shall be smaller than 20. Valid area: 16, 17, 18, 19

Example 2:

- DataLenMin = 9
  - The length shall be greater or equal 36.
- DataLenMax = 0
  - The length shall be smaller than 256. Valid area: 36 to 255

11.8 CRC co-processor

Only the CRC Preset Value of the CRC co-processor can be configured. The CRC preset value could be either 0000h, 6363h, A671h or FFFFh depending on the bits CRCPreset in register ModeReg.

The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$.

The CRC coprocessor can be configured to handle the MSB and LSB requirements for the different protocols.

The following registers allow the configuration of the CRC-coprocessor:

The registers CRCResultReg indicate the result of the CRC calculation. This register is split into two 8-bit registers indicating the higher and lower byte.

The bit MSBFirst in the register ModeReg indicates that data will be loaded with MSB first.

12. FIFO-buffer

12.1 Overview

An 64*8-bit FIFO-buffer is implemented in the PN512. It buffers the input and output data stream between the host controller and the internal state machine of the PN512. Thus, it is possible to handle data streams with lengths of up to 64 bytes without taking timing constraints into account.

12.2 Accessing the FIFO-buffer

12.2.1 Access rules

The FIFO-buffer input and output data bus is connected to the register FIFODataReg. Writing to this register stores one byte in the FIFO-buffer and increments the internal FIFO-buffer write-pointer. Reading from this register shows the FIFO-buffer contents stored at the FIFO-buffer read-pointer and decrements the FIFO-buffer read-pointer. The distance between the write- and read-pointer can be obtained by reading the register FIFOLevelReg.

When the µ-Controller starts a command, the PN512 may, while the command is in progress, access the FIFO-buffer according to that command. Physically only one FIFO-buffer is implemented, which can be used in input- and output direction. Therefore the µ-Controller has to take care, not to access the FIFO-buffer in an unintended way.

12.3 Controlling the FIFO-buffer

Besides writing to and reading from the FIFO-buffer, the FIFO-buffer pointers might be reset by setting the bit FlushBuffer in the register FIFOLevelReg to 1. Consequently, the FIFOLevel bits are set to logic 0 the bit BufferOvfl in the register ErrorReg is cleared, the actually stored bytes are not accessible any more and the FIFO-buffer can be filled with another 64 bytes again.

12.4 Status information about the FIFO-buffer

The host controller may obtain the following data about the FIFO-buffers status:

- Number of bytes already stored in the FIFO-buffer: FIFOLevel in register FIFOLevelReg
- Warning, that the FIFO-buffer is almost full: HiAlert in register Status1Reg
- Warning, that the FIFO-buffer is almost empty: LoAlert in register Status1Reg
- Indication, that bytes were written to the FIFO-buffer although it was already full: BufferOvfl in register ErrorReg. BufferOvfl can be cleared only by setting bit FlushBuffer in the register FIFOLevelReg.

The PN512 can generate an interrupt signal

- If LoAlertIEn in register CommIEnReg is set to logic 1 it will activate pin IRQ when LoAlert in the register Status1Reg changes to 1.
- If HiAlertIEN in register CommIEnReg is set to logic 1 it will activate pin IRQ when HiAlert in the register Status1Reg changes to 1.

The bit HiAlert is set to logic 1 if maximum WaterLevel bytes (as set in register WaterLevelReg) or less can be stored in the FIFO-buffer. It is generated according to the following equation:

$$HiAlert = (64 - FIFOLength) \leq WaterLevel$$

The bit LoAlert is set to logic 1 if WaterLevel bytes (as set in register WaterLevelReg) or less are actually stored in the FIFO-buffer. It is generated according to the following equation:

$$LoAlert = FIFOLength \leq WaterLevel$$

13. Timer unit

A timer unit is implemented in the PN512. The external host controller may use this timer to manage timing relevant tasks. The timer unit may be used in one of the following configurations:

- Time-out counter
- Watch-dog counter
- Stop watch
- Programmable one-shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events which will be explained in the following, but the timer itself does not influence any internal event (e.g. A time-out during data reception does not influence the reception process automatically). Furthermore, several timer related bits are set and these bits can be used to generate an interrupt.

Timer

The timer has an input clock of 13.56 MHz (derived from the 27.12 MHz quartz). The timer consists of two stages: 1 prescaler and 1 counter.

The prescaler is a 12-bit counter. The reload value for TPrescaler can be defined between 0 and 4095 in register TModeReg and TPrescalerReg.

The reload value for the counter is defined by 16 bits in a range of 0 to 65535 in the register TReloadReg.

The current value of the timer is indicated by the register TCounterValReg.

If the counter reaches 0 an interrupt will be generated automatically indicated by setting the TimerIRq bit in the register CommonIRqReg. If enabled, this event can be indicated on the IRQ line. The bit TimerIRq can be set and reset by the host controller. Depending on the configuration the timer will stop at 0 or restart with the value from register TReloadReg.

The status of the timer is indicated by bit TRunning in register Status1Reg.

The timer can be manually started by TStartNow in register ControlReg or manually stopped by TStopNow in register ControlReg.
Furthermore the timer can be activated automatically by setting the bit TAuto in the register TModeReg to fulfill dedicated protocol requirements automatically.

The time delay of a timer stage is the reload value +1.
The definition of total time is: t = ((TPrescaler*2+1)*TReload+1)/13.56MHz

Maximum time: TPrescaler = 4095,TReloadVal = 65535
=> (2*4095 +1)*65536/13.56 MHz = 39.59 s

Example:

To indicate 25 us it is required to count 339 clock cycles. This means the value for TPrescaler has to be set to TPrescaler = 169.The timer has now an input clock of 25 us. The timer can count up to 65535 timeslots of each 25 μs.

14. Interrupt request system

14.1 Overview

The PN512 indicates certain events by setting bit IRq in the register Status1Reg and additionally, if activated, by pin IRQ. The signal on pin IRQ may be used to interrupt the host controller using its interrupt handling capabilities. This allows the implementation of efficient host controller software.

14.1.1 Interrupt sources overview

The following table shows the available interrupt bits, the corresponding source and the condition for its activation.

The interrupt bit TimerIRq in register CommIRqReg indicates an interrupt set by the timer unit. The setting is done when the timer decrements from 1 to 0.

The TxIRq bit in register CommIRqReg indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit sets the interrupt bit automatically.

The CRC co-processor sets the bit CRCIRq in the register DivIRqReg after having processed all data from the FIFO-buffer. This is indicated by the bit CRCReady = 1.

The RxIRq bit in register CommIRqReg indicates an interrupt when the end of the received data is detected.

The bit IdleIRq in register CommIRqReg is set if a command finishes and the content of the command register changes to idle.

The bit HiAlertIRq in register CommIRqReg is set to logic 1 if the HiAlert bit is set to logic 1, that means the FIFO-buffer has reached the level indicated by the bit WaterLevel.

The bit LoAlertIRq in register CommIRqReg is set to logic 1 if the LoAlert bit is set to logic 1, that means the FIFO-buffer has reached the level indicated by the bit WaterLevel.

The bit RFOnIRq in register DivIRqReg is set to logic 1, when the RF level detector detects an external RF field.

The bit RFOffIRq in register DivIRqReg is set to logic 1, when a present external RF field is switched off.

The bit ErrIRq in register CommIRqReg indicates an error detected by the contactless UART during sending or receiving. This is indicated by any bit set to 1 in register ErrorReg.

The bit ModeIRq in register DivIRqReg indicates that the Data mode detector has detected the Current mode.

Table 153. Interrupt sources

Interrupt bit	Interrupt source	Is set automatically, when
TimerIRq	Timer Unit	the timer counts from 1 to 0
TxIRq	Transmitter	a transmitted data stream ends
CRCIRq	CRC co-processor	all data from the FIFO-buffer has been processed
RxIRq	Receiver	a received data stream ends
IdleIRq	Command Register	a command execution finishes
HiAlertIRq	FIFO-buffer	the FIFO-buffer is getting full
LoAlertIRq	FIFO-buffer	the FIFO-buffer is getting empty
RFOnIRq	RF Level Detector	an external RF field is detected
RFOffIRq	RF Level Detector	a present external RF field is switched off
ErrIRq	contactless UART	an error is detected
ModeIRq	data mode detector	the mode has been detected

15. Oscillator circuitry

The clock applied to the PN512 acts as time basis for the coder and decoder of the synchronous system. Therefore stability of the clock frequency is an important factor for proper performance. To obtain highest performance, clock jitter has to be as small as possible. This is best achieved by using the internal oscillator buffer with the recommended circuitry. If an external clock source is used, the clock signal has to be applied to pin OSCIN. In this case special care for clock duty cycle and clock jitter is needed and the clock quality has to be verified.

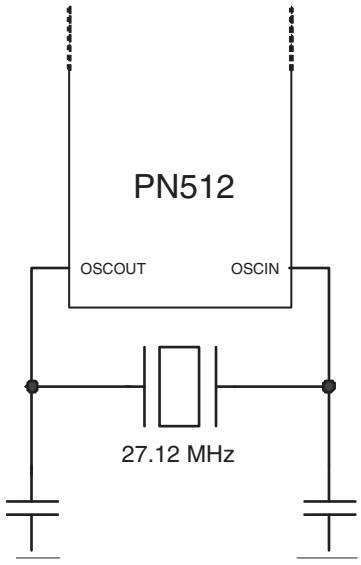


Fig 35. Quartz connection

16. Power reduction modes

16.1 Hard Power-down

A Hard Power-down is enabled with LOW level on pin NRSTPD. This turns off all internal current sinks as well as the oscillator. All digital input buffers are separated from the input pads and clamped internally (except pin NRSTPD itself). The output pins are frozen at a certain value.

The RF level detector is not working.

16.2 Soft Power-down

The Soft Power-down mode is entered immediately after setting the bit Power-down in the register CommandReg to 1. All internal current sinks are switched off (including the oscillator buffer).

In opposition to the Hard Power-down mode, the digital input-buffers are not separated from the input pads and keep their functionality. The digital output pins do not change their state.

During Soft Power-down all registers values, the FIFO's content and the configuration itself will keep its content and the RF level detector is working.

If the bit AutoWakeUp in the register TxAutoReg is set and an external RF field is detected, the Soft Power-down mode is left automatically.

After setting bit Power-down in the register CommandReg to 0 it takes 1024 clocks until the Soft Power-down mode is left as indicated by the Power-down bit itself. Setting it to logic 0 does not immediately clear it. It is cleared automatically by the PN512 when the Soft Power-down mode is left.

Note: If the internal oscillator is used, you have to take into account that it is supplied by AVDD and it will take a certain time t_{osc} until the oscillator is stable and the clock cycles can be detected by the internal logic.

Note: If the serial UART interface is used, then the PN512 recovers from soft Power-down mode by sending the value 55 (hex) to the PN512. For further access to the registers the oscillator must be stable. The first read or write access must be to address 0.

For the serial UART it is recommended to send the value 55 (hex) first and perform read accesses to address 0 till the PN512 answers to the last read command with the register content of address 0. This indicates that the PN512 is active for further operation.

This procedure also has to be performed, when the bit AutoWakeUp in the register TxAutoReg is set and the PN512 detects an external RF field.

16.3 Transmitter Power-down

The Transmitter Power-down mode switches off the internal antenna drivers to turn off the RF field by setting either Tx1RfEn or TX2RFEn in the register TXControlReg to 0. The receiver is still switched on, so the PN512 can be accessed by a second NFC device as a target.

17. Reset and Oscillator start up time

17.1 Reset timing requirements

The reset signal is filtered by a hysteresis circuit and a spike filter (rejects signals shorter than 10 ns) before it enters the digital circuit. In order to perform a reset, the signal has to be low for at least 100 ns.

17.2 Oscillator start up time

Having set the PN512 to a Power-down mode or supplying the IC with XVDD the following figure describes the startup timing for the oscillator.

The time $t_{startup}$ defines the start-up time of crystal oscillator circuit. The crystal oscillator start-up time is defined by the crystal itself.

The t_{delay} defines the internal delay time of the PN512 when the clock signal is stable before the PN512 can be addressed. The delay time is calculated as follows:
t_{delay} [µs] = 1024/27.12 = 37.76 µs.

The time t_{osc} is defined as the sum of the time t_{delay} and $t_{startup}$.

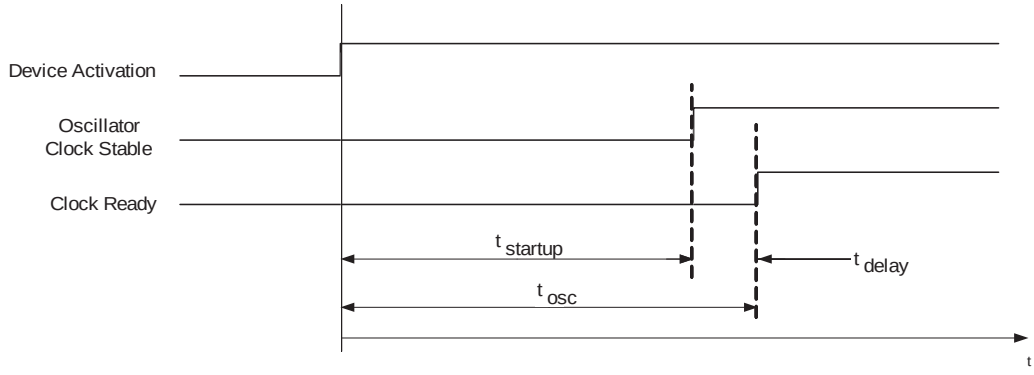


Fig 36. Oscillator Start up time

18. PN512 Command set

18.1 General description

The PN512 behavior is determined by a state machine capable to perform a certain set of commands. By writing the according command to the Command-Register the command is executed.

Arguments and/or data necessary to process a command are exchanged via the FIFO-buffer.

18.2 General behavior

- Each command, that needs a data stream (or data byte stream) as input will immediately process the data it finds in the FIFO-buffer. An exception to this rule is the Transceive command. Using this command the transmission is started with the StartSend bit in the BitFramingReg register.
- Each command that needs a certain number of arguments will start processing only when it has received the correct number of arguments via the FIFO-buffer.
- The FIFO-buffer is not cleared automatically at command start. Therefore, it is also possible to write the command arguments and/or the data bytes into the FIFO-buffer and start the command afterwards.
- Each command may be interrupted by the host controller by writing a new command code into the Command-Register e.g.: the Idle-Command.

18.3 PN512 Commands overview

Table 154. Command overview

Command	Command code	Action
Idle	0000	No action; cancels current command execution.
Config	0001	Configures the PN512 for FeliCa, MIFARE and NFCIP-1 communication
Generate RandomID	0010	Generates a 10 byte random ID number
CalcCRC	0011	Activates the CRC co-processor or performs a selftest.
Transmit	0100	Transmits data from the FIFO-buffer.
NoCmd Change	0111	No command change. This command can be used to modify different bits in the command register without touching the command. E.G. Power down bit.
Receive	1000	Activates the receiver circuitry.
Transceive	1100	If bit Initiator in the register ControlReg is set to 1: Transmits data from FIFO-buffer and automatically activates the receiver after transmission is finished. If bit Initiator in the register ControlReg is set to 0: Receives data and automatically activates the transmitter after reception.
AutoColl	1101	Handles FeliCa polling (Card Operation mode only) and MIFARE anticollision (Card Operation mode only)
MFAuthent	1110	Performs the MIFARE authentication in MIFARE Reader/Writer mode only
Soft Reset	1111	Resets the PN512

18.3.1 PN512 Command description

18.3.1.1 Idle command

The PN512 is in Idle mode. This command is also used to terminate the actual command.

18.3.1.2 Config command

To use the automatic MIFARE Anticollision, FeliCa Polling and NFCID3 the data used for these transactions has to be stored internally. All the following data have to be written to the FIFO in this order:

- SENS_RES (2 bytes); in order byte 0, byte 1
- NFCID1 (3 bytes); in order byte 0, byte 1, byte 2; the first NFCID1 byte is fixed to 08h and the check byte is calculated automatically.
- SEL_RES (1 byte)
- polling response (2 bytes (shall be 01h, FEh) + 6 bytes NFCID2 + 8 bytes Pad + 2 bytes system code)
- NFCID3 (1 byte)

In total 25 bytes are transferred into an internal buffer.

The complete NFCID3 is 10 bytes long and consists of the 3 NFCID1 bytes, the 6 NFCID2 bytes and the one NFCIP3 byte which are listed above.

To read out this configuration the command Config with an empty FIFO-buffer has to be started. In this case the 25 bytes are transferred from the internal buffer to the FIFO.

The PN512 has to be configured after each power up, before using the automatic Anticollision/Polling function (AutoColl command). During a hard power down (reset pin) this configuration remains unchanged.

This command terminates automatically when finished and the active command is idle.

18.3.1.3 Generate RandomID command

This command generates a 10 byte random number stored in the internal buffer and overwrites the 10 bytes NFCID3 of the internal buffer. This command can be used for a fast regeneration of all necessary ID bytes.

This command terminates automatically when finished and the PN512 returns to idle.

Note: To configure the PN512 the command Config has to be used first.

18.3.1.4 CalcCRC command

The content of the FIFO is transferred to the CRC co-processor and a CRC calculation is started. The result of this calculation is stored in the CRCResultReg register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped, when the FIFO gets empty during the data stream. The next byte written to the FIFO is added to the calculation.

The pre-set value of the CRC is controlled by the CRCPreset bits of the ModeReg register and the chosen value is loaded to the CRC co-processor when the command is started.

This command has to be terminated by writing any command to the Command-register e.g. the command Idle.

If the SelfTest bits in the register AutoTestReg are set correct, the PN512 is in Self Test mode and starting the CalcCRC command performs a digital selftest. The result of the selftest is written to the FIFO.

18.3.1.5 Transmit command

The content of the FIFO is transmitted immediately after starting the command. Before transmitting the FIFO content all relevant register have to be set to transmit data in the selected mode.

This command terminates automatically when the FIFO gets empty. It can be terminated by any other command written to the command register.

18.3.1.6 NoCmdChange command

This command does not influence any ongoing command in the CommandReg register. It can be used to manipulate any bit except the command bits in the CommandReg register, e.g. the bits RcvOff or Power-down.

18.3.1.7 Receive command

The PN512 activates the receiver path and waits for any data stream to be received. The correct settings for the expected mode have to be chosen before starting this command.

This command terminates automatically when the received data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected framing and speed.

Note: If the bit RxMultiple in the RxModeReg register is set to logic 1 the Receive command does not terminate automatically. It has to be terminated by activating any other command in the CommandReg register.

18.3.1.8 Transceive command

This circular command repeats transmitting data from the FIFO and receiving data from the RF field continuously. If the bit Initiator in the register ControlReg is set to logic 1, it indicates that the first action is transmitting and after having finished transmission the receiver is activated to receive data. If the bit Initiator in the register ControlReg is set to logic 0, the first action is receiving and after having received a data stream, the transmitter is activated to transmit data. In the second configuration the PN512 first acts as a receiver and if a data stream is received it switches to the Transmit mode.

Initiator =1	....	Initiator=0	....
Send	....	Receive	....
Receive	....	Send	....
Send	....	Receive	....
Receive	....	Send	....

Each transmission process has to be started by setting bit StartSend in the register BitFramingReg to 1. This command has to be cleared by software by writing any command to the Command-register e.g. the command idle.

Note: If the bit RxMultiple in register RxModeReg is set to logic 1, this command will never leave the receiving state, because the receiving will not be cancelled automatically.

18.3.1.9 AutoColl command

This command automatically handles the MIFARE activation and the FeliCa polling in the Card Operation mode. The bit Initiator in the register ControlReg has to be set to logic 0 for correct operation. During this command also the mode detector is active if not deactivated by setting the bit ModeDetOff in the ModeReg register. After the mode detector detects a mode, all the mode dependent registers are set according to the received data. In case of no external RF field this command resets the internal state machine and returns to the initial state but it will not be terminated. When the command terminates the transceive command gets active.

During protocol processing the IRQ bits are not supported. Only the last received frame will serve the IRQ's. The treatment of the TxCRCEn and RxCRCEn bits is different to the protocol. During ISO/IEC 14443A activation the enable bits are defined by the command AutoColl. The changes cannot be observed at the register TxModeReg and RxModeReg. After the Transceive command is active, the value of the register bit is relevant.

Note: Pay attention, that the FIFO will also receive the two CRC check bytes of the last command even if they are already checked and correct, if the state machine (Anticollision and Select routine) has to not been executed, and 106 kbit is detected.

During Felica activation the register bit is always relevant and is not overruled by the command settings.

This command can be cleared by software by writing any other command to the CommandReg register, e.g. the idle command. Writing the same content again to the CommandReg register resets the state machine.

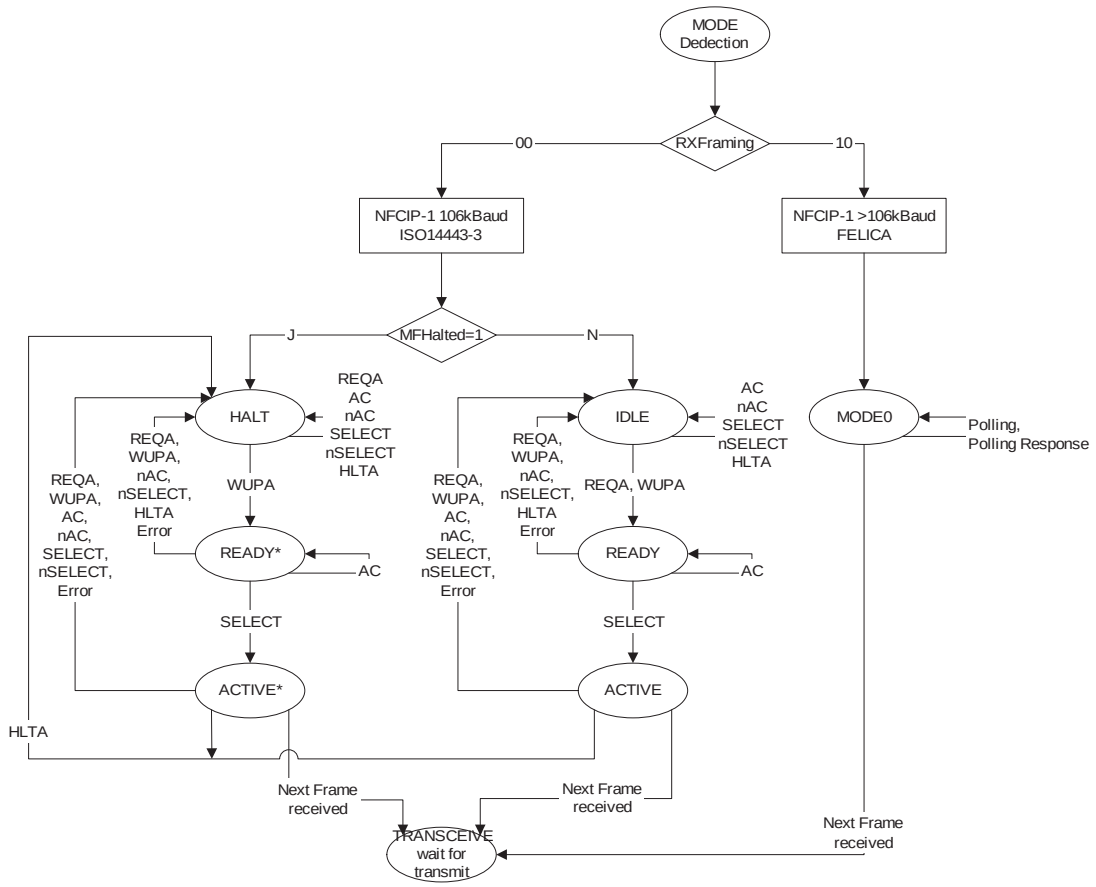


Fig 37. Autocoll Command

NFCIP-1 106 kbps Passive Communication mode:

The MIFARE anticollision is finished and the command has automatically changed to Transceive. The FIFO contains the ATR_REQ frame including the start byte F0h. The bit TargetActivated in the Status2Reg register is set to logic 1.

NFCIP-1 212/424 kbps Passive Communication mode:

The FeliCa polling command is finished and the command has automatically changed to Transceive. The FIFO contains the ATR_REQ. The bit TargetActivated in the Status2Reg register is set to logic 1.

NFCIP-1 106/212/424 kbps Active Communication mode:

This command is changing automatically to the command Transceive. The FIFO contains the ATR REQ. The bit TargetActivated in the Status2Reg register is set to logic 0. For 106 kbps only, the first byte in the FIFO indicates the start byte F0h and the CRC is added to the FIFO.

MIFARE (Card Operation mode):

The MIFARE anticollision is finished and the command has automatically changed to transceive. The FIFO contains the first command after the Select. The bit TargetActivated in the Status2Reg register is set to logic 1.

FeliCa (Card Operation mode):

The FeliCa polling command is finished and the command has automatically changed to transceive. The FIFO contains the first command followed after the Polling by the FeliCa protocol.The bit TargetActivated in the Status2Reg register is set to logic 1.

18.3.1.10 MFAuthent command

This command handles the MIFARE authentication in Reader/Writer mode to enable a secure communication to any MIFARE card. The following data shall be written to the FIFO before the command can be activated:

- Authentication command code (60h, 61h)
- Block address.
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total 12 bytes shall be written to the FIFO.

Note: When the MFAuthent command is active, any FIFO access is blocked. Anyhow if there is an access to the FIFO, the bit WrErr in the ErrorReg register is set.

This command terminates automatically when the MIFARE card is authenticated and the bit MFCrypto1On in the Status2Reg register is set to logic 1.

This command does not terminate automatically, when the card does not answer, therefore the timer should be initialized to automatic mode. In this case, beside the bit IdleIRq the bit TimerIRq can be used as termination criteria. During authentication processing the bits RxIRq and TxIRq are blocked. The Crypto1On bit is only valid after termination of the authent command (either after processing the protocol or after writing IDLE to the command register).

In case there is an error during Authentication the bit ProtocolErr in the ErrorReg register is set to logic 1 and the bit Crypto1On in register Status2Reg is set to logic 0.

18.3.1.11 SoftReset Command

This command performs a reset of the device. The configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command terminates automatically when finished.

Note: The SerialSpeedReg register is reset and therefore the serial data rate is set to 9.6 kbps.

19. Testsignals

19.1 Selftest

The PN512 has the capability to perform a digital selftest. To start the selftest the following procedure has to be performed:

1. Perform a soft reset.
2. Clear the internal buffer by writing 25 bytes of 00h and perform the Config Command.
3. Enable the Selftest by writing the value 09h to the register AutoTestReg.
4. Write 00h to the FIFO.
5. Start the Selftest with the CalcCRC Command.
6. The Selftest will be performed.
7. When the Selftest is finished, the FIFO contains the following bytes:
   - Correct answer for VersionReg equal to 80h:

     0x00, 0xaa, 0xe3, 0x29, 0x0c, 0x10, 0x29, 0x6b
     0x76, 0x8d, 0xaf, 0x4b, 0xa2, 0xda, 0x76, 0x99
     0xc7, 0x5e, 0x24, 0x69, 0xd2, 0xba, 0xfa, 0xbc
     0x3e, 0xda, 0x96, 0xb5, 0xf5, 0x94, 0xb0, 0x3a
     0x4e, 0xc3, 0x9d, 0x94, 0x76, 0x4c, 0xea, 0x5e
     0x38, 0x10, 0x8f, 0x2d, 0x21, 0x4b, 0x52, 0xbf
     0xfb, 0xf4, 0x19, 0x94, 0x82, 0x5a, 0x72, 0x9d
     0xba, 0x0d, 0x1f, 0x17, 0x56, 0x22, 0xb9, 0x08

19.2 Testbus

The testbus is implemented for production test purposes. The following configuration can be used to improve the design of a system using the PN512. The testbus allows to route internal signals to the digital interface. The testbus signals are selected by accessing TestBusSel in register TestSel2Reg.

Table 155. Testsignal routing (TestSel2Reg = 07h)

Pins	D6	D5	D4	D3	D2	D1	D0
Testsignal	sdata	scoll	svalid	sover	RCV_reset	RFon, filtered	Envelope

Table 156. Description of Testsignals

Pins	Testsignal	Description
D6	sdata	shows the actual received data stream.
D5	scoll	shows if in the actual bit a collision has been detected (106 kbit only)
D4	svalid	shows if sdata and scoll are valid
D3	sover	shows that the receiver has detected a stop condition (ISO/IEC 14443A/ MIFARE mode only).
D2	RCV_reset	shows if the receiver is reset
D1	RFon, filtered	shows the value of the internal RF level detector
D0	Envelope	shows the output of the internal coder

Table 157. Testsignal routing (TestSel2Reg = 0Dh)

Pins	D6	D5	D4	D3	D2	D1	D0
Testsignal	clkstable	clk27/8	clk27rf/8	clkrf13rf/4	clk27	clk27rf	clk13rf

Table 158. Description of Testsignals

Pins	Testsignal	Description
D6	clkstable	shows if the oscillator delivers a stable signal.
D5	clk27/8	shows the output signal of the oscillator divided by 8
D4	clk27rf/8	shows the clk27rf signal divided by 8
D3	clkrf13/4	shows the clk13rf divided by 4.
D2	clk27	shows the output signal of the oscillator
D1	clk27rf	shows the RF clock multiplied by 2.
D0	clk13rf	shows the RF clock of 13.56 MHz

Table 159. Testsignal routing (TestSel2Reg = 19h)

Pins	D6	D5	D4	D3	D2	D1	D0
Testsignal	-	TRunning	-	-	-	-	-

Table 160. Description of Testsignals

Pins	Testsignal	Description
D6	-	-
D5	TRunning	TRunning stops 1 clockcycle after TimerIRQ is raised
D4	-	-
D3	-	-
D2	-	-
D1	-	-
D0	-	-

19.3 Testsignals at pin AUX

Table 161. Testsignals description

SelAux	Description for Aux1 / Aux2
0000	Tristate
0001	DAC: register TestDAC 1/2
0010	DAC: testsignal corr1
0011	DAC: testsignal corr2
0100	DAC: testsignal MinLevel
0101	DAC: ADC_I
0110	DAC: ADC_Q
0111	DAC: testsignal ADC_I combined with ADC_Q
1000	Testsignal for production test
1001	SAM clock
1010	High
1011	low
1100	TxActive
1101	RxActive
1110	Subcarrier detected
1111	TstBusBit

Each signal can be switched to pin AUX1 or AUX2 by setting SelAux1 or SelAux2 in the register AnalogTestReg.

Note: The DAC has a current output, it is recommended to use a 1 kΩ pull-down resistance at pins AUX1/AUX2.

19.4 PRBS

Enables the PRBS9 or PRBS15 sequence according to ITU-TO150. To start the transmission of the defined datastream the command send has to be activated. The preamble/Sync byte/start bit/parity bit are generated automatically depending on the selected mode.

Note: All relevant register to transmit data have to be configured before entering PRBS mode according ITU-TO150.

20. Application design-in information

The figure below shows a typical circuit diagram, using a complementary antenna connection to the PN512.

The antenna tuning and RF part matching is described in the application note “NFC Transmission Module Antenna and RF Design Guide”.

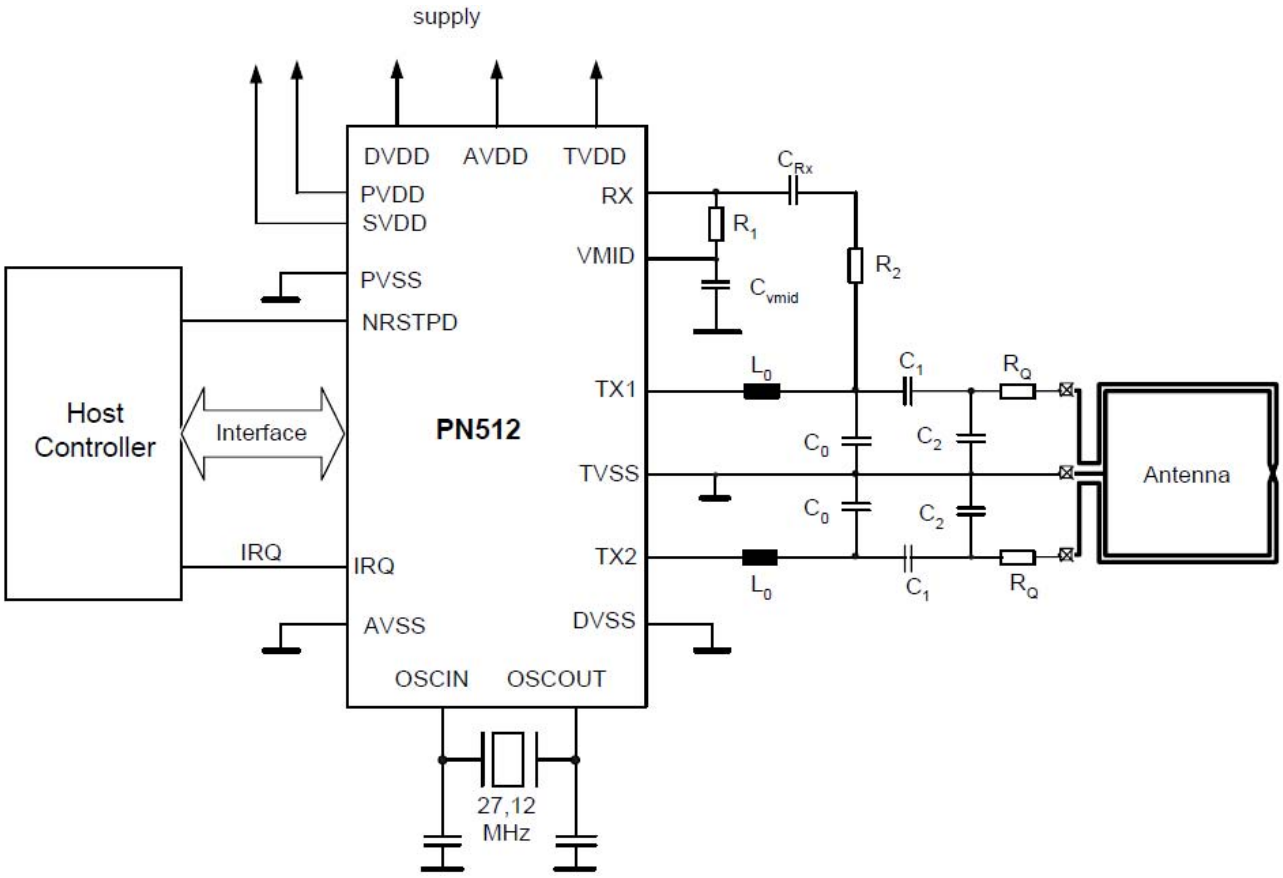


Fig 38. Typical circuit diagram

21. Limiting values

Table 162. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
AV_{DD}	Supply voltage		-0.5	+4.0	V
DV_{DD}					
PV_{DD}					
TV_{DD}					
SV_{DD}					
$V_{in, abs}$	Input voltage	for all input-pins except SigIn and Rx	PV_{SS} -0.5	PV_{DD} +0.5	V
$V_{in, SigIn}$		for SigIn	PV_{SS} -0.5	SV_{DD} +0.5	V
P_{tot}	Total power dissipation per package (V_{BUS} and DV_{DD} in short cut mode)		-	200	mW
T_J	Junction temperature range			100	°C
ESDH	ESD Susceptibility (Human Body model)	1500 Ω, 100 pF; JESD22-A114-B		2000	V
ESDM	ESD Susceptibility (Machine model)	0.75 μH, 200 pF; JESD22-A114-A		200	V
ESDC	ESD Susceptibility (Charge Device model)	Field induced model; JESC22-C101-A		500	V

22. Recommended operating conditions

Table 163. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb}	Ambient Temperature	HVQFN32, HVQFN40		-30	-	+85	°C
AV_{DD}	Supply Voltage	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V , $PV_{DD} \leq AV_{DD} = DV_{DD} = TV_{DD}$	[1][2]	2.5	-	3.6	V
DV_{DD}			[1][2]				
TV_{DD}			[1][2]				
PV_{DD}			[3]	1.6	-	3.6	V
SV_{DD}	Supply Voltage	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V		1.6	-	3.6	V

[1] Supply voltage below 3 V reduces the performance (e.g. the achievable operating distance).

[2] AV_{DD}, DV_{DD} and TV_{DD} shall always be on the same voltage level.

[3] PV_{DD} shall always be on the same or lower voltage level than DV_{DD}.

23. Thermal characteristics

Table 164. Thermal characteristics

Symbol	Parameter	Conditions	Package	Typ	Unit
R_{thj-a}	Thermal resistance from junction to ambient	In still air with exposed pad soldered on a 4 layer Jedec PCB In still air	HVQFN32	40	K/W
			HVQFN40	35	K/W

24. Characteristics

24.1 Input pin characteristics

24.1.1 Input pin characteristics for pins A0, A1, A2, A3, A4, A5, NCS, NWR, NRD and NRESET

Table 165. Input pin characteristics for pins A0, A1, A2, A3, A4, A5, NCS, NWR, NRD, SIGIN and NRESET

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 PV_{DD}	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 PV_{DD}	V

24.1.2 Input pin characteristics for pin SIGIN

Table 166. Input pin characteristics for Pin SIGIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 SV_{DD}	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 SV_{DD}	V

24.1.3 Input/Output pin characteristics for pins D0, D1, D2, D3, D4, D5, D6 and D7

Table 167. Input/Output pin characteristics for pins D0, D1, D2, D3, D4, D5, D6 and D7

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 PV_{DD}	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 PV_{DD}	V
V_{OH}	Output voltage High	PV_{DD} = 3 V, I_O = 4 mA	PV_{DD} -400 mV	-	PV_{DD}	V
V_{OL}	Output voltage LOW	PV_{DD} = 3 V, I_O = 4 mA	PV_{SS}	-	PV_{SS} +400 mV	V
I_{OL}	Output current drive LOW	PV_{DD} = 3 V	-	-	4	mA
I_{OH}	Output current drive HIGH	PV_{DD} = 3 V	-	-	4	mA

24.1.4 Input pin characteristics for pin ALE

Table 168. Input pin characteristics for Pin ALE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage HIGH		0.7 PV_{DD}	-	-	V
V_{IL}	Input voltage LOW		-	-	0.3 PV_{DD}	V

24.1.5 Output pin characteristics for pin SIGOUT

Table 169. Output pin characteristics for Pin SIGOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output voltage HIGH	SV_{DD} = 3 V, I_O = 4 mA	SV_{DD} -400 mV	-	SV_{DD}	V
V_{OL}	Output voltage LOW	SV_{DD} = 3 V, I_O = 4 mA	PV_{SS}	-	PV_{SS} +400 mV	V
I_{OL}	Output current drive LOW	SV_{DD} = 3 V	-	-	4	mA
I_{OH}	Output current drive HIGH	SV_{DD} = 3 V	-	-	4	mA

24.1.6 Output pin characteristics for pin IRQ

Table 170. Input/Output pin characteristics for Pin IRQ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output voltage HIGH	PV_{DD} = 3 V, I_O = 4 mA	PV_{DD} -400 mV	-	PV_{DD}	V
V_{OL}	Output voltage LOW	PV_{DD} = 3 V, I_O = 4 mA	PV_{SS}	-	PV_{SS} +400 mV	V
I_{OL}	Output current drive LOW	PV_{DD} = 3 V	-	-	4	mA
I_{OH}	Output current drive HIGH	PV_{DD} = 3 V	-	-	4	mA

24.1.7 Input pin characteristics for pin Rx

Table 171. Input/Output pin characteristics for Pin Rx

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{IN,RX}$	Input voltage range		[1]	-1	-	AV_{DD} +1 V	V
$C_{IN,RX}$	RX Input capacitance	AV_{DD} = 3 V, Receiver active, V_{RX} = 1 V_{PP}, 1.5 V_{DC} offset		-	10	-	pF
$R_{IN,RX}$	RX Input Series resistance	AV_{DD} = 3 V, Receiver active, V_{RX} = 1 V_{PP}, 1.5 V_{DC} offset		-	350	-	Ω

[1] The voltage on RX in clamped by internal diodes to AV_{SS} and AV_{DD}.

24.1.8 Input pin characteristics for pin OSCIN

Table 172. Input pin characteristics for OSCIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 AV_{DD}	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 AV_{DD}	V
C_{OSCIN}	Input capacitance	AV_{DD} = 2.8 V, V_{DC} = 0.65 V, V_{AC} = 1 V_{PP}	-	2	-	pF

24.1.9 Output pin characteristics for pins AUX1 and AUX2

Table 173. Input/Output pin characteristics for pins AUX1 and AUX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output voltage HIGH	DV_{DD} = 3 V, I_O = 4 mA	DV_{DD} -400 mV	-	DV_{DD}	V
V_{OL}	Output voltage LOW	DV_{DD} = 3 V, I_O = 4 mA	DV_{SS}	-	DV_{SS} +400 mV	V
I_{OL}	Output current drive LOW	DV_{DD} = 3 V	-	-	4	mA
I_{OH}	Output current drive HIGH	DV_{DD} = 3 V	-	-	4	mA

24.1.10 Output pin characteristics for pins TX1 and TX2

Table 174. Input/Output pin characteristics for pins TX1 and TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH,C32,3V}$	Output voltage HIGH	TV_{DD} = 3 V and I_{TX} = 32 mA, CWGsP = 3 F(hex)	TV_{DD} - 150 mV	-	-	mV
$V_{OH,C80,3V}$		TV_{DD} = 3 V and I_{TX} = 80 mA, CWGsP = 3 F(hex)	TV_{DD} - 400 mV	-	-	mV
$V_{OH,C32,2V5}$		TV_{DD} = 2.5 V and I_{TX} = 32 mA, CWGsP = 3 F(hex)	TV_{DD} - 240 mV	-	-	mV
$V_{OH,C80,2V5}$		TV_{DD} = 2.5 V and I_{TX} = 80 mA, CWGsP = 3 F(hex)	TV_{DD} - 640 mV	-	-	mV
$V_{OLC32,3V}$	Output voltage LOW	TV_{DD} = 3 V and I_{TX} = 32 mA, CWGsP = 3 F(hex)	-	-	150	mV
$V_{OL,C80,3V}$		TV_{DD} = 3 V and I_{TX} = 80 mA, CWGsP = 3 F(hex)	-	-	400	mV
$V_{OL,C32,2V5}$		TV_{DD} = 2.5 V and I_{TX} = 32 mA, CWGsP = 3 F(hex)	-	-	240	mV
$V_{OL,C80,2V5}$		TV_{DD} = 2.5 V and I_{TX} = 80 mA, CWGsP = 3 F(hex)	-	-	640	mV

24.2 Current consumption

Table 175. Current consumption

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{HPD}	Hard Power-down Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, N_{RESET} = LOW	[4]	-	-	5	µA
I_{SPD}	Soft Power-down Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, RF level detector on	[4]	-	-	10	µA
I_{DVDD}	Digital Supply Current	$DV_{DD} = 3$ V		-	6.5	9	mA
I_{AVDD}	Analog Supply Current	$AV_{DD} = 3$ V, bit RCVOff = 0		-	7	10	mA
$I_{AVDD,RCVOFF}$	Analog Supply Current, receiver switched off	$AV_{DD} = 3$ V, bit RCVOff = 1		-	3	5	mA
I_{PVDD}	Pad Supply Current		[2]	-	-	40	mA
I_{TVDD}	Transmitter Supply Current	Continuous Wave	[1][3][5]	-	60	100	mA
I_{SVDD}	S^2C Pad Supply Current		[6]	-	-	4	mA

[1] I_{TVDD} depends on TV_{DD} and the external circuitry connected to Tx1 and Tx2

[2] I_{PVDD} depends on the overall load at the digital pins.

[3] During operation with a typical circuitry the overall current is below 100 mA.

[4] I_{SPD} and I_{HPD} are the total currents over all supplies.

[5] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between TX1 and TX2 at 13.56 MHz

[6] IS_{VDD} depends on the load at the SIGOUT pin.

24.3 RX input voltage range

Table 176. RX input voltage range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RX,MinIV,Mill}$	Minimum Input voltage, Miller coded	$AV_{DD} = 3$ V, 106 kbit	-	150	-	mVpp
$V_{RX,MinIV,Man}$	Minimum Input voltage, Manchester Coded	$AV_{DD} = 3$ V, 212 and 424 kbit	-	100	-	mVpp
$V_{RX,MaxIV,Mill}$	Maximum Input voltage, Miller coded	$AV_{DD} = 3$ V, 106 kbit	-	4	-	Vpp
$V_{RX,MaxIV,Man}$	Maximum Input voltage, Manchester Coded	$AV_{DD} = 3$ V, 212 and 424 kbit	-	4	-	Vpp

Figure 39 “RX input voltage range” outlines the voltage definitions.

24.4 RX input sensitivity

Table 177. RX input sensitivity

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$m_{RX,Mill}$	Minimum Modulation index, Miller coded	AV_{DD} = 3 V, 106 kbit V_{RX} = 1.5 V_{PP}, SensMiller = 3		-	33	-	%
$V_{RXMod,Man}$	Minimum modulation voltage	AV_{DD} = 3 V, RxGain = 7	[1]	-	5	-	mV

[1] The minimum modulation voltage is valid for all modulation schemes except Miller coded signals.

Figure 39 “RX input voltage range” outlines the voltage definitions.

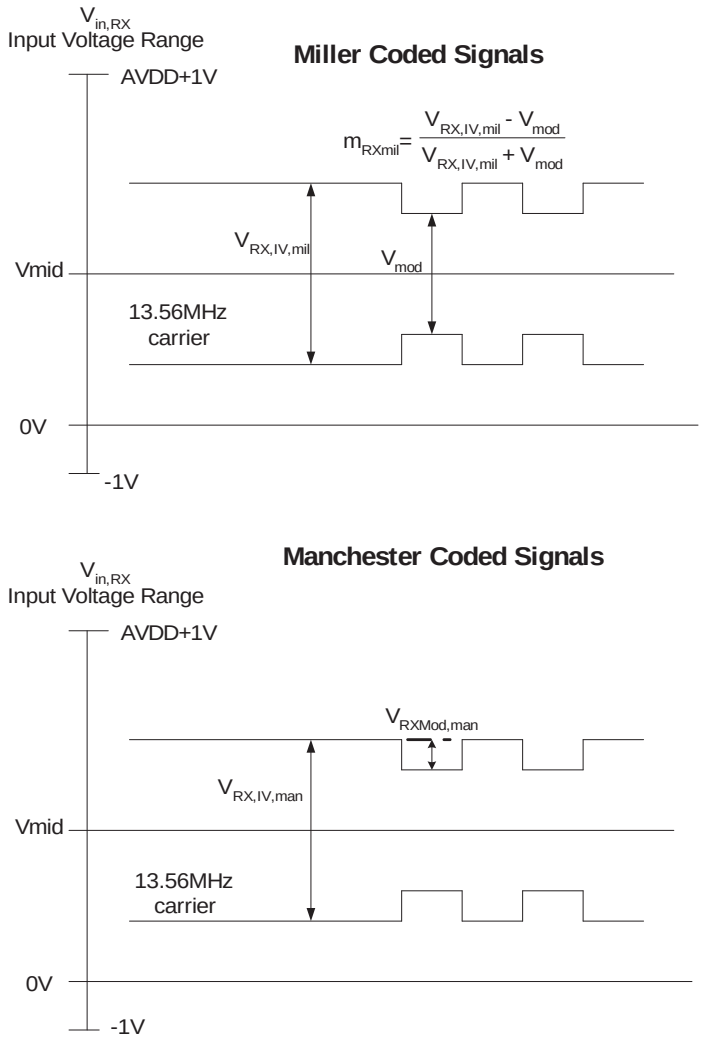


Fig 39. RX input voltage range

24.5 Clock frequency

Table 178. Clock frequency

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSCIN}	Clock Frequency		-	27.12	-	MHz
d_{FEC}	Duty Cycle of Clock Frequency		40	50	60	%
t_{jitter}	Jitter of Clock Edges		-	-	10	ps, RMS

24.6 XTAL oscillator

Table 179. XTAL oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH,OSCOUT}$	Output Voltage High XTAL2		-	1.1	-	V
$V_{OL,OSCOUT}$	Output Voltage Low XTAL2		-	0.2	-	V
$C_{IN,OSCIN}$	Input capacitance OSCIN		-	2	-	pF

24.7 Typical 27.12 MHz crystal requirements

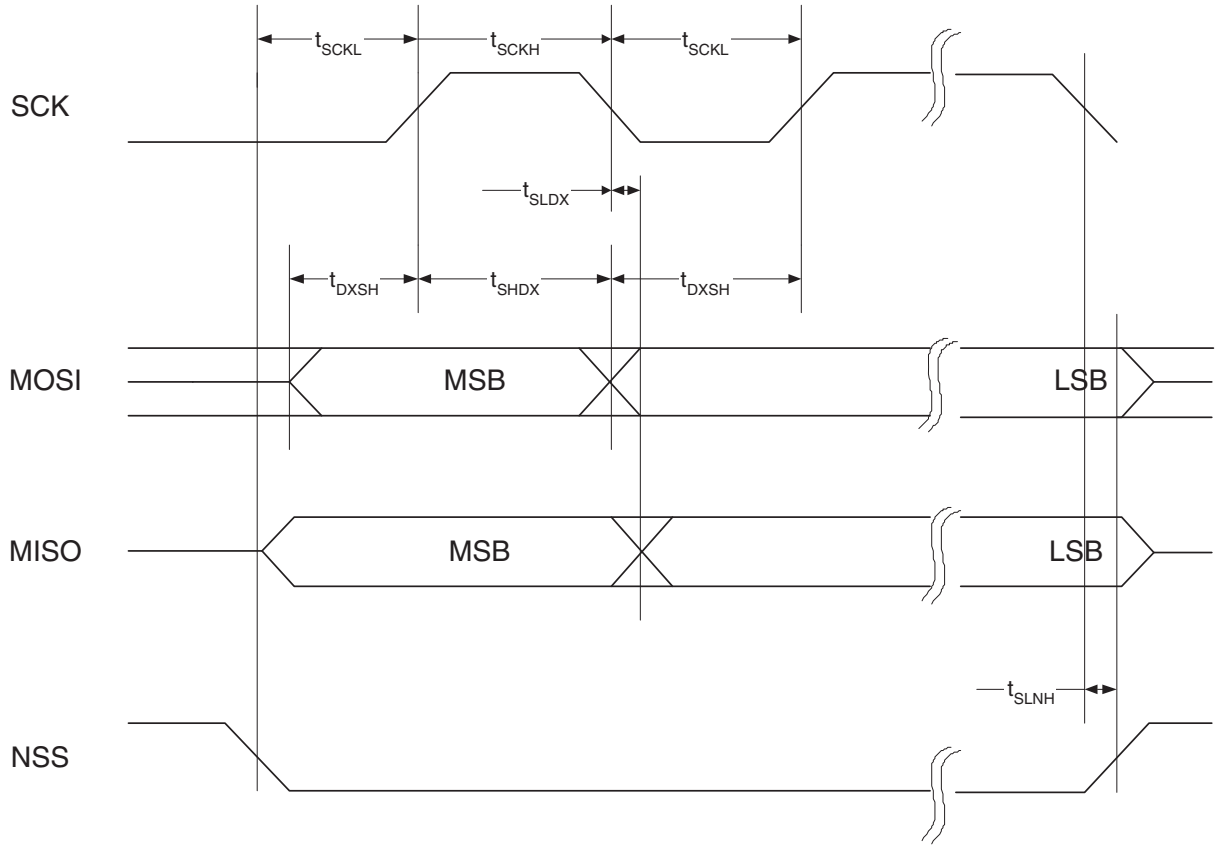
Table 180. XTAL oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XTAL}	XTAL Frequency Range		-	27.12	-	MHz
ESR	XTAL Equivalent Series resistance		-	-	100	Ω
C_L	XTAL Load capacitance		-	10	-	pF
P_{XTAL}	XTAL Drive Level		-	50	100	W

24.8 Timing for the SPI compatible interface

Table 181. Timing specification for SPI

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{NHNL}	NSS high before communication		50		-	ns
t_{SCKL}	SCK low pulse width		50		-	ns
t_{SCKH}	SCK high pulse width		50		-	ns
t_{SHDX}	SCK high to data changes		25		-	ns
t_{DXSH}	data changes to SCK high		25		-	ns
t_{SLDX}	SCK low to data changes		-		25	ns
t_{SLNH}	SCK low to NSS high		0		-	ns



Remark: The signal NSS has to be low to be able to send several bytes in one datastream.
To send more than one datastream NSS has to be set to HIGH level in between the data streams.

Fig 40. Timing diagram for SPI

24.9 I²C timing

Table 182. Overview I²C timing in fast mode

Symbol	Parameter	Fast mode		High speed mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	400	0	3400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	600	-	160	-	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	600	-	160	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	600	-	160	-	ns
t_{LOW}	LOW period of the SCL clock	1300	-	160	-	ns
t_{HIGH}	HIGH period of the SCL clock	600	-	60	-	ns
$t_{HD;DAT}$	Data hold time	0	900	0	70	ns
$t_{SU;DAT}$	Data set-up time	100	-	10	-	ns
t_{rscl}	Rise time SCL signals	20	300	10	40	ns
t_{fscl}	Fall time SCL signals	20	300	10	40	ns
t_{rsda}	Rise time of both SDA and SCL signals	20	300	10	80	ns
t_{rsda}	Fall time of both SDA and SCL signals	20	300	10	80	ns
t_{BUF}	Bus free time between a STOP and START condition	1.3	-	1.3	-	µs

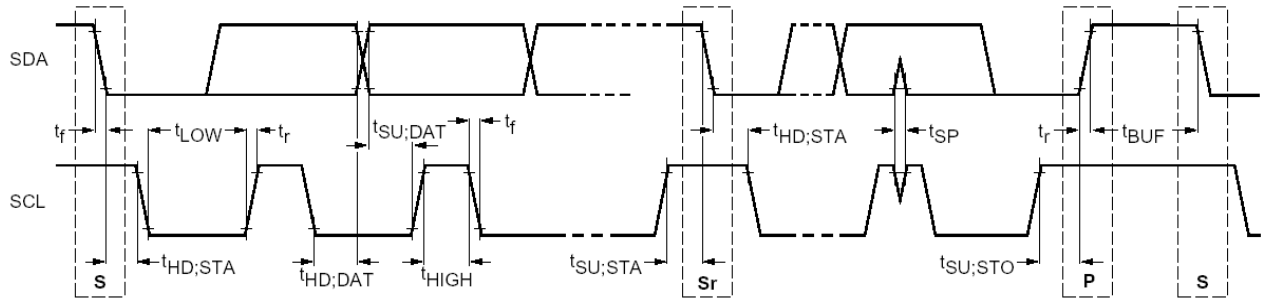


Fig 41. Timing for F/S mode devices on the I²C-bus

24.10 8-bit parallel interface timing

24.10.1 AC symbols

Each timing symbol has five characters. The first character is always 't' for time. The other characters indicate the name of a signal or the logic state of that signal (depending on position):

Table 183. AC symbols

Designation	Signal	Designation	Logic Level
A	address	H	HIGH
D	data	L	LOW
W	NWR or nWait	Z	high impedance
R	NRD or R/NW or nWrite	X	any level or data
L	ALE or AS	V	any valid signal or data
C	NCS	N	NSS
S	NDS or nDStrb and nAStrb, SCK		

Example: t_{AVLL} = time for address valid to ALE low

24.10.2 AC operating specification

24.10.2.1 Bus timing for separated Read/Write strobe

Table 184. Timing specification for separated Read/Write strobe

Symbol	Parameter	Min	Max	Unit
t_{LHLL}	ALE pulse width	10	-	ns
t_{AVLL}	Multiplexed Address Bus valid to ALE low (Address Set Up Time)	5	-	ns
t_{LLAX}	Multiplexed Address Bus valid after ALE low (Address Hold Time)	5	-	ns
t_{LLWL}	ALE low to NWR, NRD low	10	-	ns
t_{CLWL}	NCS low to NRD, NWR low	0	-	ns
t_{WHCH}	NRD, NWR high to NCS high	0	-	ns
t_{RLDV}	NRD low to DATA valid	-	35	ns
t_{RHDZ}	NRD high to DATA high impedance	-	10	ns
t_{DVWH}	DATA valid to NWR high	5	-	ns
t_{WHDX}	DATA hold after NWR high (Data Hold Time)	5	-	ns
t_{WLWH}	NRD, NWR pulse width	40	-	ns
t_{AVWL}	Separated Address Bus valid to NRD, NWR low (Set Up Time)	30	-	ns
t_{WHAX}	Separated Address Bus valid after NWR high (Hold Time)	5	-	ns
t_{WHWL}	period between sequenced read / write accesses	40	-	ns

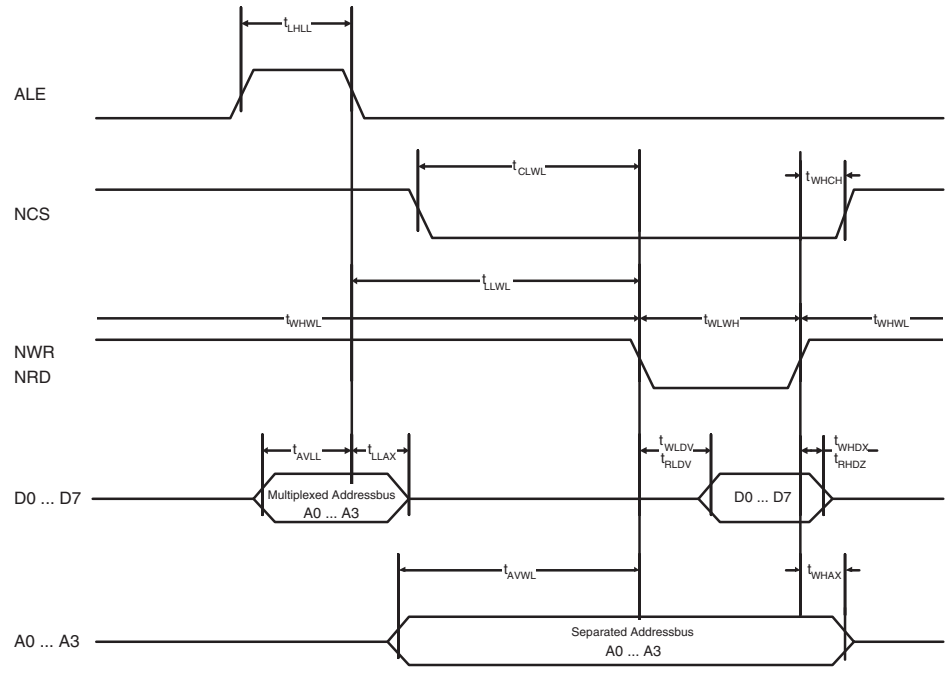


Fig 42. Timing diagram for separated Read/Write strobe

Remark: For separated address and data bus the signal ALE is not relevant and the multiplexed addresses on the data bus don't care.

For the multiplexed address and data bus the address lines A0 to A3 have to be connected as described in chapter Automatic host controller Interface Type Detection.

24.10.2.2 Bus timing for common Read/Write strobe

Table 185. Timing specification for common Read/Write strobe

Symbol	Parameter	Min	Max	Unit
t_{LHLL}	AS pulse width	10	-	ns
t_{AVLL}	Multiplexed Address Bus valid to AS low (Address Set Up Time)	5	-	ns
t_{LLAX}	Multiplexed Address Bus valid after AS low (Address Hold Time)	5	-	ns
t_{LLSL}	AS low to NDS low	10	-	ns
t_{CLSL}	NCS low to NDS low	0	-	ns
t_{SHCH}	NDS high to NCS high	0	-	ns
$t_{SLDV,R}$	NDS low to DATA valid (for read cycle)	-	35	ns
t_{SHDZ}	NDS low to DATA high impedance (read cycle)	-	10	ns
t_{DVSH}	DATA valid to NDS high (for write cycle)	5	-	ns
t_{SHDX}	DATA hold after NDS high (write cycle, Hold Time)	5	-	ns
t_{SHRX}	R/NW hold after NDS high	5	-	ns
t_{SLSH}	NDS pulse width	40	-	ns
t_{AVSL}	Separated Address Bus valid to NDS low (Hold Time)	30	-	ns
t_{SHAX}	Separated Address Bus valid after NDS high (Set Up Time)	5	-	ns

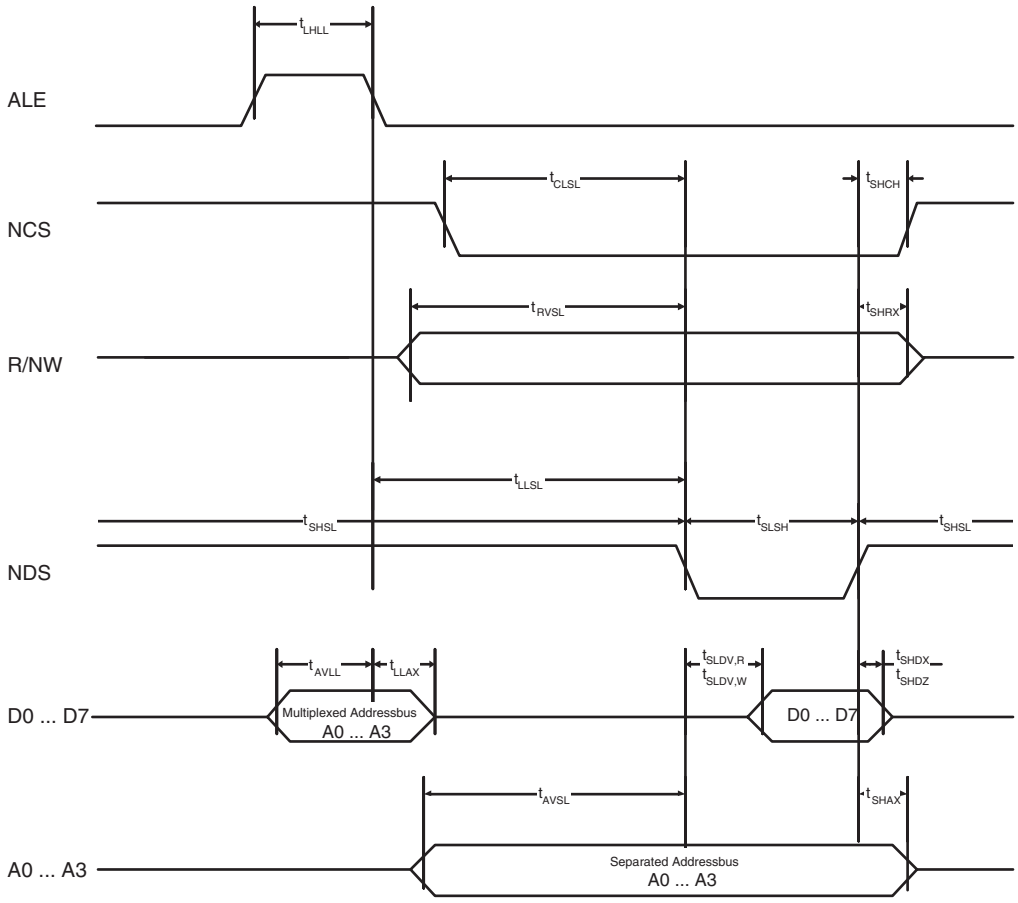


Fig 43. Timing diagram for common Read/Write strobe

Remark: For separated address and data bus the signal ALE is not relevant and the multiplexed addresses on the data bus don't care. For the multiplexed address and data bus the address lines A0 to A3 have to be connected as described in Automatic μ-Controller Interface Type Detection.

25. Package information

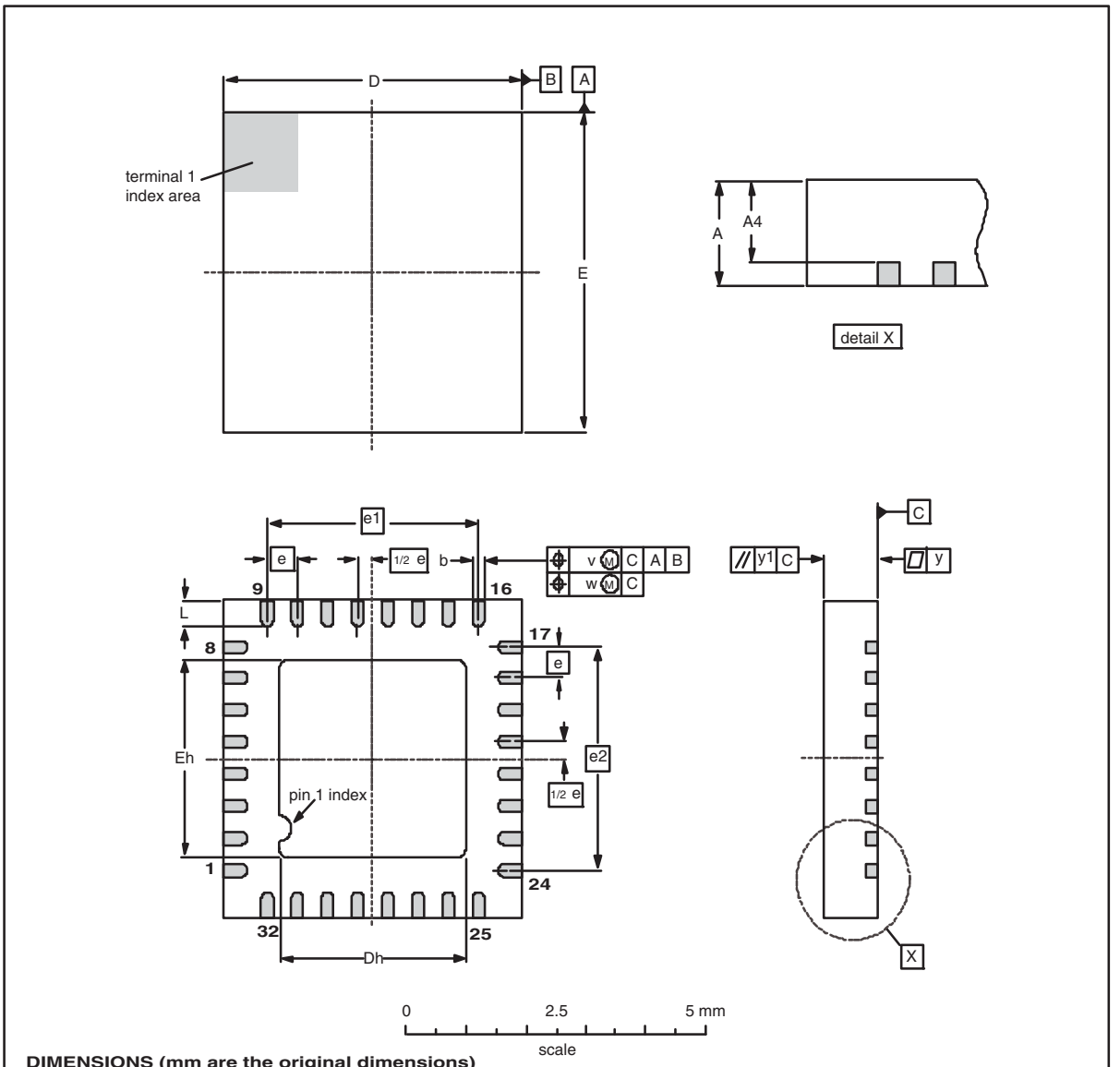
The PN512 can be delivered in 2 different packages.

Table 186. Package information

Package	Remarks
HVQFN32	8-bit parallel interface not supported
HVQFN40	Supports the 8-bit parallel interface

26. Package outline

HVQFN32: plastic, heatsink very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A4 max.	b	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1.00	0.80	0.35 0.18	5.05 4.95	3.25 2.95	5.05 4.95	3.25 2.95	0.5	3.5	3.5	0.50 0.30	0.2	0.1	0.05	0.1

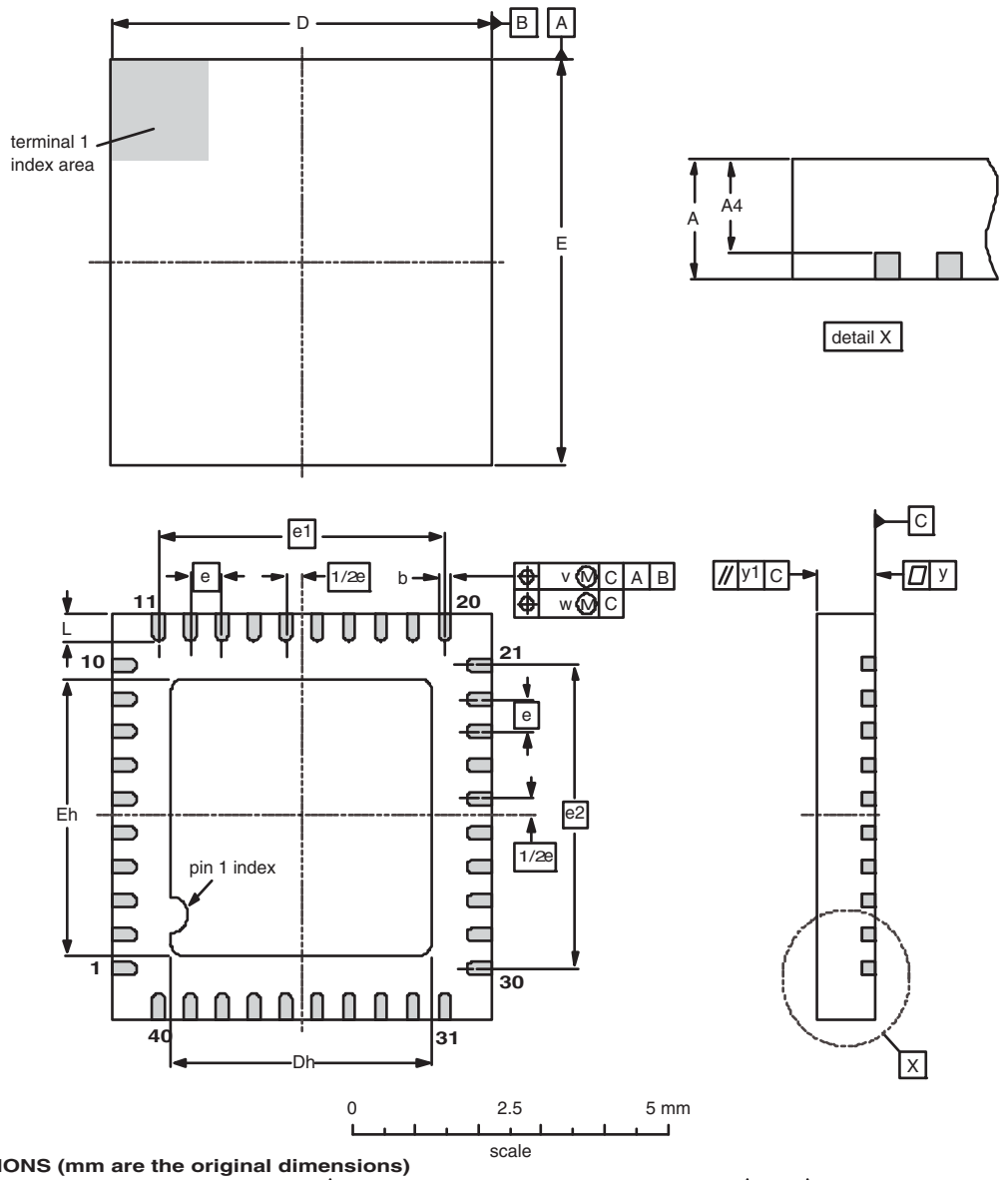
Note

1. Plastic or metal protrusions of 0.076 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT617-1		MO-220				~~01-06-07~~ 01-08-08

Fig 44. Package outline package version (HVQFN32)

HVQFN40: plastic, heatsink very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A4 max.	b	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1.00	0.80	0.35 0.18	6.05 5.95	4.25 3.95	6.05 5.95	4.25 3.95	0.5	4.5	4.5	0.50 0.30	0.2	0.1	0.05	0.1

Note

1. Plastic or metal protrusions of 0.076 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT618-1		MO-220				~~01-06-07~~ 01-08-08

Fig 45. Package outline package version (HVQFN40)

27. Abbreviations

Table 187. Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
SOF	Start of frame
EOF	End of frame
PCD	Proximity Coupling Device. Definition for a Card reader/writer according to the ISO/IEC 14443 specification.
PICC	Proximity Cards. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification.
PCD → PICC	Communication flow between a PCD and a PICC according to the ISO/IEC 14443A/MIFARE
PICC → PCD	Communication flow between a PICC and a PCD according to the ISO/IEC 14443A/MIFARE.
Initiator	Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
Modulation Index	The modulation index is defined as the voltage ratio (Vmax - Vmin)/ (Vmax + Vmin).
Loadmodulation Index	The load modulation index is defined as the card's voltage ratio (Vmax - Vmin)/ (Vmax + Vmin) measured at the card's coil.
Target	Responds to initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self generated RF field (no RF field generated by initiator).

28. Revision history

Table 188. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
111334	8 September 2009	Product data sheet		Revision 3.3
Modifications:	• Section 8.2.3.10 on page 45 ISO14443B mode added • Table 90 on page 45: update of ftimer definition • Table 92 on page 46 update of ftimer definition • Section 13 on page 91: Add-on of a formula for time calculation • Section 19.2 on page 103 Add-on new TestSignal			
111333	21 January 2009	Product data sheet		Revision 3.2
Modifications:	• General rewording of MIFARE designation and commercial conditions • Section 8.2.1.9 “Status2Reg” on page 20: update “2 to 0 modem state” specification • Section 8.2.1.10 “FIFODataReg” on page 21: update Timer specification as well as Ftimer definition • Section 10.3.1 “Connection to a host controller” on page 66: update block diagram • Section 13 “Timer unit” on page 91: Wording correction • Section 24.8 “Timing for the SPI compatible interface” on page 114: Add-on new timing on SPI interface			
111332	June 2007	Product data sheet		Revision 3.1
111331	January 2007	Product data sheet		Revision 3.0
111330	October 2006	Product data sheet		Revision 1.0
111310	June 2005			
Modifications:	• Initial version			

29. Legal information

29.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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31. Tables

continued >>

continued >>

continued >>

32. Figures

continued >>

33. Contents

continued >>

continued >>

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