

# CD4041UB Types

## CMOS Quad True/Complement Buffer

### High Voltage Types (20-Volt Rating)

■ CD4041UB types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing or sinking) capability. The CD4041UB is intended for use as a buffer, line driver, or CMOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low power dissipation are primary design requirements.

The CD4041UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

#### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	
Voltages referenced to $V_{SS}$ Terminal)	..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	..... -0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	..... $\pm 10mA$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55^\circ C$ to $+100^\circ C$	..... 500mW
For $T_A = +100^\circ C$ to $+125^\circ C$	..... Derate Linearly at 12mW/ $^\circ C$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	..... 100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	..... $-55^\circ C$ to $+125^\circ C$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	..... $-65^\circ C$ to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max	..... $+265^\circ C$

#### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A$ =Full Package-Temperature Range)	3	18	V

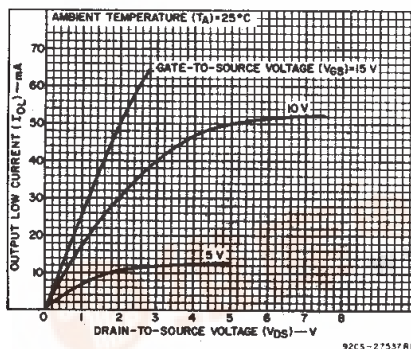


Fig. 2 - Typical output low (sink) current characteristics.

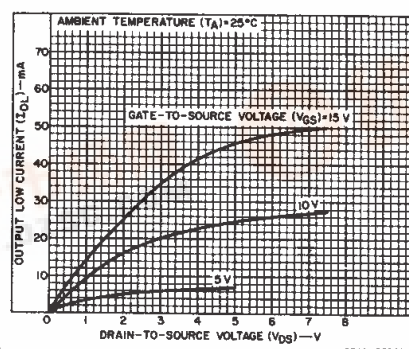


Fig. 3 - Minimum low (sink) current characteristics.

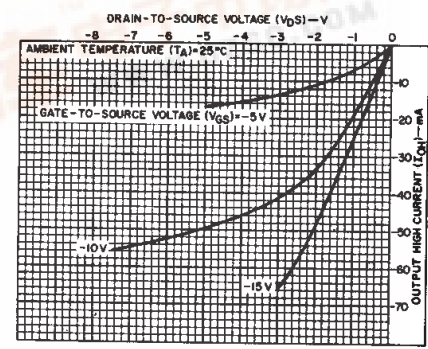


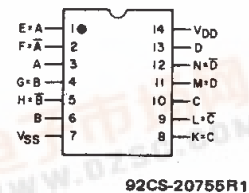
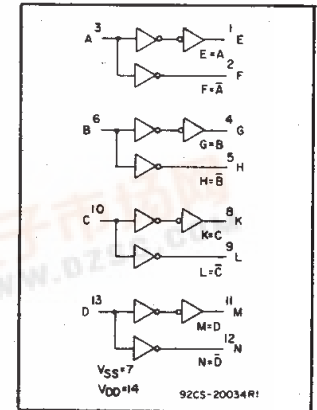
Fig. 4 - Typical output high (source) current characteristics.

#### Features:

- Balanced sink and source current; approximately 4 times standard "B" drive
- Equalized delay to true and complement outputs
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu A$  at 18 V over full package temperature range; 100 nA at 18 V and  $25^\circ C$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

#### Applications:

- High current source/sink driver
- CMOS-to-DTL/TTL Converter Buffer
- Display driver
- MOS clock driver
- Resistor network driver (Ladder or weighted R)
- Buffer
- Transmission line driver



TOP VIEW  
TERMINAL ASSIGNMENT

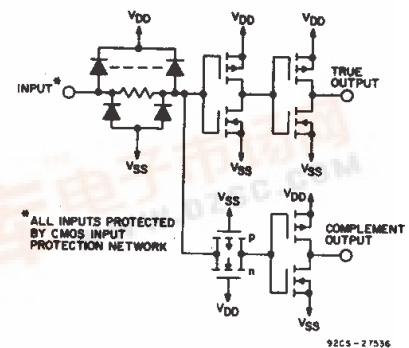


Fig. 1 - Schematic diagram 1 of 4 buffers.

# CD4041UB Types

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## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current I <sub>DD</sub> Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0,5	5	2.1	1.8	1.3	1.2	1.6	3.2	—	mA
	0.5	0,10	10	6.25	5.6	4	3.5	5	10	—	
	1.5	0,15	15	24	23	15.5	13	19	38	—	
	4.6	0,5	5	-2.1	-1.8	-1.3	-1.2	-1.6	-3.2	—	
Output High (Source) Current, I <sub>OH</sub> Min.	2.5	0,5	5	-8.4	-6.7	-5.3	-4.6	-6.4	-12.8	—	mA
	9.5	0,10	10	-6.25	-5.6	-4	-3.5	-5	-10	—	
	13.5	0,15	15	-24	-23	-15.5	-13	-19	-38	—	
	—	—	—	—	—	—	—	—	—	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
	—	—	—	—				—	—	—	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
	—	—	—	—				—	—	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5,4.5	—	5	1				—	—	1	V
	1,9	—	10	2				—	—	2	
	1.5,13.5	—	15	2.5				—	—	2.5	
	—	—	—	—				—	—	—	
Input High Voltage, V <sub>IH</sub> Min.	0.5,4.5	—	5	4				4	—	—	V
	1,9	—	10	8				8	—	—	
	1.5,13.5	—	15	12.5				12.5	—	—	
	—	—	—	—				—	—	—	
Input Current, I <sub>IN</sub> Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA

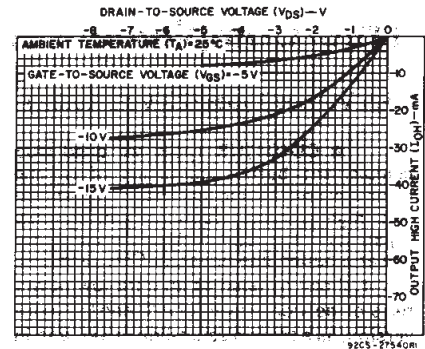


Fig. 5 — Minimum output high (source) current characteristics.

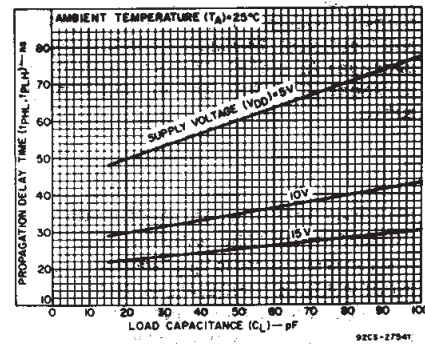


Fig. 6 — Typical propagation delay time vs. load capacitance.

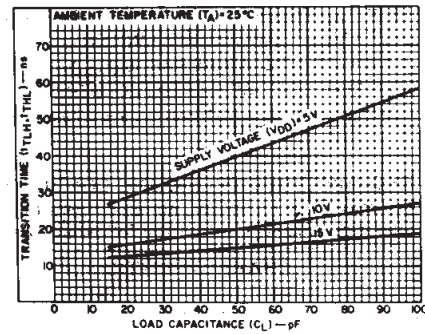


Fig. 7 — Typical transition time vs. load capacitance.

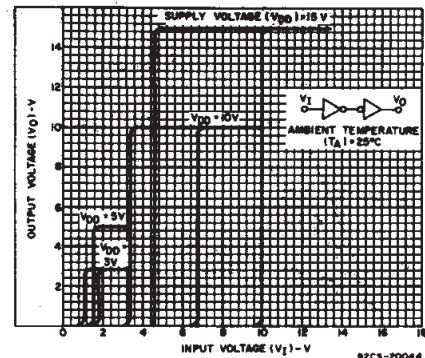


Fig. 8 — Minimum and maximum transfer characteristics — true output.

DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200 kΩ

CHARACTERISTIC	CONDITIONS	LIMITS		UNITS
		V <sub>DD</sub> Volts	Typ.    Max.	
Propagation Delay Time: t <sub>PHL</sub> , t <sub>PLH</sub>		5 10 15	60    120 35    70 25    50	ns
Transition Time        t <sub>THL</sub> , t <sub>TLH</sub>		5 10 15	40    80 20    40 15    30	ns
Input Capacitance    C <sub>IN</sub>	Any Input		15    22.5	pF

# CD4041UB Types

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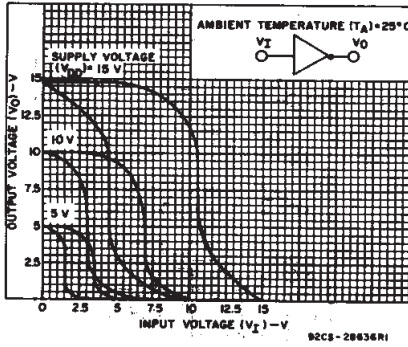


Fig. 9 - Minimum and maximum transfer characteristics - complement output.

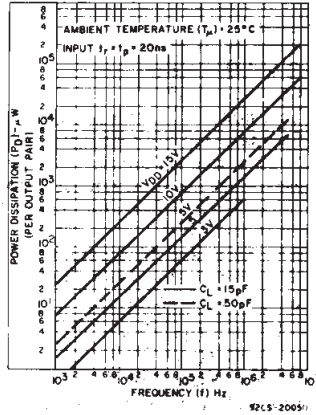


Fig. 11 - Typical power dissipation vs frequency per output pair.

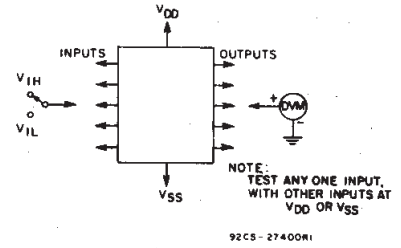


Fig. 13 - Input voltage test circuit.

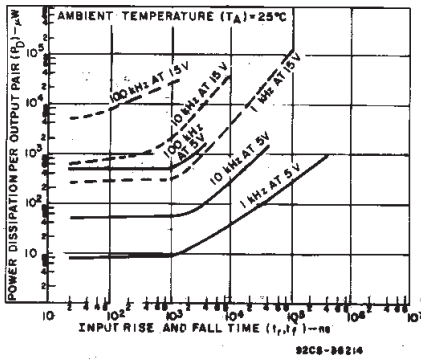


Fig. 10 - Typical power dissipation vs. input rise & fall time per output pair.

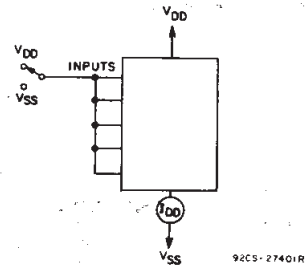


Fig. 12 - Quiescent device current test circuit.

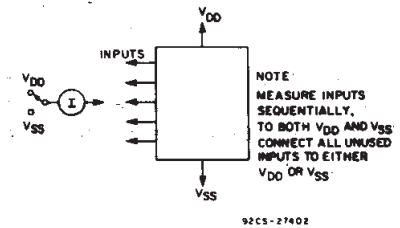
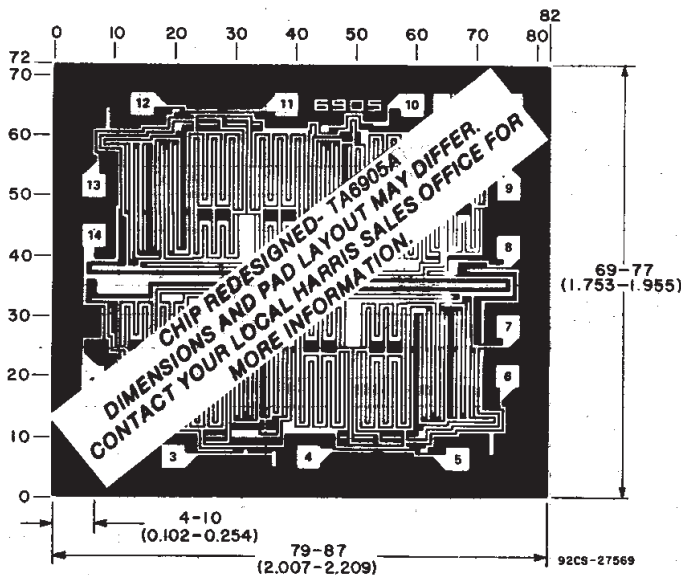


Fig. 14 - Input-leakage-current test circuit.

## Dimensions and pad layout for the CD4041UBH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD4041UBE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4041UBEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4041UBF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
CD4041UBF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
CD4041UBM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4041UBPWG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

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package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

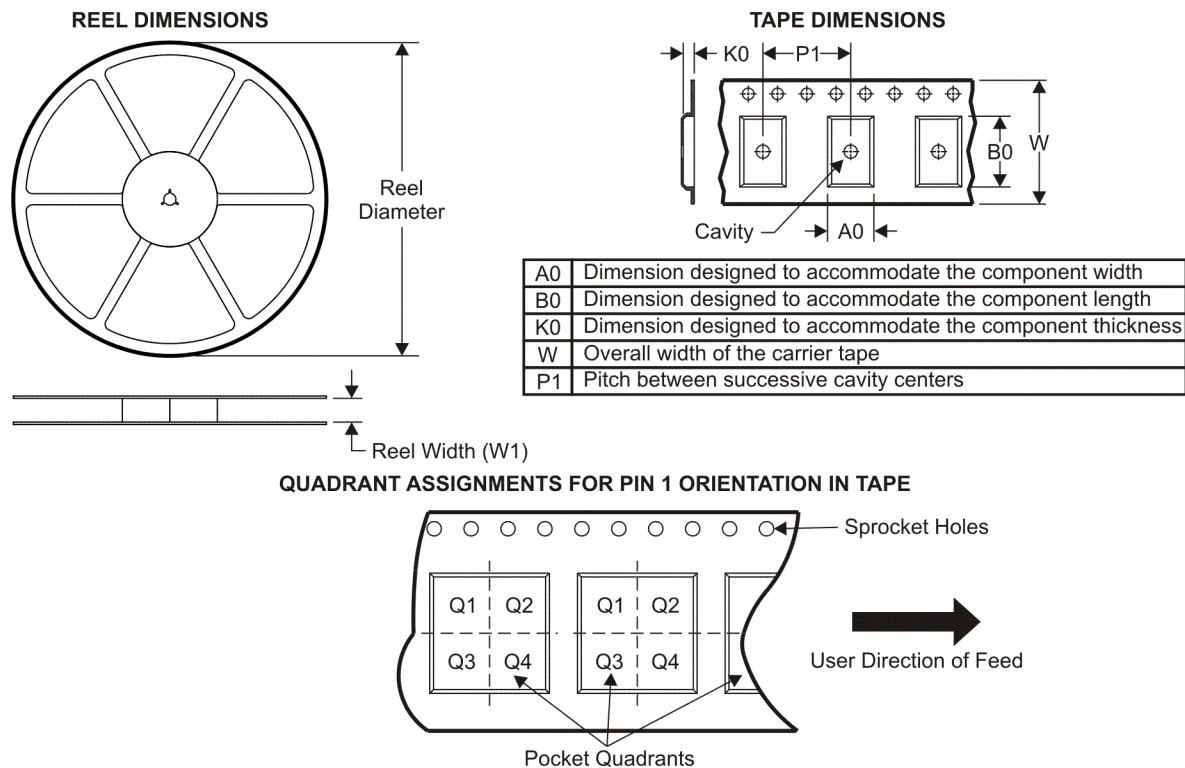
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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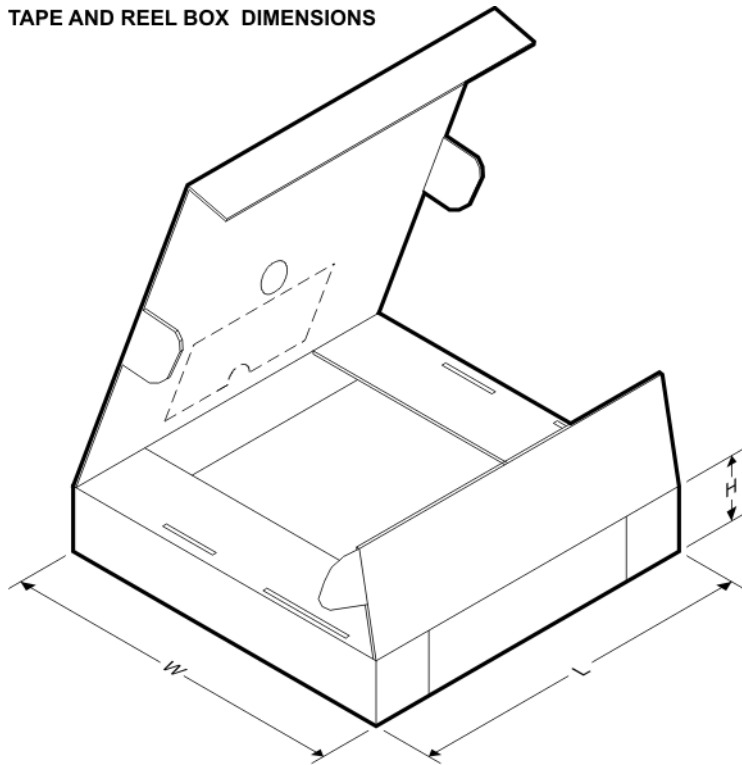
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4041UBM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4041UBMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4041UBPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



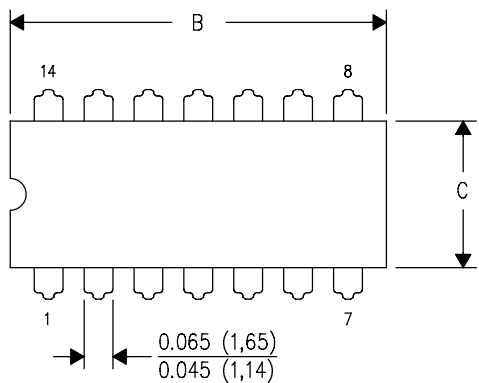
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4041UBM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4041UBMT	SOIC	D	14	250	346.0	346.0	33.0
CD4041UBPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

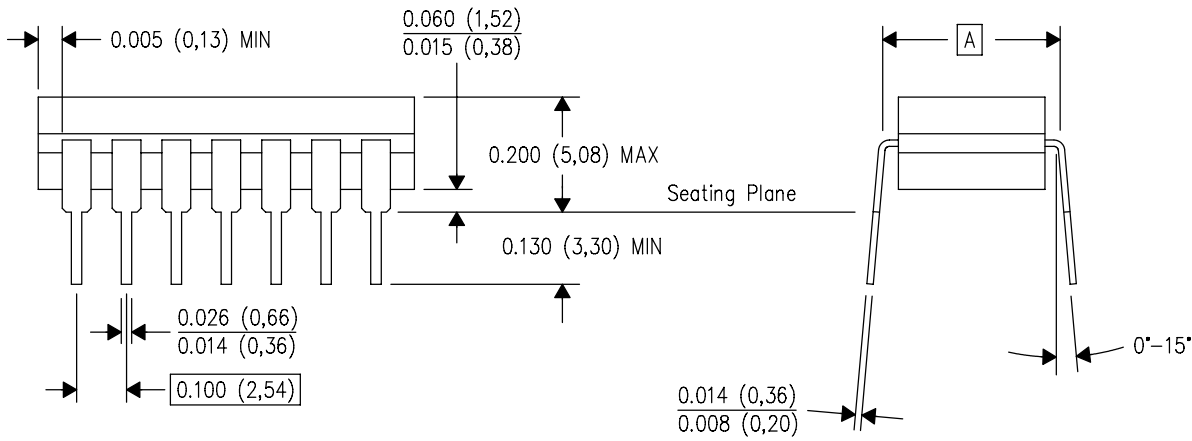
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



16 PINS SHOWN



Technical drawing of a connector housing showing dimensions and tolerances. The drawing includes a side view of the housing with a circular inset showing a detail of a pin. Dimensions are given in inches (mm) with tolerances in parentheses. A 'Seating Plane' is indicated for the pin detail.



Dimensions and Tolerances:

- Top Left:  $0.045 (1,14)$  (Total Width),  $0.030 (0,76)$  (Pin Pitch),  $\triangle D$  (Surface Finish)
- Top Center:  $0.020 (0,51) \text{ MIN}$  (Pin Height)
- Top Right:  $0.325 (8,26)$  (Housing Width),  $0.300 (7,62)$  (Pin Array Width)
- Center:  $0.200 (5,08) \text{ MAX}$  (Pin Height),  $0.125 (3,18) \text{ MIN}$  (Pin Height),  $0.100 (2,54)$  (Pin Pitch),  $0.021 (0,53)$  (Pin Height),  $0.015 (0,38)$  (Pin Height),  $\oplus 0.010 (0,25) \text{ (M)}$  (Pin Position)
- Right:  $0.015 (0,38)$  (Pin Height),  $0.010 (0,25) \text{ NOM}$  (Pin Height),  $0.430 (10,92) \text{ MAX}$  (Housing Width),  $\triangle D$  (Surface Finish)

Labels:

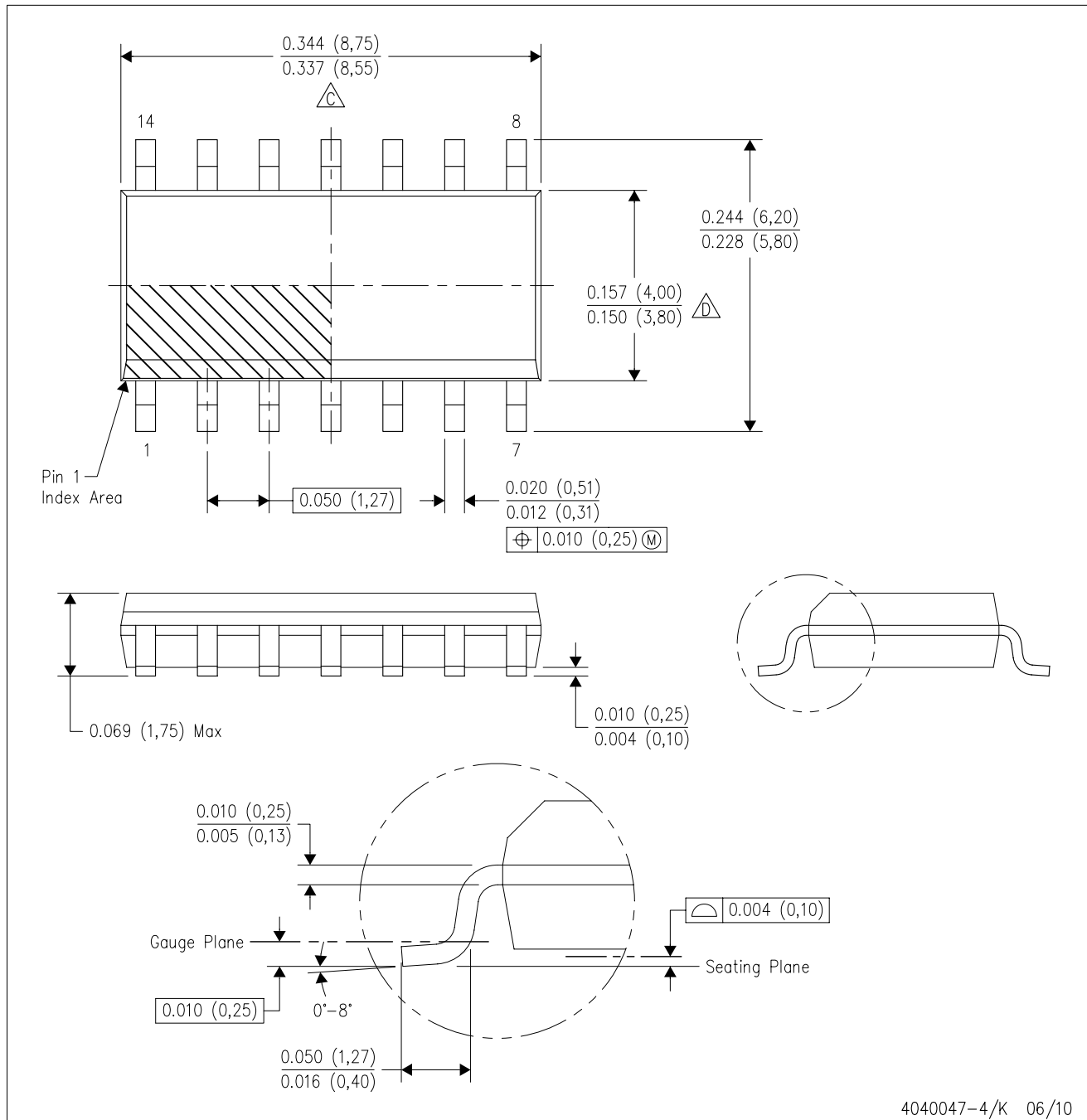
- Seating Plane
- Gauge Plane
- 14/18 Pin Only
- 20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

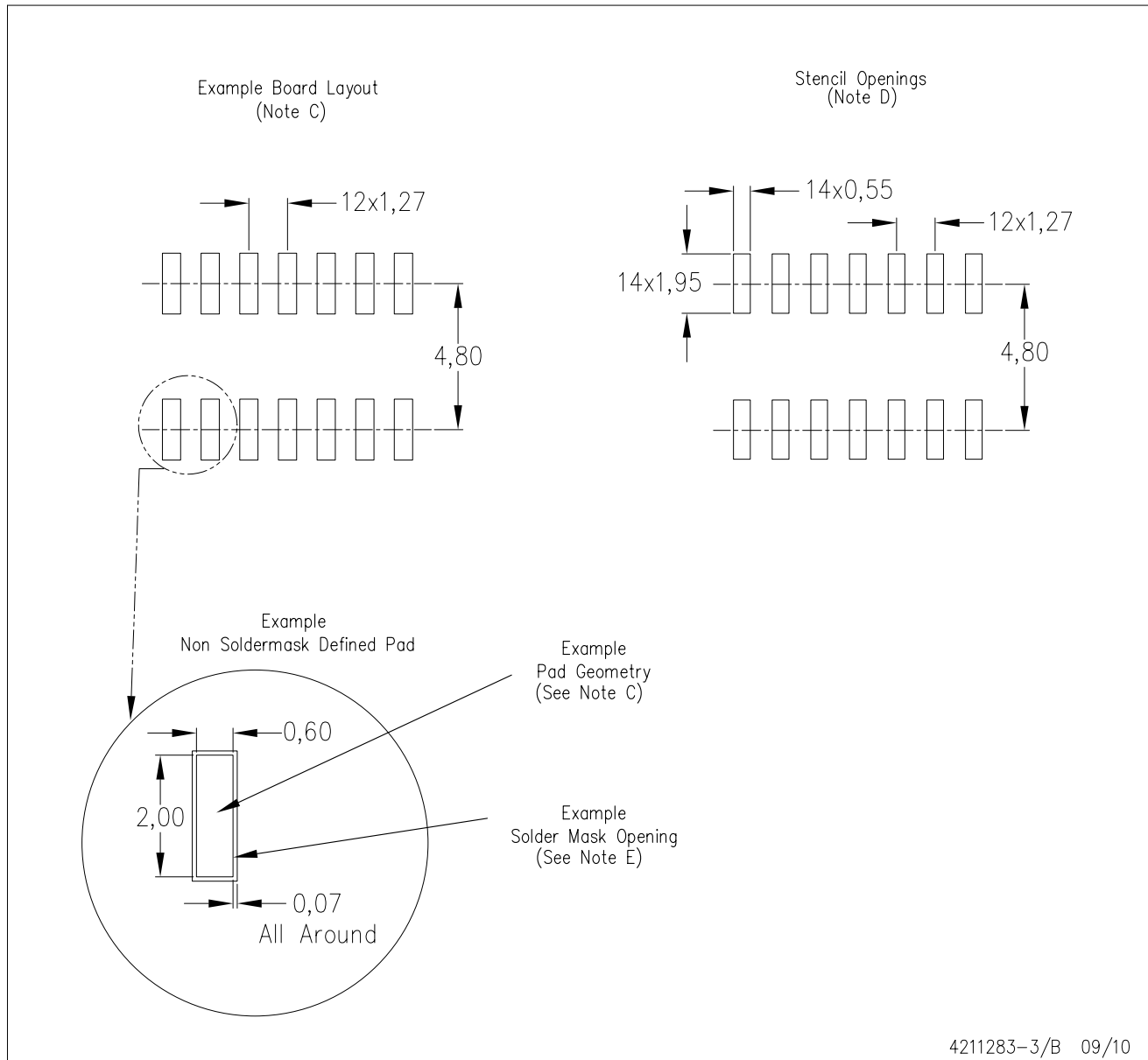


4040047-4/K 06/10

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

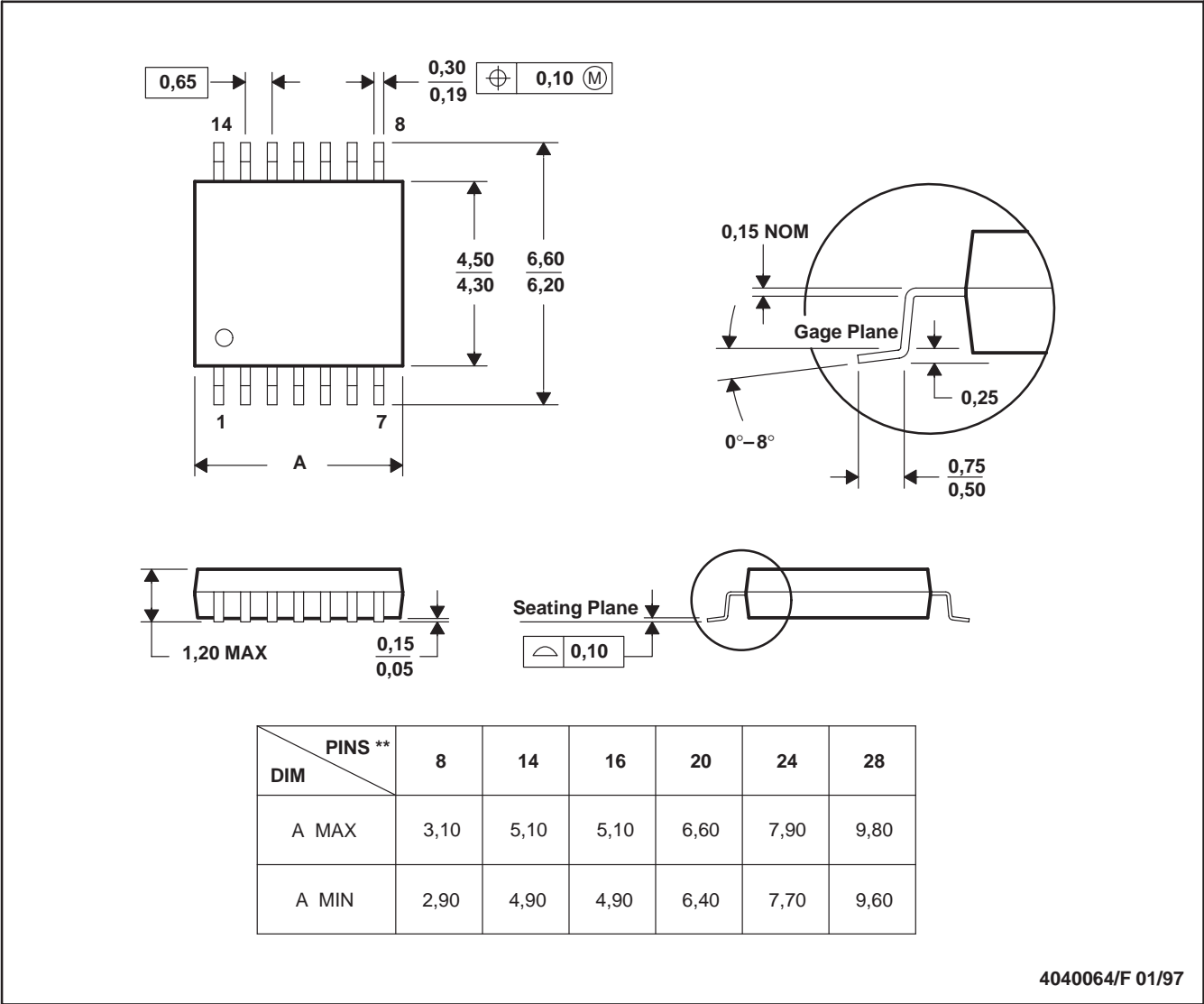
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MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

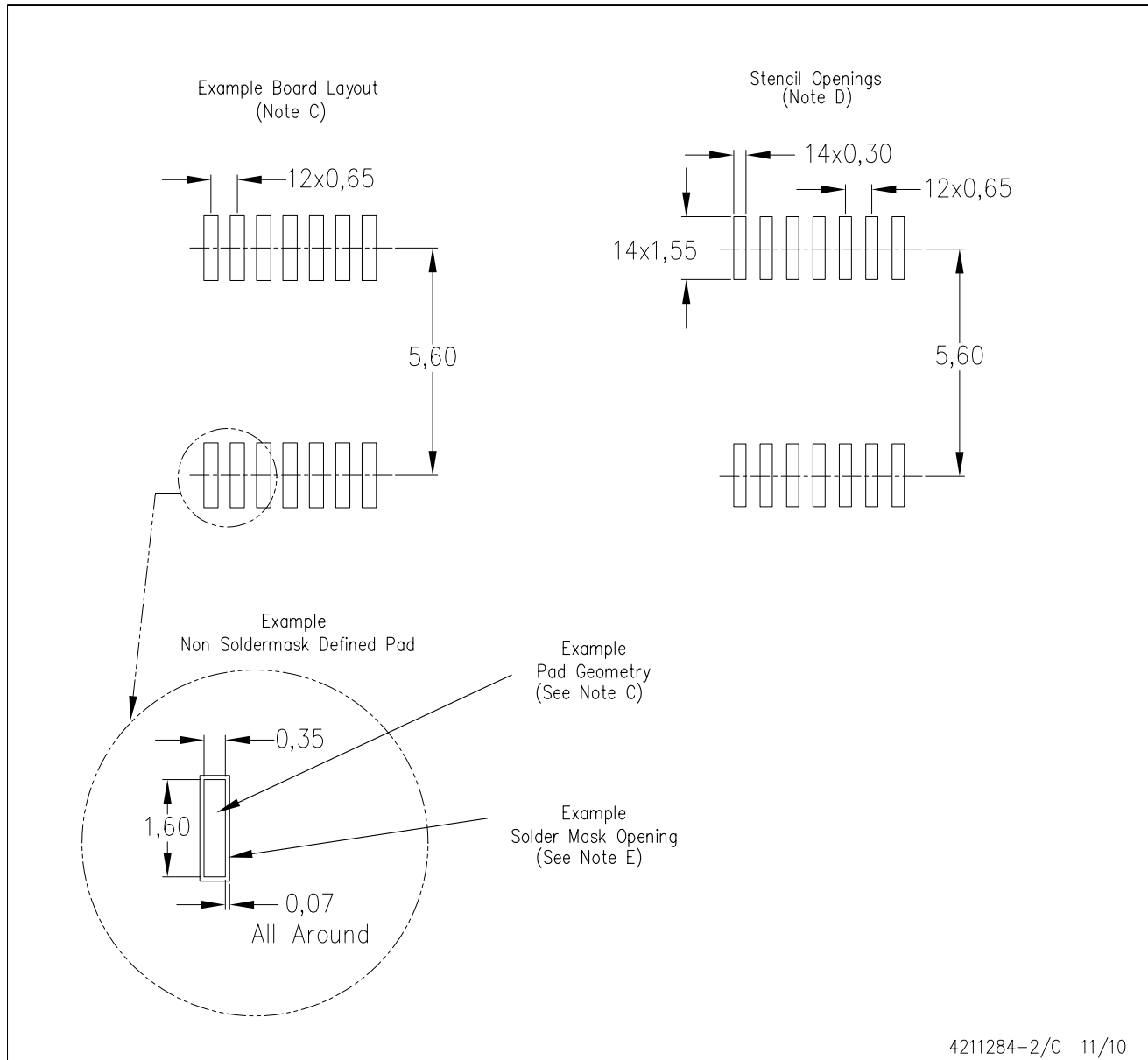
14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
D. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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