

P-Channel 80-V (D-S) MOSFET

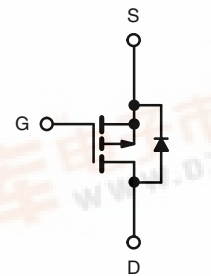
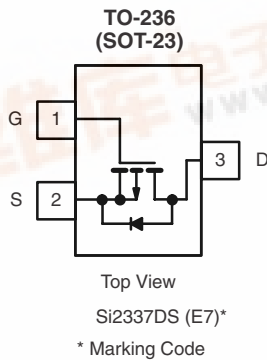
PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
- 80	0.270 at V _{GS} = - 10 V	- 2.2	7
	0.303 at V _{GS} = - 6 V	- 2.1	

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET



RoHS
 COMPLIANT
 HALOGEN
FREE
 Available



P-Channel MOSFET

Ordering Information: Si2337DS-T1-E3 (Lead (Pb)-free)
 Si2337DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 80	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 2.2	A
		T _C = 70 °C	- 1.75	
		T _A = 25 °C	- 1.2 ^{b, c}	
		T _A = 70 °C	- 0.96 ^{b, c}	
Pulsed Drain Current	I _{DM}	- 7		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	- 2.1	
		T _A = 25 °C	- 0.63 ^{b, c}	
Avalanche Current	I _{AS}	11		
Single-Pulse Avalanche Energy	E _{AS}	6.0	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	2.5	W
		T _C = 70 °C	1.6	
		T _A = 25 °C	0.76 ^{b, c}	
		T _A = 70 °C	0.48 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 50 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	120	166	°C/W	
Maximum Junction-to-Foot (Drain)	R _{thJF}	40	50		

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 166 °C/W.



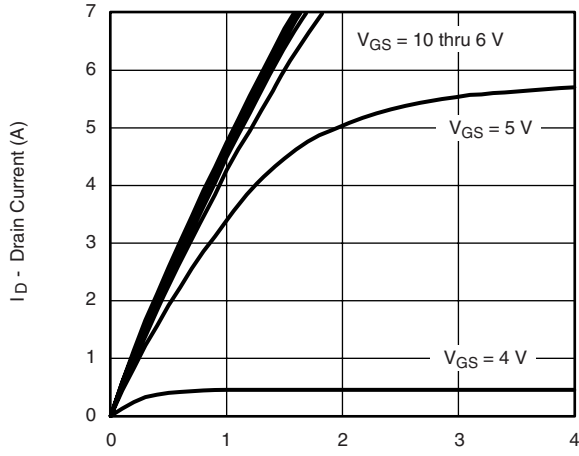
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	- 80			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\ \mu\text{A}$		- 35.8		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.45		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	- 2		- 4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = -10\text{ V}$	- 7			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -1.2\text{ A}$		0.216	0.270	Ω
		$V_{GS} = -6\text{ V}, I_D = -1.1\text{ A}$		0.242	0.303	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -1.2\text{ A}$		4.3		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		500		pF
Output Capacitance	C_{oss}			40		
Reverse Transfer Capacitance	C_{rss}			25		
Total Gate Charge	Q_g	$V_{DS} = -40\text{ V}, V_{GS} = -10\text{ V}, I_D = -1.2\text{ A}$		11	17.0	nC
				7	11.0	
Gate-Source Charge	Q_{gs}	$V_{DS} = -40\text{ V}, V_{GS} = -6\text{ V}, I_D = -1.2\text{ A}$		2.1		
Gate-Drain Charge	Q_{gd}			3.2		
Gate Resistance	R_g	$f = 1\text{ MHz}$		4.8		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -40\text{ V}, R_L = 42\ \Omega$ $I_D \cong -0.96\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$		10	15	ns
Rise Time	t_r			15	23	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			15	23	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -40\text{ V}, R_L = 42\ \Omega$ $I_D \cong -0.96\text{ A}, V_{GEN} = -6\text{ V}, R_g = 1\ \Omega$		15	23	
Rise Time	t_r			18	27	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			12	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			- 2.1	A
Pulse Diode Forward Current ^a	I_{SM}				- 7	
Body Diode Voltage	V_{SD}	$I_S = 0.63\text{ A}$		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 0.63\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		30	45	ns
Body Diode Reverse Recovery Charge	Q_{rr}			45	70	nC
Reverse Recovery Fall Time	t_a			25		ns
Reverse Recovery Rise Time	t_b			5		

Notes:

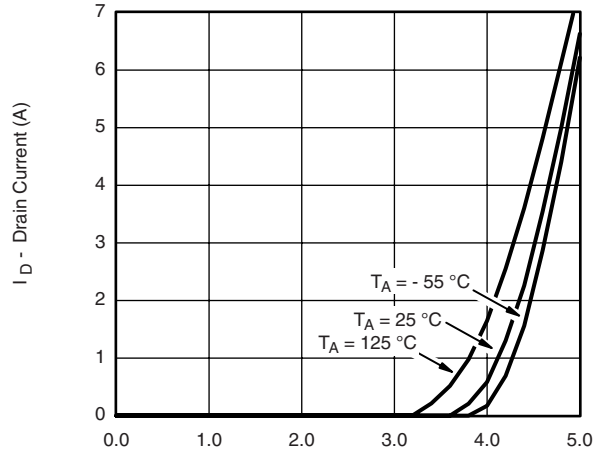
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

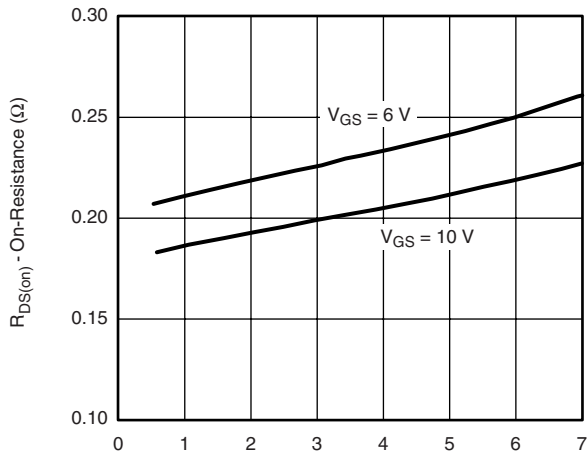
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



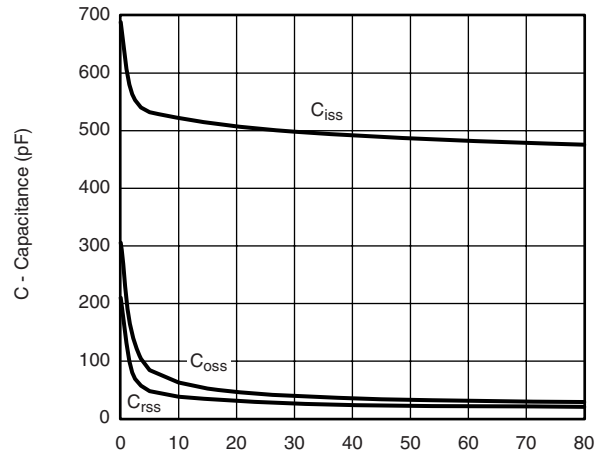
V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



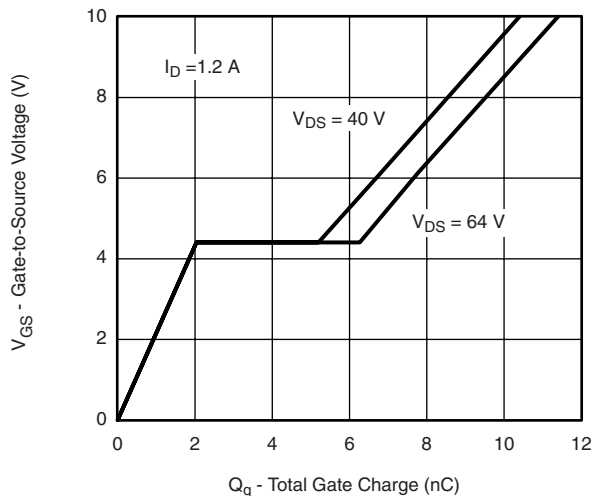
V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



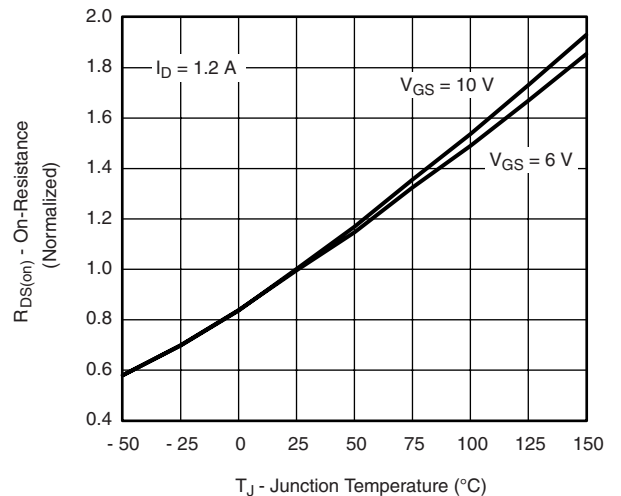
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

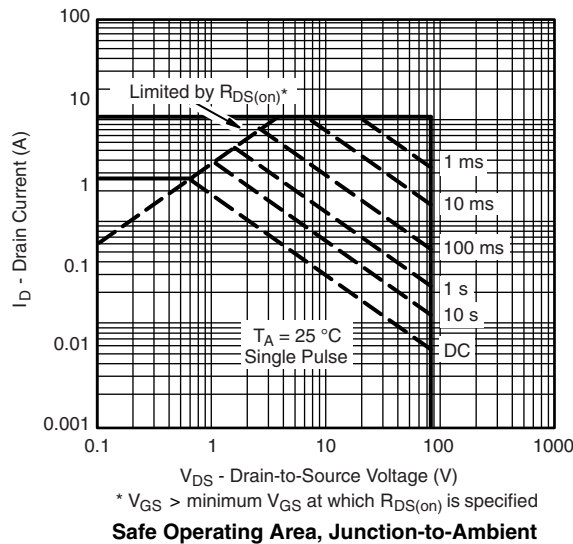
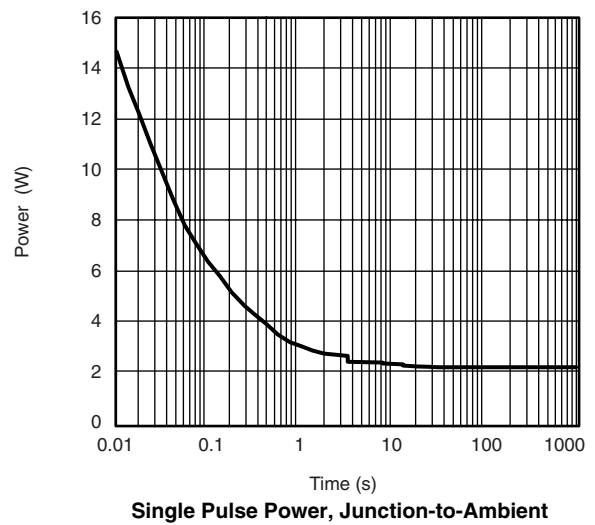
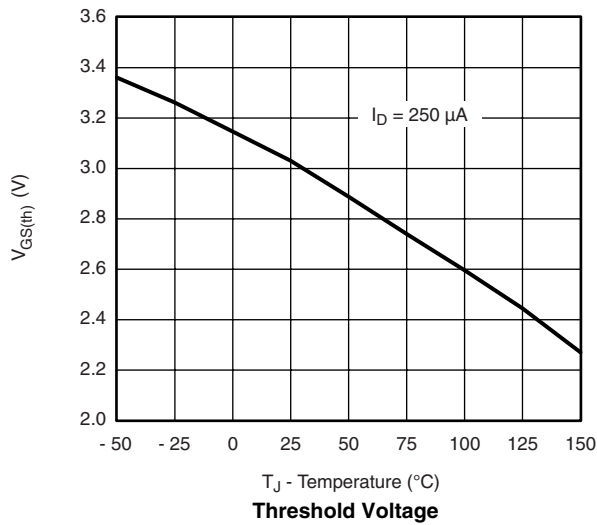
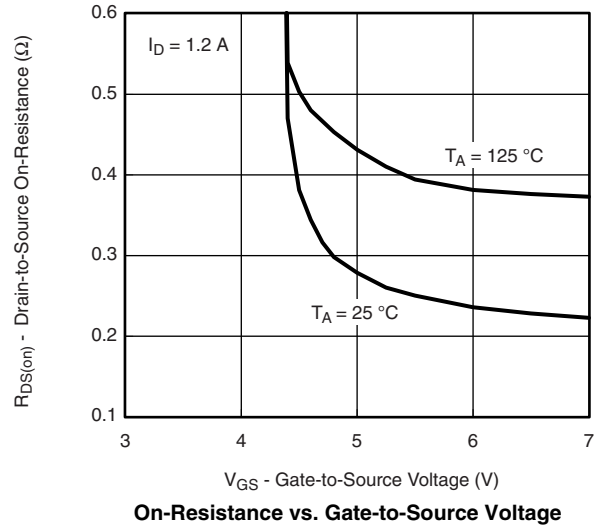
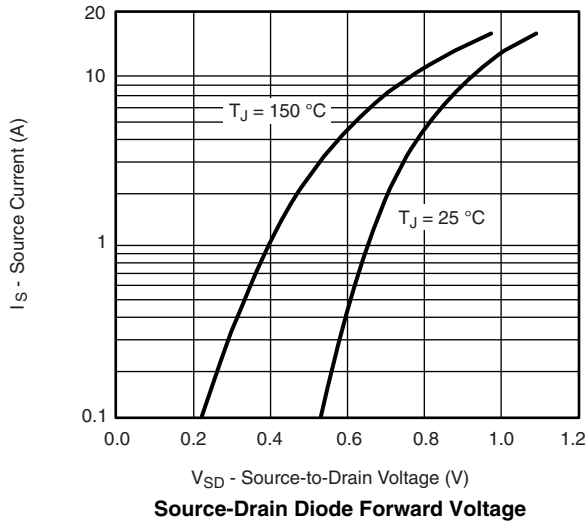


Gate Charge

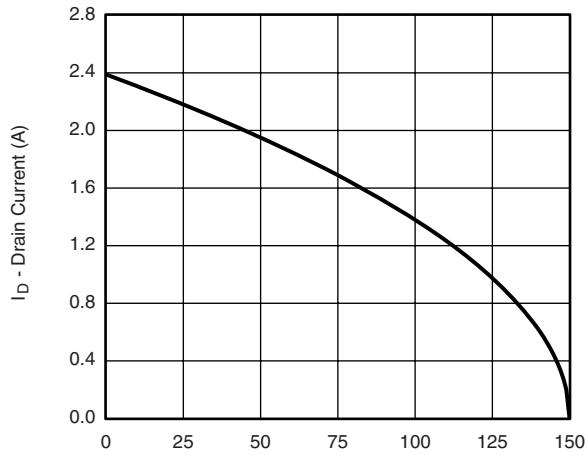


On-Resistance vs. Junction Temperature

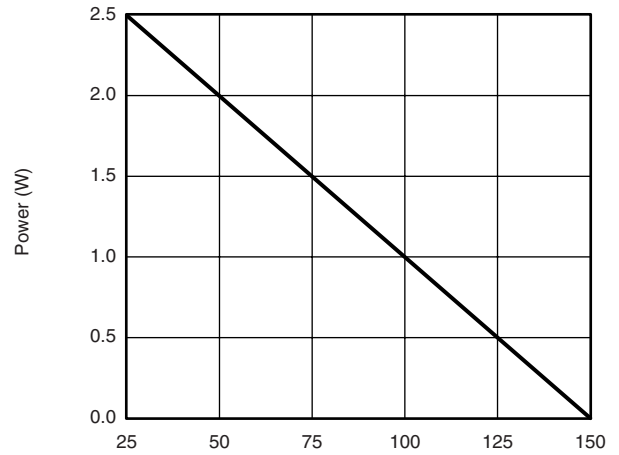
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



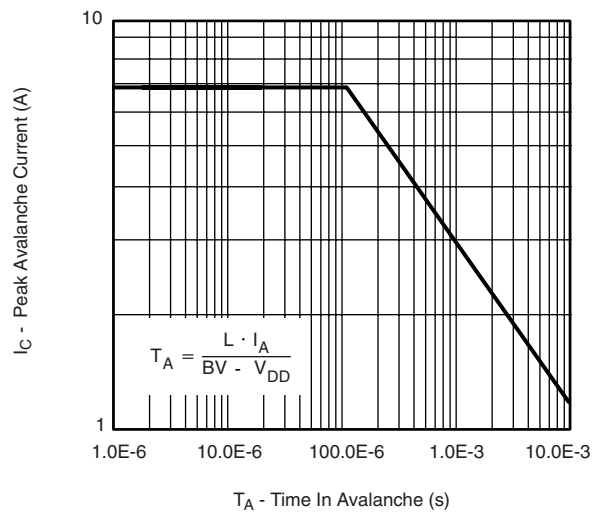
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



T_C - Case Temperature (°C)
Current Derating*



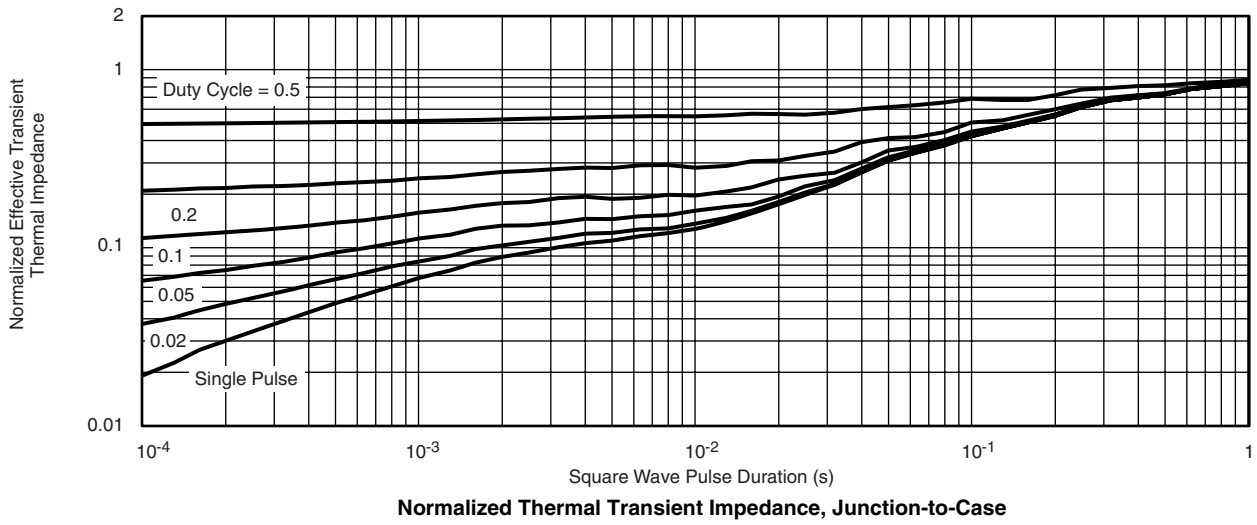
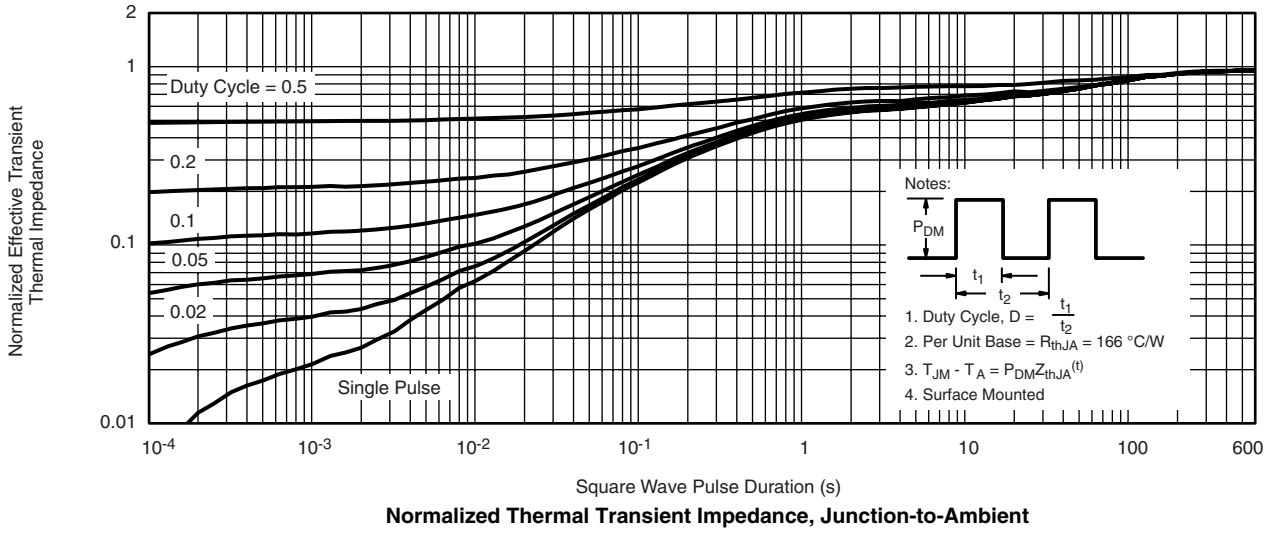
T_C - Case Temperature (°C)
Power Derating



Single Pulse Avalanche Capability

* The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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