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The RF MOSFET Line

# RF Power Field Effect Transistors

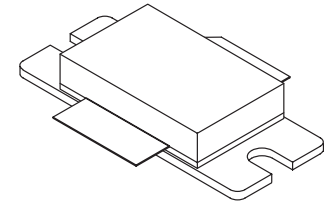
## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and EDGE base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for GSM and EDGE cellular radio applications.

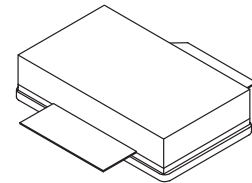
- GSM and EDGE Performances, Full Frequency Band  
Power Gain — 13.5 dB (Typ) @ 90 Watts (CW)  
Efficiency — 45% (Typ) @ 90 Watts (CW)
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

**MRF18090B**  
**MRF18090BS**

**1.90 – 1.99 GHz, 90 W, 26 V**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETS**



**CASE 465B-03, STYLE 1**  
**(NI-880)**  
**(MRF18090B)**



**CASE 465C-02, STYLE 1**  
**(NI-880S)**  
**(MRF18090BS)**

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	250 1.43	Watts W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +200	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

### ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain–Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 100\ \mu\text{Adc}$ )	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Gate–Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**ON CHARACTERISTICS**

Gate Quiescent Voltage ( $V_{DS} = 26\text{ Vdc}$ , $I_D = 750\text{ mAdc}$ )	$V_{GS(Q)}$	2.5	3.7	4.5	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1\text{ Adc}$ )	$V_{DS(on)}$	—	0.1	—	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 3\text{ Adc}$ )	$g_{fs}$	—	7.2	—	S

**DYNAMIC CHARACTERISTICS**

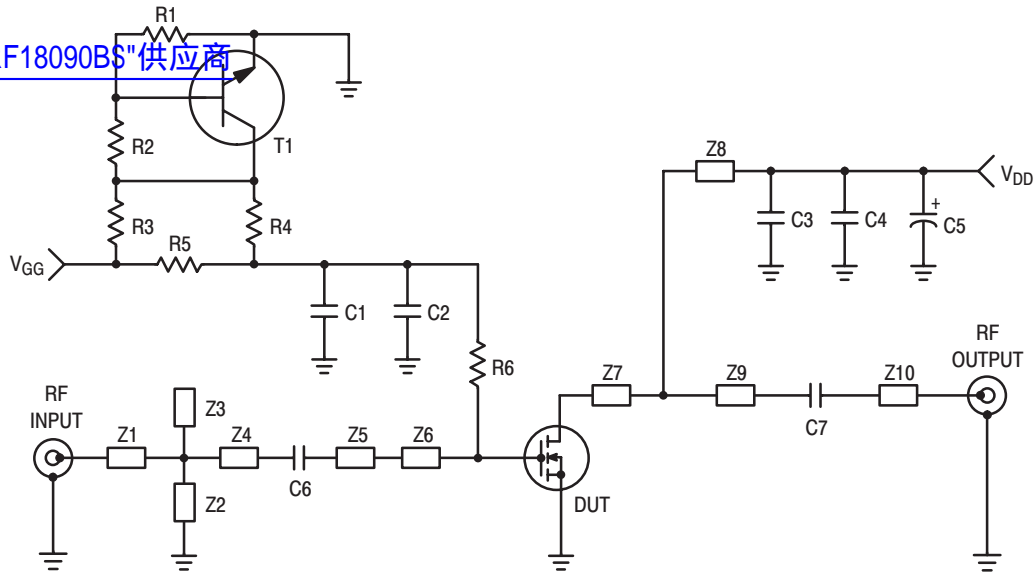
Reverse Transfer Capacitance ( $V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	4.2	—	pF
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**FUNCTIONAL TESTS** (In Motorola Test Fixture)

Common–Source Amplifier Power Gain @ 90 W (1) ( $V_{DD} = 26\text{ Vdc}$ , $I_{DQ} = 750\text{ mA}$ , $f = 1930 - 1990\text{ MHz}$ )	$G_{ps}$	12	13.5	—	dB
Drain Efficiency @ 90 W (1) ( $V_{DD} = 26\text{ Vdc}$ , $I_{DQ} = 750\text{ mA}$ , $f = 1930 - 1990\text{ MHz}$ )	$\eta$	40	45	—	%
Input Return Loss (1) ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 90\text{ W CW}$ , $I_{DQ} = 750\text{ mA}$ , $f = 1930 - 1990\text{ MHz}$ )	IRL	—	—	-10	dB
Output Mismatch Stress ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 90\text{ W CW}$ , $I_{DQ} = 750\text{ mA}$ VSWR = 10:1, All Phase Angles at Frequency of Tests)	$\Psi$	No Degradation In Output Power Before and After Test			

(1) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1900 band, ensuring batch-to-batch consistency.

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C1	1.0 $\mu$ F Chip Capacitor (0805)	Z2	Printed Inductance
C2	1.0 nF Chip Capacitor (0805)	Z3	Printed Inductance (Butterfly)
C3, C4	6.8 pF, 100B Chip Capacitors	Z4	0.70" x 0.09" Microstrip
C5	220 $\mu$ F, 50 V Electrolytic Capacitor	Z5	0.36" x 0.09" Microstrip
C6, C7	12 pF, 100B Chip Capacitors	Z6	0.21" x 1.25" Microstrip
R1	2.2 k $\Omega$ Chip Resistor (0805)	Z7	0.45" x 1.18" Microstrip
R2, R3, R6	1.0 k $\Omega$ Chip Resistors (0805)	Z8	1.37" x 0.05" Microstrip
R4	10 k $\Omega$ Chip Resistor (0805)	Z9	0.39" x 0.09" Microstrip
R5	6.8 k $\Omega$ Chip Resistor (0805)	Z10	1.25" x 0.09" Microstrip
T1	BC847 SOT-23	PCB	Teflon <sup>®</sup> Glass
Z1	0.85" x 0.09" Microstrip		

Figure 1. 1.93 – 1.99 MHz Test Fixture Schematic

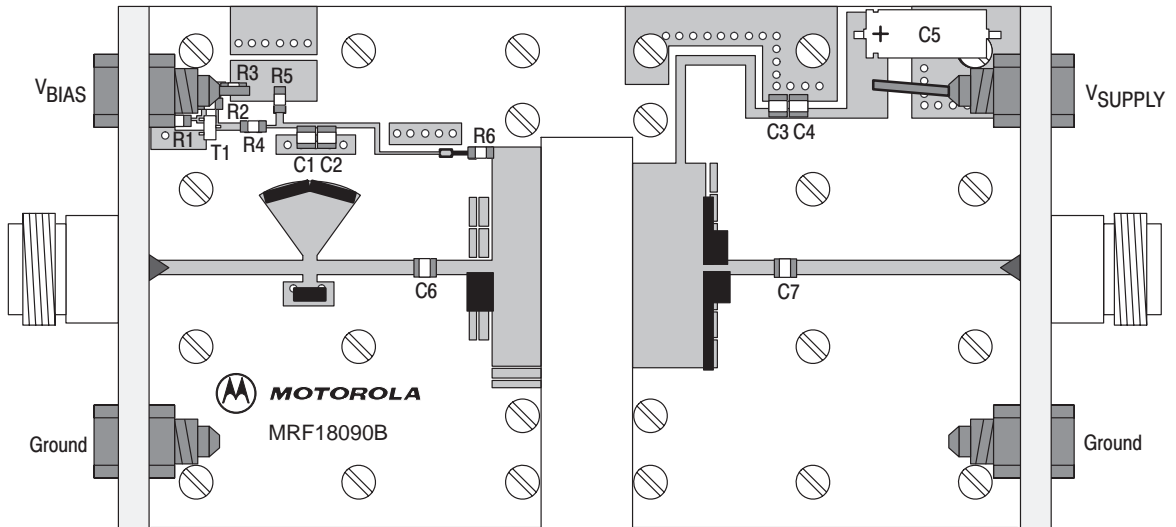
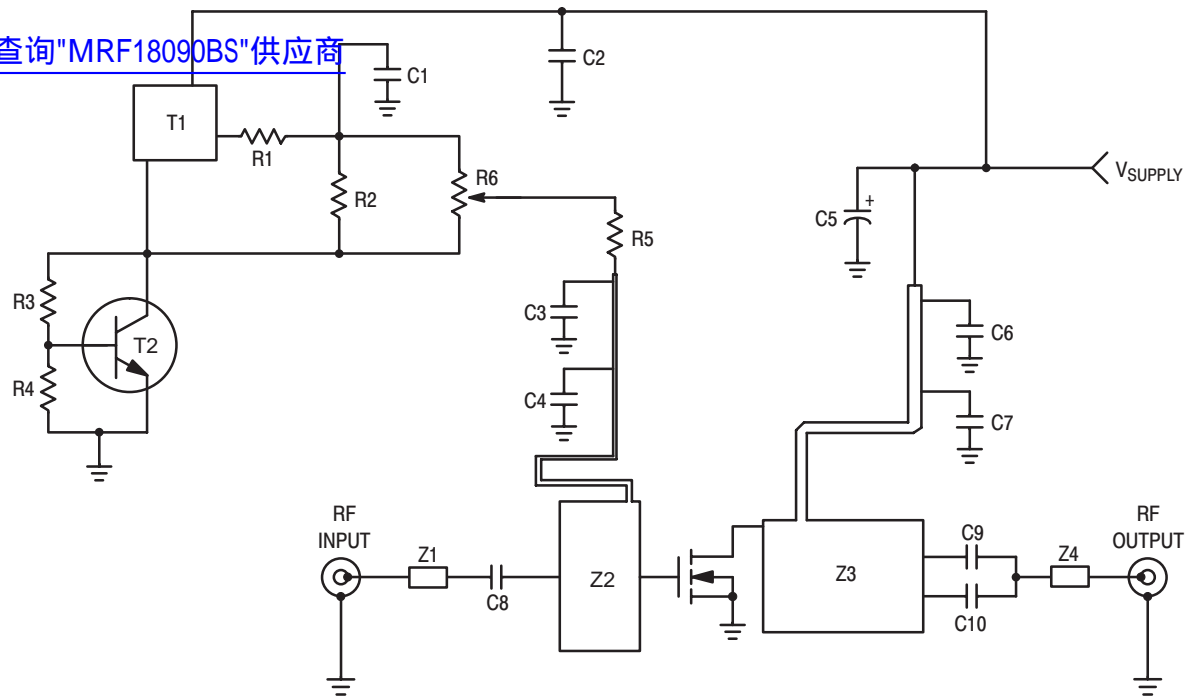


Figure 2. 1.93 – 1.99 GHz Test Fixture Component Layout

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C1, C3	1 $\mu$ F Chip Capacitors (0805)	R5	10 k $\Omega$ Chip Resistor (0603)
C2	0.1 $\mu$ F Chip Capacitor (0805)	R6	5 k $\Omega$ , SMD Potentiometer
C4	1 nF Chip Capacitor (0805)	T1	LP2951 Micro-8 Voltage Regulator
C5	220 $\mu$ F, 50 V Electrolytic Capacitor	T2	BC847 SOT-23 NPN Transistor
C6, C7	8.2 pF, 100A Chip Capacitors	Z1	0.491" x 0.110" Microstrip
C8, C9, C10	22 pF, 100A Chip Capacitors	Z2	0.756" x 1.260" Microstrip
R1	10 $\Omega$ Chip Resistor (0805)	Z3	1.433" x 1.260" Microstrip
R2, R3	1 k $\Omega$ Chip Resistors (0805)	Z4	0.567" x 0.110" Microstrip
R4	2.2 k $\Omega$ Chip Resistor (0805)		Substrate = 0.5 mm Teflon <sup>®</sup> Glass

Figure 3. 1.93 – 1.99 GHz Demo Board Schematic

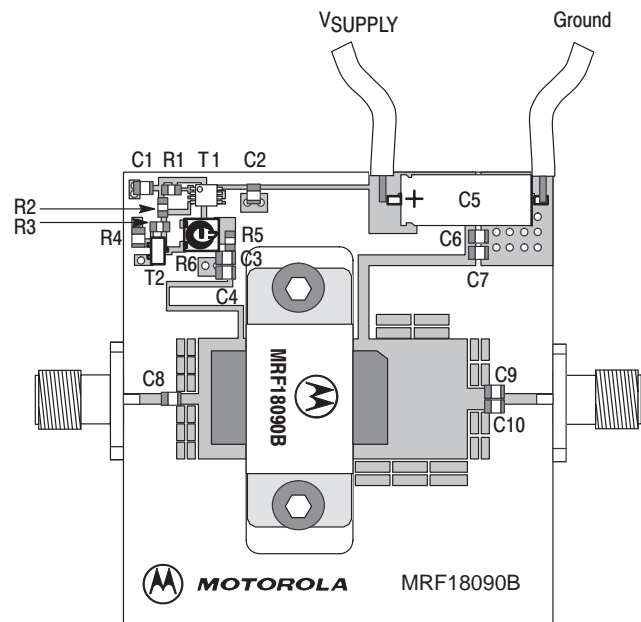


Figure 4. 1.93 – 1.99 GHz Demo Board Component Layout

## TYPICAL CHARACTERISTICS

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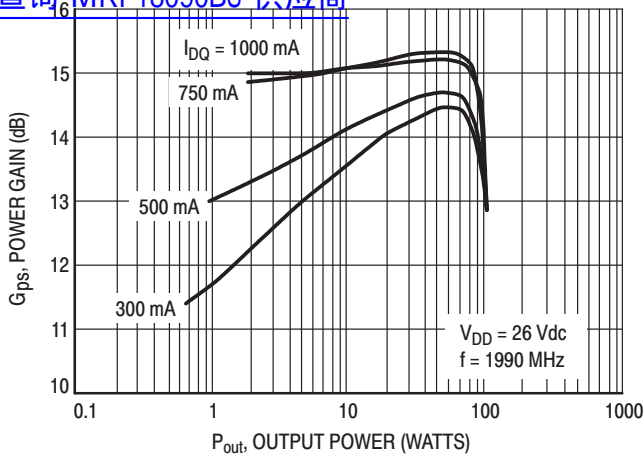


Figure 5. Power Gain versus Output Power

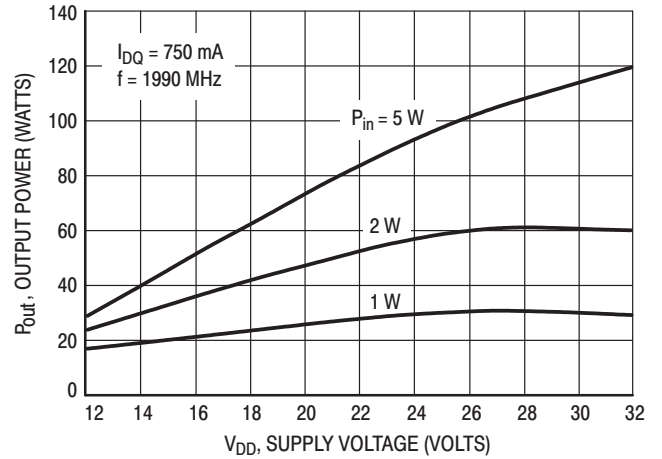


Figure 6. Output Power versus Supply Voltage

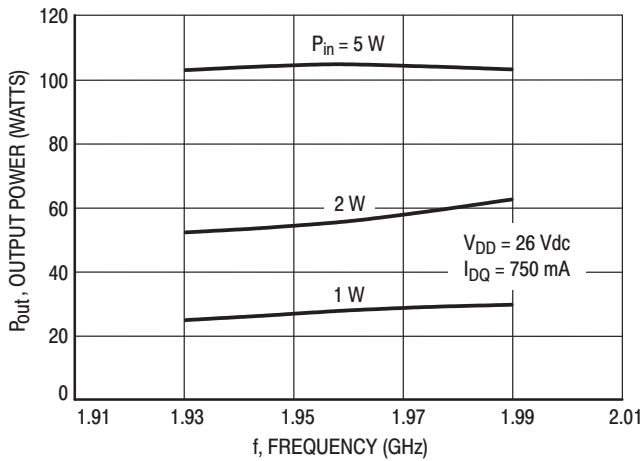


Figure 7. Output Power versus Frequency

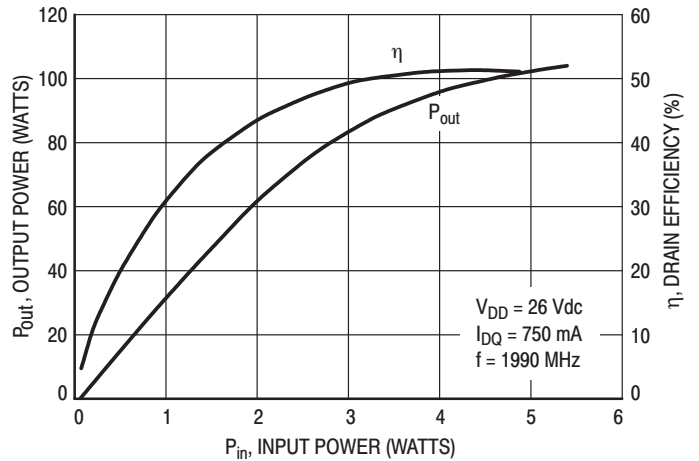


Figure 8. Output Power and Efficiency versus Input Power

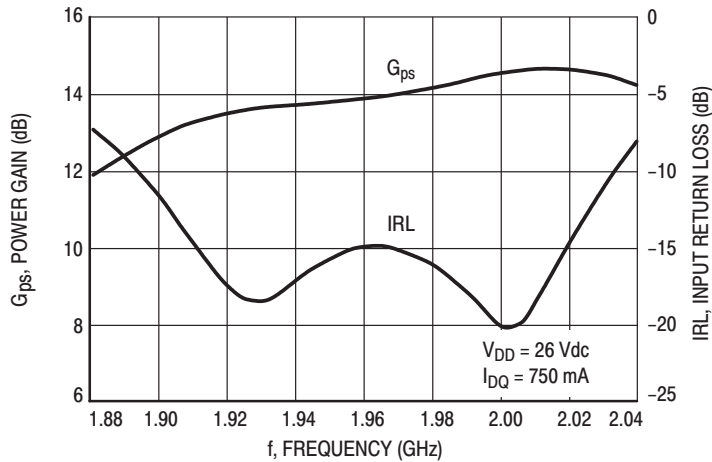
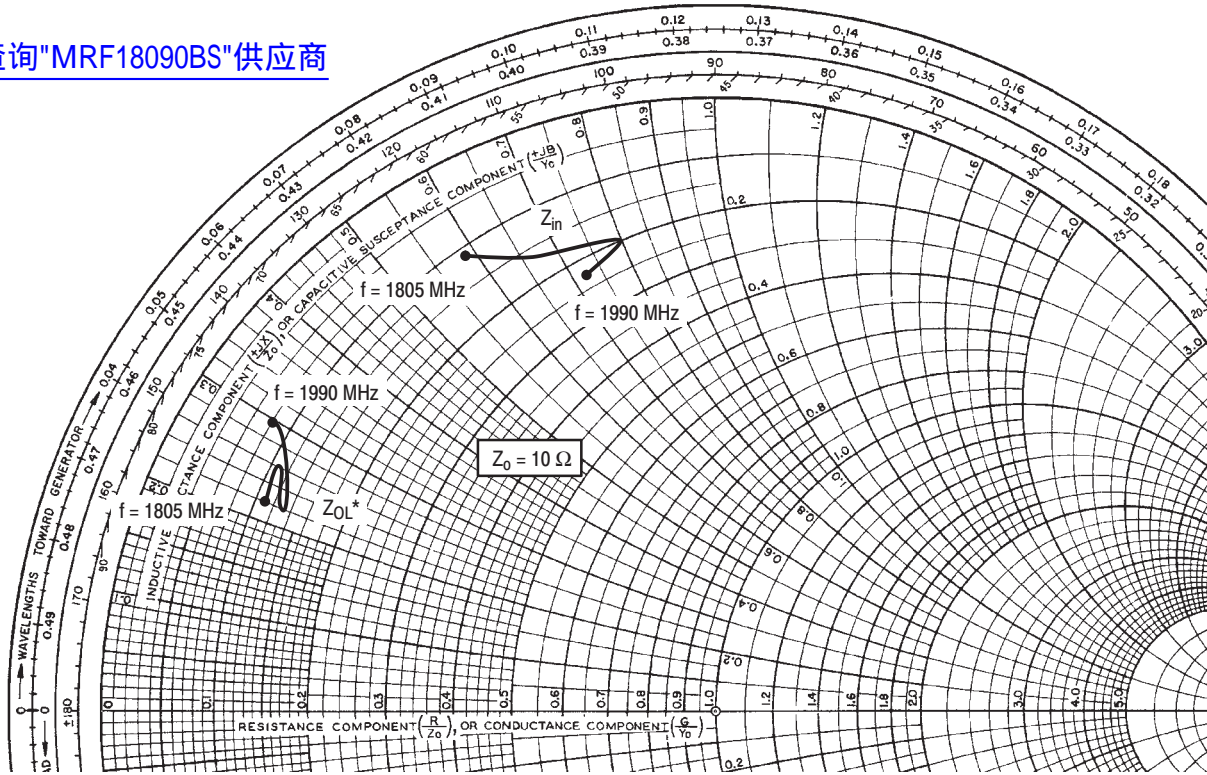


Figure 9. Wideband Gain and IRL (at Small Signal)



$V_{DD} = 26\text{ V}$ ,  $I_{DQ} = 750\text{ mA}$ ,  $P_{out} = 90\text{ Watts (CW)}$

f MHz	$Z_{in}$ $\Omega$	$Z_{OL}^*$ $\Omega$
1805	$1.10 + j5.85$	$1.15 + j2.16$
1880	$1.56 + j6.75$	$1.13 + j2.60$
1930	$2.05 + j8.00$	$1.30 + j2.23$
1990	$2.30 + j7.30$	$0.82 + j2.90$

$Z_{in}$  = Complex conjugate of the source impedance.

$Z_{OL}^*$  = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Note:  $Z_{OL}^*$  was chosen based on tradeoffs between gain, output power, and drain efficiency.

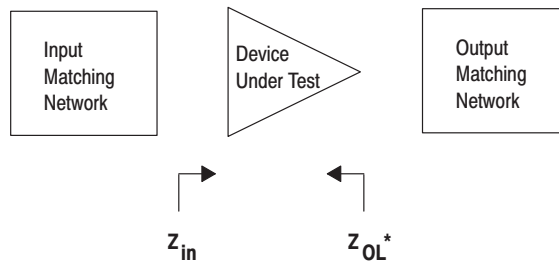


Figure 10. Large Signal Input and Output Impedance

# PACKAGE DIMENSIONS

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**2X  $\varnothing$  Q**  
 $\oplus \varnothing$  bbb (M) T A (M) B (M)

**NOTES:**  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.  
 2. CONTROLLING DIMENSION: INCH.  
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.  
 4. RECOMMENDED BOLT CENTER DIMENSION OF 1.16 (29.57) BASED ON M3 SCREW.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.175	0.205	4.44	5.21
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	$\varnothing$ 0.118	$\varnothing$ 0.138	$\varnothing$ 3.00	$\varnothing$ 3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

**STYLE 1:**  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

**CASE 465B-03  
 ISSUE C  
 (NI-880)  
 (MRF18090B)**


**NOTES:**  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.  
 2. CONTROLLING DIMENSION: INCH.  
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

**STYLE 1:**  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

**CASE 465C-02  
 ISSUE A  
 (NI-880S)  
 (MRF18090BS)**

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