National Semiconductor

MILITARY DATA SHEET

MN100302-X REV 1A0

Original Creation Date: 10/30/95
Last Update Date: 08/28/96
Last Major Revision Date: 08/21/96

LOW POWER QUINT 2-INPUT OR/NOR GATE

General Description

The 100302 is a monolithic quint 2-input OR/NOR gate with common Enable. All inputs have 50K Ohms pull-down resistors and all outputs are buffered.

Industry Part Number

100302

Prime Die

F302

NS Part Numbers

100302DMQB
100302FMQB
100302J-QMLV
100302W-QMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 43% power reduction of the 100102
- 2000V ESD protection
- Pin/function compatible with 100102
- Voltage compensated operating range = -4.2V to -5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature (Tstg)	−65 C to +150 C
Maximum Junction Temperature (Tj)	
Ceramic	+175 C
Plastic	+150 C
Vee Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	Vee to +0.5V
Output Current (DC Output HIGH)	−50mA
ESD (Note 2)	≥ 2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (Tc)	
Commercial	0 C to +85 C
Military	−55 C to +125 C
Industrial	−40 C to +85 C
Supply Voltage (Vee)	−5.7V to −4.2V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vee Range: -4.2V to -5.7V, Tc= -55C to +125C, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input HIGH Current	Vee= -5.7V, VM= -0.87V	1, 3	INPUTS		240	uA	1, 2
			1, 3	INPUTS		340	uA	3
IIL	Input LOW Current	Vee= -4.2V, VM= -1.83V	1, 3	INPUTS	0.5		uA	1, 2, 3
VOH	Output HIGH Voltage	Vee=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms To -2.0V	1, 3	OUTPUTS	-1025	-870	mV	1, 2
			1, 3	OUTPUTS	-1085	-870	mV	3
VOL	Output LOW Voltage	Vee=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1830	-1620	mV	1, 2
			1, 3	OUTPUTS	-1830	-1555	mV	3
VOHC	Output HIGH Voltage	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1035		mV	1, 2
			1, 3	OUTPUTS	-1085		mV	3
VOLC	Output LOW Voltage	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, LOADING:50 Ohms to -2.0V	1, 3	OUTPUTS		-1610	mV	1, 2
			1, 3	OUTPUTS		-1555	mV	3
VIH	Input HIGH Voltage		1, 3, 7	INPUTS	-1165	-870	mV	1, 2, 3
VIL	Input LOW Voltage		1, 3, 7	INPUTS	-1830	-1475	mV	1, 2, 3
IEE	Power Supply Current	Vee= -4.2/-5.7V	1, 3	VEE	-48	-17	mA	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vee Range: -4.2V to -5.7V, VCC=VCCA=GND, LOADING: 50 Ohms To -2.0V

tPLH/tPHL(1)	Propagation Delay	Vee= -4.2/-5.7V	2, 4	Dn to On/$\overline{On}$	0.4	1.5	ns	9
			2, 4	Dn to On/$\overline{On}$	0.4	1.7	ns	10
			2, 4	Dn to On/$\overline{On}$	0.3	1.8	ns	11
tPLH/tPHL(2)	Propagation Delay	Vee= -4.2/-5.7V	2, 4	E to On/$\overline{On}$	0.8	2.3	ns	9
			2, 4	E to On/$\overline{On}$	0.8	2.8	ns	10
			2, 4	E to On/$\overline{On}$	0.6	2.6	ns	11
tTLH/tTHL	Transition Time	Vee= -4.2/-5.7V	6	On/$\overline{On}$	0.3	1.2	ns	9, 10, 11

Note 1: Screen tested 100% on each device at -55 C, +25 C and +125 C temp., subgroups 1, 2, 3, 7 & 8.

(Continued)

Note 2: For QB devices, screen tested 100% on each device at +25C temperature only, subgroup A9. For QMLV devices, screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A9, 10 & 11.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, subgroup A9, and at +125 C & -55 C temp., subgroups A10 & 11.
Note 5: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C temp. only, subgroup A9.
Note 6: Not tested at +25 C, +125 C & -55 C temp. (DESIGN CHARACTERIZATION DATA).
Note 7: Guaranteed by applying specified input condition and testing VOH/VOL.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
J24ERJ	CERDIP(J), 24LD .400 CENTERS (P/P DWG)
P000035A	CERDIP (J), 24LD .400 CENTERS (PIN OUT)
P000036A	CERPAC, QUAD, 24 LEAD (PIN OUT)
W24BRE	CERPAC, QUAD, 24 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
J	REVISE AND REDRAW	09044	03/05/92	DEG/

MIL-M-38510
CONFIGURATION CONTROL

MILAERO
CONFIGURATION CONTROL

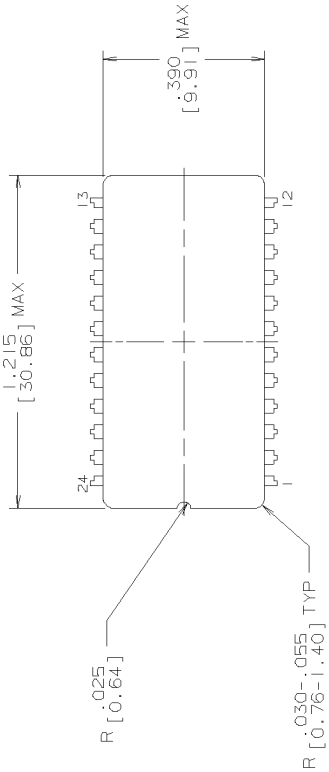
CONTROLLING DIMENSION: INCH

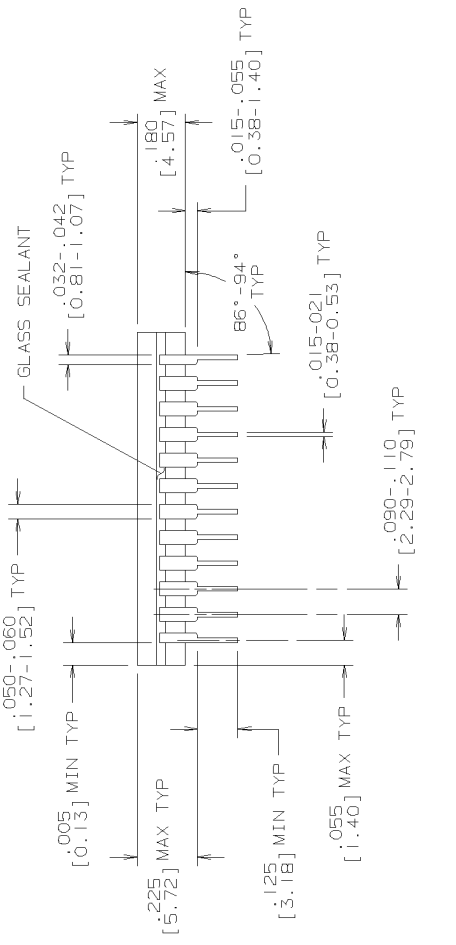
APPROVALS	DATE
DRAWN D.E. GRADY	03/05/92
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

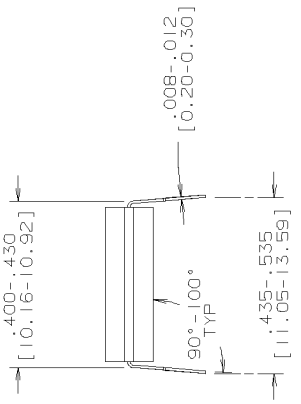
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J),
24 LEAD,
.400 CENTERS

PROJECTION | SCALE N/A | SIZE C | DRAWING NUMBER MKT-J24E | REV J
FORMERLY: N/A | SHEET 1 OF 1







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES/5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. LEAD THICKNESS MAY BE INCREASED BY .003 [0.08] MAXIMUM AFTER LEAD FINISH APPLIED.
3. BUMPERS ARE AVAILABLE ON CERTAIN PRODUCTS. BUMPERS WILL ADD .040 [1.02] MAX TO THE LENGTH OF THE PACKAGE.
4. NO JEDEC REGISTRATION AS OF 2/17/92.