

查询"74HC368D-T"供应商

HEX BUFFER/LINE DRIVER: 3-STATE INVERTING

FEATURES

- Inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT368 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT368 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs ($n\bar{Y}$) are controlled by the output enable inputs ($1\bar{OE}$, $2\bar{OE}$).

A HIGH on $n\bar{OE}$ causes the outputs to assume a high impedance OFF-state.

The "368" is identical to the "367" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to n $\bar{Y}$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	9	11	ns
C_I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF
 f_o = output frequency in MHz V_{CC} = supply voltage in V
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
 For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\bar{OE}$, $2\bar{OE}$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	$1\bar{Y}$ to $6\bar{Y}$	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

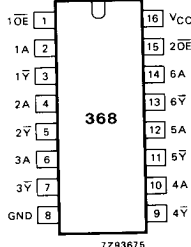


Fig. 1 Pin configuration.

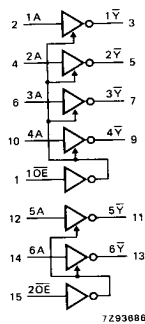


Fig. 2 Logic symbol.

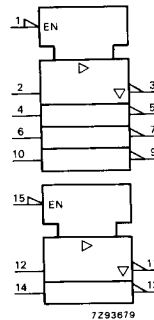


Fig. 3 IEC logic symbol.

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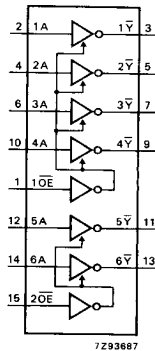


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{nOE}$	nA	$\overline{nY}$
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

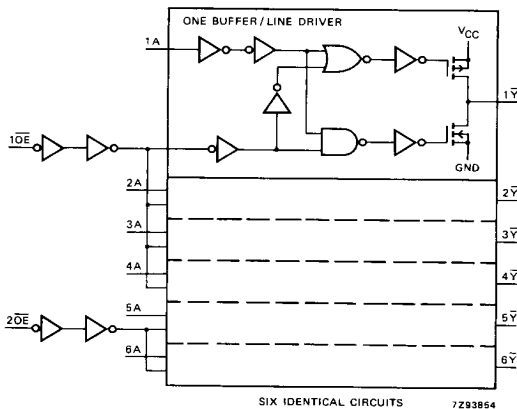


Fig. 5 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay nA to nY		30 11 9	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6	
t _{PZH} / t _{PZL}	3-state output enable time nOE to nY		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{PHZ} / t _{PLZ}	3-state output disable time nOE to nY		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1OE	1.00
2OE	0.90
nA	1.00

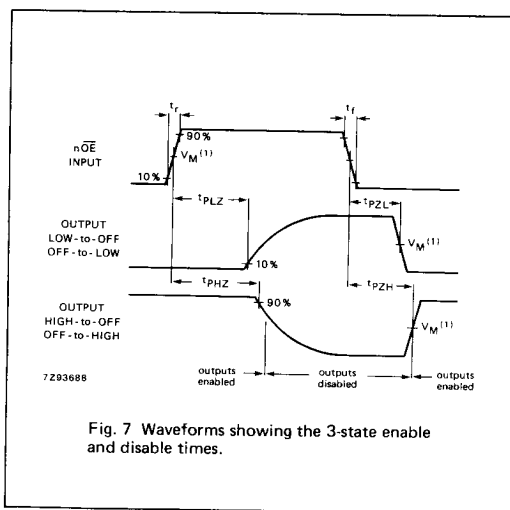
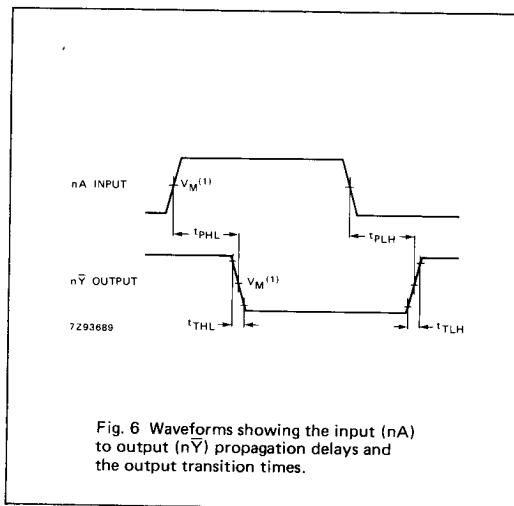
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AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay nA to nY		13	24		30		36	ns	4.5	Fig. 6	
t _{PZH} / t _{PZL}	3-state output enable time nOE to nY		17	35		44		53	ns	4.5	Fig. 7	
t _{PHZ} / t _{PLZ}	3-state output disable time nOE to nY		20	35		44		53	ns	4.5	Fig. 7	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6	

AC WAVEFORMS



Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.HCT: $V_M = 1.3$ V; $V_I = \text{GND to } 3$ V.