8-Channel, 1MSPS, 12-Bit SAR ADC with Temperature Sensor

Preliminary Technical Data

AD7298

FEATURES

12 bit SAR ADC
- **8 single-ended inputs**
- **Channel sequencer functionality**
- **Fast throughput of 1Msps**
- **Analog Input Range 0 to 2.5V**

12-bit temperature-to-digital converter
- **Temperature sensor accuracy of ±2°C typical**

Temperature range: –40°C to +125°C
Specified for V_{DD} of 2.8 V to 3.6V
Logic Voltage V_{DRIVE} = 1.65V to 3.6V
Power-down current : <10 µA
Internal 2.5V Reference
Internal Power on Reset
High speed serial interface SPI™
20-lead LFCSP

FUNCTIONAL BLOCK DIAGRAM

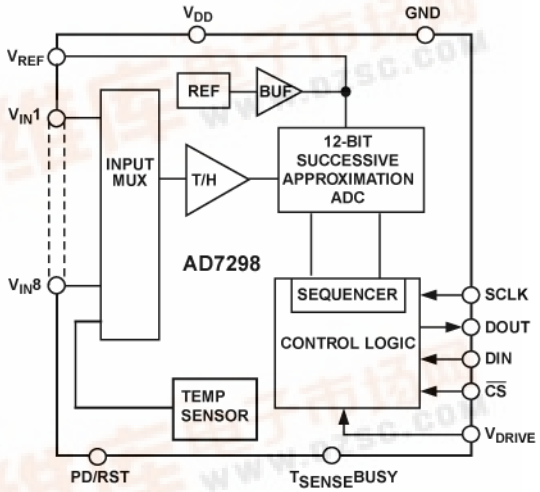

Figure 1.

GENERAL DESCRIPTION

The AD7298 is a 12-bit, high speed, low power, 8-channel, successive approximation ADC with an internal temperature sensor. The part operates from a single 3.3V power supply and features throughput rates up to 1MSPS. The device contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 70 MHz.

The AD7298 offers a programmable sequencer, which enables the selection of a pre-programmable sequence of channels for conversion. The device has an on-chip 2.5 V reference that can be disabled to allow the use of an external reference.

The AD7298 includes a high accuracy band-gap temperature sensor, which is monitored and digitized by the12-bit ADC to give a resolution of 0.25°C. The device offers a 4-wire serial interface compatible with SPI, and DSP interface standards.

The AD7298 uses advanced design techniques to achieve very low power dissipation at high throughput rates. The part also offers flexible power/throughput rate management options. The part is offered in a 20 lead LFCSP package.

PRODUCT HIGHLIGHTS

1. Ideally suited to monitoring system variables in a variety of systems including telecommunications, process and industrial control.
1. High Throughput rate of 1Msps per channel with Low Power Consumption.
2. Eight Single-Ended Inputs with a Channel Sequencer. A consecutive sequence of channels can be selected on which the ADC cycles and converts.
3. Integrated temperature sensor with 0.25°C resolution.

Table 1. AD7298 and Related Products

Device	Resolution	Interface	Features
AD7298	12-Bit	SPI	8 Channel ADC & Temp Sensor
AD7291	12-Bit	I^2C	8 Channel ADC & Temp Sensor

Rev. PrA

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SPECIFICATIONS

AD7298 SPECIFICATIONS

V_{DD} = 2.8V to 3.6V; V_{DRIVE} = 1.65 V to 3.6 V; f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, fast SCLK mode; V_{REF} = 2.5 V internal/external; T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 50 kHz sine wave
Signal-to-Noise Ratio (SNR)[1]	70	71		dB	
Signal-to-Noise (+ Distortion) Ratio (SINAD)[1]	70	71		dB	
Total Harmonic Distortion (THD)[1]		−84	78	dB	
Spurious-Free Dynamic Range (SFDR)[1]		−85	80	dB	
Intermodulation Distortion (IMD)[1]					f_A = 40.1 kHz, f_B = 41.5 kHz
Second-Order Terms		−88		dB	
Third-Order Terms		−88		dB	
Channel-to-Channel Isolation[1]		−100		dB	
SAMPLE AND HOLD					
Aperture Delay[2]			10	ns	
Aperture Jitter[2]		40		ps	
Full Power Bandwidth		TBD		MHz	@ 3 dB
		TBD		MHz	@ 0.1 dB
DC ACCURACY					
Resolution	12			Bits	
Integral Nonlinearity (INL)[1]		±0.5	±1	LSB	
Differential Nonlinearity (DNL)[1]		±0.5	±0.99	LSB	Guaranteed no missed codes to 12 bits
Offset Error		±1	±6	LSB	
Offset Error Matching		±0.5	±1	LSB	
Offset Temperature Drift		4		ppm/°C	
Gain Error		±1	±2	LSB	
Gain Error Matching		±0.5	±1	LSB	
Gain Temperature Drift		0.5		ppm/°C	
ANALOG INPUT					
Input Voltage Ranges	0		V_{REF}	V	
DC Leakage Current		±0.01	±1	µA	
Input Capacitance		32		pF	When in track
Input Impedance		TBD		kΩ	@ 1 MSPS
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[3]	2.4875	2.5	2.5125	V	±0.5% maximum @ 25°C
Long-Term Stability		150		ppm	For 1000 hours
Output Voltage Hysteresis[1]		50		ppm	
Reference Input Voltage Range[4]	2.0		2.5	V	
DC Leakage Current		±0.01	±1	µA	External reference applied to Pin V_{REF}
Input Capacitance		TBD		pF	
V_{REF} Output Impedance		1		Ω	
Reference Temperature Coefficient		6	25	ppm/°C	
V_{REF} Noise		60		µV rms	Bandwidth = TBD kHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}			V	
Input Low Voltage, V_{INL}			+0.3 x V_{DRIVE}	V	
Input Current, I_{IN}		±0.01	±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[2]		3		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2			V	
Output Low Voltage, V_{OL}			0.4	V	
Floating State Leakage Current		±0.01	±1	µA	
Floating State Output Capacitance[2]		8		pF	
TEMPERATURE SENSOR—INTERNAL					
Operating Range	–40		+125		
Accuracy		±1	±2	°C	T_A = –40°C to +85°C
		±2	±3	°C	T_A = >85°C to 125°C
Resolution		0.25		°C	LSB size
CONVERSION RATE					
Conversion Time	T_2 + 16 × t_{SCL}	1		µs	For V_{IN}0 to V_{IN}7, with one cycle Latency.
	100			µs	T_{SENSE} Channel
Track/Hold Acquisition Time[2]			TBD	ns	Full-scale step input
Throughput Rate			1	MSPS	f_{SCLK} = 20 MHz, for analog voltage conversions, one cycle Latency,
			10	KSPS	For T_{SENSE} channel, one cycle Latency
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
V_{DD}	2.8	3	3.6	V	See
V_{DRIVE}	1.65	3	3.6	V	
I_{TOTAL}[5]					V_{DD} = 3.3V
Normal Mode (Operational)[6]			5	mA	
Normal Mode (Static)			3	mA	
Partial Power-Down Mode			TBD	mA	
Full Power-Down Mode		5	60	µA	
Power Dissipation					V_{DD} = 3.3V
Normal Mode (Operational)			16.5	mW	
Normal Mode (Static)			9.9	mW	
Partial Power-Down Mode			TBD	mW	
Full Power-Down Mode			1.65	µW	

[1] See the Terminology Section.
[2] Sample tested during initial release to ensure compliance.
[3] Refers to Pin V_{REF} specified for 25°C.
[4] V_{REF} variations from 2.5V will alter the gain error of the temperature sensor, °C per LSB, and a correction factor may be required, See Section X.
[5] I_{TOTAL} is the total current flowing in V_{DD} and V_{DRIVE}.
[6] Current and power typical specifications are based on results with V_{DD} = 3V and V_{DRIVE} = 1.8V

TIMING SPECIFICATIONS

V_{DD} = 2.8V to 3.6V; V_{DRIVE} = 1.65 V to 3.6 V; V_{REF} = 2.5 V internal/external; T_A = −40°C to + 125°C, unless otherwise noted. [7]

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Test Conditions/Comments
$t_{CONVERT}$	16 × t_{SCLK}	µs max	Conversion time
	1	µs max	For each ADC channel $V_{IN}0$ to $V_{IN}7$, F_{SCLK} = 20MHz
	100	µs max	For Temperature Sensor channel
f_{SCLK}	50	kHz min	Frequency of external serial clock
	20	MHz max	Frequency of external serial clock
t_{QUIET}	TBD	ns min	Minimum quiet time required between the end of serial read and the start of the next voltage conversion in repeat and non-repeat mode.
	TBD	ns min	Minimum quiet time required between the end of serial read and the start of the next temperature conversion, for consecutive Temperature conversions.
t_2	10	ns min	CS to SCLK setup time
t_3	25	ns max	Delay from CS until DOUT three-state disabled
t_4	TBD	ns max	Data access time after SCLK falling edge
t_5	0.4 × t_{SCLK}	ns min	SCLK low pulsewidth
t_6	0.4 × t_{SCLK}	ns min	SCLK high pulsewidth
t_7	TBD	ns min	SCLK to DOUT valid hold time
t_8	15/45	ns min/max	SCLK falling edge to DOUT high impedance
t_9	10	ns min	DIN setup time prior to SCLK falling edge
t_{10}	5	ns min	DIN hold time after SCLK falling edge
t_{11}	TBD	ns min	T_{SENSE}BUSY falling edge to $\overline{CS}$ falling edge
$t_{POWER-UP\_PARTIAL}$	TBD	µs max	Power-up time from partial power-down
$t_{POWER-UP}$	TBD	µs max	Power-up time from full power-down

[7] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD} to AGND, DGND,	−0.3 V to +5 V
V_{DRIVE} to AGND, DGND,	−0.3 V to + 5 V
Analog Input Voltage to AGND	−0.3 V to 3V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
V_{REF} to AGND	−0.3 V to +3V
AGND to DGND	−0.3 V to +0.3V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LFCSP Package	
θ_{JA} Thermal Impedance	TBD°C/W
θ_{JC} Thermal Impedance	TBD°C/W
Pb-free Temperature, Soldering Reflow	260(+0)°C
ESD	2 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

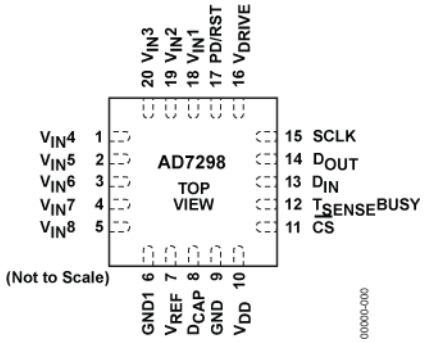

Figure 2. Pin Configuration

Note: The exposed metal paddle on the bottom of the LFCSP package should be soldered to PCB ground for proper heat dissipation & performance

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1-5, 18, 19, 20	V_{IN1}, $V_{N2,}$ V_{N3}, $V_{N4,}$ V_{N5}, V_{N6} V_{N7}, V_{N8}	Analog Inputs. The AD7298 has 8 single-ended analog inputs that are multiplexed into the on-chip track-and-hold. Each input channel can accept analog inputs from 0V to 2.5V. Any unused input channels should be connected to GND1 to avoid noise pickup.
14	D_{OUT}	Serial Data Output. The conversion result from the AD7298 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7298 consists of four address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data (MSB first). The output coding is straight binary for the voltage channels and two's complement for the temperature sensor result.
16	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at the voltage at which the interface operates. This pin should be decoupled to GND. The voltage range on this pin is 1.65V to 3.6V and may be less than the voltage at V_{DD}, but should never exceed it by more than 0.3V.
10	V_{DD}	Supply Voltage, 2.8 V to 3.6 V. This supply should be decoupled to GND with 10 µF and 100 nF decoupling capacitors.
7	V_{REF}	Internal Reference / External Reference supply. The nominal internal reference voltage of 2.5V appears at this pin. Provided the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system. Decoupling capacitors should be connected to this pin to decouple the reference buffer. For best performance, it is recommended to use a 10 µF decoupling capacitor on this pin to GND1. The internal reference can be disabled and an external reference supplied to this pin if required. The input voltage range for the external reference is 2.0 V to 2.5V.
6	GND1	Ground. Ground reference point for the internal reference circuitry on the AD7298. The external reference signals and all analog input signals should be referred to this GND1 voltage. The GND1 pin should be connected to the GND plane of a system. All GND1 pins should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. The V_{REF} should be decoupled to this ground pin via a 10 µF decoupling cap.
9	GND	Ground. Ground reference point for all analog and digital circuitry on the AD7298. The GND pin should be connected to the GND plane of the system. All GND pins should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. Both D_{CAP} and V_{DD} should be decoupled to this GND pin.
11	$\overline{CS}$	Chip Select, Active Low Logic Input. This pin is edge triggered, on the falling edge of this input, the track/hold goes into hold mode and a conversion is initiated. This input also frames the serial data transfer. When $\overline{CS}$ is low, the output bus is enabled, and the conversion result becomes available on the D_{OUT} output.
15	SCLK	Serial Clock, Logic Input. A serial clock input provides the SCLK for accessing the data from the AD7298.

Pin No.	Mnemonic	Description
12	T_{SENSE}_BUSY	Busy Output. BUSY transitions high when a temperature sensor conversion starts and remains high until the conversion completes
13	D_{IN}	Data In. Logic input. Data to be written to the AD7298 control register is provided on this input and is clocked into the register on the falling edge of SCLK.
17	$\overline{PD}$/RST	Power Down Pin. This pin will place the part into a full power down mode and will enable power conservation when the parts operation is not required. This pin can be used to RESET the device by toggling the pin LOW for a minimum of TBD ns and a maximum of 100ns. If the maximum time is exceeded the part will enter power-down mode.
8	D_{CAP}	Decoupling Capacitor Pins. Decoupling capacitors (1 µF recommended) are connected to this pins to decouple the internal LDO.

CONTROL REGISTER

The control register of the AD7298 is a 16-bit, write-only register. Data is loaded from the DIN pin of the AD7298 on the falling edge of SCLK. The data is transferred on the DIN line at the same time that the conversion result is read from the part. The data transferred on the DIN line corresponds to the AD7298 configuration for the next conversion. This requires 16 serial clocks for every data transfer. Only the information provided on the first 16 falling clock edges (after the falling edge of $\overline{CS}$) is loaded to the control register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table 6 and Table 7. On power up the default content of the control register is all zero's.

Table 6. Control Register Bit Functions

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WRITE	REPEAT	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	T_{SENSE}	DONTC	DONTC	EXT_REF	T_{SENSE} AVG	PD

Table 7. Control Register Bit Function Description

Bit	Mnemonic	Description
15	WRITE	The value written to this bit of the control register determines whether the following 15 bits are loaded to the control register. If this bit is a 1, the following 15 bits are written to the control register; if it is a 0, then the remaining 15 bits are not loaded to the control register and it remains unchanged.
	REPEAT	This bit enables the repeated conversion of the selected sequence of channels.
	CH1 to CH8	Channel selection bits: These eight bits are loaded at the end of the current conversion and select which analog input channel is to be converted in the next serial transfer, or they may select the sequence of channels for conversion in the subsequent serial transfers. Each CH_X bit corresponds to an analog input channel. A channel or sequence of channels is selected for conversion by writing a 1 to the appropriate CH_X bit/bits. Channel address bits corresponding to the conversion result are output on D_{OUT} prior to the 12 bits of data. The next channel to be converted on is selected by the mux on the 14th SCLK falling edge.
	T_{SENSE}	Writing a 1 to this bit enables the temperature conversion. When the temperature sensor is selected for conversion the TSENSE_BUSY pin will go high after the next CS falling edge to indicate that the conversion is in progress, the previous conversion result can be read while the temperature conversion is in progress. Once TSENSE_Busy goes low, $\overline{CS}$ can be brought low Tx ns later to read the T_{SENSE} conversion result.
	DONTC	Don't care.
	EXT_REF	Writing a logic 1 to this bit, enables the use of an external reference. The input voltage range for the external reference is 2V to 2.5V. The external reference should not exceed 2.5V or the device performance will be affected.
	T_{SENSE} AVG	Writing a 1 to this bit enables the temperature sensor averaging function. When averaging is enabled, the AD7298 internally computes a running average of the conversion results to determine the final T_{SENSE} result (See page 14 for more details). This mode will reduce the influence of noise on the final T_{SENSE} result. Selecting this feature does not automatically select the T_{SENSE} for conversion. The T_{SENSE} bit must also be set to start a temperature sensor conversion.
	PD	Partial Power Down. This mode is selected by writing a 1 to this bit in the control register. In this mode, some of the internal analog circuitry is powered down. The AD7298 retains the information in the control register while in partial power down mode. The part remains in this mode until a 0 is written to this bit.

Table 8. Channel Address bits

ADD3	ADD2	ADD1	ADD0	Analog Input Channel
0	0	0	0	$V_{IN}1$
0	0	0	1	$V_{IN}2$
0	0	1	0	$V_{IN}3$
0	0	1	1	$V_{IN}4$
0	1	0	0	$V_{IN}5$
0	1	0	1	$V_{IN}6$
0	1	1	0	$V_{IN}7$
0	1	1	1	$V_{IN}8$
1	0	0	0	T_{SENSE}
1	0	0	1	T_{SENSE} with averaging enabled

MODES OF OPERATION

The AD7298 has a number of different modes of operation, which are designed to provide additional flexibility for the user. These options can be chosen by programming the content of the control register to select the desired mode.

TRADITIONAL MULTI-CHANNEL MODE OF OPERATION

The AD7298 can operate as a traditional multi-channel ADC, where each serial transfer selects the next channel for conversion. One must write to the control register to configure and select the desired input channel prior to initiating any conversions. In traditional mode of operation, the $\overline{CS}$ signal is used to frame the first write to the converter on the D_{IN} pin. In this mode of operation the REPEAT bits in the control register is set to a low logic level, 0, hence the REPEAT function is not in use. The data, which appears on the D_{OUT} pin during the initial write to the control register, is invalid. The first $\overline{CS}$ falling edge will initiate a write to the control register to configure the device, a conversion is then initiated for the selected analog input channel ($V_{IN}1$) on the subsequent (2^{nd}) $\overline{CS}$ falling edge, the third $\overline{CS}$ falling edge will have the result ($V_{IN}1$) available for reading. The AD7298 operates with one cycle latency; hence the conversion result corresponding to each conversion is available once serial read cycle after the cycle in which the conversion was initiated.

As the device operates with one cycle latency, the control register configuration sets up the configuration for the next conversion, which is initiated on the next $\overline{CS}$ falling edge but the first bit of the corresponding result is not clocked out until the subsequent falling $\overline{CS}$ edge as shown in Figure 3.

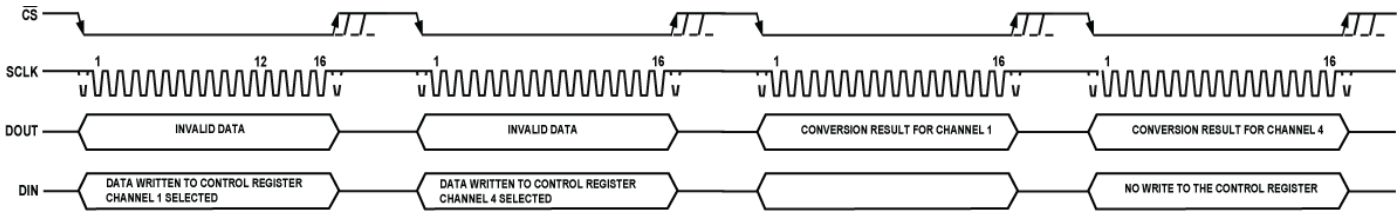

Figure 3. Configuring a conversion and read with the AD7298. One channel selected for conversion.

If more than one channel is selected in the control register, the AD7298 will convert all selected channels sequentially in ascending order on successive $\overline{CS}$ falling edges. Once all the selected channels in the control register are converted the AD7298 will cease converting until the user rewrites to the control register to select the next channel for conversion. This operation is shown in Figure 4

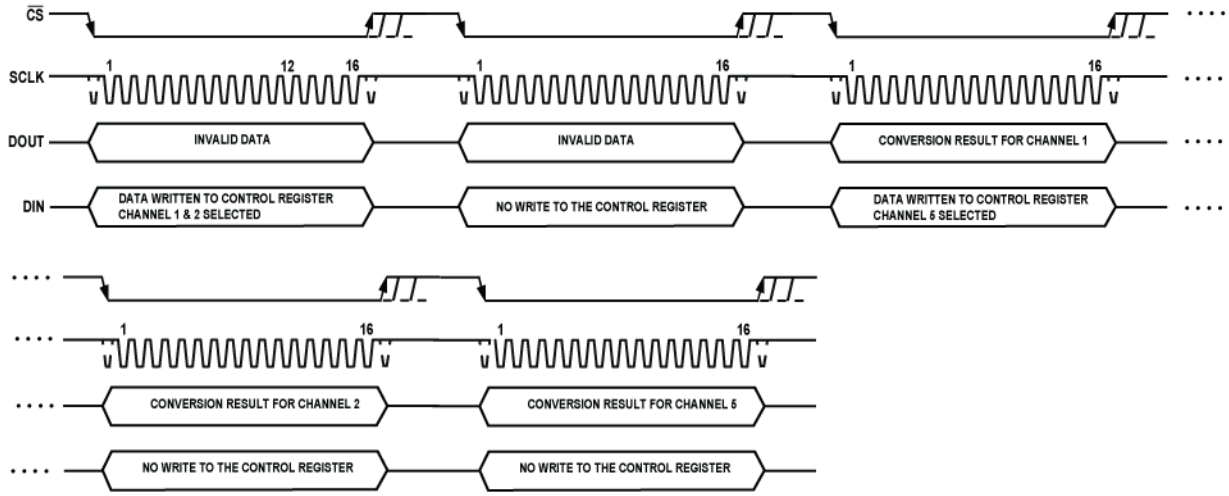

Figure 4. Configuring a conversion and read with the AD7298. Numerous channels selected for conversion

REPEAT OPERATION

The REPEAT bit in the control register allows the user to select a sequence of channels on which the AD7298 will continuously convert. When the REPEAT bit is set in the control register, the AD7298 will continuously cycle through the selected channels in ascending order, beginning with the lowest channel and converting all channels selected in the control register. On completion of the sequence, the AD7298 returns to the first selected channel in the control register and recommences the sequence again. The conversion sequence of the selected channels in the repeat mode of operation continues until such time as the control register of the AD7298 is reprogrammed. If the T_{SENSE} bit is selected in the Control Register then the temperature conversion will be available for conversion after the last analog input channel in the sequence has been converted. It is not necessary to write to the control register once a REPEAT operation has been initiated unless a change in the AD7298 configuration is required. The WRITE bit must be set to zero or the DIN line tied low to ensure that the control register is not accidentally overwritten, or the automatic conversion sequence interrupted. A write to the control register during REPEAT mode of operation will reset the cycle even if the selected channels are unchanged. Hence, the next conversion by the AD7298 after a write operation will be the first selected channel in the sequence.

To select a sequence of channels, the associated channel bit must be set to a logic high state (1) for each analog input whose conversion is required. For example, if the REPEAT bit = 1 and CH1, CH2 and CH3 =1. The $V_{IN}1$ analog input will be converted on the first $\overline{CS}$ falling edge following the write to the control register, the $V_{IN}2$ channel will be converted on the subsequent $\overline{CS}$ falling edge and the $V_{IN}1$ conversion result will be available for reading, the third $\overline{CS}$ falling edge following the write operation will initiate a conversion on $V_{IN}3$ and have the $V_{IN}2$ result available for reading. The AD7298 operates with one cycle latency; hence the conversion result corresponding to each conversion is available once serial read cycle after the cycle in which the conversion was initiated.

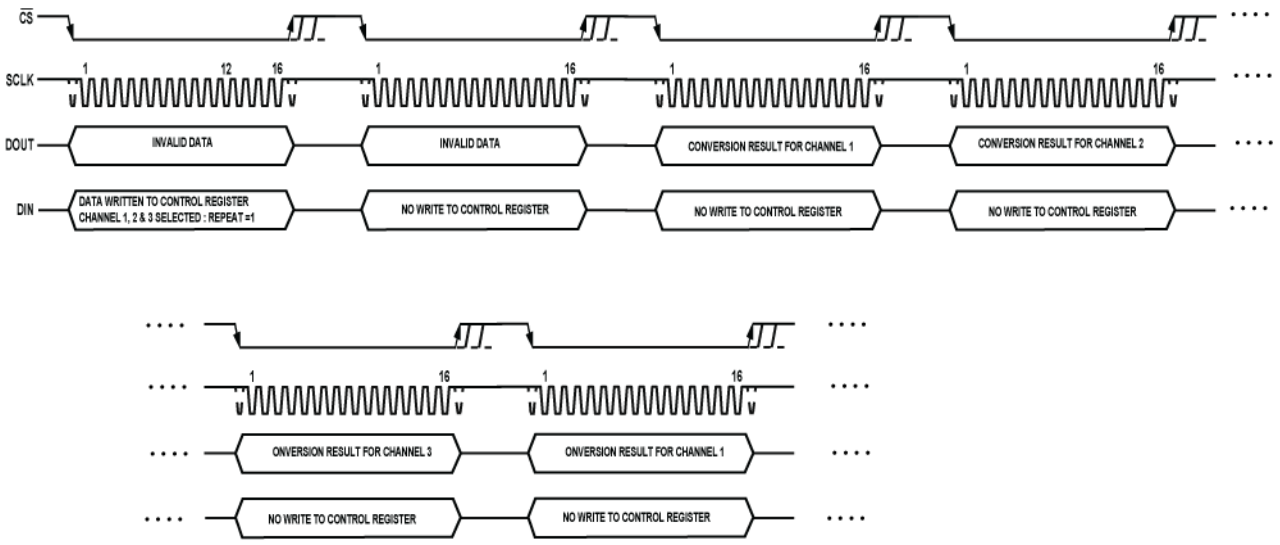

Figure 5. Configuring a conversion and read in REPEAT mode.

This mode of operation simplifies the operation of the device by allowing consecutive channels to be converted without having to reprogram the control register or write to the part on each serial transfer. Figure 5 illustrates how to setup the AD7298 to continuously convert on a particular sequence of channels. To exit REPEAT mode of operation and revert back to the traditional mode of operation of a multi-channel ADC, ensure that the REPEAT bit = 0 on the next serial write.

POWER-DOWN MODES

The AD7298 has a number of power conservation modes of operation, which are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements. The power-down modes of operation of the AD7298 is controlled by the power-down bit, in the control register and the PD pin on the device. When power supplies are first applied to the AD7298, care should be taken to ensure that the part is placed in the required mode of operation

NORMAL MODE

This mode is intended for the fastest throughput rate performance because the user does not have to worry about any power-up times with the AD7298 remaining fully powered at all times. Figure 6 shows the general diagram of the operation of the AD7298 in this mode. The conversion is initiated on the falling edge of $\overline{CS}$ and the track-and-hold enters hold mode. On the14th SCLK falling edge the track-and-hold returns to track mode and starts acquiring the analog input, as described in the serial interface section. The data presented to the AD7298 on the DIN line during the first 16 clock cycles of the data transfer are loaded into the control register (provided the WRITE bit is 1). The part remains fully powered up in normal mode at the end of the conversion as long as PD bit is set to 0 in the write transfer during that conversion. To ensure continued operation in normal mode, the PD bit should be loaded with 0 on every data write operation. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. For specified performance, the throughput rate should not exceed 1MSPS. Once a conversion is complete and the $\overline{CS}$ has returned high, a minimum of the quiet time, t_{QUIET}, must elapse before bringing $\overline{CS}$ low again to initiate another conversion and access the previous conversion result.

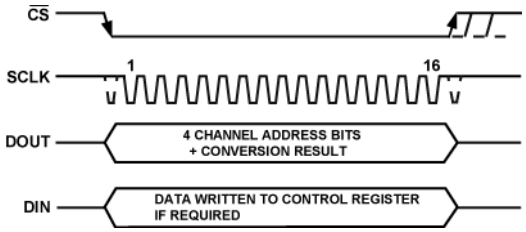

Figure 6. Normal Mode Operation

PARTIAL POWER DOWN MODE

In this mode, part of the internal circuitry on the AD7298 is powered-down. The AD7298 enters partial power-down on the $\overline{CS}$ rising edge once the current serial write operation containing 16 SCLK clock cycles is completed. To enter partial power-down the PD bit in the control register should be set to one on the last required read transfer from the AD7298. Once in partial power-down mode the AD7298 transmits all ones on the D_{OUT} pin if $\overline{CS}$ is toggled low. If the averaging feature for the temperature sensor is enabled in the control register, the averaging is reset once the device enters partial power-down mode.

The AD7298 remains in partial power-down until the power-down bit, PD, in the control register is changed to a logic level zero (0). The AD7298 begins powering up on the rising edge of $\overline{CS}$ following the write to the control register disabling the power-down bit. Once T_{QUITE} has elapsed, a full 16-SCLK write to the control register must be completed to update its content with the desired channel configuration for the subsequent conversion. A valid conversion is then initiated on the next $\overline{CS}$ falling edge. Since the AD7298 has once cycle latency, the first conversion result after exiting partial power-down mode is available in the fourth serial transfer as shown in Figure 7; 1st cycle to update PD bit, 2nd cycle to update configuration and Channel ID bits, 3rd to complete conversion, 4th access D_{OUT} valid result. The use of this mode enables a reduction in the overall power consumption of the device.

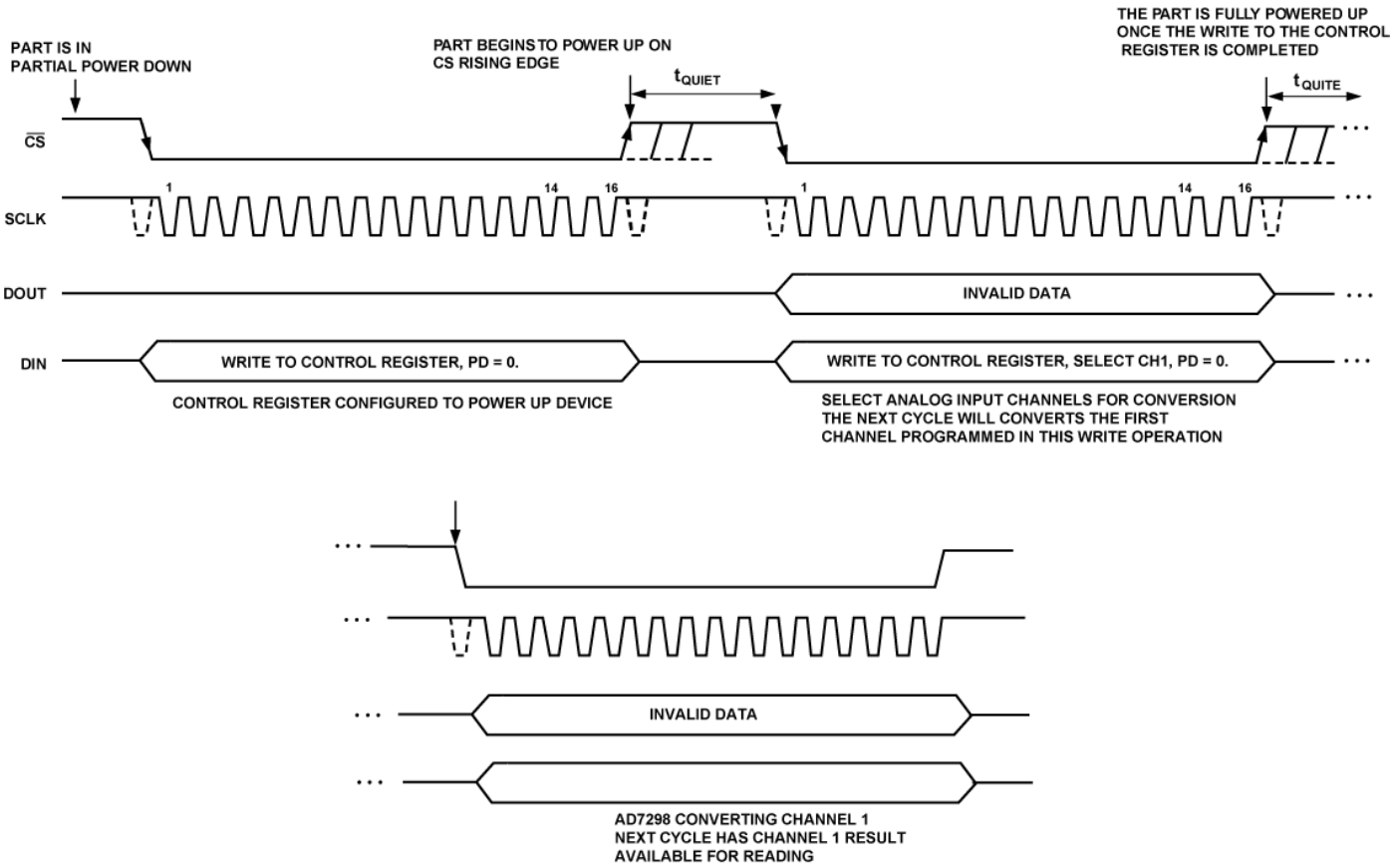

Figure 7. Partial Power Down Mode of Operation

FULL POWER-DOWN MODE

In this mode, all internal circuitry on the AD7298 is powered-down and no information is retained in the control register or any other internal register. If the averaging feature for the temperature sensor is enabled in the control register (T_{SENSE}AVG), the averaging is reset once the device enters power-down mode. The AD7298 is placed into full power-down mode by bringing the logic level on the PD pin low for greater than 100ns. The PD pin is asynchronous to the clock, hence it can be triggered at any time. The part can be powered up for normal operation by bringing the PD pin logic level back to a high logic state. The full power-down feature can be used to reduce the average power consumed by the AD7298 when operating at lower throughput rates. The user should ensure that t_{POWER_UP} has elapsed prior to programming the control register and initiating a valid conversion.

POWERING UP THE AD7298

The AD7298 contains a power on reset circuit, which sets the control register to its default setting of all zero's, hence the internal reference is enabled and the device is configured for normal mode of operation. It takes 100µs to power up the AD7298 when using the internal reference. When an external reference is used TBD µs are required to power up the AD7298 with a 1µF decoupling capacitor.

When supplies are first applied to the AD7298, the user must wait the specified power up time, $t_{POWER\ UP}$, before programming the control register to select the desired channels for conversion.

RESET

The AD7298 includes a reset feature, which can be used to reset the device and the content of all internal registers including the control register to their default state. To activate the reset operation, the PD pin should be brought low for a minimum of TBD ns and a maximum of 100ns and is asynchronous to the clock, hence it can be triggered at any time. If the PD pin is held low for greater than 100ns the part will enter full power-down mode. It is imperative that the PD pin be held at a stable logic level at all times to ensure normal operation.

CIRCUIT INFORMATION

The AD7298 is a high speed, 8-channel, 12-bit, ADC with internal temperature sensor. The part can be operated from a 2.8 V to 3.6 V supply and is capable of throughput rates of 1MSPS per analog input channel.

The AD7298 provides the user with an on-chip, track-and-hold ADC and a serial interface housed in a 20-lead LFCSP. The AD7298 has eight single-ended input channels with channel repeat functionality, which allows the user to select a channel sequence through which the ADC can cycle with each consecutive $\overline{CS}$ falling edge. The serial clock input accesses data from the part, controls the transfer of data written to the ADC, and provides the clock source for the successive approximation ADC. The analog input range for the AD7928 is 0V to $V_{REF.}$ The AD7298 operates with one cycle latency, which means that conversion result is available in the serial transfer following the cycle in which the conversion is performed.

The AD7298 includes a high accuracy band-gap temperature sensor, which is monitored and digitized by the 12-bit ADC to give a resolution of 0.25°C. The AD7298 provides flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the power-down bit, PD, in the control register.

CONVERTER OPERATION

The AD7298 is a 12-bit successive approximation ADC based around a capacitive DAC. Figure 8 and Figure 9 show simplified schematics of the ADC. The ADC is comprised of control logic, SAR, and a capacitive DAC that are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 8 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected V_{IN} channel.

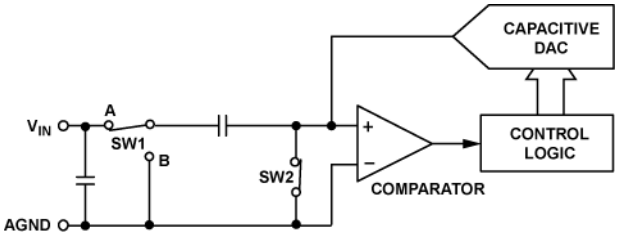

Figure 8. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 9), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 11 shows the ADC's transfer functions.

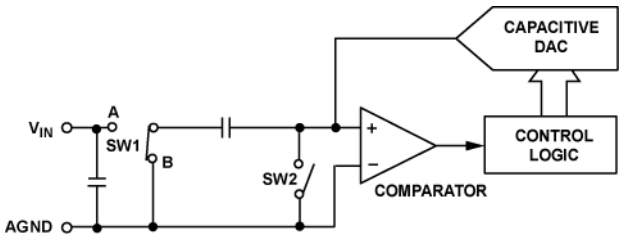

Figure 9. ADC Conversion Phase

ANALOG INPUT

Figure 11 shows an equivalent circuit of the analog input structure of the AD7298. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the internally generated LDO voltage of 2.5V (D_{CAP}) by more than 300 mV. This causes the diodes to become forward biased and start conducting current into the substrate. 10 mA is the maximum current these diodes can conduct without causing irreversible damage to the part. Capacitor C1, in Figure 10 is typically about TBD pF and can primarily be attributed to pin capacitance. The Resistor R1 is a lumped component made up of the on resistance of a switch (track-and-hold switch) and also includes the on resistance of the input multiplexer. The total resistance is typically about TBD Ω. The capacitor, C2, is the ADC sampling capacitor and has a capacitance of TBD pF typically.

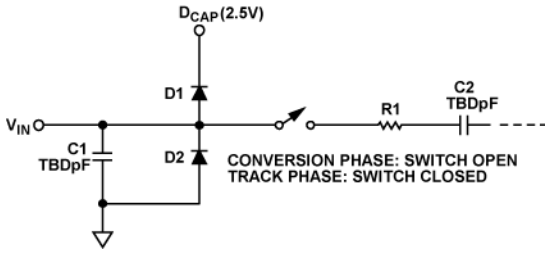

Figure 10. Equivalent Analog Input Circuit

For AC applications, removing high frequency components from the analog input signal is recommended by using an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratios are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application performance criteria.

ADC Transfer Function

The output coding of the AD7298 is straight binary for the analog input channel conversion results and twos complement, for the temperature conversion result. The designed code transitions occur at successive LSB values (that is, 1 LSB, 2 LSBs, and so forth). The LSB size is $V_{REF}/4096$ for the AD7298. The ideal transfer characteristic for the AD7298 for straight binary coding is shown in Figure 11.

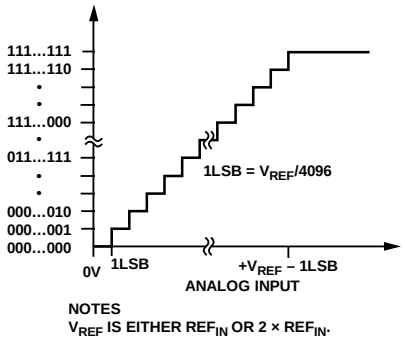

Figure 11. Straight Binary Transfer Characteristic

TEMPERATURE SENSOR OPERATION

The AD7298 contains one local temperature sensor. The on-chip, band gap temperature sensor measures the temperature of the AD7298 die. The temperature sensor module on the AD7298 is based on the three current principle (see Figure 12), where three currents are passed through a diode and the forward voltage drop is measured, allowing the temperature to be calculated free of errors caused by series resistance.

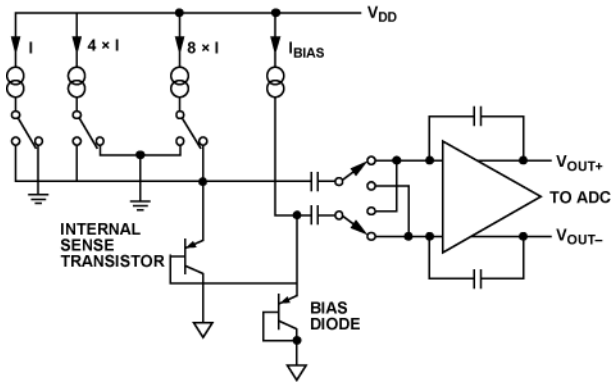

Figure 12. Top Level Structure of Internal Temperature Sensor

The temperature conversion consists of two phases, the integration followed by the conversion. The integration is initiated on the $\overline{CS}$ falling edge. It takes a period of approximately100µs to complete the integration and conversion of the temperature result. When the integration is completed the conversion is initiated automatically. Once the temperature integration is initiated, the T_{SENSE}BUSY signal goes high to indicate that a temperature conversion is in progress and remains high until the conversion is completed.

Theoretically, the temperature measuring circuit can measure temperatures from −512°C to +511°C with a resolution of 0.25°C. However, temperatures outside T_A (the specified temperature range for the AD7298) are outside the guaranteed operating temperature range of the device. The temperature sensor is selected by setting the T_{SENSE} bit in the control register.

Temperature Sensor Averaging

The AD7298 incorporates a temperature sensor averaging feature to enhance the accuracy of the temperature measurements. To enable the temperature sensor averaging feature both the T_{SENSE}AVG bit and the T_{SENSE} bit must be enabled in the control register. In this mode the temperature is internally averaged to reduce the effect of noise on the temperature result. The temperature is measured each time a T_{SENSE} conversion is performed and a moving average method is used to determine the result in the T_{SENSE} Average Result Register. The average result is given by the following equation;

$$TSENSE\_AVG = \frac{7}{8}(\text{Previous\_Result}) + \frac{1}{8}(Current\_\text{Result})$$

The T_{SENSE} result read when averaging is enabled is T_{SENSE}AVG result, a moving average temperature measurement.

The first T_{SENSE} conversion result given by the AD7298 after the temperature sensor and averaging mode has been selected in the control register (bit D1 & D5) is the actual first T_{SENSE} conversion result. If the control register is written to and the content of the T_{SENSE}AVG bit changed the averaging function is reset and the next T_{SENSE} average conversion result is the current temperature conversion result. If the status of the T_{SENSE}AVG bit is not changed on successive writes to the control register, the averaging function will not be reinitialized and will continue calculating the cumulative average.

The user has the option of disabling the averaging by setting bit T_{SENSE}AVG to '0' in the control register. The AD7298 defaults on power-up with the averaging function disabled. The total time to measure, a temperature channel is typically 100 µs.

Temperature Value Format

One LSB of the ADC corresponds to 0.25°C. The temperature reading from the ADC is stored in a 12-bit twos complement format, to accommodate both positive and negative temperature measurements. The temperature data format is provided in Table 9.

Table 9. Temperature Data Format

Temperature (°C)	Digital Output
−40	1111 0110 0000
−25	1111 1001 1100
−10	1111 1101 1000
−0.25	1111 1111 1111
0	0000 0000 0000
+0.25	0000 0000 0001
+10	0000 0010 1000
+25	0000 0110 0100
+50	0000 1100 1000
+75	0001 0010 1100
+100	0001 1001 0000
+105	0001 1010 0100
+125	0001 1111 0100

Temperature Conversion Formula:

Positive Temperature = *ADC Code*/4

Negative Temperature = (4096 - *ADC Code*)/4

V_{DRIVE}

The AD7298 also has the V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both a 1.8V and 3V processors. For example, if the AD7298 were operated with a V_{DD} of 3.3V, the V_{DRIVE} pin could be powered from a 1.8V supply. This enables the AD7298 to operate with a larger dynamic range with an V_{DD} of 3.3V while still being able to interface to 1.8V processors. Take care to ensure V_{DRIVE} does not exceed V_{DD} by more than 0.3V (see the Maximum Ratings Section).

THE REFERENCE

The AD7298 can operate with either the internal 2.5V on-chip reference or an externally applied reference. The EXT_REF bit in the control register is used to determine whether the internal reference is used. If the EXT_REF bit is selected in the control register, an external reference can be supplied through the V_{REF} pin. On power-up, the internal reference is enabled. Suitable external reference sources for the AD7298 include AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5V band-gap reference and a reference buffer. When the AD7298 is operated in internal reference mode, the 2.5V internal reference is available at the V_{REF} pin, which should be decoupled to AGND using a 10 µF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system. The internal reference is capable of sourcing up to TBD µA of current when the converter is static. The reference buffer requires 10ms to power up and charge the TBD µF decoupling capacitor during the power-up time.

SERIAL INTERFACE

Figure 13 shows the detailed timing diagram for the serial interface to the AD7298. The serial clock provides the conversion clock and controls the transfer of information to and from the AD7298 during each conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode at which point the analog input is sampled and the bus is taken out of three-state. The conversion is also initiated at this point and requires 16 SCLK cycles to complete. The track-and-hold goes back into track on the 14th SCLK falling edge as shown in Figure 13 at Point B. On the 16th SCLK falling edge or on the rising edge of $\overline{CS}$, the D_{OUT} line goes back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion is terminated, the D_{OUT} line goes back into tri-state, and the control register is not updated; otherwise D_{OUT} returns to three-state on the 16th SCLK falling edge. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7298.

For the AD7298, four-channel address bits (ADD3 to ADD0) identify which channel the conversion result corresponds, to precede the 12 bits of data. The $\overline{CS}$ going low provides the first address bit to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with a second address bit. Thus, the first falling clock edge on the serial clock has the first address bit provided for reading and also clocks out the second address bit. The 3 remaining address bits and 12 data bits are clocked out by subsequent SCLK falling edges. The final bit in the data transfer is valid for reading on the 16th falling edge having been clocked out on the previous (15th) falling edge.

In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge depending on the SCLK frequency. The first rising edge of SCLK after the $\overline{CS}$ falling edge would have the first address bit provided, and the 15th rising SCLK edge would have last data bit provided.

Writing information to the control register takes place on the first 16 falling edges of SCLK in a data transfer, assuming the MSB (that is, the WRITE bit) has been set to 1. The 16-bit word read from the AD7298 always contains four channel address bits that the conversion result corresponds to, followed by the 12-bit conversion result.

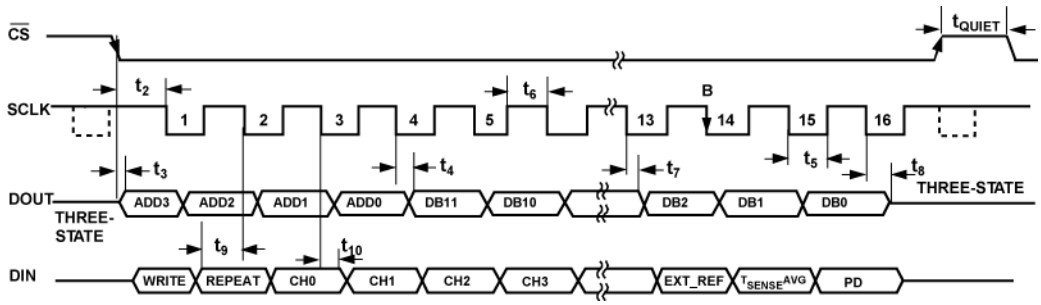

Figure 13. Serial Interface Timing Diagram

TEMPERATURE SENSOR READ.

The temperature sensor conversion involves two phases, the integration phase and the conversion phase as detailed in the Temperature Sensor Operation Section. The integration phase is initiated on the falling edge of $\overline{CS}$ and once completed the conversion is automatically initiated internally by the AD7298. When a temperature conversion integration is initiated, the T_{SENSE}BUSY signal goes high to indicate that a temperature conversion is in progress and remains high until the conversion is completed.

The total time to measure and convert a temperature channel with the AD7298 is 100 µs max. Once the T_{SENSE}BUSY signal goes low to indicate that the temperature conversion is completed, t_{11}ns must elapse prior to the next falling edge of $\overline{CS}$. If a minimum of t_{11} ns is not adhered to between the falling edge of T_{SENSE}BUSY and the subsequent falling edge of $\overline{CS}$, the next conversion will be corrupted but the temperature result that is framed by the $\overline{CS}$ will not be affected. This restriction is in place to ensure that sufficient acquisition time is allowed for the next conversion.

Once the T_{SENSE}BUSY signal goes high, the user may provide a $\overline{CS}$ falling edge to frame the read of the previous conversion and program the control register if required, see Figure 14. Once the previous conversion result has been read, any subsequent $\overline{CS}$ falling edges which occur while the T_{SENSE}BUSY signal is high are internally ignored by the AD7298. If additional $\overline{CS}$ falling edges are provided while T_{SENSE}BUSY is high, the AD7298 will provide an invalid digital output of all 1's. Alternatively, if $\overline{CS}$ remains high while, T_{SENSE}BUSY is high then the D_{OUT} bus will remain in three-state.

If the user writes to the control register during the first 16 SCLK cycles following T_{SENSE}BUSY going high, the configuration of the device for the next conversion, which will be initiated on the subsequent $\overline{CS}$ falling edge after T_{SENSE}BUSY goes low, is altered. If the user configures the part for partial power down in a write to the control register during the first 16 SCLK cycles following T_{SENSE}BUSY going high, the temperature sensor conversion will be aborted and the part will enter partial power down on the 16th SCLK falling edge.

It is thus recommended not to write to the control register if the $\overline{CS}$ signal will be toggling while T_{SENSE}BUSY is high. Hence, care should be taken to ensure that the write bit is set to zero during the temperature conversion phase when $\overline{CS}$ is toggling.

If an SCLK frequency of more than 10kHz is used, the temperature conversion will require more than one standard read cycle to complete. In this case, the user can monitor the T_{SENSE}BUSY signal to determine when the conversion is completed and the result is available for reading.

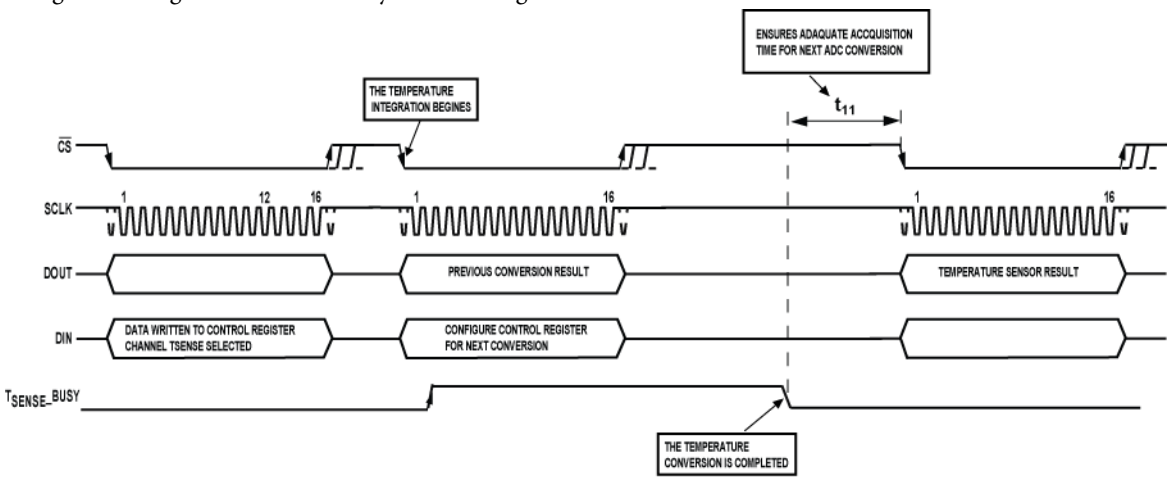

Figure 14. Serial Interface Timing Diagram for the Temperature Sensor Conversion.

OUTLINE DIMENSIONS

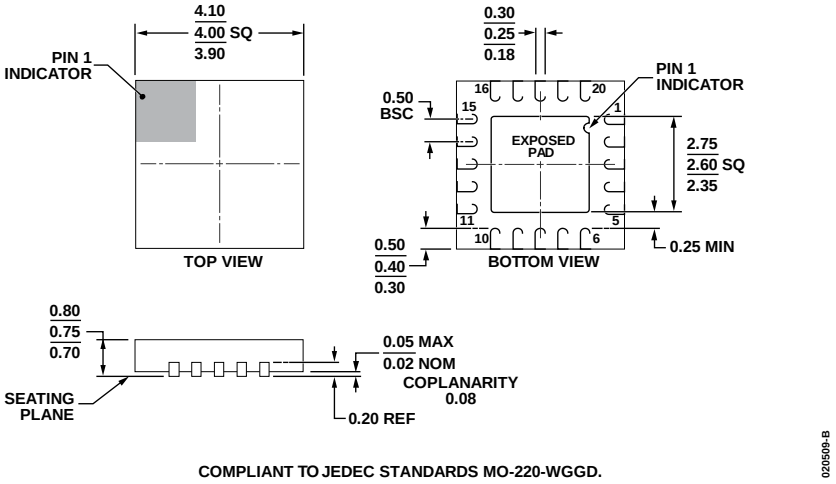

Figure 15. 20 Lead- Lead Frame Chip Scale Package

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7298BCPZ	−40°C to +125°C	20 Lead - Lead Frame Chip Scale package	CP-20-8
AD7298BCPZ-RL7	−40°C to +125°C	20 Lead - Lead Frame Chip Scale package	CP-20-8

PR08754-0-12/09(PrA)