

Power Amplifier/Antenna Switch + Low Noise Down Conversion Mixer for PHS

Description

The CXG7003FN is a MMIC consisting of the power amplifier, diversity antenna supported switch and low noise down conversion mixer.

This IC is designed using the Sony's GaAs J-FET process featuring a single positive power supply operation.

Features

- Operates at a single positive power supply: $V_{DD} = 3V$
- Diversity antenna supported switch
- Small mold package: 26-pin HSOF

<Power amplifier/antenna switch transmitter block>

- Low current consumption: $I_{DD} = 150mA$
($P_{OUT} = 20.2dBm$, $f = 1.9GHz$)
- High power gain: $G_p = 40dB$ Typ.
($P_{OUT} = 20.2dBm$, $f = 1.9GHz$)

<Antenna switch receiver block/
low noise down conversion mixer>

- Low current consumption: $I_{DD} = 5.5mA$ Typ.
(When no signal)
- High conversion gain: $G_c = 19.5dB$ Typ. ($f = 1.9GHz$)
- Low distortion: Input $IP_3 = -12dBm$ Typ. ($f = 1.9GHz$)
- High image suppression ratio: $IMR = 40dBc$ Typ.
($f = 1.9GHz$)
- High 1/2 IF suppression ratio: $1/2IFR = 47dBc$ Typ.
($f = 1.9GHz$)

Applications

Digital cordless telephones (PHS)

Structure

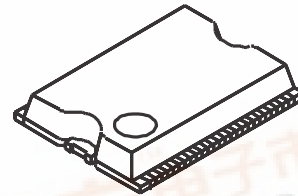
GaAs J-FET MMIC

Notes on Handling

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

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26 pin HSOF (Plastic)



Absolute Maximum Ratings

<Power amplifier block>

• Supply voltage	V_{DD}	6	V
• Voltage between gate and source	V_{GSO}	1.5	V
• Drain current	I_{DD}	550	mA
• Allowable power dissipation	P_D	3	W

<Switch block>

• Control voltage	V_{CTL}	6	V
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<Front-end block>

• Supply voltage	V_{DD}	6	V
• Input power	P_{RF}	10	dBm

<Common to each block>

• Channel temperature	T_{ch}	150	°C
• Operating temperature	T_{opr}	-35 to +85	°C
• Storage temperature	T_{stg}	-65 to +150	°C

Recommended Operating Conditions

<Common to each block>

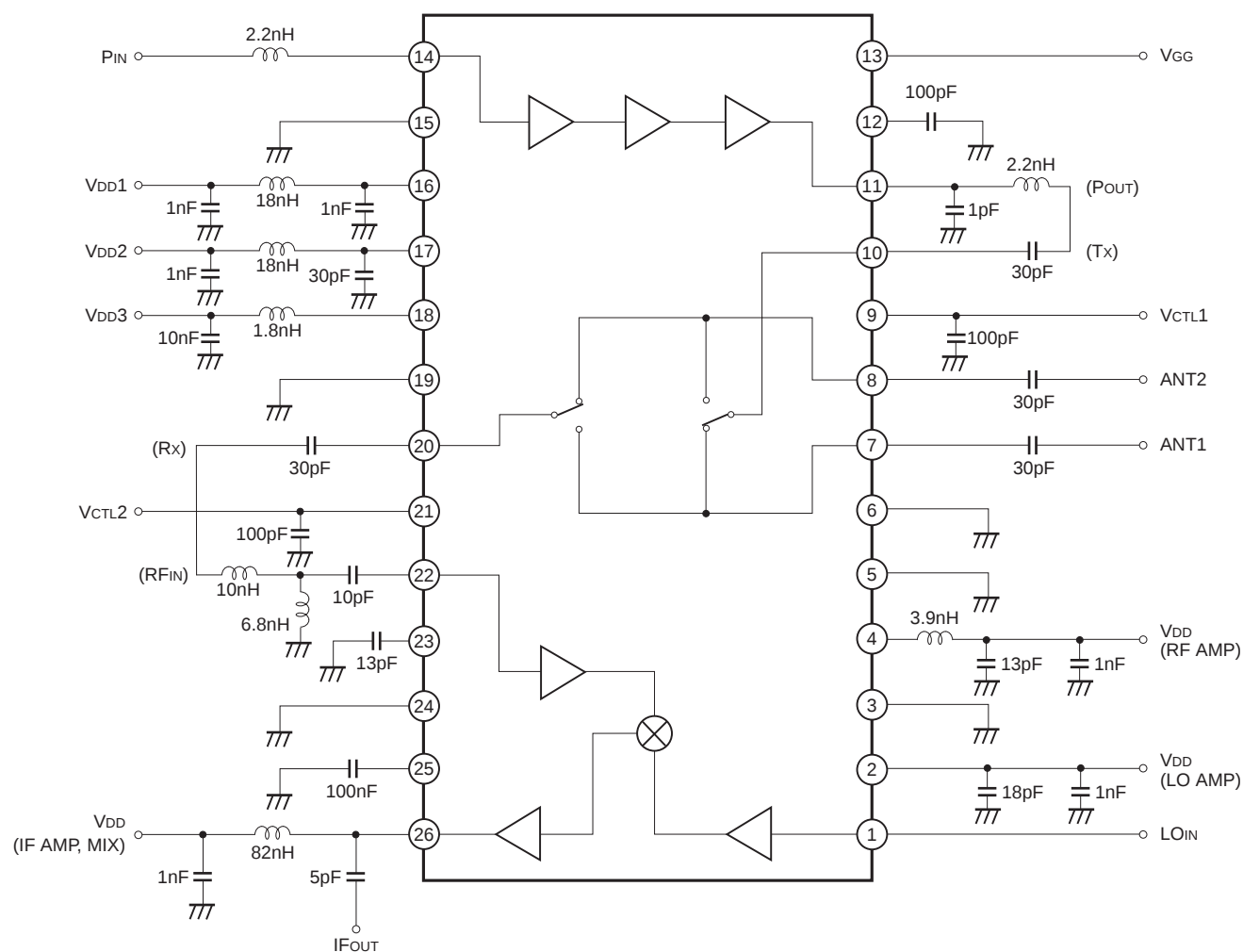
• Supply voltage	V_{DD}	2.7 to 3.3	V
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<Switch block>

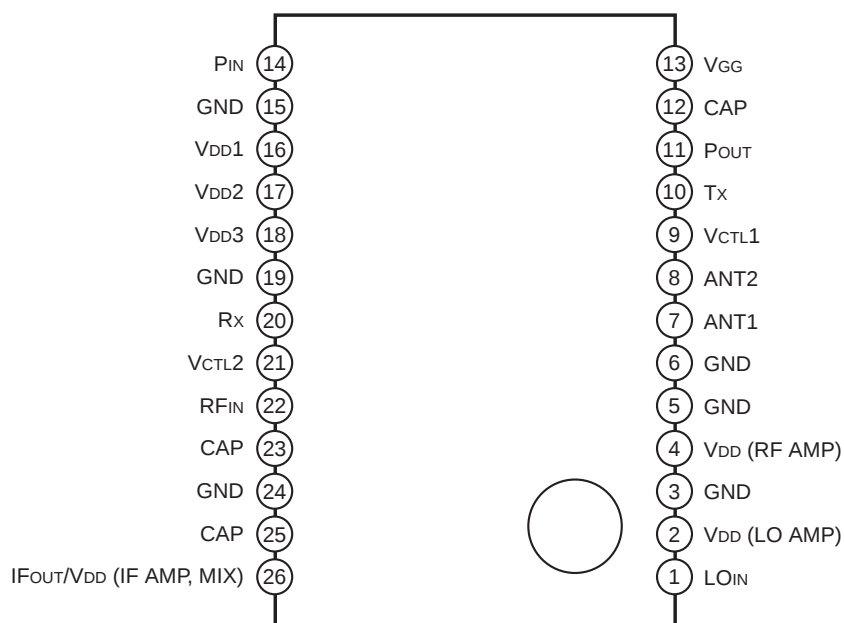
• Control voltage (H)	$V_{CTL}(H)$	2.9 to 3.3	V
• Control voltage (L)	$V_{CTL}(L)$	0 to 0.2	V

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Block Diagram and External Circuit



Pin Configuration



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Pin Description

Pin No.	Symbol	Description
1	LO _{IN}	Local signal input pin
2	V _{DD} (LO AMP)	V _{DD} pin of local amplifier
3	GND	GND pin
4	V _{DD} (RF AMP)	V _{DD} pin of RF amplifier
5	GND	GND pin
6	GND	GND pin
7	ANT1	Antenna switch pin. This pin is ANT1-Tx or ANT1-Rx by setting of V _{CTL1} and V _{CTL2} .
8	ANT2	Antenna switch pin. This pin is ANT2-Tx or ANT2-Rx by setting of V _{CTL1} and V _{CTL2} .
9	V _{CTL1}	Antenna switch control 1 pin
10	T _x	Tx pin. Signal is input to antenna switch during ANT-Tx.
11	P _{OUT}	Power amplifier output pin
12	CAP	Connection pin of external capacitor (for noise elimination)
13	V _{GG}	Gate voltage adjustment pin of power amplifier (first stage, middle stage, rear-end FET)
14	P _{IN}	Signal input pin to power amplifier
15	GND	GND pin
16	V _{DD1}	V _{DD1} pin of power amplifier (first stage FET)
17	V _{DD2}	V _{DD2} pin of power amplifier (middle stage FET)
18	V _{DD3}	V _{DD3} pin of power amplifier (rear-end FET)
19	GND	GND pin
20	R _x	Rx pin. ANT input signal is output to this pin during ANT1-Rx or ANT2-Rx.
21	V _{CTL2}	Antenna switch control 2 pin
22	R _{FIN}	RF signal input pin
23	CAP	External capacitor connection pin. This pin is connected to LNA FET source. RF amplifier characteristic is optimized during 1.9GHz by the capacitor of 13pF (Typ.).
24	GND	GND pin
25	CAP	External capacitor connection pin. IF amplifier distortion is improved by this capacitor.
26	I _{FOUT} /V _{DD} (IF AMP, MIX)	IF output and IF AMP, MIX V _{DD}

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Electrical Characteristics

These specifications are when the Sony's recommended evaluation board shown on page 8 is used.

1. Control Pin Logic for Antenna Switch

Conditions of control pins	ANT1 – Tx ANT2 – Rx	ANT2 – Tx ANT1 – Rx
$V_{CTL1} = 3V$, $V_{CTL2} = 0V$	ON	OFF
$V_{CTL1} = 0V$, $V_{CTL2} = 3V$	OFF	ON

2. Power Amplifier Block + Antenna Switch Transmitter Block

These specifications are common to the ANT1 transmission and ANT2 transmission.

Unless otherwise specified: $V_{DD} = 3V$, $I_{DD} = 150mA$, $P_{OUT} = 20.2dBm$, $f = 1.9GHz$

When ANT1 transmission: $V_{CTL1} = 3V$, $V_{CTL2} = 0V$

When ANT2 transmission: $V_{CTL1} = 0V$, $V_{CTL2} = 3V$

($T_a = 25^{\circ}C$)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}			150		mA
Gate voltage adjustment value	V_{GG}		0.04		0.6	V
Output power	P_{OUT}	Measured with the ANT pin	20.2			dBm
Power gain	G_P		36	40		dB
Adjacent channel leak power ratio ($600 \pm 100kHz$)	ACPR600kHz	Measured with the ANT pin		-63	-55	dBc
Adjacent channel leak power ratio ($900 \pm 100kHz$)	ACPR900kHz	Measured with the ANT pin		-70	-60	dBc
Occupied bandwidth	OBW	Measured with the ANT pin		250	275	kHz
2nd-order harmonic level	—	Measured with the ANT pin			-25	dBc
3rd-order harmonic level	—	Measured with the ANT pin			-25	dBc

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3. Antenna Switch Receiver Block + Low Noise Down Conversion Mixer Block

These specifications are common to the ANT1 reception and ANT2 reception.

Unless otherwise specified: $V_{DD} = 3V$, $RF1 = 1.90GHz/-35dBm$, $LO = 1.66GHz/-15dBm$

When ANT1 reception: $V_{CTL1} = 0V$, $V_{CTL2} = 3V$

When ANT2 reception: $V_{CTL1} = 3V$, $V_{CTL2} = 0V$

($T_a = 25^{\circ}C$)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}	When no signal		5.5	7.5	mA
Conversion gain	G_c	When a small signal	17	19.5		dB
Noise figure	NF	When a small signal		4.4	5.5	dB
Input IP3	IIP3	*1	-17	-12		dBm
Image suppression ratio	IMR	$RF2 = 1.42GHz/-35dBm$	25	40		dBc
1/2 IF suppression ratio	1/2IFR	$RF2 = 1.78GHz/-35dBm$	41	47		dBc
$2 \times LO-IF$ suppression ratio	—	$RF2 = 3.08GHz/-35dBm$	39	45		dBc
$2 \times LO+IF$ suppression ratio	—	$RF2 = 3.56GHz/-35dBm$	34	65		dBc
LO to ANT leak	P_{LK}			-50	-40	dBm

*1 Conversion from IM3 suppression ratio during $RF1 = 1.9000GHz/-35dBm$ and $RF2 = 1.9006GHz/-35dBm$ input.

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Example of Representative Characteristics

1. Power Amplifier + Antenna Switch Transmitter Block (f = 1.9GHz, Ta = 25°C)

P_{OUT}, ACPR600kHz vs. P_{IN}

V_{DD} = 3V, V_{GG} = const.,

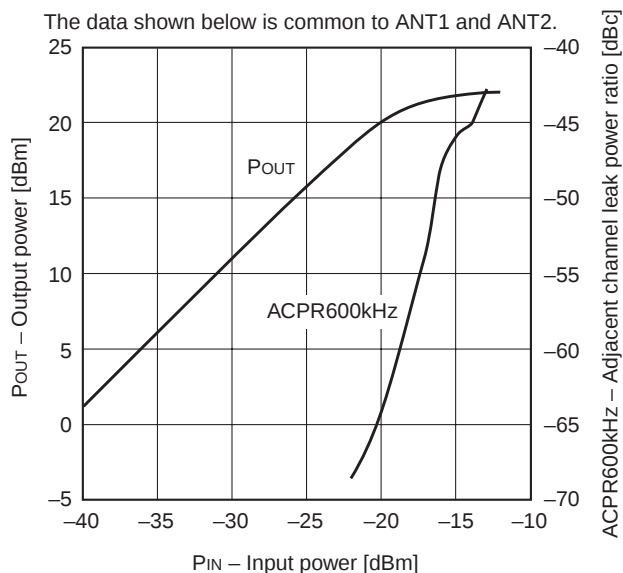
I_{DD} = 150mA (@P_{OUT} = 20.2dBm),

P_{IN} = var.

When ANT1 transmission: V_{CTL1} = 3V, V_{CTL2} = 0V

When ANT2 transmission: V_{CTL1} = 0V, V_{CTL2} = 3V

The data shown below is common to ANT1 and ANT2.



P_{OUT}, ACPR600kHz vs. V_{DD}

V_{DD} = var., V_{GG} = const.,

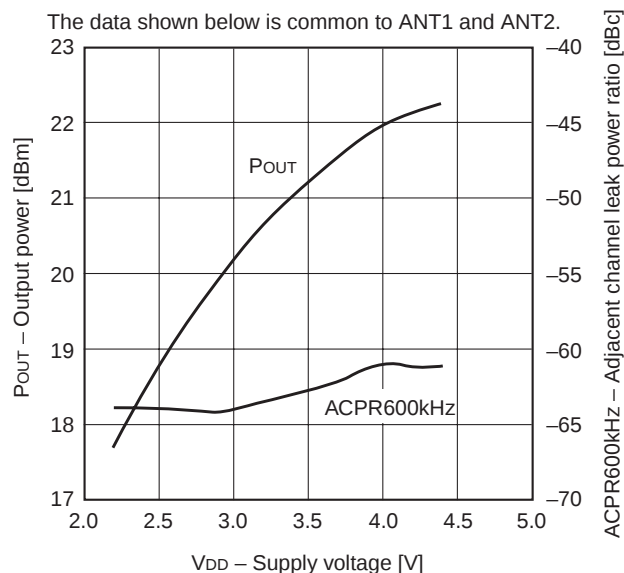
I_{DD} = 150mA (@V_{DD} = 3V, P_{OUT} = 20.2dBm),

P_{IN} = -19.7dBm

When ANT1 transmission: V_{CTL1} = 3V, V_{CTL2} = 0V

When ANT2 transmission: V_{CTL1} = 0V, V_{CTL2} = 3V

The data shown below is common to ANT1 and ANT2.



G_p, ACPR600kHz vs. I_{DD}

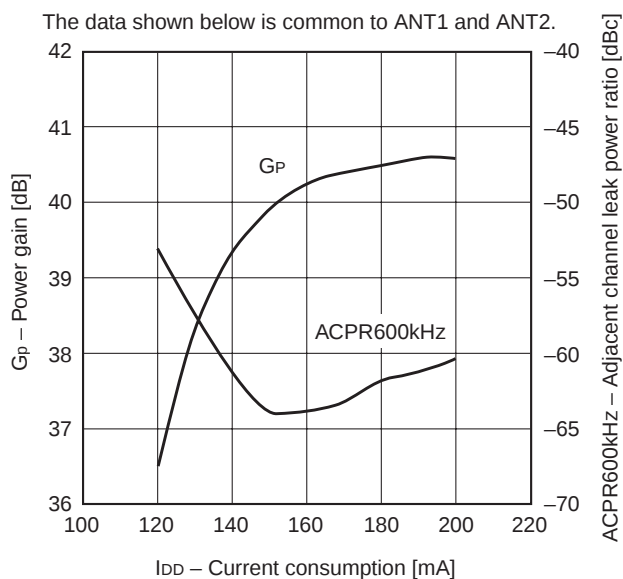
V_{DD} = 3V, V_{GG} = var., I_{DD} = var., P_{IN} = var.,

P_{OUT} = 20.2dBm

When ANT1 transmission: V_{CTL1} = 3V, V_{CTL2} = 0V

When ANT2 transmission: V_{CTL1} = 0V, V_{CTL2} = 3V

The data shown below is common to ANT1 and ANT2.

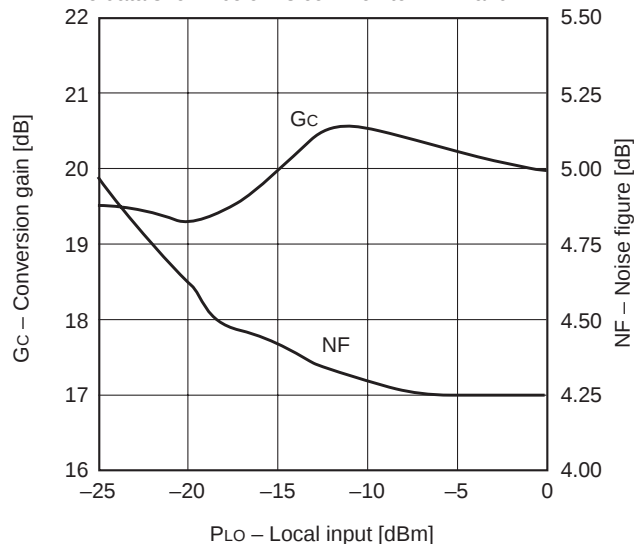


2. Antenna Switch Receiver Block + Low Noise Down Conversion Mixer ($T_a = 25^\circ\text{C}$)

Gc, NF vs. PLO

$V_{DD} = 3\text{V}$, $\text{RF1} = 1.90\text{GHz}$ /small signal,
 $\text{LO} = 1.66\text{GHz}$
 When ANT1 reception: $V_{CTL1} = 0\text{V}$, $V_{CTL2} = 3\text{V}$
 When ANT2 reception: $V_{CTL1} = 3\text{V}$, $V_{CTL2} = 0\text{V}$

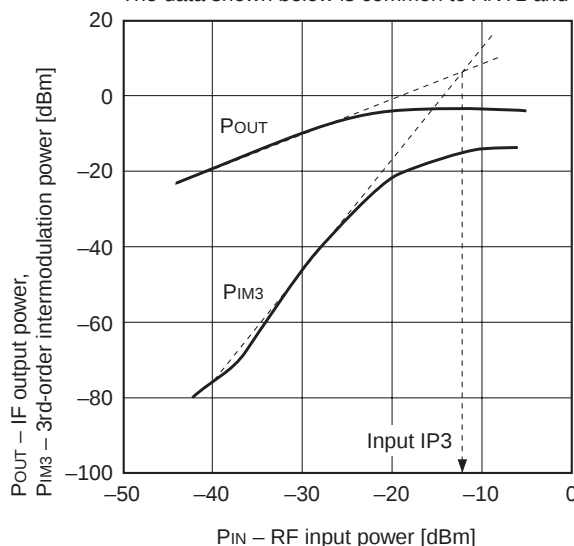
The data shown below is common to ANT1 and ANT2.



Pout, PIM3 vs. Pin

$V_{DD} = 3\text{V}$, $\text{RF1} = 1.9000\text{GHz}$, $\text{RF2} = 1.9006\text{GHz}$,
 $\text{LO} = 1.66\text{GHz}$ /-15dBm
 When ANT1 reception: $V_{CTL1} = 0\text{V}$, $V_{CTL2} = 3\text{V}$
 When ANT2 reception: $V_{CTL1} = 3\text{V}$, $V_{CTL2} = 0\text{V}$

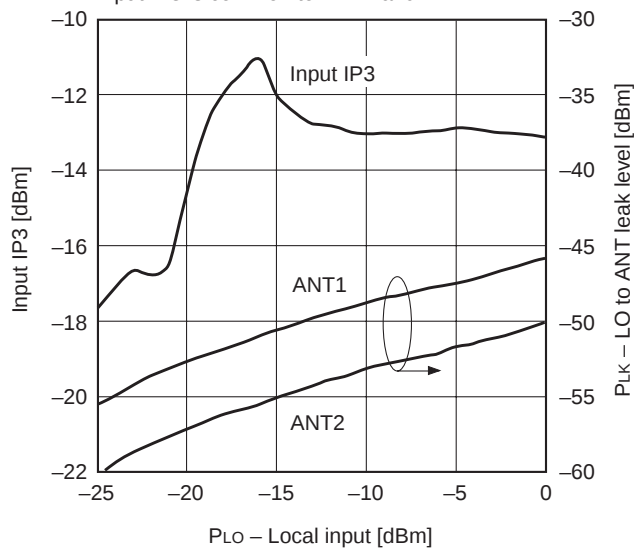
The data shown below is common to ANT1 and ANT2.



Input IP3, PLK vs. PLO

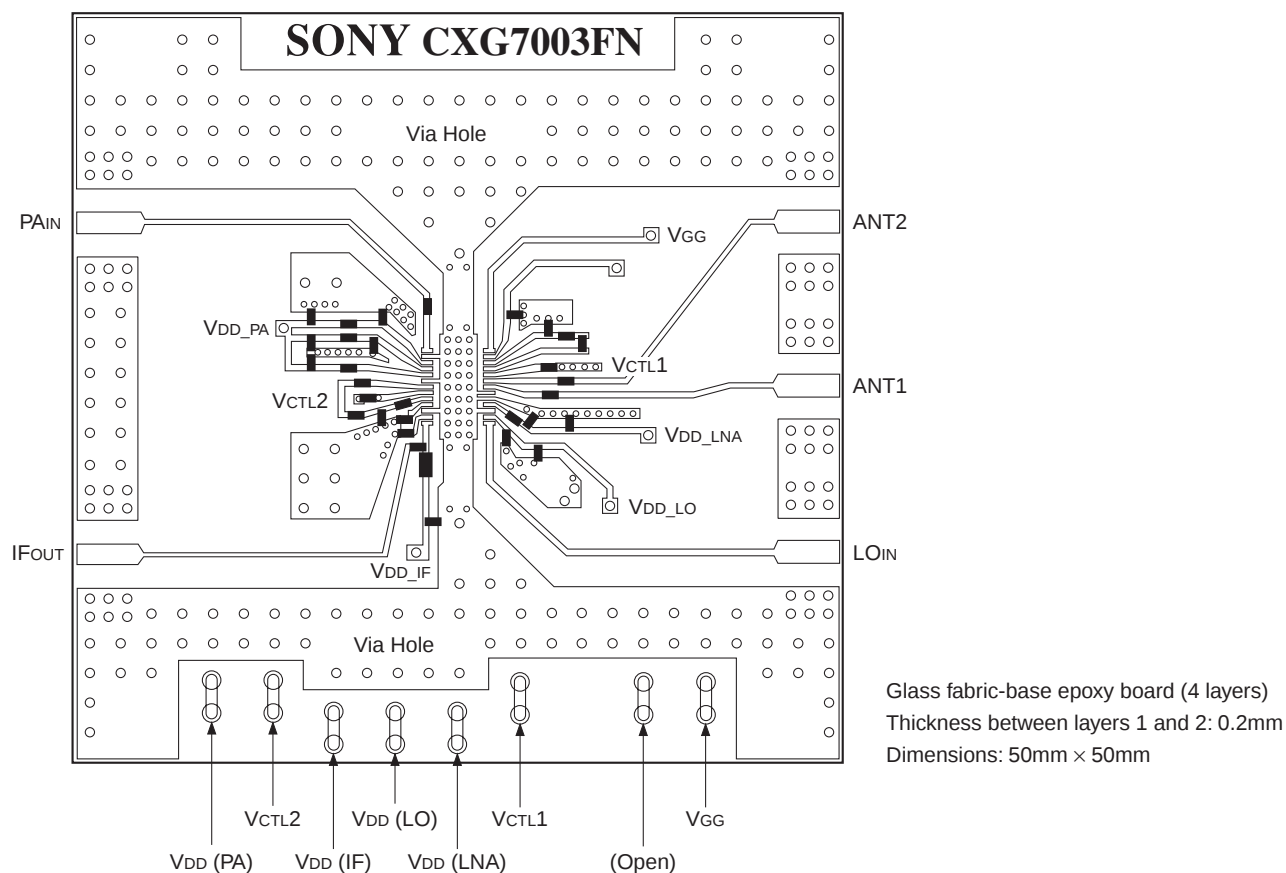
$V_{DD} = 3\text{V}$, $\text{RF} = 1.90\text{GHz}$ /-35dBm,
 $\text{LO} = 1.66\text{GHz}$
 When ANT1 reception: $V_{CTL1} = 0\text{V}$, $V_{CTL2} = 3\text{V}$
 When ANT2 reception: $V_{CTL1} = 3\text{V}$, $V_{CTL2} = 0\text{V}$

Input IP3 is common to ANT1 and ANT2.

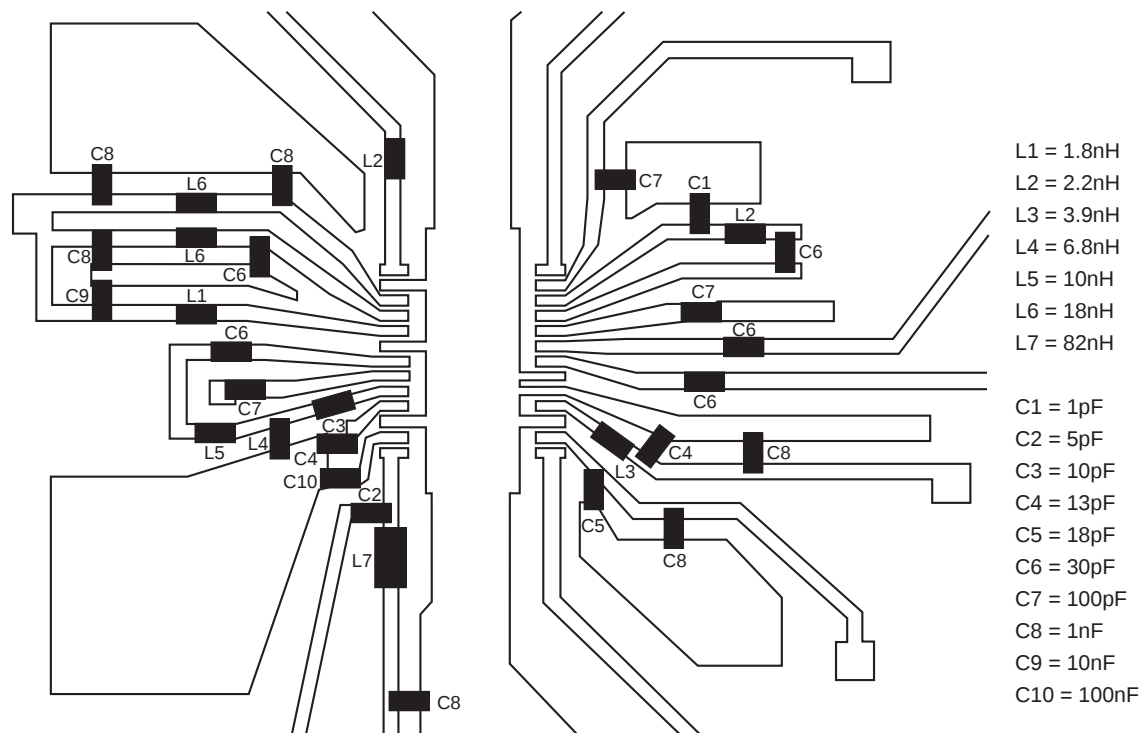


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Recommended Evaluation Board



Enlarged Diagram of External Circuit Block



Package Outline Unit: mm

Technical drawing of a rectangular component, showing three views: Top View, Side View, and End View. The drawing includes dimensions and tolerances.

Top View:

- Overall width: 5.6 ± 0.05
- Overall height: 4.4 ± 0.1
- Inner width (excluding side flanges): 26
- Inner height (excluding top and bottom flanges): 3.8 ± 0.05
- Top flange width: 14
- Bottom flange width: 13
- Central circular hole diameter: $0.07 (M) S A$
- Side flange thickness: 0.4

Side View:

- Overall width: 0.9 ± 0.1
- Overall height: 0.4
- Feature: Solder Plating (S)

End View:

- Overall width: 5.5
- Overall height: 0.4
- Inner width (excluding side flanges): 4.2
- Inner height (excluding top and bottom flanges): 0.2
- Top flange width: 0.2
- Bottom flange width: 0.2
- Central rectangular hole width: 4.4
- Central rectangular hole height: 0.2
- Side flange thickness: 0.4
- Feature: Solder Plating (S)

DETAIL B:

- Overall width: 0.2 ± 0.05
- Overall height: $0.14 - 0.03$
- Inner width (excluding side flanges): 0.2
- Inner height (excluding top and bottom flanges): $+0.05$
- Top flange width: 0.2
- Bottom flange width: 0.2
- Central rectangular hole width: 0.2
- Central rectangular hole height: $+0.05$
- Side flange thickness: 0.4
- Feature: Solder Plating (S)

PACKAGE STRUCTURE

SONY CODE	HSOF-26P-01
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.06g

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm