NLX2G07

Dual Non-Inverting Buffer, Open Drain

The NLX2G07 MiniGate™ is an advanced high−speed CMOS dual non−inverting buffer with open drain output in ultra−small footprint.

The NLX2G07 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: t_{PD} = 2.3 ns (Typ) @ V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra−Small Packages
- These are Pb−Free Devices

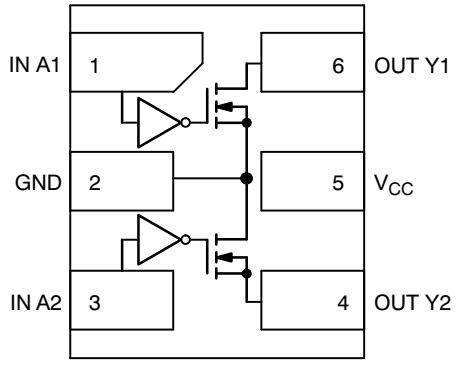


Figure 1. Pinout (Top View)

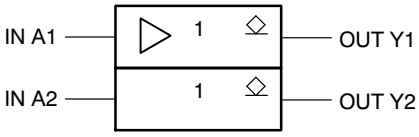


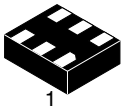
Figure 2. Logic Symbol

ON Semiconductor®

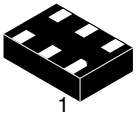
http://onsemi.com

MARKING DIAGRAMS

ULLGA6
1.0 x 1.0
CASE 613AD



ULLGA6
1.2 x 1.0
CASE 613AE



ULLGA6
1.45 x 1.0
CASE 613AF

R = Device Marking
M = Date Code

PIN ASSIGNMENT

1	IN A1
2	GND
3	IN A2
4	OUT Y2
5	V_{CC}
6	OUT Y1

FUNCTION TABLE

A	Y
L	L
H	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to +7.0	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current Per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		150	°C
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating Oxygen	Index: 28 to 34	UL 94 V−0 @ 0.125 in	
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125 °C (Note 5)		±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/UESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IN}	Digital Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	5.5	V
T_A	Operating Free−Air Temperature		−55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25 °C			T_A = +85°C		T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Low−Level Input Voltage		1.65−1.95	0.75 x V_{CC}			0.75 x V_{CC}		0.75 x V_{CC}		V
			2.3 to 5.5	0.70 x V_{CC}			0.70 x V_{CC}		0.70 x V_{CC}		
V_{IL}	Low−Level Input Voltage		1.65−1.95			0.25 x V_{CC}		0.25 x V_{CC}		0.25 x V_{CC}	V
			2.3 to 5.5			0.30 x V_{CC}		0.30 x V_{CC}		0.30 x V_{CC}	
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	1.65−5.5			0.1		0.1		0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 12 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA	 1.65 2.3 2.7 3.0 3.0 4.5		 0.08 0.2 0.22 0.28 0.38 0.42	 0.24 0.3 0.4 0.4 0.55 0.55		 0.24 0.3 0.4 0.4 0.55 0.55		 0.24 0.3 0.4 0.4 0.55 0.55	
I_{LKG}	Z−State Output Leakage Current	V_{IN} = V_{IH}, V_{OUT} = V_{CC} or GND	5.5			±5.0		±10		±10	μA
I_{IN}	Input Leakage Current	0 ≤ V_{IN} ≤ 5.5 V	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{OFF}	Power Off Input Leakage Current	0 ≤ V_{IN}, V_{OUT} ≤ 5.5 V	0			1.0		10		10	μA
I_{CC}	Quiescent Supply Current	0 ≤ V_{IN} ≤ V_{CC}	5.5			1.0		10		10	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ nS)

Symbol	Parameter	V_{CC} (V)	Test Condition	T_A = 25 °C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PZL}	Propagation Delay (Figures 3 and 4)	1.65–1.95	$R_L = R_1 = 5000\ \Omega$, $C_L = 15$ pF	1.8	5.3	11.5	1.8	12	ns
		2.3–2.7	$R_L = R_1 = 500\ \Omega$, $C_L = 50$ pF	1.2	3.7	5.8	1.2	6.4	
		3.0–3.6	$R_L = R_1 = 500\ \Omega$, $C_L = 50$ pF	0.8	2.9	4.4	0.8	4.8	
		4.5–5.5	$R_L = R_1 = 500\ \Omega$, $C_L = 50$ pF	0.5	2.3	3.5	0.5	3.9	
t_{PLZ}	Propagation Delay (Figures 3 and 4)	1.65–1.95	$R_L = R_1 = 5000\ \Omega$, $C_L = 15$ pF	1.8	5.3	11.5	1.8	12	ns
		2.3–2.7	$R_L = R_1 = 500\ \Omega$, $C_L = 50$ pF	1.2	2.8	5.8	1.2	6.4	
		3.0–3.6	$R_L = R_1 = 500\ \Omega$, $C_L = 50$ pF	0.8	2.1	4.4	0.8	4.8	
		4.5–5.5	$R_L = R_1 = 500\ \Omega$, $C_L = 50$ pF	0.5	1.4	3.5	0.5	3.9	
C_{IN}	Input Capacitance	5.5	V_{IN} = 0 V or V_{CC}		2.5				pF
C_{OUT}	Output Capacitance	5.5	V_{IN} = 0 V or V_{CC}		4				pF
C_{PD}	Power Dissipation Capacitance (Note 6)	3.3 5.5	10 MHz V_{IN} = 0 V or V_{CC}		4				pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

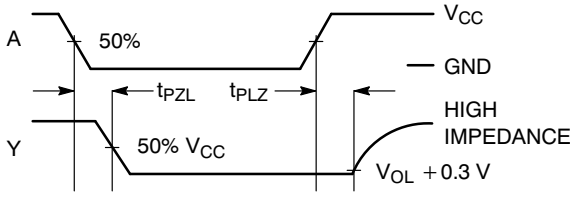
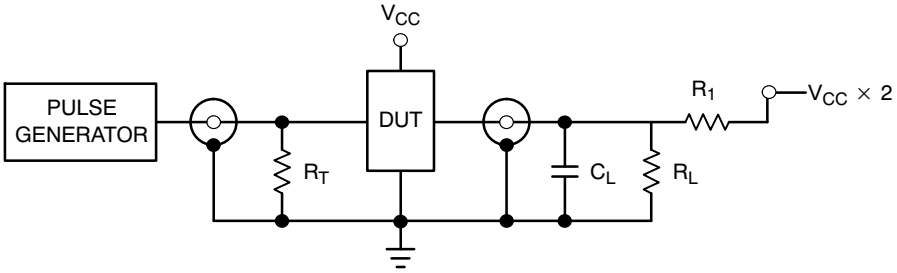


Figure 3. Switching Waveforms



R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

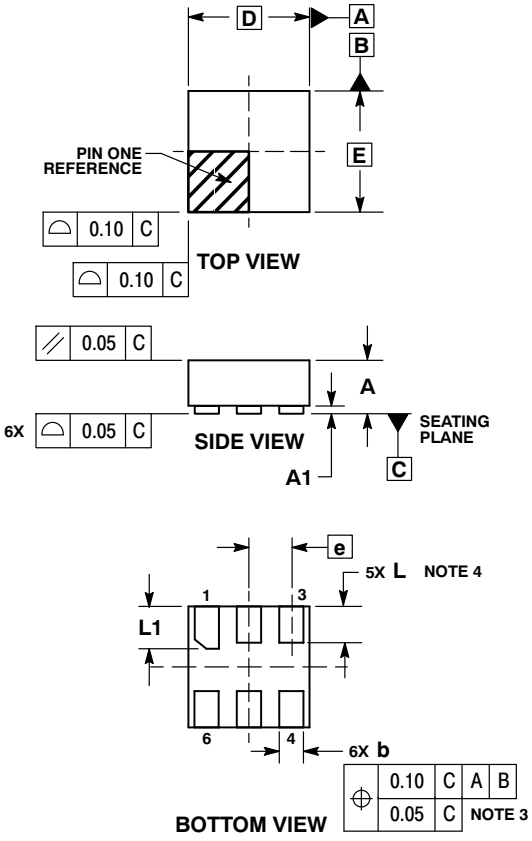
ORDERING INFORMATION

Device	Package	Shipping†
NLX2G07AMX1TCG	ULLGA6, 1.45 x 1.0, 0.5P (Pb−Free)	3000 / Tape & Reel
NLX2G07BMX1TCG	ULLGA6, 1.2 x 1.0, 0.4P (Pb−Free)	3000 / Tape & Reel
NLX2G07CMX1TCG	ULLGA6, 1.0 x 1.0, 0.35P (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

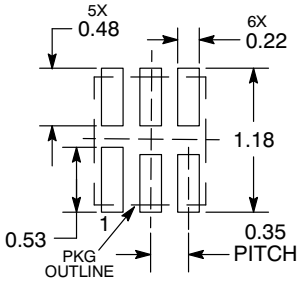
ULLGA6 1.0x1.0, 0.35P
CASE 613AD−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

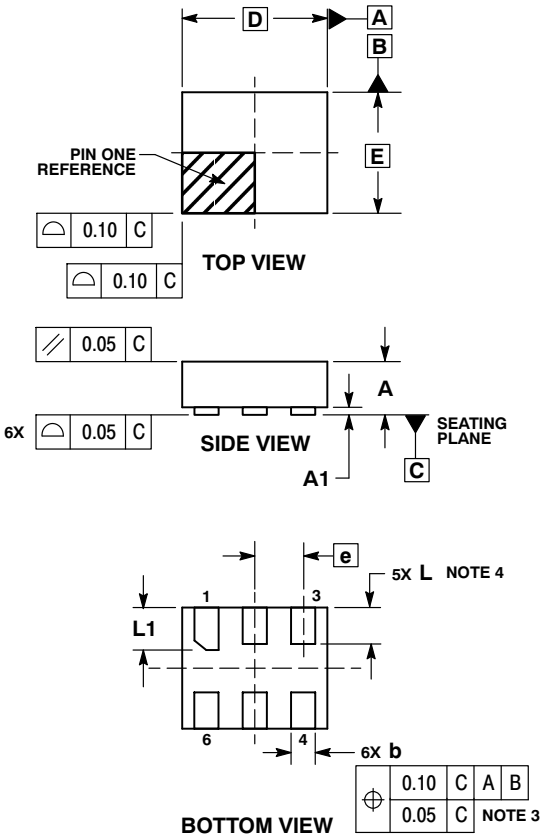


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

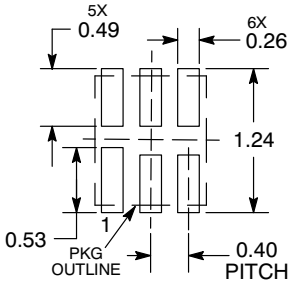
ULLGA6 1.2x1.0, 0.4P
CASE 613AE−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.35	0.45

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

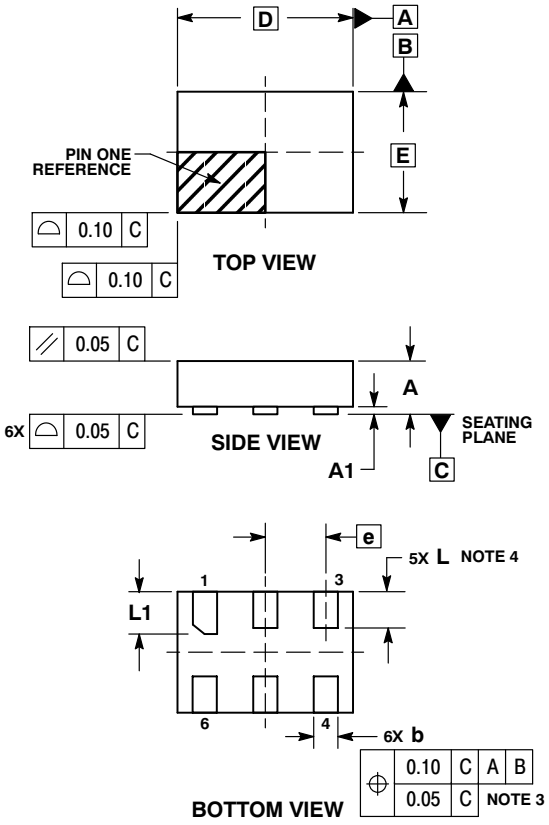


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

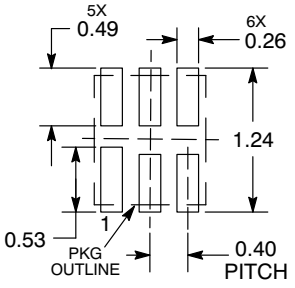
ULLGA6 1.45x1.0, 0.5P
CASE 613AF−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative