RoHS

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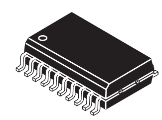
Surface Mount Micromachined Accelerometer

MMA3201KEG

MMA3201KEG: XY-AXIS SENSITIVITY MICROMACHINED ACCELEROMETER ±40g

The MMA3201 series of dual axis (X and Y) silicon capacitive, micromachined accelerometers features signal conditioning, a 4-pole low pass filter and temperature compensation, and separate outputs for the two axes. Zero-g offset full scale span and filter cut-off are factory set and require no external devices. A full system self-test capability verifies system functionality.



**KEG SUFFIX (Pb-FREE)
20-LEAD SOIC
CASE 475A-02**

Features

- Sensitivity in two separate axes: 40g X-axis and 40g Y-axis
- Integral Signal Conditioning
- Linear Output
- Ratiometric Performance
- 4th Order Bessel Filter Preserves Pulse Shape Integrity
- Calibrated Self-test
- Low Voltage Detect, Clock Monitor, and EPROM Parity Check Status
- Transducer Hermetically Sealed at Wafer Level for Superior Reliability
- Robust Design, High Shocks Survivability
- Qualified AEC-Q100, Rev. F Grade 2 (-40°C/ +105°C)

Typical Applications

- Vibration Monitoring and Recording
- Impact Monitoring
- Appliance Control
- Mechanical Bearing Monitoring
- Computer Hard Drive Protection
- Computer Mouse and Joysticks
- Virtual Reality Input Devices
- Sports Diagnostic Devices and Systems

ORDERING INFORMATION

Device Name	Temperature Range	Case No,	Package
MMA3201EG	–40 to +125°C	475A-02	SOIC-20
MMA3201EGR2	–40 to +125°C	475A-02	SOIC-20, Tape & Reel
MMA3201KEG*	–40 to +125°C	475A-02	SOIC-20
MMA3201KEGR2*	–40 to +125°C	475A-02	SOIC-20, Tape & Reel

*Part number sourced from a different facility.

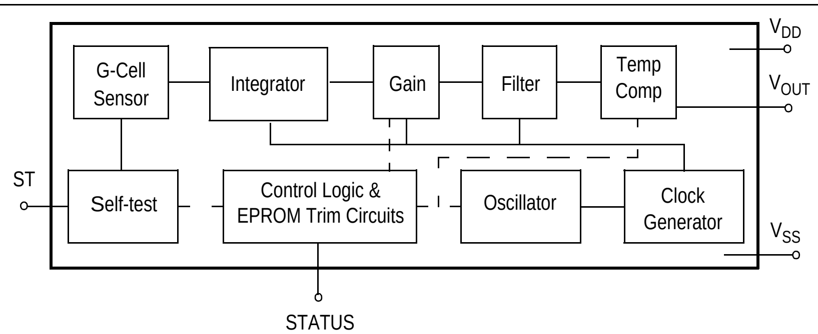


Figure 1. Simplified Accelerometer Functional Block Diagram

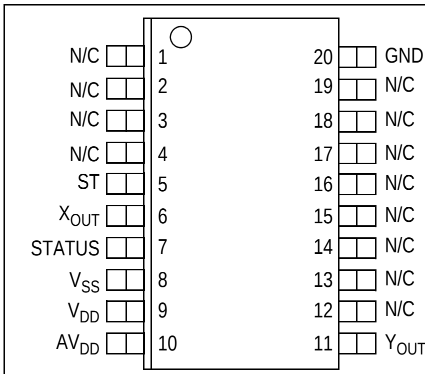


Figure 2. Pin Connections

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Table 1. Maximum Ratings
(Maximum ratings are the limits to which the device can be exposed without causing permanent damage.)

Rating	Symbol	Value	Unit
Powered Acceleration (all axes)	G_{pd}	1500	g
Unpowered Acceleration (all axes)	G_{upd}	2000	g
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Drop Test[1]	D_{drop}	1.2	m
Storage Temperature Range	T_{stg}	–40 to +125	°C

1. Dropped onto concrete surface from any axis.

ELECTRO STATIC DISCHARGE (ESD)

WARNING: This device is sensitive to electrostatic discharge.

Although the Freescale accelerometers contain internal 2 kV ESD protection circuitry, extra precaution must be taken by the user to protect the chip from ESD. A charge of over 2000 volts can accumulate on the human body or associated test equipment. A charge of this magnitude can alter the performance or cause failure of the chip. When handling the accelerometer, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its performance.

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Table 2. Operating Characteristics

(Unless otherwise noted: –40°C ≤ T_A ≤ +105°C, 4.75 ≤ V_{DD} ≤ 5.25, X and Y Channels, Acceleration = 0g, Loaded output.[1])

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Range[2]					
Supply Voltage[3]	V_{DD}	4.75	5.00	5.25	V
Supply Current	I_{DD}	6	8	10	mA
Operating Temperature Range	T_A	–40	—	+125	°C
Acceleration Range	g_{FS}	—	45	—	g
Output Signal					
Zero g (T_A = 25°C, V_{DD} = 5.0 V)[4]	V_{OFF}	2.35	2.5	2.65	V
Zero g	$V_{OFF,V}$	0.46 V_{DD}	0.50 V_{DD}	0.54 V_{DD}	V
Sensitivity (T_A = 25°C, V_{DD} = 5.0 V)[5]	S	45	50	55	mV/g
Sensitivity	S_V	9.3	10	10.7	mV/g/V
Bandwidth Response	$f_{–3dB}$	360	400	440	Hz
Nonlinearity	NL_{OUT}	–1.0	—	+1.0	% FSO
Noise					
RMS (.01 Hz – 1 kHz)	n_{RMS}	—	—	2.8	mVrms
Power Spectral Density	n_{PSD}	—	110	—	μV/($Hz^{1/2}$)
Clock Noise (without RC load on output)[6]	n_{CLK}	—	2.0	—	mVpk
Self-Test					
Output Response	g_{ST}	9.6	12	14.4	g
Input Low	V_{IL}	V_{SS}	—	0.3 × V_{DD}	V
Input High	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input Loading[7]	I_{IN}	–30	–110	–300	μA
Response Time[8]	t_{ST}	—	2.0	–	ms
Status[9], [10]					
Output Low (I_{load} = 100 μA)	V_{OL}	—	—	0.4	V
Output High (I_{load} = 100 μA)	V_{OH}	V_{DD} – 0.8	—	—	V
Minimum Supply Voltage (LVD Trip)	V_{LVD}	2.7	3.25	4.0	V
Clock Monitor Fail Detection Frequency	f_{min}	50	—	260	kHz
Output Stage Performance					
Electrical Saturation Recovery Time[11]	t_{DELAY}	—	0.2	—	ms
Full Scale Output Range (I_{OUT} = 200 μA)	V_{FSO}	0.25	—	V_{DD}–0.25	V
Capacitive Load Drive[12]	C_L	—	—	100	pF
Output Impedance	Z_O	—	300	—	Ω
Mechanical Characteristics					
Transverse Sensitivity[13]	$V_{XZ,YZ}$	—	—	5.0	% FSO
Package Resonance	f_{PKG}	—	10	—	kHz

1. For a loaded output the measurements are observed after an RC filter consisting of a 1 kΩ resistor and a 0.01 μF capacitor to ground.
2. These limits define the range of operation for which the part will meet specification.
3. Within the supply range of 4.75 and 5.25 volts, the device operates as a fully calibrated linear accelerometer. Beyond these supply limits the device may operate as a linear device but is not guaranteed to be in calibration.
4. The device can measure both + and – acceleration. With no input acceleration the output is at midsupply. For positive acceleration the output will increase above V_{DD}/2 and for negative acceleration the output will decrease below V_{DD}/2.
5. The device is calibrated at 20g.
6. At clock frequency ≅70 kHz.
7. The digital input pin has an internal pull-down current source to prevent inadvertent self test initiation due to external board level leakages.
8. Time for the output to reach 90% of its final value after a self-test is initiated.
9. The Status pin output is not valid following power-up until at least one rising edge has been applied to the self-test pin. The Status pin is high whenever the self-test input is high, as a means to check the connectivity of the self-test and Status pins in the application.
10. The Status pin output latches high if a Low Voltage Detection or Clock Frequency failure occurs, or the EPROM parity changes to odd. The Status pin can be reset low if the self-test pin is pulsed with a high input for at least 100 μs, unless a fault condition continues to exist.
11. Time for amplifiers to recover after an acceleration signal causing them to saturate.
12. Preserves phase margin (60°) to guarantee output amplifier stability.
13. A measure of the device's ability to reject an acceleration applied 90° from the true axis of sensitivity.

PRINCIPLE OF OPERATION

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The Freescale accelerometer is a surface-micromachined integrated-circuit accelerometer.

The device consists of a surface micromachined capacitive sensing cell (g-cell) and a CMOS signal conditioning ASIC contained in a single integrated circuit package. The sensing element is sealed hermetically at the wafer level using a bulk micromachined “cap" wafer.

The g-cell is a mechanical structure formed from semiconductor materials (polysilicon) using semiconductor processes (masking and etching). It can be modeled as a set of beams attached to a movable central mass that move between fixed beams. The movable beams can be deflected from their rest position by subjecting the system to an acceleration (Figure 3).

As the beams attached to the central mass move, the distance from them to the fixed beams on one side will increase by the same amount that the distance to the fixed beams on the other side decreases. The change in distance is a measure of acceleration.

The g-cell beams form two back-to-back capacitors (Figure 4). As the central mass moves with acceleration, the distance between the beams change and each capacitor's value will change, ($C = NA\varepsilon/D$). Where A is the area of the facing side of the beam, ε is the dielectric constant, D is the distance between the beams, and N is the number of beams. The X-Y device contains two structures at right angles to each other.

The CMOS ASIC uses switched capacitor techniques to measure the g-cell capacitors and extract the acceleration data from the difference between the two capacitors. The ASIC also signal conditions and filters (switched capacitor) the signal, providing a high level output voltage that is ratiometric and proportional to acceleration.

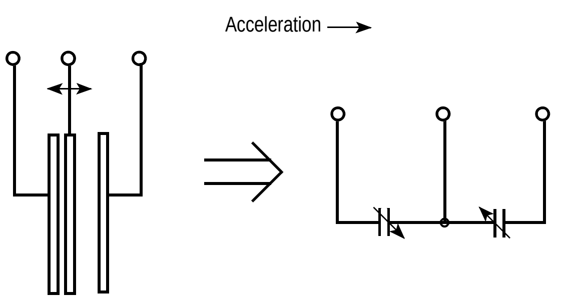

Figure 3. Transducer Physical Model

Figure 4. Equivalent Circuit Model

SPECIAL FEATURES

Filtering

The Freescale accelerometers contain an on board 4-pole switched capacitor filter. A Bessel implementation is used because it provides a maximally flat delay response (linear phase) thus preserving pulse shape integrity. Because the filter is realized using switched capacitor techniques, there is no requirement for external passive components (resistors and capacitors) to set the cut-off frequency.

Self-Test

The sensor provides a self-test feature that allows the verification of the mechanical and electrical integrity of the accelerometer at any time before or after installation. This feature is critical in applications such as automotive airbag systems where system integrity must be ensured over the life of the vehicle. A fourth “plate" is used in the g-cell as a self-test plate. When the user applies a logic high input to the self-test pin, a calibrated potential is applied across the self-test plate and the moveable plate. The resulting electrostatic force ($Fe = {}^{1}/_{2} AV^2/d^2$) causes the center plate to deflect. The resultant deflection is measured by the accelerometer's control ASIC and a proportional output voltage results. This procedure assures that both the mechanical (g-cell) and electronic sections of the accelerometer are functioning.

Ratiometricity

Ratiometricity simply means that the output offset voltage and sensitivity will scale linearly with applied supply voltage. That is, as you increase supply voltage the sensitivity and offset increase linearly; as supply voltage decreases, offset and sensitivity decrease linearly. This is a key feature when interfacing to a microcontroller or an A/D converter because it provides system level cancellation of supply induced errors in the analog to digital conversion process.

Status

Freescale accelerometers include fault detection circuitry and a fault latch. The Status pin is an output from the fault latch, OR'd with self-test, and is set high whenever one (or more) of the following events occur:

- Supply voltage falls below the Low Voltage Detect (LVD) voltage threshold
- Clock oscillator falls below the clock monitor minimum frequency
- Parity of the EPROM bits becomes odd in number.

The fault latch can be reset by a rising edge on the self-test input pin, unless one (or more) of the fault conditions continues to exist.

BASIC CONNECTIONS

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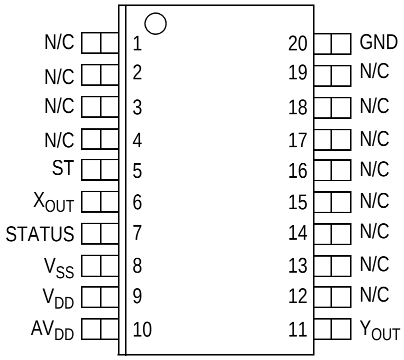
Pinout Description



Pin No.	Pin Name	Description
1 thru 3	—	Leave unconnected.
4	—	No internal connection. Leave unconnected.
5	ST	Logic input pin used to initiate self-test.
6	X_{OUT}	Output voltage of the accelerometer. X Direction.
7	STATUS	Logic output pin to indicate fault.
8	V_{SS}	The power supply ground.
9	V_{DD}	The power supply input.
10	AV_{DD}	Power supply input (Analog).
11	Y_{OUT}	Output voltage of the accelerometer. Y Direction.
12 thru 16	—	Used for factory trim. Leave unconnected.
17 thru 19	—	No internal connection. Leave unconnected.
20	GND	Ground.

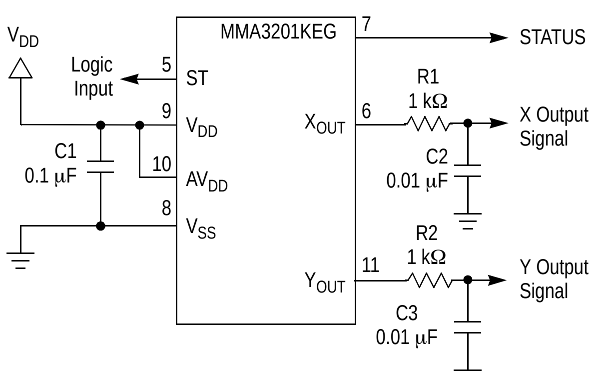


Figure 5. SOIC Accelerometer with Recommended Connection Diagram

PCB Layout

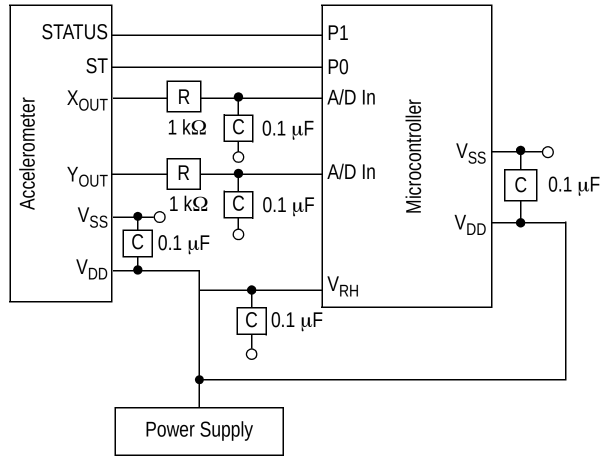


Figure 6. Recommended PCB Layout for Interfacing Accelerometer to Microcontroller

NOTES:

1. Use a 0.1 μF capacitor on V_{DD} to decouple the power source.
2. Physical coupling distance of the accelerometer to the microcontroller should be minimal.
3. Place a ground plane beneath the accelerometer to reduce noise, the ground plane should be attached to all of the open ended terminals shown in Figure 6.
4. Use an RC filter of 1 kΩ and 0.01 μF on the output of the accelerometer to minimize clock noise (from the switched capacitor filter circuit).
5. PCB layout of power and ground should not couple power supply noise.
6. Accelerometer and microcontroller should not be a high current path.
7. A/D sampling rate and any external power supply switching frequency should be selected such that they do not interfere with the internal accelerometer sampling frequency. This will prevent aliasing errors.

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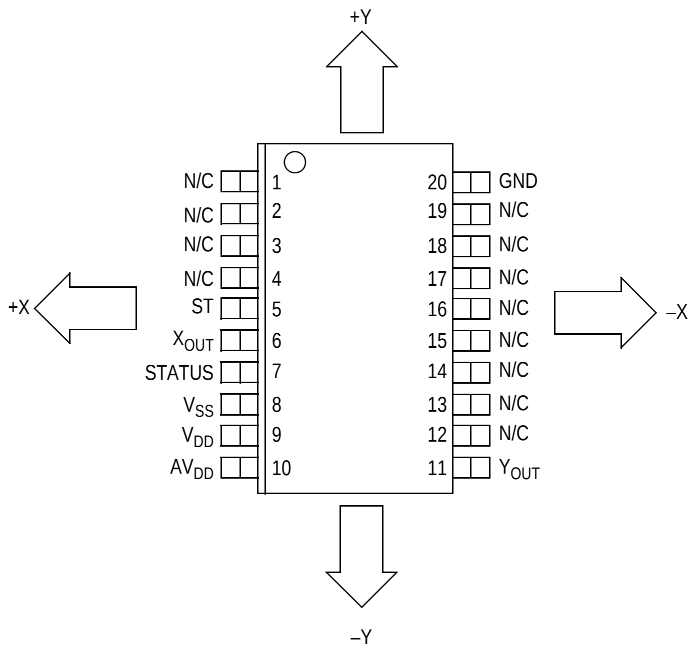
Dynamic Acceleration Sensing Direction

Acceleration of the package in the +X and +Y direction (center plates move in the -X and -Y direction) will result in an increase in the X and Y outputs.

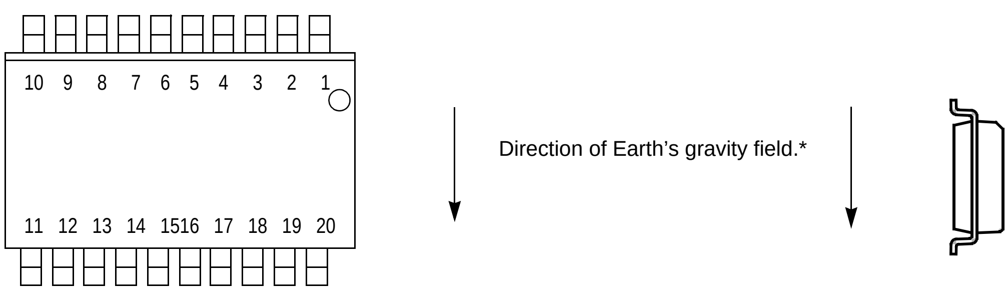


Activation of Self test moves the center plates in the -X and -Y direction, resulting in an increase in the X and Y outputs.

20-Pin SOIC Package
N/C pins are recommended to be left FLOATING

Top View

Static Acceleration Sensing Direction



Front View **Side View**

* When positioned as shown, the Earth's gravity will result in a positive 1g output in the X channel.

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

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Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct footprint, the packages will self-align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

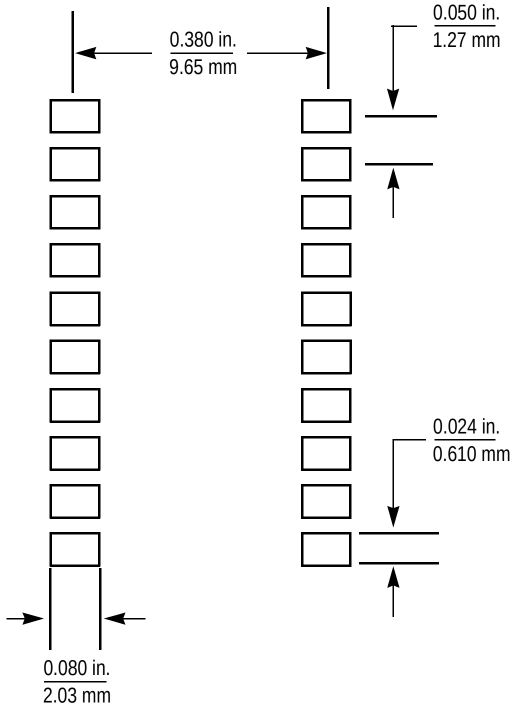

Figure 7. Footprint SOIC-20 (Case 475A-01)

PACKAGE DIMENSIONS

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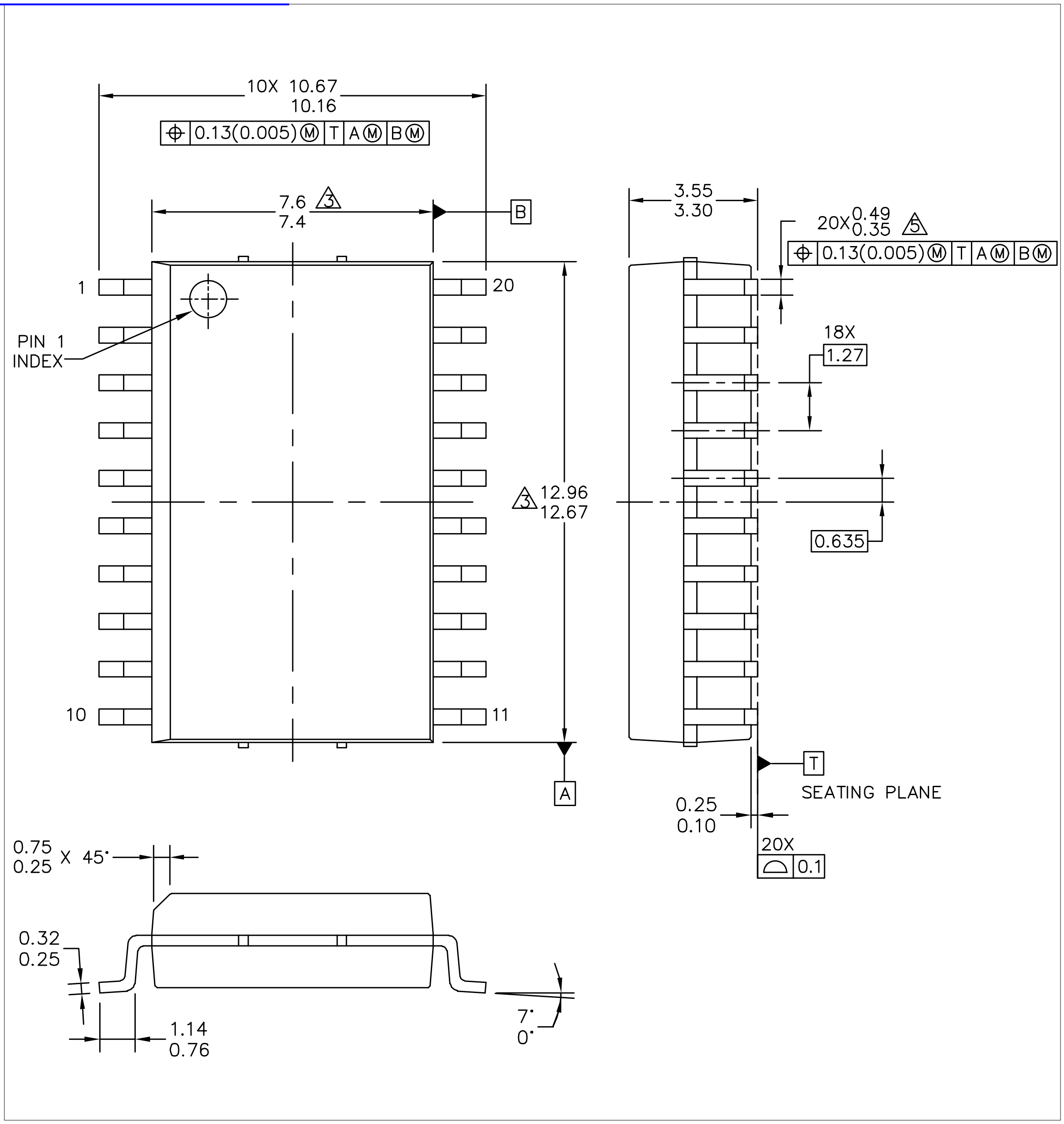

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	CASE NUMBER: 475A-02	06 JUL 2006
	STANDARD: NON-JEDEC	

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CASE 475A-02
ISSUE C
20-LEAD SOIC

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PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. (△) THIS DIMENSION DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15(0.006) PER SIDE.
5. (△) THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13(0.005) TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

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CASE 475A-02
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