

ADSP-BF531/ADSP-BF532/ADSP-BF533

FEATURES

- Up to 600 MHz high performance Blackfin processor
- Two 16-bit MACs, two 40-bit ALUs, four 8-bit video ALUs, 40-bit shifter
- RISC-like register and instruction model for ease of programming and compiler-friendly support
- Advanced debug, trace, and performance monitoring
- 0.85 V to 1.30 V core V_{DD} with on-chip voltage regulation
- 1.8 V, 2.5 V, and 3.3 V compliant I/O
- 160-ball CSP_BGA, 169-ball PBGA, and 176-lead LQFP packages

MEMORY

- Up to 148K bytes of on-chip memory:
 - 16K bytes of instruction SRAM/Cache
 - Up to 64K bytes of instruction SRAM
 - Up to 32K bytes of data SRAM/Cache
 - Up to 32K bytes of data SRAM
 - 4K bytes of scratchpad SRAM
- Memory management unit providing memory protection

- External memory controller with glueless support for SDRAM, SRAM, flash, and ROM
- Flexible memory booting options from SPI® and external memory

PERIPHERALS

- Parallel peripheral interface PPI/GPIO, supporting ITU-R 656 video data formats
- Two dual-channel, full duplex synchronous serial ports, supporting eight stereo I²S channels
- Four memory-to-memory DMAs
- Eight peripheral DMAs
- SPI-compatible port
- Three 32-bit timer/counters with PWM support
- Real-time clock and watchdog timer
- 32-bit core timer
- Up to 16 general-purpose I/O pins (GPIO)
- UART with support for IrDA®
- Event handler
- Debug/JTAG interface
- On-chip PLL capable of 0.5× to 64× frequency multiplication

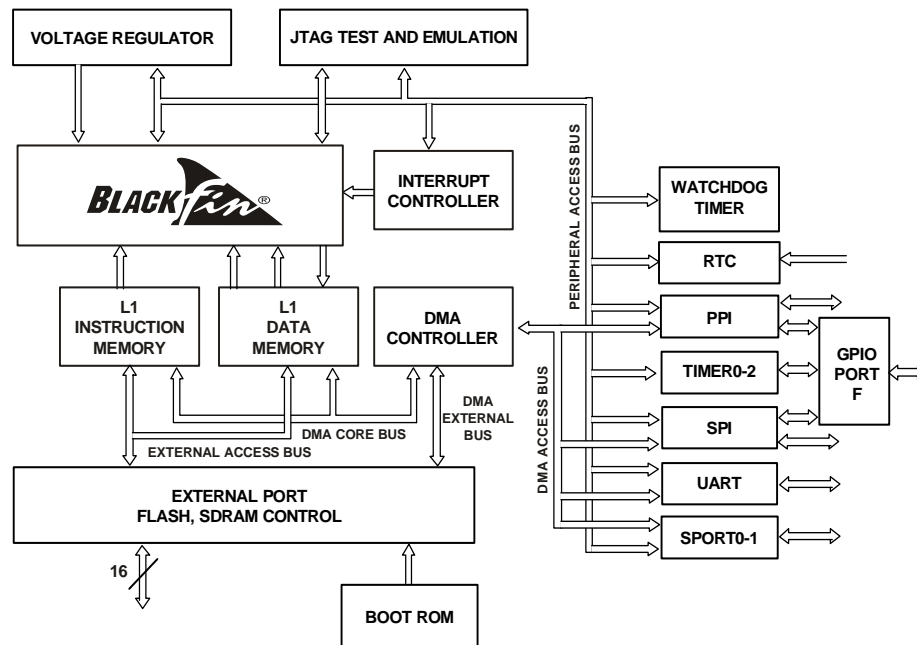


Figure 1. Functional Block Diagram

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Rev. E

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REVISION HISTORY

7/07—Revision E: Changed from Rev. D to Rev. E

| | |
|---|----|
| Combined ADSP-BF531/532 Rev D and ADSP-BF533 Rev D | |
| Data sheets into this Revision E | 1 |
| Changed Features | 1 |
| Reformatted Processor Comparison | 3 |
| Rewrote General-Purpose I/O Port F | 10 |
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| Reformatted Pin Descriptions | 18 |
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| Added Figures to Parallel Peripheral Interface Timing | 30 |
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8/06—Revision D: Changed from Rev. C to Rev. D

GENERAL DESCRIPTION

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are members of the Blackfin family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single instruction, multiple data (SIMD) multimedia capabilities into a single instruction set architecture.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are completely code and pin-compatible, differing only with respect to their performance and on-chip memory. Specific performance and memory configurations are shown in [Table 1](#).

Table 1. Processor Comparison

| Features | ADSP-BF531 | ADSP-BF532 | ADSP-BF533 | |
|-------------------------------|---------------------------|------------|------------|-----------|
| SPORTs | 2 | 2 | 2 | |
| UART | 1 | 1 | 1 | |
| SPI | 1 | 1 | 1 | |
| GP Timers | 3 | 3 | 3 | |
| Watchdog Timers | 1 | 1 | 1 | |
| RTC | 1 | 1 | 1 | |
| Parallel Peripheral Interface | 1 | 1 | 1 | |
| GPIOs | 16 | 16 | 16 | |
| Memory Configuration | L1 Instruction SRAM/Cache | 16K bytes | 16K bytes | 16K bytes |
| | L1 Instruction SRAM | 16K bytes | 32K bytes | 64K bytes |
| | L1 Data SRAM/Cache | 16K bytes | 32K bytes | 32K bytes |
| | L1 Data SRAM | | | 32K bytes |
| | L1 Scratchpad | 4K bytes | 4K bytes | 4K bytes |
| | L3 Boot ROM | 1K bytes | 1K bytes | 1K bytes |
| Maximum Speed Grade | 400 MHz | 400 MHz | 600 MHz | |
| Package Options: | | | | |
| CSP_BGA | 160-Ball | 160-Ball | 160-Ball | |
| Plastic BGA | 169-Ball | 169-Ball | 169-Ball | |
| LQFP | 176-Lead | 176-Lead | 176-Lead | |

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature dynamic power management—the ability to vary both the voltage and frequency of operation to significantly lower overall

power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are highly integrated system-on-a-chip solutions for the next generation of digital communication and consumer multimedia applications. By combining industry-standard interfaces with a high performance signal processing core, users can develop cost-effective solutions quickly without the need for costly external components. The system peripherals include a UART port, an SPI port, two serial ports (SPORTs), four general-purpose timers (three with PWM capability), a real-time clock, a watchdog timer, and a parallel peripheral interface.

ADSP-BF531/ADSP-BF532/ADSP-BF533 PROCESSOR PERIPHERALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the functional block diagram in [Figure 1 on Page 1](#)). The general-purpose peripherals include functions such as UART, timers with PWM (pulse-width modulation) and pulse measurement capability, general-purpose I/O pins, a real-time clock, and a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. In addition to these general-purpose peripherals, the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors contain high speed serial and parallel ports for interfacing to a variety of audio, video, and modem codec functions; an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources; and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, real-time clock, and timers, are supported by a flexible DMA structure. There is also a separate memory DMA channel dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors include an on-chip voltage regulator in support of the processor's dynamic power management capability. The voltage regulator provides a range of core voltage levels from a single 2.25 V to 3.6 V input. The voltage regulator can be bypassed at the user's discretion.

BLACKFIN PROCESSOR CORE

As shown in [Figure 2 on Page 5](#), the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-bit, 16-bit, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions includes byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). Quad 16-bit operations are possible using the second ALU.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency on-chip memory as cache or SRAM, and larger, lower cost and performance off-chip memory systems. See [Figure 4 on Page 6](#), [Figure 5 on Page 6](#), and [Figure 3 on Page 6](#).

The L1 memory system is the primary highest performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor has three blocks of on-chip memory providing high bandwidth access to the core.

The first is the L1 instruction memory, consisting of up to 80K bytes SRAM, of which 16K bytes can be configured as a four way set-associative cache. This memory is accessed at full processor speed.

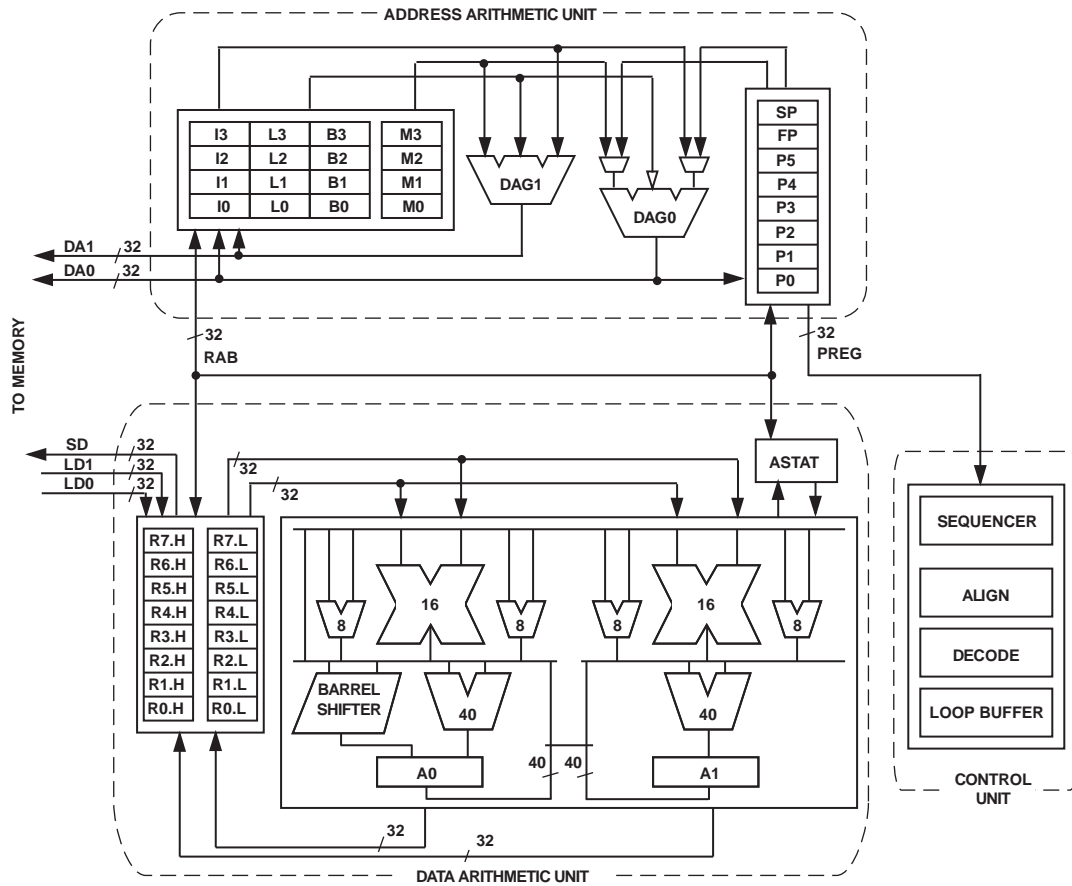


Figure 2. Blackfin Processor Core

The second on-chip memory block is the L1 data memory, consisting of one or two banks of up to 32K bytes. The memory banks are configurable, offering both cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM and cannot be configured as cache memory.

External (Off-Chip) Memory

External memory is accessed via the external bus interface unit (EBIU). This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The PC133-compliant SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. The SDRAM controller allows one row to be open for each internal SDRAM bank, for up to four internal SDRAM banks, improving overall system performance.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a

1M byte segment regardless of the size of the devices used, so that these banks will only be contiguous if each is fully populated with 1M byte of memory.

I/O Memory Space

Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one containing the control MMRs for all core functions, and the other containing the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor contains a small boot kernel, which configures the appropriate peripheral for booting. If the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor is configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see [Booting Modes on Page 14](#).

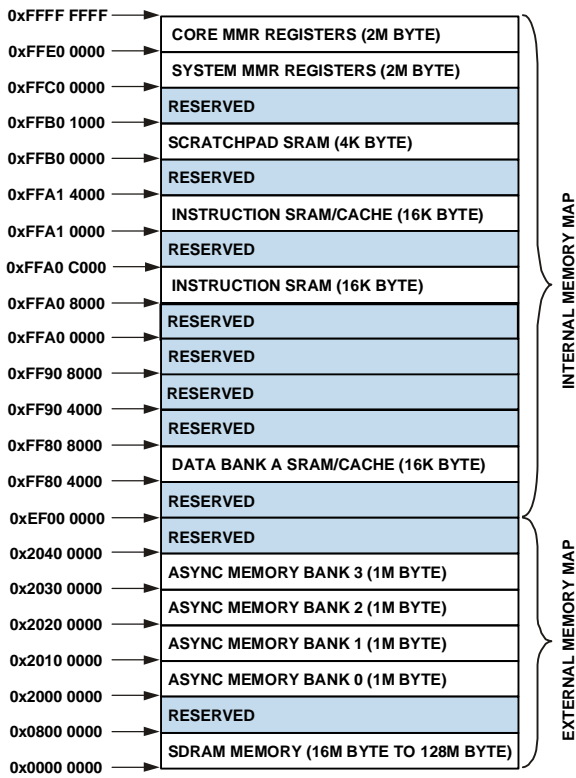


Figure 3. ADSP-BF531 Internal/External Memory Map

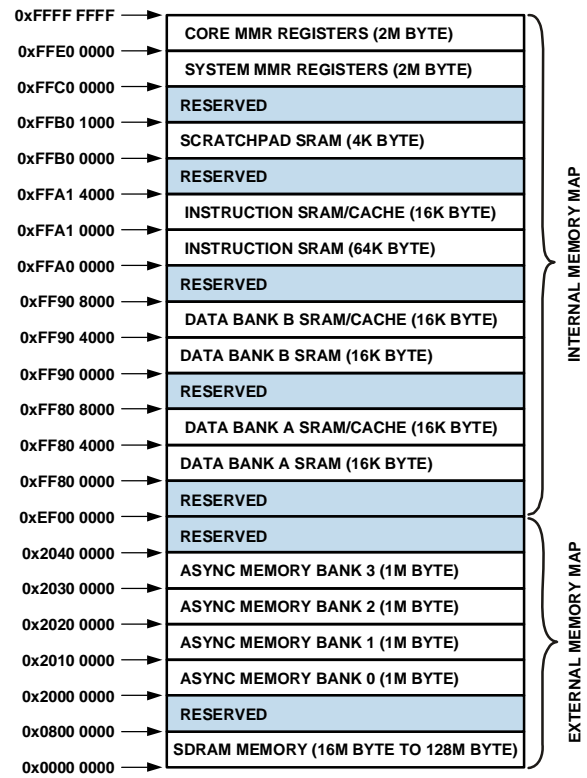


Figure 5. ADSP-BF533 Internal/External Memory Map

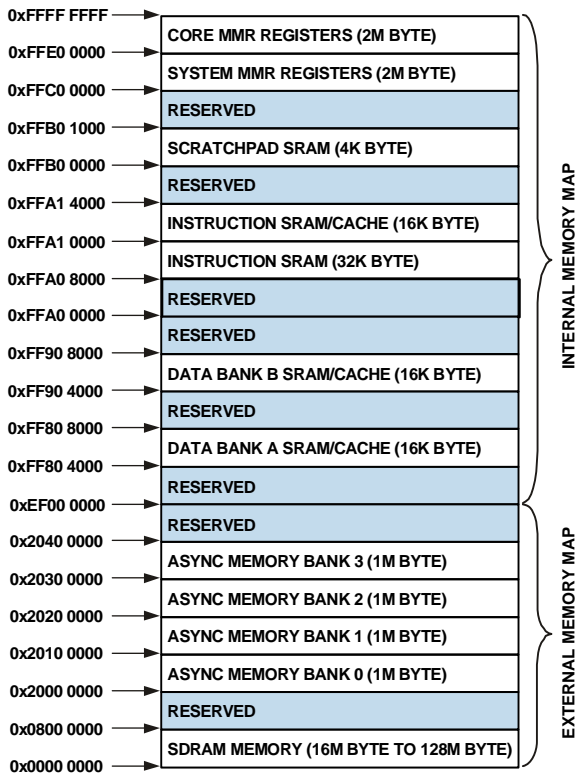


Figure 4. ADSP-BF532 Internal/External Memory Map

Event Handling

The event controller on the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor handles all asynchronous and synchronous events to the processor. The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shut-down of the system.
- Exceptions – Events that occur synchronously to program flow (i.e., the exception will be taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

Table 2. Core Event Controller (CEC)

| Priority (0 is Highest) | Event Class | EVT Entry |
|----------------------------|------------------------|-----------|
| 0 | Emulation/Test Control | EMU |
| 1 | Reset | RST |
| 2 | Nonmaskable Interrupt | NMI |
| 3 | Exception | EVX |
| 4 | Reserved | |
| 5 | Hardware Error | IVHW |
| 6 | Core Timer | IVTMR |
| 7 | General Interrupt 7 | IVG7 |
| 8 | General Interrupt 8 | IVG8 |
| 9 | General Interrupt 9 | IVG9 |
| 10 | General Interrupt 10 | IVG10 |
| 11 | General Interrupt 11 | IVG11 |
| 12 | General Interrupt 12 | IVG12 |
| 13 | General Interrupt 13 | IVG13 |
| 14 | General Interrupt 14 | IVG14 |
| 15 | General Interrupt 15 | IVG15 |

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor provides a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 3. System Interrupt Controller (SIC)

| Peripheral Interrupt Event | Default Mapping |
|----------------------------------|-----------------|
| PLL Wakeup | IVG7 |
| DMA Error | IVG7 |
| PPI Error | IVG7 |
| SPORT 0 Error | IVG7 |
| SPORT 1 Error | IVG7 |
| SPI Error | IVG7 |
| UART Error | IVG7 |
| Real-Time Clock | IVG8 |
| DMA Channel 0 (PPI) | IVG8 |
| DMA Channel 1 (SPORT 0 Receive) | IVG9 |
| DMA Channel 2 (SPORT 0 Transmit) | IVG9 |
| DMA Channel 3 (SPORT 1 Receive) | IVG9 |
| DMA Channel 4 (SPORT 1 Transmit) | IVG9 |
| DMA Channel 5 (SPI) | IVG10 |
| DMA Channel 6 (UART Receive) | IVG10 |
| DMA Channel 7 (UART Transmit) | IVG10 |
| Timer 0 | IVG11 |
| Timer 1 | IVG11 |
| Timer 2 | IVG11 |
| Port F GPIO Interrupt A | IVG12 |
| Port F GPIO Interrupt B | IVG12 |
| Memory DMA Stream 0 | IVG13 |
| Memory DMA Stream 1 | IVG13 |
| Software Watchdog Timer | IVG13 |

Event Control

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor provides the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 32 bits wide:

- CEC interrupt latch register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it may also be written to clear (cancel) latched events. This register may be read while in supervisor mode and may only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and will be processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register may be read or written while in supervisor mode.

Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.

- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in [Table 3](#).

- SIC interrupt mask register (SIC_IMASK) – This register controls the masking and unmasking of each peripheral interrupt event. When a bit is set in this register, that peripheral event is unmasked and will be processed by the system when asserted. A cleared bit in this register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status register (SIC_ISR) – As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wakeup enable register (SIC_IWR) – By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. See [Dynamic Power Management on Page 11](#).

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC will recognize and queue the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor has multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller

and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor DMA controller supports both 1-dimensional (1-D) and 2-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to $\pm 32K$ elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, autorefreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two pairs of memory DMA channels provided for transfers between the various memories of the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

REAL-TIME CLOCK

The processor real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

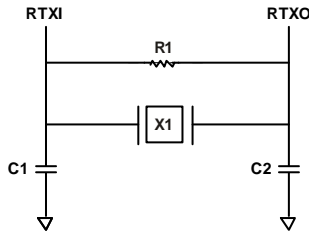
The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60 second counter, a 60 minute counter, a 24 hour counter, and a 32,768 day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from a powered-down state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 6.



SUGGESTED COMPONENTS:
 X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
 EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
 C1 = 22 pF
 C2 = 22 pF
 R1 = 10 M Ω
 NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1.
 CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2
 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 6. External Components for RTC

WATCHDOG TIMER

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor includes a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK} .

TIMERS

There are four general-purpose programmable timer units in the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor. Three timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to

clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin (TACLK), an external clock input to the PPI_CLK pin (TMRCLK), or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS (SPORTs)

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor incorporates two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I²S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I²S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from ($f_{SCLK}/131,070$) Hz to ($f_{SCLK}/2$) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ -law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.

ADSP-BF531/ADSP-BF532/ADSP-BF533

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- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data-word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1,024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

An additional 250 mV of SPORT input hysteresis can be enabled by setting Bit 15 of the PLL_CTL register. When this bit is set, all SPORT input pins have the increased hysteresis.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor has an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSI, and master input-slave output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7-1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface which supports both master/slave modes and multimaster environments.

The baud rate and clock phase/polarities for the SPI port are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI DMA controller can only service unidirectional accesses at any given time.

The SPI port clock rate is calculated as:

$$\text{SPI Clock Rate} = \frac{f_{\text{SCLK}}}{2 \times \text{SPI_BAUD}}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor provides a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 data bits to 8 data bits, 1 stop bit or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer

data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The baud rate, serial data format, error code generation and status, and interrupts for the UART port are programmable.

The UART programmable features include:

- Supporting bit rates ranging from ($f_{\text{SCLK}}/1,048,576$) bits per second to ($f_{\text{SCLK}}/16$) bits per second.
- Supporting data formats from seven bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$\text{UART Clock Rate} = \frac{f_{\text{SCLK}}}{16 \times \text{UART_Divisor}}$$

Where the 16-bit UART_Divisor comes from the UART_DLH register (most significant 8 bits) and UART_DLL register (least significant 8 bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UART are further extended with support for the Infrared Data Association (IrDA) serial infrared physical layer link specification (SIR) protocol.

GENERAL-PURPOSE I/O PORT F

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor has 16 bidirectional, general-purpose I/O pins on Port F (PF15–0). Each general-purpose I/O pin can be individually controlled by manipulation of the GPIO control, status and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual PFx pin as input or output.
- GPIO control and status registers – The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor employs a “write one to modify” mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set GPIO pin values, one register is written in order to clear GPIO pin values, one register is written in order to toggle GPIO pin values, and one register is written in order to specify GPIO pin values. Reading the GPIO status register allows software to interrogate the sense of the GPIO pin.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual GPIO pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function. PFx

pins defined as inputs can be configured to generate hardware interrupts, while output PFX pins can be triggered by software interrupts.

- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual PFX pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel A/D and D/A converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications.

Three distinct submodes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor provides four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the processor peripherals also reduces power consumption. See [Table 4](#) for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the full-on mode is entered. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the full-on or sleep modes.

Table 4. Power Settings

| Mode | PLL | PLL Bypassed | Core Clock (CCLK) | System Clock (SCLK) | Core Power |
|------------|----------------------|--------------|-------------------|---------------------|------------|
| Full-On | Enabled | No | Enabled | Enabled | On |
| Active | Enabled/ Disabled | Yes | Enabled | Enabled | On |
| Sleep | Enabled | | Disabled | Enabled | On |
| Deep Sleep | Disabled | | Disabled | Disabled | On |
| Hibernate | Disabled | | Disabled | Disabled | Off |

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity will wake up the processor. When in the sleep mode, assertion of wakeup will cause the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor will transition to the full-on mode. If BYPASS is enabled, the processor will transition to the active mode.

When in the sleep mode, system DMA access to L1 memory is not supported.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but will not be able to access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous

interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full-on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. In addition to disabling the clocks, this sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device prior to removing power if the processor state is to be preserved. Since V_{DDEXT} is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current. The internal supply regulator can be woken up either by a real-time clock wakeup or by asserting the $\overline{\text{RESET}}$ pin.

Power Savings

As shown in Table 5, the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor supports three different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of dynamic power management without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

| Power Domain | V_{DD} Range |
|------------------------------------|-----------------------|
| All internal logic, except RTC | V_{DDINT} |
| RTC internal logic and crystal I/O | V_{DDRTC} |
| All other I/O | V_{DDEXT} |

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The dynamic power management feature of the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The savings in power dissipation can be modeled using the power savings factor and % power savings calculations.

The power savings factor is calculated as:

$$\begin{aligned} & \text{power savings factor} \\ &= \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}} \right)^2 \times \left(\frac{t_{RED}}{t_{NOM}} \right) \end{aligned}$$

where the variables in the equation are:

- $f_{CCLKNOM}$ is the nominal core clock frequency
- $f_{CCLKRED}$ is the reduced core clock frequency
- $V_{DDINTNOM}$ is the nominal internal supply voltage
- $V_{DDINTRED}$ is the reduced internal supply voltage
- t_{NOM} is the duration running at $f_{CCLKNOM}$
- t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\% \text{ power savings} = (1 - \text{power savings factor}) \times 100\%$$

VOLTAGE REGULATION

The Blackfin processor provides an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See [Operating Conditions on Page 21](#) for regulator tolerances and acceptable V_{DDEXT} ranges for specific models. [Figure 7](#) shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in the hibernate state, I/O power is still being applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state either through an RTC wakeup or by asserting $\overline{\text{RESET}}$, both of which will then initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

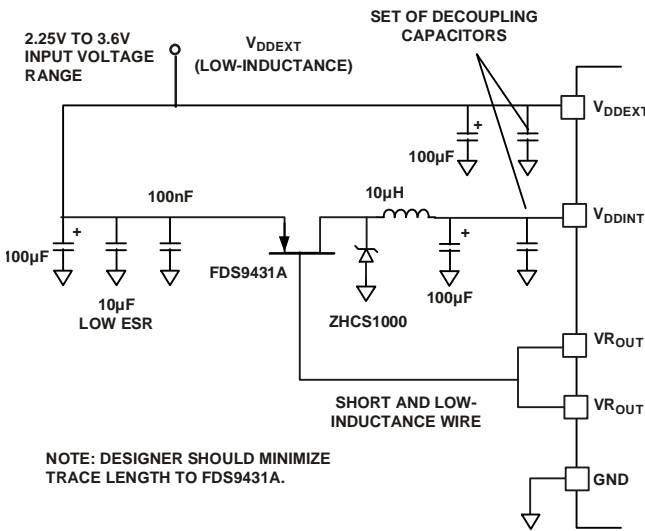


Figure 7. Voltage Regulator Circuit

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1-0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)* applications note on the Analog Devices web site (www.analog.com)—use site search on “EE-228”.

CLOCK SIGNALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor includes an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in [Figure 8](#).

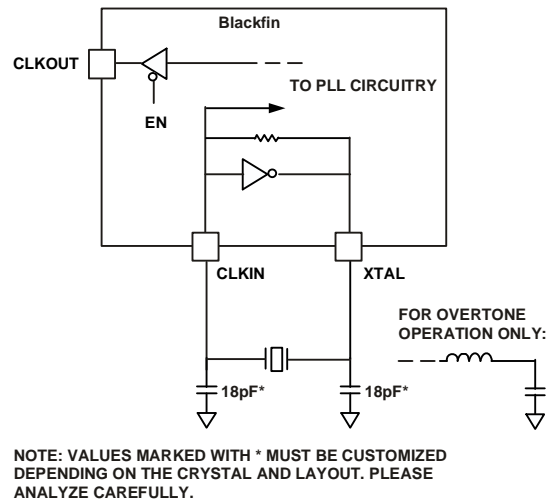


Figure 8. External Crystal Connections

A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in [Figure 8](#) fine tune the phase and amplitude of the sine

frequency. The capacitor and resistor values shown in Figure 8 are typical values only. The capacitor values are dependent upon the crystal manufacturer's load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 8.

As shown in Figure 9, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 10×, but it can be modified by a software instruction sequence. On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register.

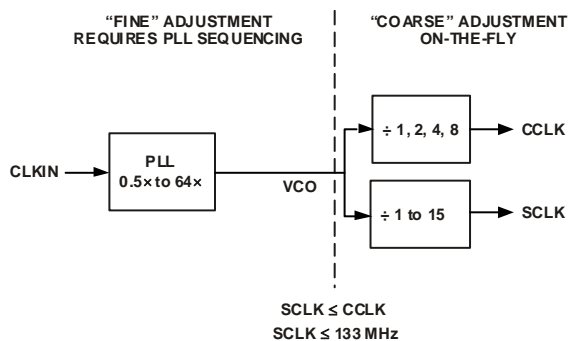


Figure 9. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3-0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios.

Table 6. Example System Clock Ratios

| Signal Name SSEL3-0 | Divider Ratio VCO/SCLK | Example Frequency Ratios (MHz) | |
|------------------------|---------------------------|-----------------------------------|------|
| | | VCO | SCLK |
| 0001 | 1:1 | 100 | 100 |
| 0011 | 3:1 | 400 | 133 |
| 1010 | 10:1 | 500 | 50 |

The maximum frequency of the system clock is f_{SCLK} . The divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK} . The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values

to the PLL divisor register (PLL_DIV). When the SSEL value is changed, it will affect all the peripherals that derive their clock signals from the SCLK signal.

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1-0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. This programmable core clock capability is useful for fast core frequency modifications.

Table 7. Core Clock Ratios

| Signal Name CSEL1-0 | Divider Ratio VCO/CCLK | Example Frequency Ratios (MHz) | |
|------------------------|---------------------------|-----------------------------------|------|
| | | VCO | CCLK |
| 00 | 1:1 | 300 | 300 |
| 01 | 2:1 | 300 | 150 |
| 10 | 4:1 | 400 | 100 |
| 11 | 8:1 | 200 | 25 |

BOOTING MODES

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor has two mechanisms (listed in Table 8) for automatically loading internal L1 instruction memory after a reset. A third mode is provided to execute from external memory, bypassing the boot sequence.

Table 8. Booting Modes

| BMODE1-0 | Description |
|----------|---|
| 00 | Execute from 16-bit external memory (bypass boot ROM) |
| 01 | Boot from 8-bit or 16-bit FLASH |
| 10 | Boot from serial master connected to SPI |
| 11 | Boot from serial slave EEPROM /flash (8-, 16-, or 24-bit address range, or Atmel AT45DB041, AT45DB081, or AT45DB161 serial flash) |

The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Execute from 16-bit external memory – Execution starts from address 0x2000 0000 with 16-bit packing. The boot ROM is bypassed in this mode. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from 8-bit or 16-bit external flash memory – The flash boot routine located in boot ROM memory space is set up using asynchronous Memory Bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from SPI serial EEPROM/flash (8-, 16-, or 24-bit addressable, or Atmel AT45DB041, AT45DB081, or AT45DB161) – The SPI uses the PF2 output pin to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0x00) until a valid 8-, 16-, or

24-bit addressable EEPROM/flash device is detected, and begins clocking data into the processor at the beginning of L1 instruction memory.

- Boot from SPI serial master – The Blackfin processor operates in SPI slave mode and is configured to receive the bytes of the LDR file from an SPI host (master) agent. To hold off the host device from transmitting while the boot ROM is busy, the Blackfin processor asserts a GPIO pin, called host wait (HWAIT), to signal the host device not to send any more bytes until the flag is deasserted. The GPIO pin is chosen by the user and this information is transferred to the Blackfin processor via bits[10:5] of the FLAG header in the LDR image.

For each of the boot modes, a 10-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the start of L1 instruction SRAM.

In addition, Bit 4 of the reset configuration register can be set by application code to bypass the normal boot sequence during a software reset. For this case, the processor jumps directly to the beginning of L1 instruction memory.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/CPU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.

- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processor is supported by a complete set of CROSSCORE[†] software and hardware development tools, including Analog Devices emulators and VisualDSP++[‡] development environment. The same emulator hardware that supports other Blackfin processors also fully emulates the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to processor assembly. The processor has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information).
- Insert breakpoints.
- Set conditional breakpoints on registers, memory, and stacks.

[†] CROSSCORE is a registered trademark of Analog Devices, Inc.

[‡] VisualDSP++ is a registered trademark of Analog Devices, Inc.

- Trace instruction execution.
- Perform linear or statistical profiling of program execution.
- Fill, dump, and graphically plot the contents of memory.
- Perform source level debugging.
- Create custom debugger windows.

The VisualDSP++ IDDE lets programmers define and manage software development. Its dialog boxes and property pages let programmers configure and manage all of the Blackfin development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state, when debugging an application that uses the VDK.

Use the expert linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color coded graphical form, easily move code and data to different areas of the processor or external memory with the drag of the mouse, and examine runtime stack and heap usage. The expert linker is fully compatible with existing linker definition file (LDF), allowing the developer to move between the graphical and textual environments.

Analog Devices emulators use the IEEE 1149.1 JTAG test access port of the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor to monitor and control the target board processor during emulation. The emulator provides full speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the Blackfin processor family.

Hardware tools include Blackfin processor PC plug-in cards. Third party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

EZ-KIT Lite Evaluation Board

Analog Devices offers a range of EZ-KIT Lite[®] evaluation platforms to use as a cost effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite includes an evaluation board along with an evaluation suite of the VisualDSP++ development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board flash device to store user-specific boot code, enabling the board to run as a standalone unit without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom defined system. Connecting one of Analog Devices JTAG emulators to the EZ-KIT Lite board enables high speed, non-intrusive emulation.

For evaluation of ADSP-BF531/ADSP-BF532/ADSP-BF533 processors, use the EZ-KIT Lite board available from Analog Devices. Order part number ADDS-BF533-EZLITE. The board comes with on-chip emulation capabilities and is equipped to enable software development. Multiple daughter cards are available.

DESIGNING AN EMULATOR-COMPATIBLE PROCESSOR BOARD

The Analog Devices family of emulators are tools that every system developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG test access port (TAP) on each JTAG processor. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the processor system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the processor's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see the *Analog Devices JTAG Emulation Technical Reference (EE-68)* on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

RELATED DOCUMENTS

The following publications that describe the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF533 Blackfin Processor Hardware Reference*
- *ADSP-BF53x/BF56x Blackfin Processor Programming Reference*
- *ADSP-BF531 Blackfin Processor Anomaly List*
- *ADSP-BF532 Blackfin Processor Anomaly List*
- *ADSP-BF533 Blackfin Processor Anomaly List*

PIN DESCRIPTIONS

ADSP-BF531/ADSP-BF532/ADSP-BF533 processor pin definitions are listed in [Table 9](#).

All pins are three-stated during and immediately after reset, except the memory interface, asynchronous memory control, and synchronous memory control pins, which are driven high.

If \overline{BR} is active, then the memory pins are also three-stated. All unused I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs as noted in the table footnotes.

In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functionality. In cases where pin functionality is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

Table 9. Pin Descriptions

| Pin Name | Type | Function | Driver Type ¹ |
|------------------------------------|------|--|--------------------------|
| <i>Memory Interface</i> | | | |
| ADDR19–1 | O | Address Bus for Async/Sync Access | A |
| DATA15–0 | I/O | Data Bus for Async/Sync Access | A |
| $\overline{ABE1-0/SDQM1-0}$ | O | Byte Enables/Data Masks for Async/Sync Access | A |
| \overline{BR} | I | Bus Request (This pin should be pulled HIGH if not used.) | |
| \overline{BG} | O | Bus Grant | A |
| \overline{BGH} | O | Bus Grant Hang | A |
| <i>Asynchronous Memory Control</i> | | | |
| $\overline{AMS3-0}$ | O | Bank Select | A |
| ARDY | I | Hardware Ready Control (This pin should be pulled HIGH if not used.) | |
| \overline{AOE} | O | Output Enable | A |
| \overline{ARE} | O | Read Enable | A |
| \overline{AWE} | O | Write Enable | A |
| <i>Synchronous Memory Control</i> | | | |
| \overline{SRAS} | O | Row Address Strobe | A |
| \overline{SCAS} | O | Column Address Strobe | A |
| \overline{SWE} | O | Write Enable | A |
| SCKE | O | Clock Enable | A |
| CLKOUT | O | Clock Output | B |
| SA10 | O | A10 Pin | A |
| \overline{SMS} | O | Bank Select | A |
| <i>Timers</i> | | | |
| TMR0 | I/O | Timer 0 | C |
| TMR1/PPI_FS1 | I/O | Timer 1/PPI Frame Sync1 | C |
| TMR2/PPI_FS2 | I/O | Timer 2/PPI Frame Sync2 | C |
| <i>PPI Port</i> | | | |
| PPI3–0 | I/O | PPI3–0 | C |
| PPI_CLK/TMRCLK | I | PPI Clock/External Timer Reference | |

Table 9. Pin Descriptions (Continued)

| Pin Name | Type | Function | Driver Type ¹ |
|---|------|---|--------------------------|
| <i>Port F: GPIO/Parallel Peripheral Interface Port/SPI/Timers</i> | | | |
| PF0/ \overline{SPISS} | I/O | GPIO/SPI Slave Select Input | C |
| PF1/ $\overline{SPISEL1}/TACLK$ | I/O | GPIO/SPI Slave Select Enable 1/Timer Alternate Clock Input | C |
| PF2/ $\overline{SPISEL2}$ | I/O | GPIO/SPI Slave Select Enable 2 | C |
| PF3/ $\overline{SPISEL3}/PPI_FS3$ | I/O | GPIO/SPI Slave Select Enable 3/PPI Frame Sync 3 | C |
| PF4/ $\overline{SPISEL4}/PPI15$ | I/O | GPIO/SPI Slave Select Enable 4/PPI 15 | C |
| PF5/ $\overline{SPISEL5}/PPI14$ | I/O | GPIO/SPI Slave Select Enable 5/PPI 14 | C |
| PF6/ $\overline{SPISEL6}/PPI13$ | I/O | GPIO/SPI Slave Select Enable 6/PPI 13 | C |
| PF7/ $\overline{SPISEL7}/PPI12$ | I/O | GPIO/SPI Slave Select Enable 7/PPI 12 | C |
| PF8/PPI11 | I/O | GPIO/PPI 11 | C |
| PF9/PPI10 | I/O | GPIO/PPI 10 | C |
| PF10/PPI9 | I/O | GPIO/PPI 9 | C |
| PF11/PPI8 | I/O | GPIO/PPI 8 | C |
| PF12/PPI7 | I/O | GPIO/PPI 7 | C |
| PF13/PPI6 | I/O | GPIO/PPI 6 | C |
| PF14/PPI5 | I/O | GPIO/PPI 5 | C |
| PF15/PPI4 | I/O | GPIO/PPI 4 | C |
| <i>JTAG Port</i> | | | |
| TCK | I | JTAG Clock | |
| TDO | O | JTAG Serial Data Out | C |
| TDI | I | JTAG Serial Data In | |
| TMS | I | JTAG Mode Select | |
| \overline{TRST} | I | JTAG Reset (This pin should be pulled LOW if JTAG is not used.) | |
| \overline{EMU} | O | Emulation Output | C |
| <i>SPI Port</i> | | | |
| MOSI | I/O | Master Out Slave In | C |
| MISO | I/O | Master In Slave Out (This pin should be pulled HIGH through a 4.7 k Ω resistor if booting via the SPI port.) | C |
| SCK | I/O | SPI Clock | D |
| <i>Serial Ports</i> | | | |
| RSCLK0 | I/O | SPORT0 Receive Serial Clock | D |
| RFS0 | I/O | SPORT0 Receive Frame Sync | C |
| DR0PRI | I | SPORT0 Receive Data Primary | |
| DR0SEC | I | SPORT0 Receive Data Secondary | |
| TSCLK0 | I/O | SPORT0 Transmit Serial Clock | D |
| TFS0 | I/O | SPORT0 Transmit Frame Sync | C |
| DT0PRI | O | SPORT0 Transmit Data Primary | C |
| DT0SEC | O | SPORT0 Transmit Data Secondary | C |
| RSCLK1 | I/O | SPORT1 Receive Serial Clock | D |

ADSP-BF531/ADSP-BF532/ADSP-BF533

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Table 9. Pin Descriptions (Continued)

| Pin Name | Type | Function | Driver Type ¹ |
|---------------------------|------|--|--------------------------|
| RFS1 | I/O | SPORT1 Receive Frame Sync | C |
| DR1PRI | I | SPORT1 Receive Data Primary | |
| DR1SEC | I | SPORT1 Receive Data Secondary | |
| TSCLK1 | I/O | SPORT1 Transmit Serial Clock | D |
| TFS1 | I/O | SPORT1 Transmit Frame Sync | C |
| DT1PRI | O | SPORT1 Transmit Data Primary | C |
| DT1SEC | O | SPORT1 Transmit Data Secondary | C |
| <i>UART Port</i> | | | |
| RX | I | UART Receive | |
| TX | O | UART Transmit | C |
| <i>Real-Time Clock</i> | | | |
| RTXI | I | RTC Crystal Input (This pin should be pulled LOW when not used.) | |
| RTXO | O | RTC Crystal Output | |
| <i>Clock</i> | | | |
| CLKIN | I | Clock/Crystal Input (This pin needs to be at a level or clocking.) | |
| XTAL | O | Crystal Output | |
| <i>Mode Controls</i> | | | |
| $\overline{\text{RESET}}$ | I | Reset (This pin is always active during core power-on.) | |
| NMI | I | Nonmaskable Interrupt (This pin should be pulled LOW when not used.) | |
| BMODE1-0 | I | Boot Mode Strap (These pins must be pulled to the state required for the desired boot mode.) | |
| <i>Voltage Regulator</i> | | | |
| VROUT1-0 | O | External FET Drive | |
| <i>Supplies</i> | | | |
| V _{DDEXT} | P | I/O Power Supply | |
| V _{DDINT} | P | Core Power Supply | |
| V _{DDRTC} | P | Real-Time Clock Power Supply | |
| GND | G | External Ground | |

¹ Refer to Figure 30 on Page 43 to Figure 41 on Page 45.

SPECIFICATIONS

Component specifications are subject to change without notice.

OPERATING CONDITIONS

| Parameter | Conditions | Min | Nominal | Max | Unit |
|---|--|------|-------------|-------|------|
| V_{DDINT} Internal Supply Voltage ¹ | Nonautomotive 400 MHz and 500 MHz speed grade models ² | 0.8 | 1.2 | 1.32 | V |
| V_{DDINT} Internal Supply Voltage ¹ | Nonautomotive 533 MHz speed grade models ² | 0.8 | 1.25 | 1.375 | V |
| V_{DDINT} Internal Supply Voltage ¹ | 600 MHz speed grade models ² | 0.8 | 1.30 | 1.45 | V |
| V_{DDINT} Internal Supply Voltage ¹ | Automotive grade models ² | 0.95 | 1.2 | 1.32 | V |
| V_{DDEXT} External Supply Voltage | Nonautomotive grade models ² | 1.75 | 1.8/2.5/3.3 | 3.6 | V |
| V_{DDEXT} External Supply Voltage | Automotive grade models ² | 2.7 | 3.3 | 3.6 | V |
| V_{DDRTC} Real-Time Clock Power Supply Voltage | Nonautomotive grade models ² | 1.75 | 1.8/2.5/3.3 | 3.6 | V |
| V_{DDRTC} Real-Time Clock Power Supply Voltage | Automotive grade models ² | 2.7 | 3.3 | 3.6 | V |
| V_{IH} High Level Input Voltage ^{3,4} | $V_{DDEXT} = 1.85\text{ V}$ | 1.3 | | 3.6 | V |
| V_{IH} High Level Input Voltage ^{3,4} | $V_{DDEXT} = \text{Maximum}$ | 2.0 | | 3.6 | V |
| $V_{IHCLKIN}$ High Level Input Voltage ⁵ | $V_{DDEXT} = \text{Maximum}$ | 2.2 | | 3.6 | V |
| V_{IL} Low Level Input Voltage ^{3,6} | $V_{DDEXT} = 1.75\text{ V}$ | -0.3 | | +0.3 | V |
| V_{IL} Low Level Input Voltage ^{3,6} | $V_{DDEXT} = 2.25\text{ V}$ | -0.3 | | +0.6 | V |
| T_J Junction Temperature | 160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT} = 0^\circ\text{C to } +70^\circ\text{C}$ | 0 | | +95 | °C |
| T_J Junction Temperature | 160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT} = -40^\circ\text{C to } +85^\circ\text{C}$ | -40 | | +105 | °C |
| T_J Junction Temperature | 160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT} = -40^\circ\text{C to } +105^\circ\text{C}$ | -40 | | +125 | °C |
| T_J Junction Temperature | 169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT} = -40^\circ\text{C to } +105^\circ\text{C}$ | -40 | | +125 | °C |
| T_J Junction Temperature | 169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT} = -40^\circ\text{C to } +85^\circ\text{C}$ | -40 | | +105 | °C |
| T_J Junction Temperature | 176-Lead Quad Flatpack (LQFP) @ $T_{AMBIENT} = -40^\circ\text{C to } +85^\circ\text{C}$ | -40 | | +100 | °C |

¹ The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with -5% to +10% tolerance, 1.25 V with -4% to +10% tolerance, and 1.3 V with -0% to +10% tolerance.

² See [Ordering Guide on Page 59](#).

³ Applies to all input and bidirectional pins except CLKIN.

⁴ The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are 3.3 V tolerant (always accepts up to 3.6 V maximum V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT} , because V_{OH} (maximum) approximately equals V_{DDEXT} (maximum). This 3.3 V tolerance applies to bidirectional pins (DATA15-0, TMR2-0, PF15-0, PPI3-0, RSCLK1-0, TSCLK1-0, RFS1-0, TFS1-0, MOSI, MISO, SCK) and input only pins (\overline{BR} , ARDY, PPI_CLK, DR0PRI, DR0SEC, DR1PRI, DR1SEC, RX, RTXI, TCK, TDI, TMS, TRST, CLKIN, RESET, NMI, and BMODE1-0).

⁵ Applies to CLKIN pin only.

⁶ Applies to all input and bidirectional pins.

ADSP-BF531/ADSP-BF532/ADSP-BF533

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ELECTRICAL CHARACTERISTICS

| Parameter | Test Conditions | Low Power ¹ | | | High Speed ² | | | Unit | |
|--|--|--|---------|-----|-------------------------|----------------|-----|----------------|----|
| | | Min | Typical | Max | Min | Typical | Max | | |
| V _{OH} | High Level Output Voltage ³ | @ V _{DDEXT} = 1.75 V, I _{OH} = -0.5 mA | | | 1.5 | | | V | |
| V _{OH} | High Level Output Voltage ³ | @ V _{DDEXT} = 2.25 V, I _{OH} = -0.5 mA | | | 1.9 | | | V | |
| V _{OH} | High Level Output Voltage ³ | @ V _{DDEXT} = 3.0 V, I _{OH} = -0.5 mA | | | 2.4 | | | V | |
| V _{OL} | Low Level Output Voltage ³ | @ V _{DDEXT} = 1.75 V, I _{OL} = 2.0 mA | | | 0.2 | | | V | |
| V _{OL} | Low Level Output Voltage ³ | @ V _{DDEXT} = 2.25 V/3.0 V, I _{OL} = 2.0 mA | | | 0.4 | | | V | |
| I _{IH} | High Level Input Current ⁴ | @ V _{DDEXT} = Maximum, V _{IN} = V _{DD} Maximum | | | 10.0 | | | μA | |
| I _{IHP} | High Level Input Current JTAG ⁵ | @ V _{DDEXT} = Maximum, V _{IN} = V _{DD} Maximum | | | 50.0 | | | μA | |
| I _{IL} ⁶ | Low Level Input Current ⁴ | @ V _{DDEXT} = Maximum, V _{IN} = 0 V | | | 10.0 | | | μA | |
| I _{OZH} | Three-State Leakage Current ⁷ | @ V _{DDEXT} = Maximum, V _{IN} = V _{DD} Maximum | | | 10.0 | | | μA | |
| I _{OZL} ⁶ | Three-State Leakage Current ⁷ | @ V _{DDEXT} = Maximum, V _{IN} = 0 V | | | 10.0 | | | μA | |
| C _{IN} | Input Capacitance ⁸ | f _{IN} = 1 MHz, T _{AMBIENT} = 25°C, V _{IN} = 2.5 V | | | 4 | 8 ⁹ | 4 | 8 ⁹ | pF |
| I _{DDHIBERNATE} | V _{DDINT} Current in Hibernate State | V _{DDEXT} = 3.65 V with voltage regulator off (V _{DDINT} = 0 V) | | | 50 | | | μA | |
| I _{DDRTC} | V _{DDRTC} Current | V _{DDRTC} = 3.3 V, T _{JUNCTION} = 25°C | | | 20 | | | μA | |
| I _{DDDEEPSLEEP} ¹⁰ | V _{DDINT} Current in Deep Sleep Mode | V _{DDINT} = 0.8 V, T _{JUNCTION} = 25°C | | | 7.5 | | | 35 | mA |
| I _{DDSLLEEP} | V _{DDINT} Current in Sleep Mode | V _{DDINT} = 0.8 V, T _{JUNCTION} = 25°C, SCLK = 25 MHz | | | 10 | | | 37.5 | mA |
| I _{DD_TYP} ^{10, 11} | V _{DDINT} Current Dissipation (Typical) | V _{DDINT} = 0.8 V, f _{CCLK} = 50 MHz, T _{JUNCTION} = 25°C | | | 20 | | | 47 | mA |
| I _{DD_TYP} ^{10, 11} | V _{DDINT} Current Dissipation (Typical) | V _{DDINT} = 1.14 V, f _{CCLK} = 400 MHz, T _{JUNCTION} = 25°C | | | 132 | | | 198 | mA |
| I _{DD_TYP} ^{10, 11} | V _{DDINT} Current Dissipation (Typical) | V _{DDINT} = 1.2 V, f _{CCLK} = 500 MHz, T _{JUNCTION} = 25°C | | | | | | 240 | mA |
| I _{DD_TYP} ^{10, 11} | V _{DDINT} Current Dissipation (Typical) | V _{DDINT} = 1.2 V, f _{CCLK} = 533 MHz, T _{JUNCTION} = 25°C | | | | | | 250 | mA |
| I _{DD_TYP} ^{10, 11} | V _{DDINT} Current Dissipation (Typical) | V _{DDINT} = 1.3 V, f _{CCLK} = 600 MHz, T _{JUNCTION} = 25°C | | | | | | 308 | mA |

¹ Applies to all 400 MHz speed grade models. See [Ordering Guide on Page 59](#).

² Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See [Ordering Guide on Page 59](#).

³ Applies to output and bidirectional pins.

⁴ Applies to input pins except JTAG inputs.

⁵ Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).

⁶ Absolute value.

⁷ Applies to three-statable pins.

⁸ Applies to all signal pins.

⁹ Guaranteed, but not tested.

¹⁰ See *Estimating Power for ADSP-BF531/BF532/BF533 Blackfin Processors (EE-229)* on the Analog Devices website (www.analog.com)—use site search on “EE-229.”

¹¹ Processor executing 75% dual MAC, 25% ADD with moderate data bus activity.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in the table may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameter | Rating |
|--|-------------------------------|
| Internal (Core) Supply Voltage (V_{DDINT}) | -0.3 V to +1.4 V |
| External (I/O) Supply Voltage (V_{DDEXT}) | -0.5 V to +3.8 V |
| Input Voltage ¹ | -0.5 V to +3.8 V |
| Output Voltage Swing | -0.5 V to $V_{DDEXT} + 0.5$ V |
| Load Capacitance ² | 200 pF |
| Storage Temperature Range | -65 C to +150°C |
| Junction Temperature Under Bias | 125°C |

¹ Applies to 100% transient duty cycle. For other duty cycles see Table 10.

² For proper SDRAM controller operation, the maximum load capacitance is 50 pF (at 3.3 V) or 30 pF (at 2.5 V) for ADDR19-1, DATA15-0, ABE1-0/SDQM1-0, CLKOUT, SCKE, SA10, SRAS, SCAS, SWE, and SMS.

Table 10. Maximum Duty Cycle for Input Transient Voltage¹

| V_{IN} Min (V) | V_{IN} Max (V) ² | Maximum Duty Cycle |
|------------------|-------------------------------|--------------------|
| -0.50 | +3.80 | 100% |
| -0.70 | +4.00 | 40% |
| -0.80 | +4.10 | 25% |
| -0.90 | +4.20 | 15% |
| -1.00 | +4.30 | 10% |

¹ Applies to all signal pins with the exception of CLKIN, XTAL, VROUT1-0.

² Only one of the listed options can apply to a particular design.

ESD SENSITIVITY



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be take to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 10 and Table 11 provides details about the package branding for the Blackfin processors. For a complete listing of product availability, see the Ordering Guide on Page 59.



Figure 10. Product Information on Package

Table 11. Package Brand Information

| Brand Key | Field Description |
|------------|--|
| ADSP-BF53x | Either ADSP-BF531, ADSP-BF532, or ADSP-BF533 |
| t | Temperature Range |
| pp | Package Type |
| Z | RoHS Compliant Part |
| cc | See Ordering Guide |
| vvvvv.x | Assembly Lot Code |
| n.n | Silicon Revision |
| yyww | Date Code |

ADSP-BF531/ADSP-BF532/ADSP-BF533

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TIMING SPECIFICATIONS

Table 12 through Table 15 describe the timing requirements for the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock as described

in Absolute Maximum Ratings on Page 23, and the voltage controlled oscillator (VCO) operating frequencies described in Table 14. Table 14 describes phase-locked loop operating conditions.

Table 12. Core Clock (CCLK) Requirements—400 MHz Models¹

| Parameter | Internal Regulator Setting | T _{JUNCTION} = 125°C | All ² Other T _{JUNCTION} | Unit |
|---|----------------------------|-------------------------------|--|------|
| | | Max | Max | |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 1.14 V Minimum) | 1.20 V | 400 | 400 | MHz |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 1.045 V Minimum) | 1.10 V | 333 | 364 | MHz |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 0.95 V Minimum) | 1.00 V | 295 | 333 | MHz |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 0.85 V Minimum) | 0.90 V | | 280 | MHz |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 0.8 V Minimum) | 0.85 V | | 250 | MHz |

¹ See Ordering Guide on Page 59.

² See Operating Conditions on Page 21.

Table 13. Core Clock (CCLK) Requirements—500 MHz, 533 MHz, and 600 MHz Models

| Parameter | Internal Regulator Setting | Max | Unit |
|---|----------------------------|-----|------|
| f _{CCLK} CCLK Frequency (V _{DDINT} = 1.3 V Minimum) ¹ | 1.30 V | 600 | MHz |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 1.2 V Minimum) ² | 1.25 V | 533 | MHz |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 1.14 V Minimum) ³ | 1.20 V | 500 | MHz |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 1.045 V Minimum) | 1.10 V | 444 | MHz |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 0.95 V Minimum) | 1.00 V | 400 | MHz |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 0.85 V Minimum) | 0.90 V | 333 | MHz |
| f _{CCLK} CCLK Frequency (V _{DDINT} = 0.8 V Minimum) | 0.85 V | 250 | MHz |

¹ Applies to 600 MHz models only. See Ordering Guide on Page 59.

² Applies to 533 MHz and 600 MHz models only. See Ordering Guide on Page 59. 533 MHz models cannot support internal regulator levels above 1.25 V.

³ Applies to 500 MHz, 533 MHz, and 600 MHz models. See Ordering Guide on Page 59. 500 MHz models cannot support internal regulator levels above 1.20 V.

Table 14. Phase-Locked Loop Operating Conditions

| Parameter | Min | Max | Unit |
|--|-----|---------------------------|------|
| f _{VCO} Voltage Controlled Oscillator (VCO) Frequency | 50 | Maximum f _{CCLK} | MHz |

Table 15. System Clock (SCLK) Requirements

| Parameter ¹ | | V _{DDEXT} = 1.8 V | V _{DDEXT} = 2.5 V/3.3 V | Unit |
|------------------------|---|----------------------------|----------------------------------|------|
| | | Max | Max | |
| MBGA/PBGA | | | | |
| f _{SCLK} | CLKOUT/SCLK Frequency (V _{DDINT} ≥ 1.14 V) | 100 | 133 | MHz |
| f _{SCLK} | CLKOUT/SCLK Frequency (V _{DDINT} < 1.14 V) | 100 | 100 | MHz |
| LQFP | | | | |
| f _{SCLK} | CLKOUT/SCLK Frequency (V _{DDINT} ≥ 1.14 V) | 100 | 133 | MHz |
| f _{SCLK} | CLKOUT/SCLK Frequency (V _{DDINT} < 1.14 V) | 83 | 83 | MHz |

¹ t_{SCLK} (= 1/f_{SCLK}) must be greater than or equal to t_{CCLK}.

Clock and Reset Timing

Table 16 and Figure 11 describe clock and reset operations. Per Absolute Maximum Ratings on Page 23, combinations of CLKIN and clock multipliers/divisors must not result in core/

system clocks exceeding the maximum limits allowed for the processor, including system clock restrictions related to supply voltage.

Table 16. Clock and Reset Timing

| Parameter | Min | Max | Unit |
|---|---------------|-------|------|
| <i>Timing Requirements</i> | | | |
| t_{CKIN} CLKIN Period ^{1, 2, 3, 4} | 25.0 | 100.0 | ns |
| t_{CKINL} CLKIN Low Pulse | 10.0 | | ns |
| t_{CKINH} CLKIN High Pulse | 10.0 | | ns |
| t_{WRST} \overline{RESET} Asserted Pulse Width Low ⁵ | 11 t_{CKIN} | | ns |

¹ Applies to PLL bypass mode and PLL nonbypass mode.

² CLKIN frequency must not change on the fly.

³ Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO} , f_{CLK} , and f_{SCLK} settings discussed in Table 12 on Page 24 through Table 15 on Page 24. Since the default behavior of the PLL is to multiply the CLKIN frequency by 10, the 400 MHz speed grade parts cannot use the full CLKIN period range.

⁴ If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.

⁵ Applies after power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2,000 CLKIN cycles, while \overline{RESET} is asserted, assuming stable power supplies and CLKIN (not including start-up time of external clock oscillator).

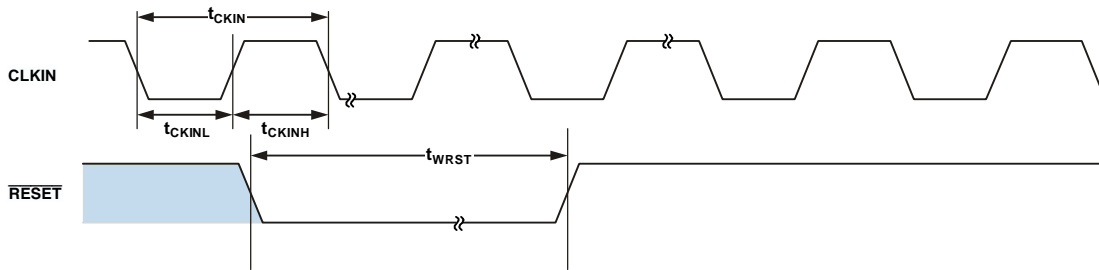


Figure 11. Clock and Reset Timing

Asynchronous Memory Read Cycle Timing

Table 17. Asynchronous Memory Read Cycle Timing

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ | | Unit |
|----------------------------------|--|-----|---|-----|------|
| | Min | Max | Min | Max | |
| <i>Timing Requirements</i> | | | | | |
| t_{SDAT} | DATA15-0 Setup Before CLKOUT | | 2.1 | 2.1 | ns |
| t_{HDAT} | DATA15-0 Hold After CLKOUT | | 1.0 | 0.8 | ns |
| t_{SARDY} | ARDY Setup Before CLKOUT | | 4.0 | 4.0 | ns |
| t_{HARDY} | ARDY Hold After CLKOUT | | 1.0 | 0.0 | ns |
| <i>Switching Characteristics</i> | | | | | |
| t_{DO} | Output Delay After CLKOUT ¹ | | 1.0 | 6.0 | ns |
| t_{HO} | Output Hold After CLKOUT ¹ | | 1.0 | 0.8 | ns |

¹ Output pins include $\overline{\text{AMS}}3-0$, $\overline{\text{ABE}}1-0$, $\overline{\text{ADDR}}19-1$, $\text{DATA}15-0$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$.

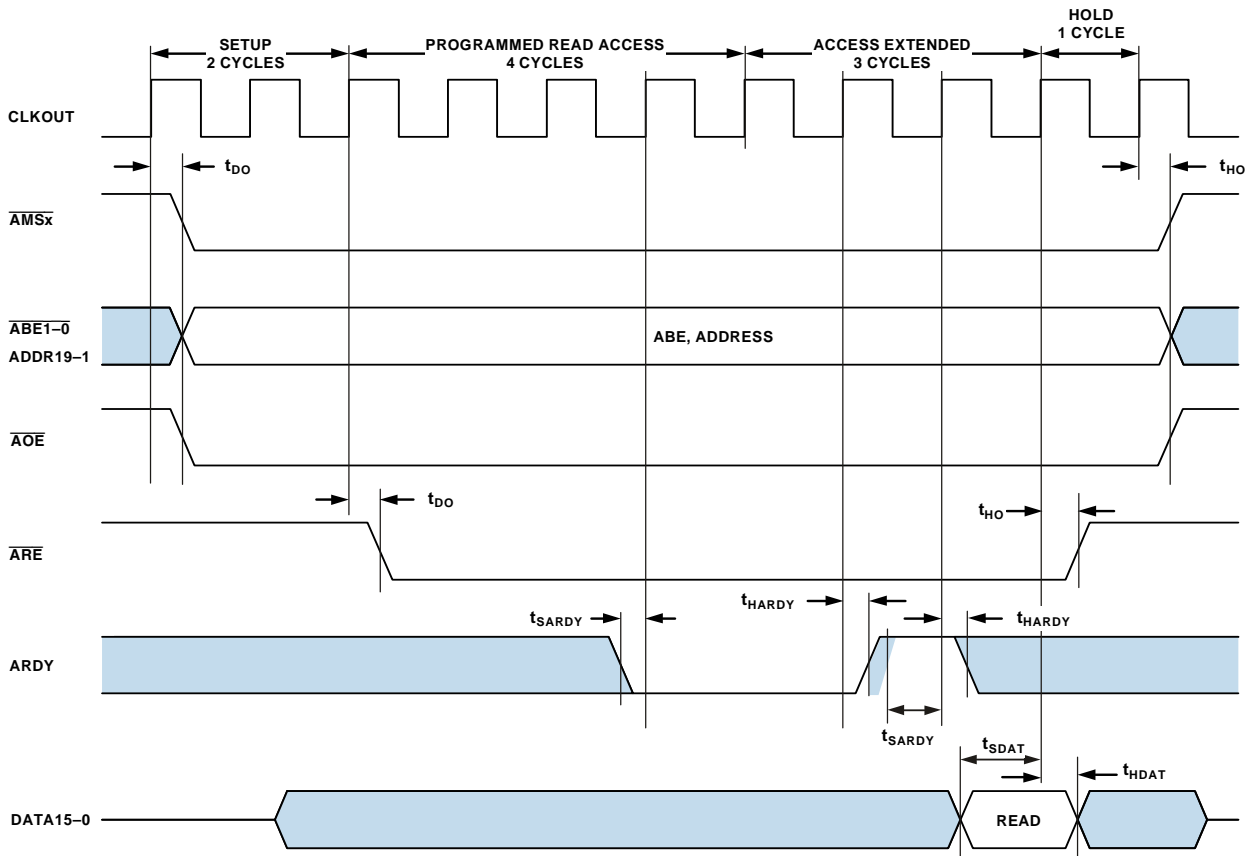


Figure 12. Asynchronous Memory Read Cycle Timing

Asynchronous Memory Write Cycle Timing

Table 18. Asynchronous Memory Write Cycle Timing

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ | | Unit |
|---|----------------------------|-----|---|-----|------|
| | Min | Max | Min | Max | |
| <i>Timing Requirements</i> | | | | | |
| t_{SARDY} ARDY Setup Before CLKOUT | 4.0 | | 4.0 | | ns |
| t_{HARDY} ARDY Hold After CLKOUT | 1.0 | | 0.0 | | ns |
| <i>Switching Characteristics</i> | | | | | |
| t_{DDAT} DATA15-0 Disable After CLKOUT | | 6.0 | | 6.0 | ns |
| t_{ENDAT} DATA15-0 Enable After CLKOUT | 1.0 | | 1.0 | | ns |
| t_{DO} Output Delay After CLKOUT ¹ | | 6.0 | | 6.0 | ns |
| t_{HO} Output Hold After CLKOUT ¹ | 1.0 | | 0.8 | | ns |

¹ Output pins include AMS3-0, ABE1-0, ADDR19-1, DATA15-0, AOE, AWE.

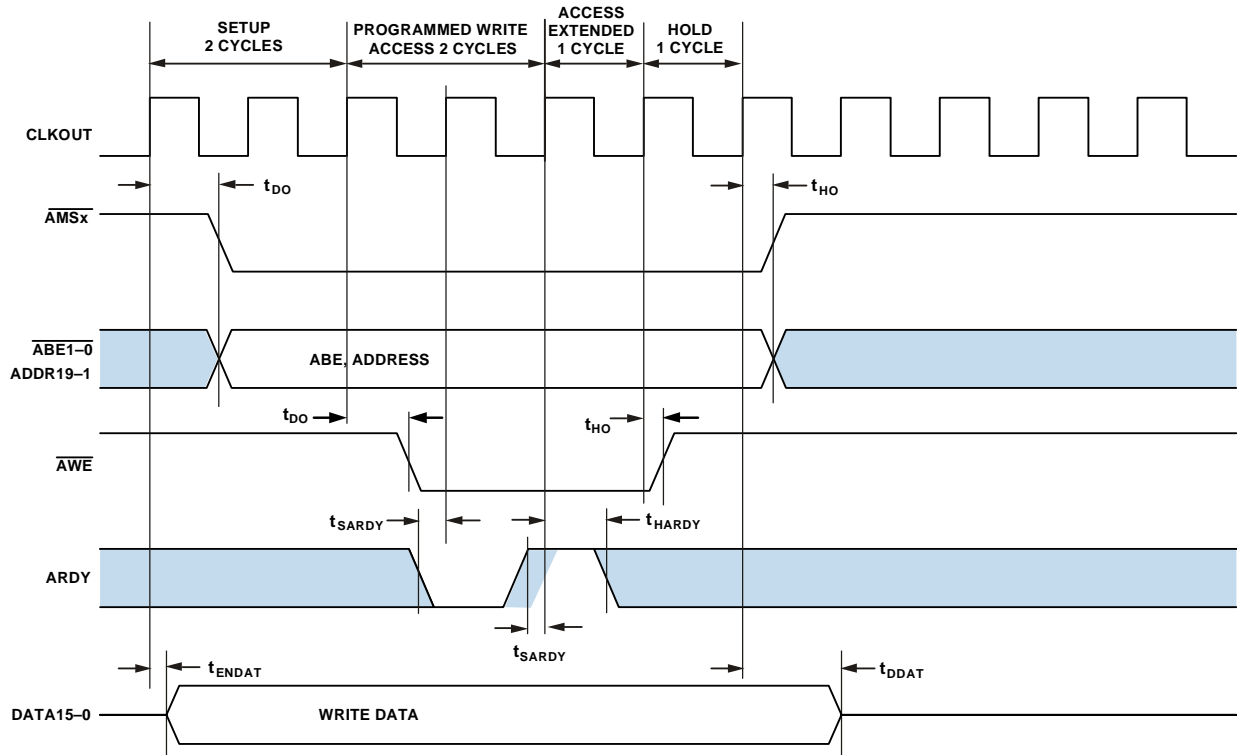


Figure 13. Asynchronous Memory Write Cycle Timing

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SDRAM Interface Timing

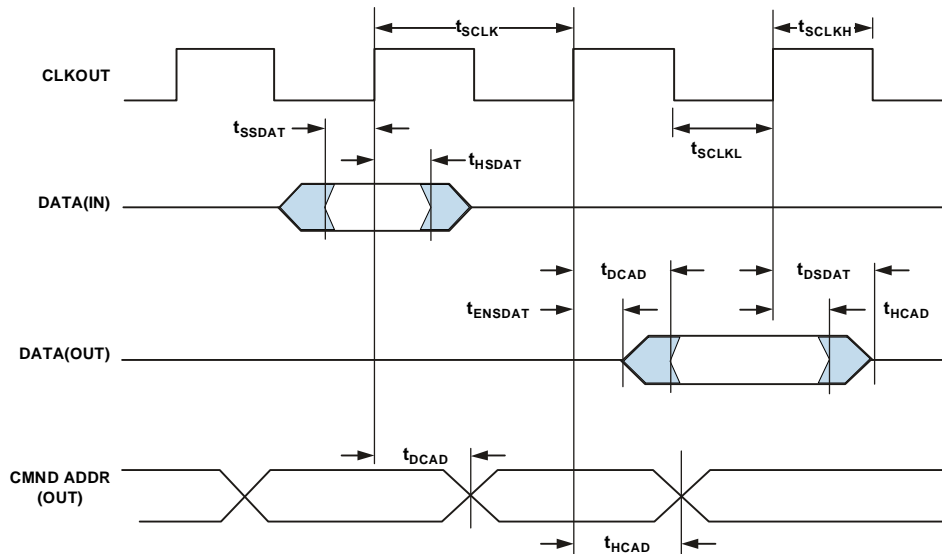
Table 19. SDRAM Interface Timing¹

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ | | Unit |
|--|----------------------------|-----|---|-----|------|
| | Min | Max | Min | Max | |
| <i>Timing Requirements</i> | | | | | |
| t_{SSDAT} DATA Setup Before CLKOUT | 2.1 | | 1.5 | | ns |
| t_{HSDAT} DATA Hold After CLKOUT | 0.8 | | 0.8 | | ns |
| <i>Switching Characteristics</i> | | | | | |
| t_{SCLK} CLKOUT Period ² | 10.0 | | 7.5 | | ns |
| t_{SCLKH} CLKOUT Width High | 2.5 | | 2.5 | | ns |
| t_{SCLKL} CLKOUT Width Low | 2.5 | | 2.5 | | ns |
| t_{DCAD} Command, ADDR, Data Delay After CLKOUT ³ | | 6.0 | | 4.0 | ns |
| t_{HCAD} Command, ADDR, Data Hold After CLKOUT ¹ | 1.0 | | 1.0 | | ns |
| t_{DSDAT} Data Disable After CLKOUT | | 6.0 | | 4.0 | ns |
| t_{ENSDAT} Data Enable After CLKOUT | 1.0 | | 1.0 | | ns |

¹ SDRAM timing for $T_{JUNCTION} = 125^{\circ}\text{C}$ is limited to 100 MHz.

² Refer to Table 15 on Page 24 for maximum f_{SCLK} at various V_{DDINT} .

³ Command pins include: \overline{SRAS} , \overline{SCAS} , \overline{SWE} , \overline{SDQM} , \overline{SMS} , SA10, SCKE.



NOTE: COMMAND = \overline{SRAS} , \overline{SCAS} , \overline{SWE} , \overline{SDQM} , \overline{SMS} , SA10, SCKE.

Figure 14. SDRAM Interface Timing

External Port Bus Request and Grant Cycle Timing

Table 20 and Figure 15 describe external port bus request and bus grant operations.

Table 20. External Port Bus Request and Grant Cycle Timing

| Parameter | V _{DDEXT} = 1.8 V LQFP/PBGA Packages | | V _{DDEXT} = 1.8 V MBGA Package | | V _{DDEXT} = 2.5 V/3.3 V All Packages | | Unit |
|---|--|-----|--|-----|--|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| <i>Timing Requirements</i> | | | | | | | |
| t _{BS} $\overline{\text{BR}}$ Asserted to CLKOUT High Setup | 4.6 | | 4.6 | | 4.6 | | ns |
| t _{BH} CLKOUT High to $\overline{\text{BR}}$ Deasserted Hold Time | 1.0 | | 1.0 | | 0.0 | | ns |
| <i>Switching Characteristics</i> | | | | | | | |
| t _{SD} CLKOUT Low to $\overline{\text{AMSx}}$, Address, and $\overline{\text{ARE/AWE}}$ Disable | | 4.5 | | 4.5 | | 4.5 | ns |
| t _{SE} CLKOUT Low to $\overline{\text{AMSx}}$, Address, and $\overline{\text{ARE/AWE}}$ Enable | | 4.5 | | 4.5 | | 4.5 | ns |
| t _{DBG} CLKOUT High to $\overline{\text{BG}}$ High Setup | | 6.0 | | 4.6 | | 3.6 | ns |
| t _{EBG} CLKOUT High to $\overline{\text{BG}}$ Deasserted Hold Time | | 6.0 | | 4.6 | | 3.6 | ns |
| t _{DBH} CLKOUT High to $\overline{\text{BGH}}$ High Setup | | 6.0 | | 4.6 | | 3.6 | ns |
| t _{EBH} CLKOUT High to $\overline{\text{BGH}}$ Deasserted Hold Time | | 6.0 | | 4.6 | | 3.6 | ns |

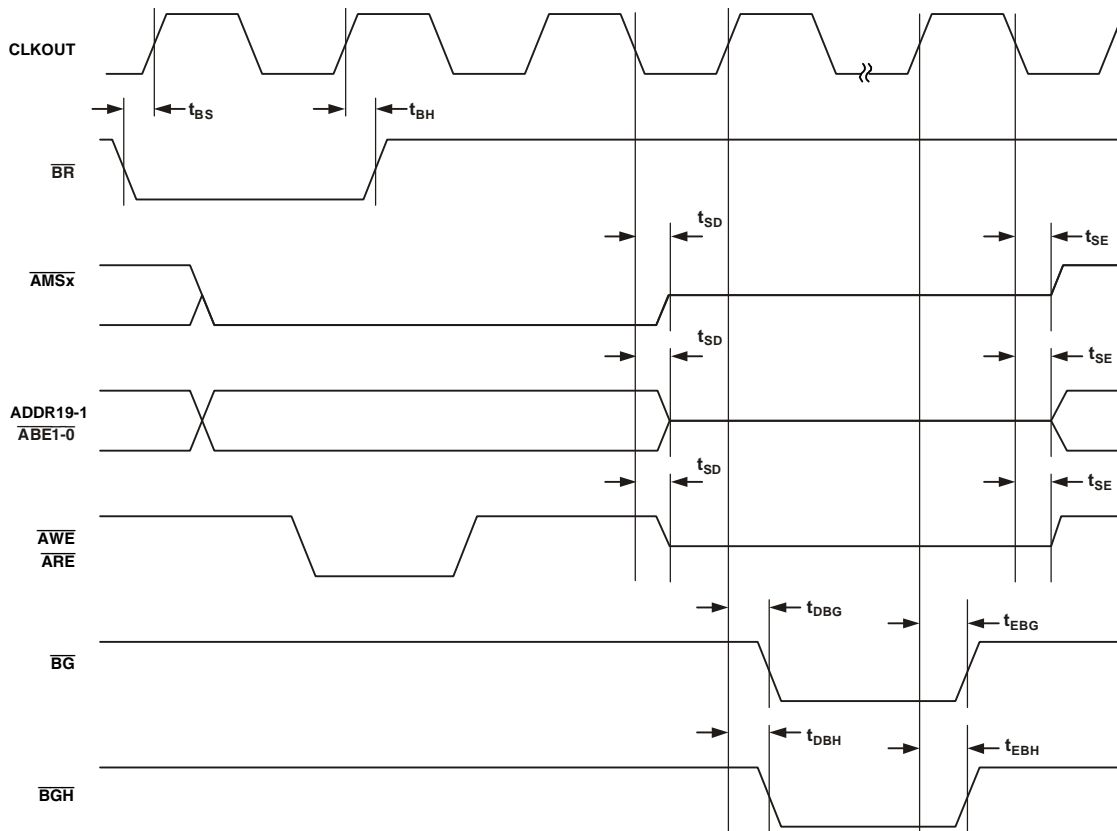


Figure 15. External Port Bus Request and Grant Cycle Timing

Parallel Peripheral Interface Timing

Table 21 and Figure 16 through Figure 21 on Page 33 describe parallel peripheral interface operations.

Table 21. Parallel Peripheral Interface Timing

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ LQFP/PBGA Packages | | $V_{DDEXT} = 1.8\text{ V}$ MBGA Package | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ All Packages | | Unit |
|--|--|------|--|-----|---|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| <i>Timing Requirements</i> | | | | | | | |
| t_{PCLKW} PPI_CLK Width | 8.0 | | 8.0 | | 6.0 | | ns |
| t_{PCLK} PPI_CLK Period ¹ | 20.0 | | 20.0 | | 15.0 | | ns |
| t_{SFSPE} External Frame Sync Setup Before PPI_CLK Edge (Nonsampling Edge for Rx, Sampling Edge for Tx) | 6.0 | | 6.0 | | 4.0 ² | | ns |
| t_{HFSPE} External Frame Sync Hold After PPI_CLK | 1.0 ² 2.0 ³ | | 1.0 ² 2.0 ³ | | 1.0 ² 2.0 ³ | | ns |
| t_{SDRPE} Receive Data Setup Before PPI_CLK | 3.5 | | 3.5 | | 3.5 | | ns |
| t_{HDRPE} Receive Data Hold After PPI_CLK | 1.5 | | 1.5 | | 1.5 | | ns |
| <i>Switching Characteristics—GP Output and Frame Capture Modes</i> | | | | | | | |
| t_{DFSPE} Internal Frame Sync Delay After PPI_CLK | | 11.0 | | 8.0 | | 8.0 | ns |
| t_{HOFSP} Internal Frame Sync Hold After PPI_CLK | 1.7 | | 1.7 | | 1.7 | | ns |
| t_{DDTPE} Transmit Data Delay After PPI_CLK | | 11.0 | | 9.0 | | 9.0 | ns |
| t_{HDTPE} Transmit Data Hold After PPI_CLK | 1.8 | | 1.8 | | 1.8 | | ns |

¹ PPI_CLK frequency cannot exceed $f_{SCLK}/2$

² Applies when PPI_CONTROL Bit 8 is cleared. See Figure 17 on Page 31 and Figure 20 on Page 32.

³ Applies when PPI_CONTROL Bit 8 is set. See Figure 18 on Page 31 and Figure 21 on Page 33.

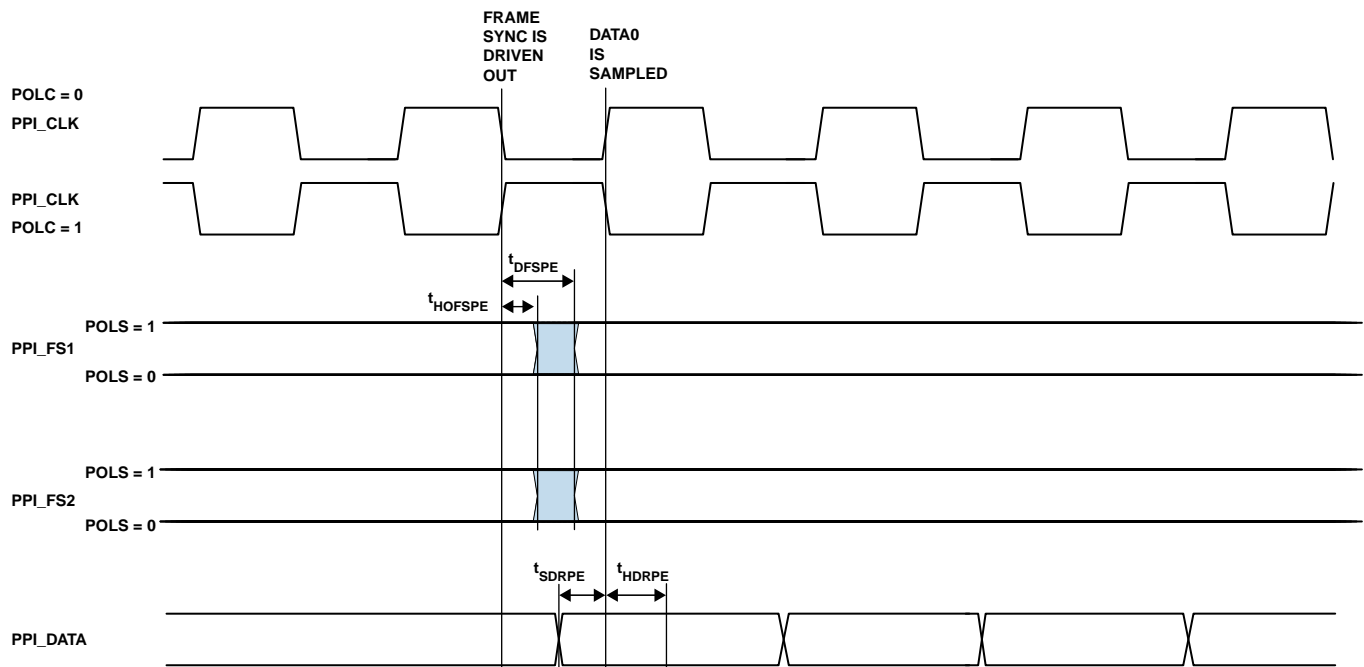


Figure 16. PPI GP Rx Mode with Internal Frame Sync Timing

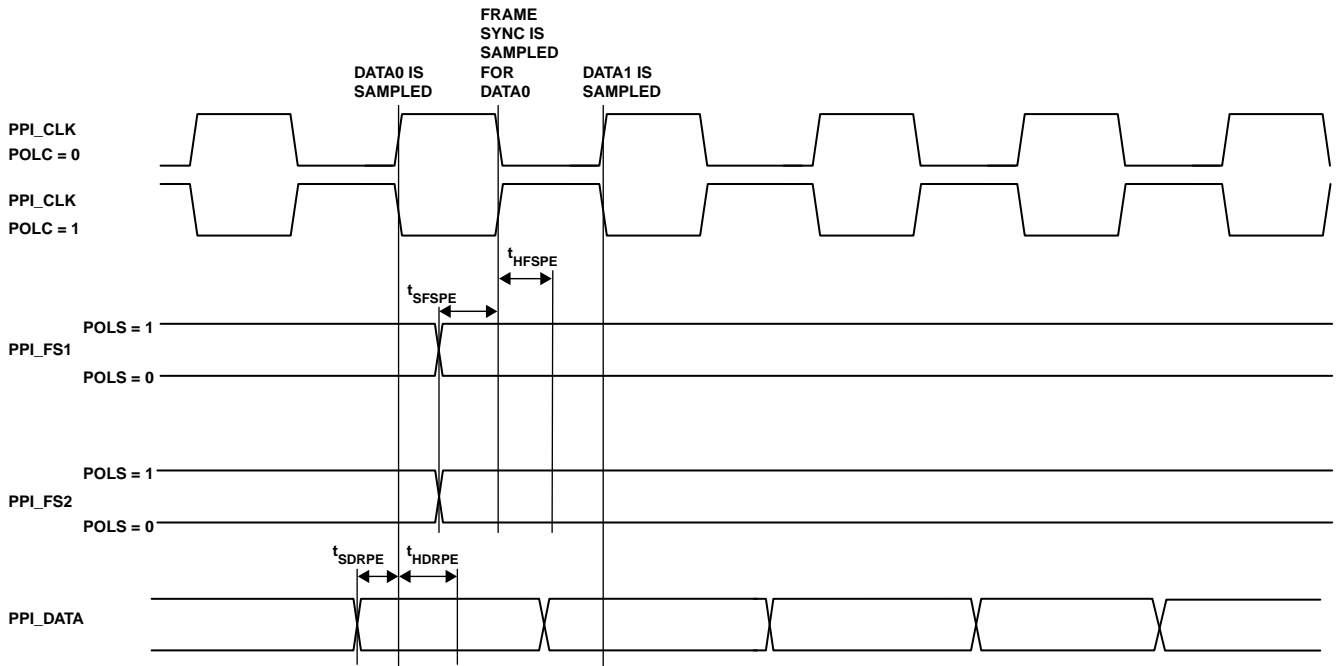


Figure 17. PPI GP Rx Mode with External Frame Sync Timing

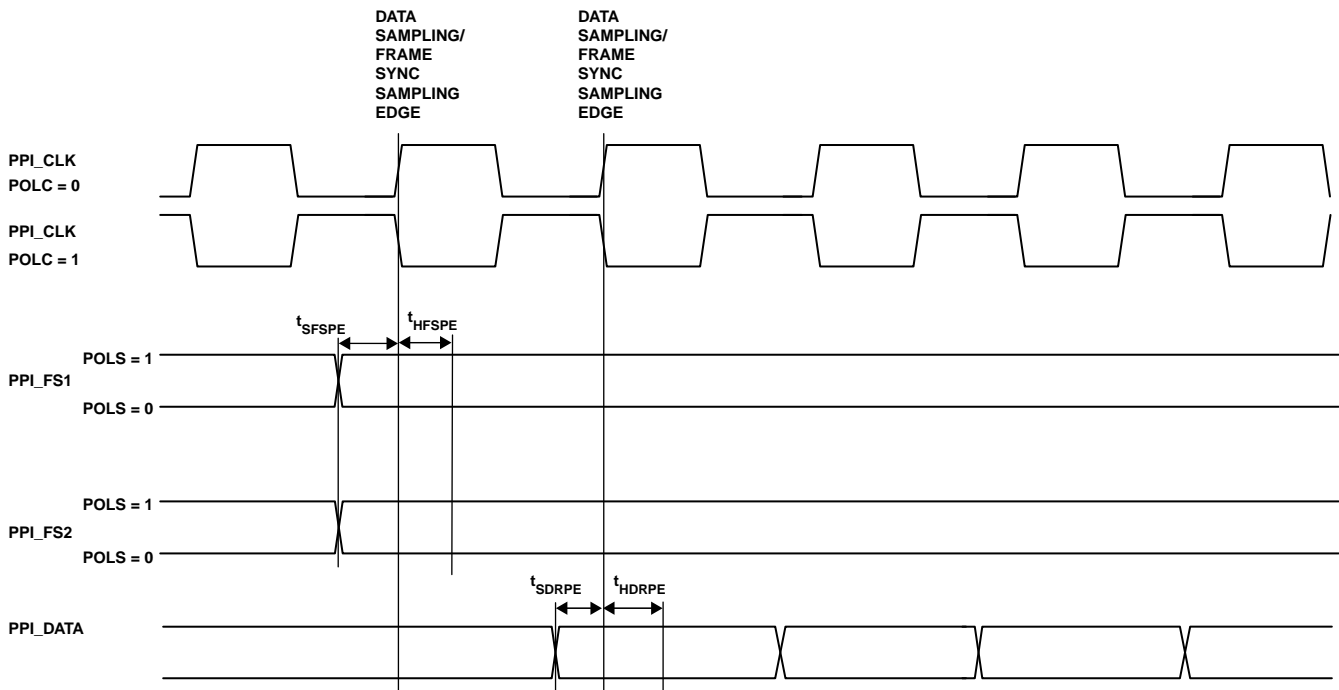


Figure 18. PPI GP Rx Mode with External Frame Sync Timing (Bit 8 of PPI_CONTROL Set)

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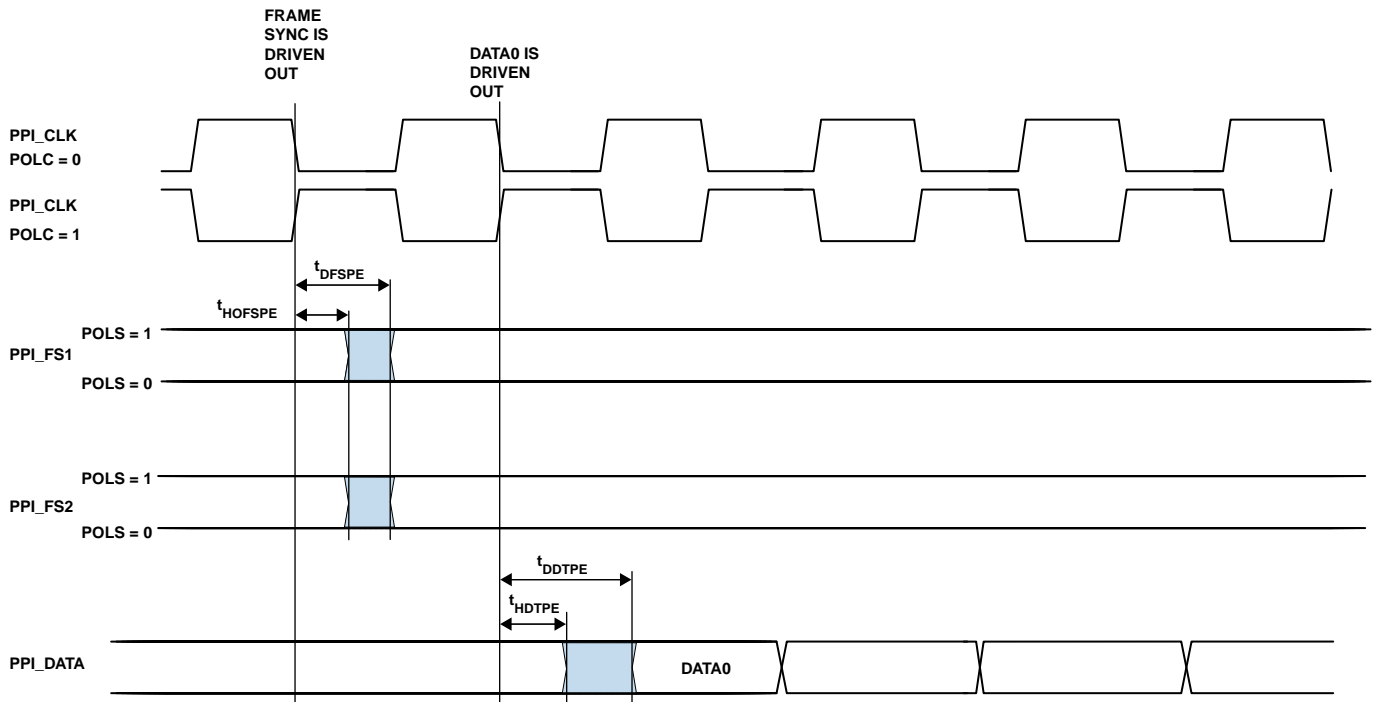


Figure 19. PPI GP Tx Mode with Internal Frame Sync Timing

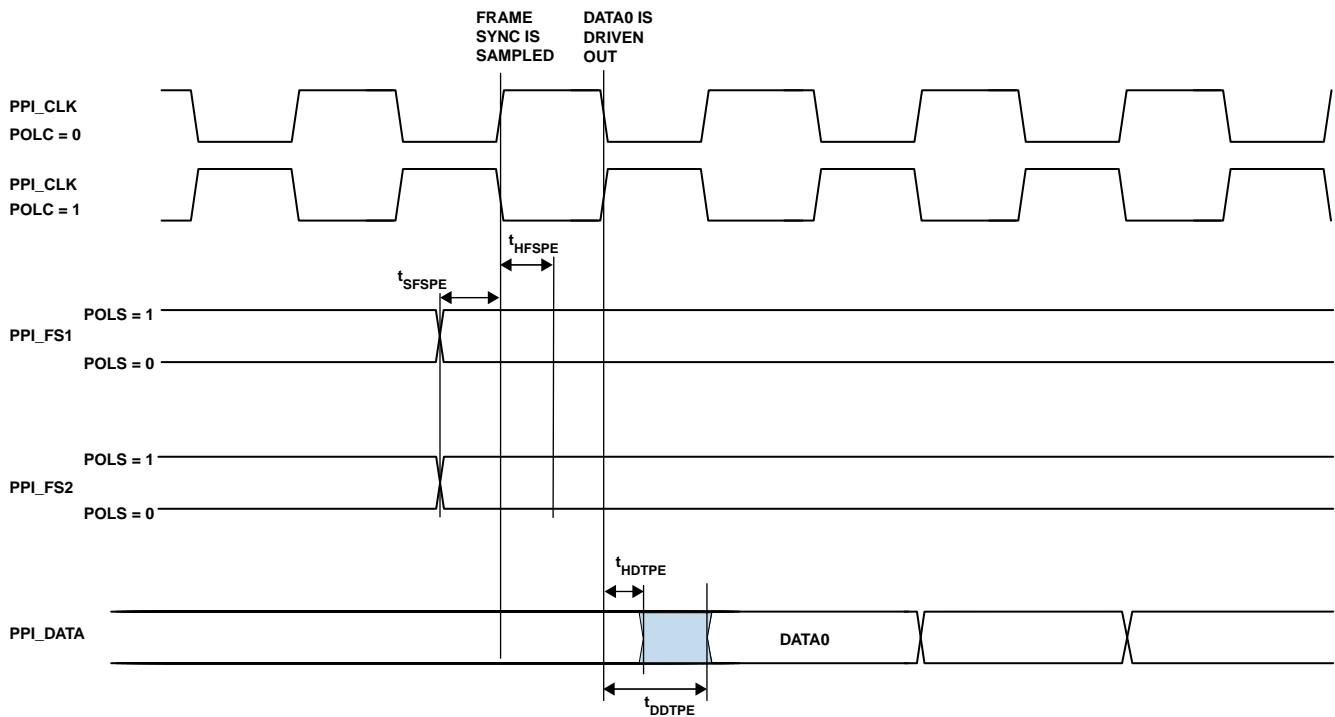


Figure 20. PPI GP Tx Mode with External Frame Sync Timing

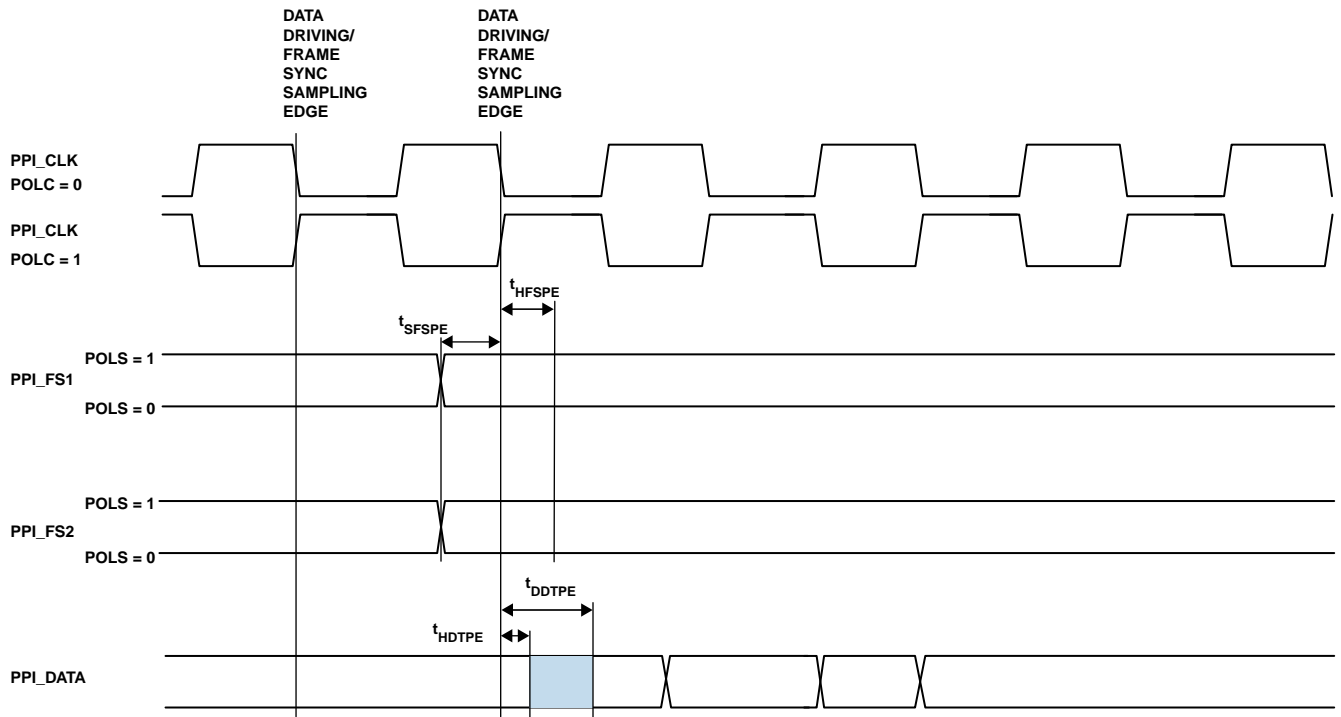


Figure 21. PPI GP Tx Mode with External Frame Sync Timing (Bit 8 of PPI_CONTROL Set)

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Serial Ports

Table 22 through Table 25 on Page 35 and Figure 22 on Page 35 through Figure 23 on Page 36 describe Serial Port operations.

Table 22. Serial Ports—External Clock

| Parameter | V _{DDEXT} = 1.8 V | | V _{DDEXT} = 2.5 V/3.3 V | | Unit |
|---|----------------------------|------|----------------------------------|------|------|
| | Min | Max | Min | Max | |
| <i>Timing Requirements</i> | | | | | |
| t _{SFSE} TFSx/RFSx Setup Before TSCLKx/RSCLKx ¹ | 3.0 | | 3.0 | | ns |
| t _{HFSE} TFSx/RFSx Hold After TSCLKx/RSCLKx ¹ | 3.0 | | 3.0 | | ns |
| t _{SDRE} Receive Data Setup Before RSCLKx ¹ | 3.0 | | 3.0 | | ns |
| t _{HDRE} Receive Data Hold After RSCLKx ¹ | 3.0 | | 3.0 | | ns |
| t _{SCLKEW} TSCLKx/RSCLKx Width | 8.0 | | 4.5 | | ns |
| t _{SCLKE} TSCLKx/RSCLKx Period | 20.0 | | 15.0 ² | | ns |
| <i>Switching Characteristics</i> | | | | | |
| t _{DFSE} TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ³ | | 10.0 | | 10.0 | ns |
| t _{HOFSE} TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ¹ | 0.0 | | 0.0 | | ns |
| t _{DDTE} Transmit Data Delay After TSCLKx ¹ | | 10.0 | | 10.0 | ns |
| t _{HDTE} Transmit Data Hold After TSCLKx ¹ | 0.0 | | 0.0 | | ns |

¹ Referenced to sample edge.

² For receive mode with external RSCLKx and external RFSx only, the maximum specification is 11.11 ns (90 MHz).

³ Referenced to drive edge.

Table 23. Serial Ports—Internal Clock

| Parameter | V _{DDEXT} = 1.8 V LQFP/PBGA Packages | | V _{DDEXT} = 1.8 V MBGA Package | | V _{DDEXT} = 2.5 V/3.3 V All Packages | | Unit |
|---|---|-----|--|-----|--|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| <i>Timing Requirements</i> | | | | | | | |
| t _{SFSI} TFSx/RFSx Setup Before TSCLKx/RSCLKx ¹ | 11.0 | | 11.0 | | 9.0 | | ns |
| t _{HFSI} TFSx/RFSx Hold After TSCLKx/RSCLKx ¹ | -2.0 | | -2.0 | | -2.0 | | ns |
| t _{SDRI} Receive Data Setup Before RSCLKx ¹ | 9.5 | | 9.0 | | 9.0 | | ns |
| t _{HDRI} Receive Data Hold After RSCLKx ¹ | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{SCLKEW} TSCLKx/RSCLKx Width | 4.5 | | 4.5 | | 4.5 | | ns |
| t _{SCLKE} TSCLKx/RSCLKx Period | 20.0 | | 15.0 | | 15.0 | | ns |
| <i>Switching Characteristics</i> | | | | | | | |
| t _{DFSI} TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ² | | 3.0 | | 3.0 | | 3.0 | ns |
| t _{HOFSI} TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ¹ | -1.0 | | -1.0 | | -1.0 | | ns |
| t _{DDTI} Transmit Data Delay After TSCLKx ¹ | | 3.0 | | 3.0 | | 3.0 | ns |
| t _{HDTI} Transmit Data Hold After TSCLKx ¹ | -2.5 | | -2.0 | | -2.0 | | ns |
| t _{SCLKIW} TSCLKx/RSCLKx Width | 6.0 | | 6.0 | | 4.5 | | ns |

¹ Referenced to sample edge.

² Referenced to drive edge.

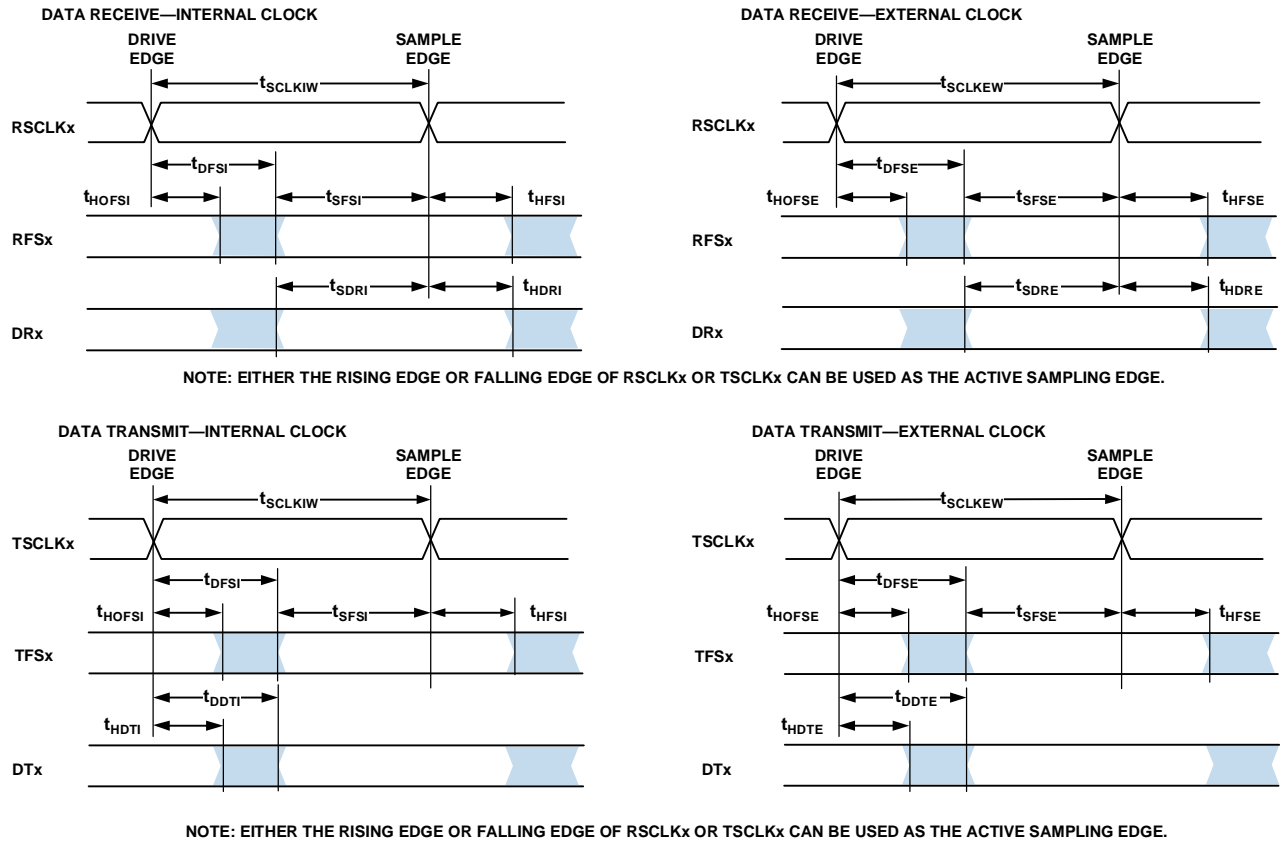


Figure 22. Serial Ports

Table 24. Serial Ports—Enable and Three-State

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ | | Unit |
|---|----------------------------|------|---|------|------|
| | Min | Max | Min | Max | |
| <i>Switching Characteristics</i> | | | | | |
| t_{DTENE} Data Enable Delay from External TSCLKx ¹ | 0 | | 0 | | ns |
| t_{DDTE} Data Disable Delay from External TSCLKx ¹ | | 10.0 | | 10.0 | ns |
| t_{DTENI} Data Enable Delay from Internal TSCLKx ¹ | -2.0 | | -2.0 | | ns |
| t_{DDTI} Data Disable Delay from Internal TSCLKx ¹ | | 3.0 | | 3.0 | ns |

¹Referenced to drive edge.

Table 25. External Late Frame Sync

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ LQFP/PBGA Packages | | $V_{DDEXT} = 1.8\text{ V}$ MBGA Package | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ All Packages | | Unit |
|--|--|------|--|------|---|------|------|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DDTLFSE}$ Data Delay from Late External TFSx or External RFSx with MCE = 1, MFD = 0 ^{1,2} | | 10.5 | | 10.0 | | 10.0 | ns |
| $t_{DTENLFS}$ Data Enable from Late FS or MCE = 1, MFD = 0 ^{1,2} | 0 | | 0 | | 0 | | ns |

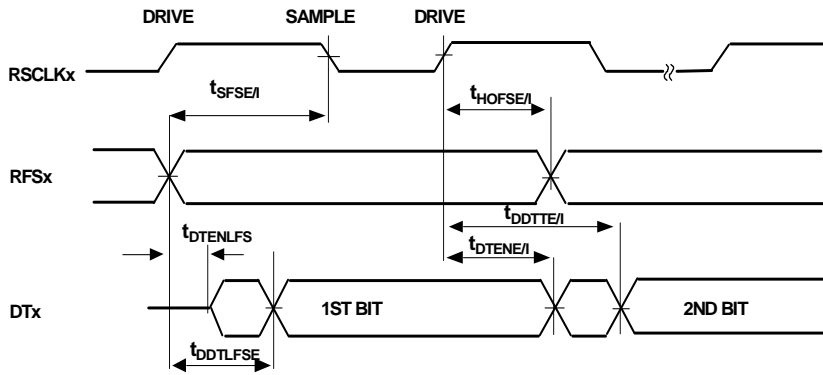
¹MCE = 1, TFSx enable and TFSx valid follow $t_{DTENLFS}$ and $t_{DDTLFSE}$.

²If external RFSx/TFSx setup to RSCLKx/TSCLK x > $t_{SCLKE}/2$, then $t_{DDTE/i}$ and $t_{DTENE/i}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

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EXTERNAL RFSx WITH MCE = 1, MFD = 0



LATE EXTERNAL TFSx

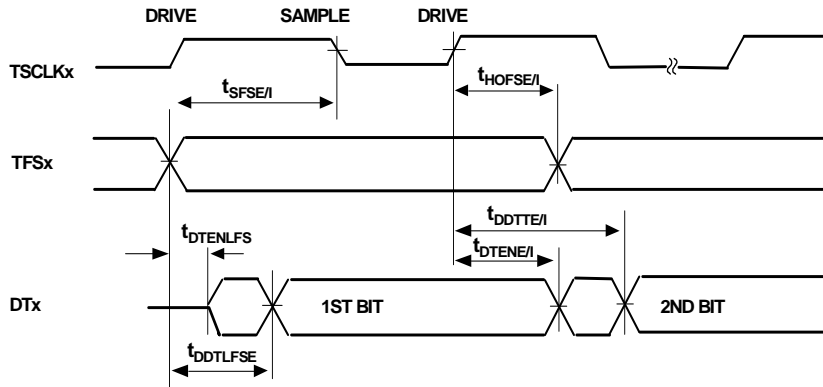


Figure 23. External Late Frame Sync

Serial Peripheral Interface (SPI) Port
—Master Timing

Table 26 and Figure 24 describe SPI port master operations.

Table 26. Serial Peripheral Interface (SPI) Port—Master Timing

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ LQFP/PBGA Packages | | $V_{DDEXT} = 1.8\text{ V}$ MBGA Package | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ All Packages | | Unit |
|--|--|------|--|------|---|------|------|
| | Min | Max | Min | Max | Min | Max | |
| <i>Timing Requirements</i> | | | | | | | |
| t_{SSPIDM} Data Input Valid to SCK Edge (Data Input Setup) | 10.5 | | 8.5 | | 7.5 | | ns |
| t_{HSPIDM} SCK Sampling Edge to Data Input Invalid | -1.5 | | -1.5 | | -1.5 | | ns |
| <i>Switching Characteristics</i> | | | | | | | |
| t_{SDSCIM} $\overline{\text{SPISELx}}$ Low to First SCK Edge | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | ns |
| t_{SPICHM} Serial Clock High Period | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | ns |
| t_{SPICLM} Serial Clock Low Period | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | ns |
| t_{SPICLK} Serial Clock Period | $4t_{SCLK} - 1.5$ | | $4t_{SCLK} - 1.5$ | | $4t_{SCLK} - 1.5$ | | ns |
| t_{HDSTM} Last SCK Edge to $\overline{\text{SPISELx}}$ High | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | ns |
| t_{SPITDM} Sequential Transfer Delay | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | ns |
| $t_{DDSPIDM}$ SCK Edge to Data Out Valid (Data Out Delay) | 0 | 6 | 0 | 6 | 0 | 6 | ns |
| $t_{HDSPIDM}$ SCK Edge to Data Out Invalid (Data Out Hold) | -1.0 | +4.0 | -1.0 | +4.0 | -1.0 | +4.0 | ns |

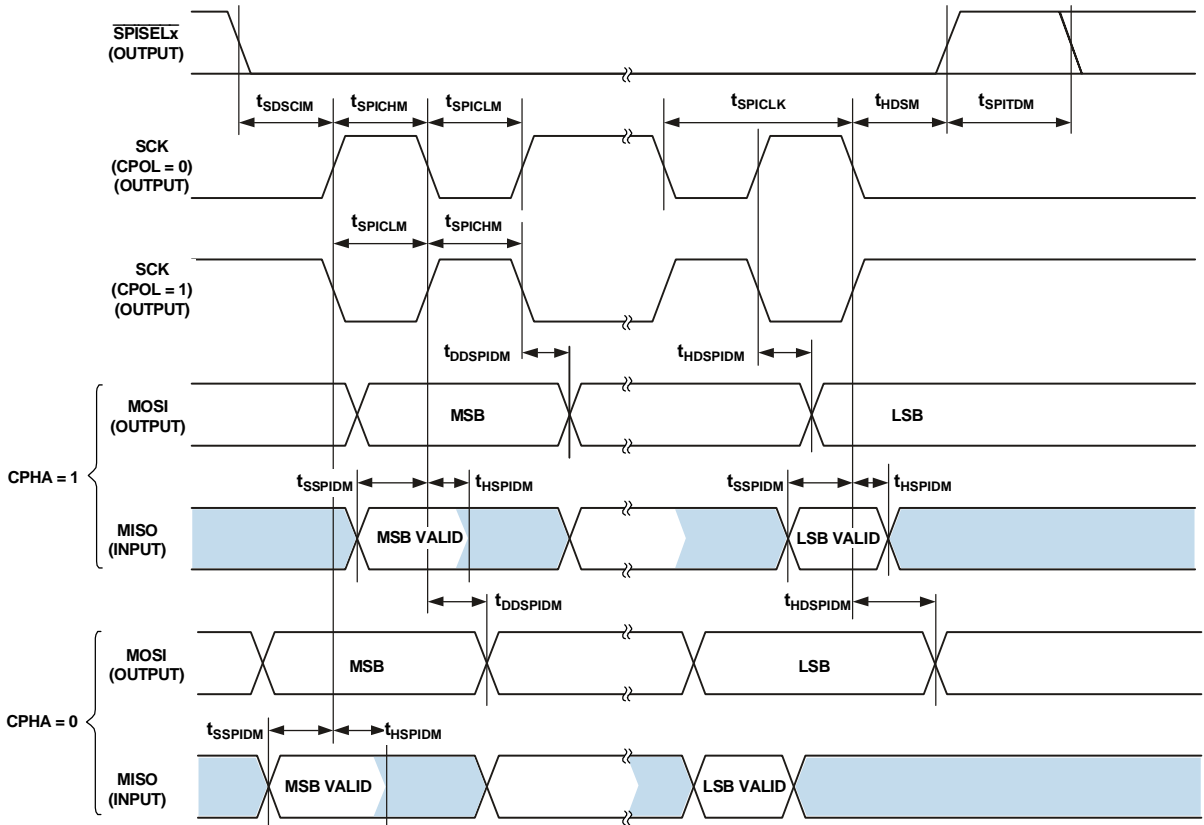


Figure 24. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port —Slave Timing

Table 27 and Figure 25 describe SPI port slave operations.

Table 27. Serial Peripheral Interface (SPI) Port—Slave Timing

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ LQFP/PBGA Packages | | $V_{DDEXT} = 1.8\text{ V}$ MBGA Package | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ All Packages | | Unit |
|--|--|-----|--|-----|---|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| <i>Timing Requirements</i> | | | | | | | |
| t_{SPICHS} Serial Clock High Period | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | ns |
| t_{SPICLS} Serial Clock Low Period | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | ns |
| t_{SPICLK} Serial Clock Period | $4t_{SCLK} - 1.5$ | | $4t_{SCLK} - 1.5$ | | $4t_{SCLK} - 1.5$ | | ns |
| t_{HDS} Last SCK Edge to $\overline{\text{SPISS}}$ Not Asserted | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | ns |
| t_{SPITDS} Sequential Transfer Delay | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | ns |
| t_{SDSCI} $\overline{\text{SPISS}}$ Assertion to First SCK Edge | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | $2t_{SCLK} - 1.5$ | | ns |
| t_{SSPID} Data Input Valid to SCK Edge (Data Input Setup) | 1.6 | | 1.6 | | 1.6 | | ns |
| t_{HSPID} SCK Sampling Edge to Data Input Invalid | 1.6 | | 1.6 | | 1.6 | | ns |
| <i>Switching Characteristics</i> | | | | | | | |
| t_{DSOE} $\overline{\text{SPISS}}$ Assertion to Data Out Active | 0 | 10 | 0 | 9 | 0 | 8 | ns |
| t_{DSDHI} $\overline{\text{SPISS}}$ Deassertion to Data High Impedance | 0 | 10 | 0 | 9 | 0 | 8 | ns |
| t_{DDSPID} SCK Edge to Data Out Valid (Data Out Delay) | 0 | 10 | 0 | 10 | 0 | 10 | ns |
| t_{HDSPID} SCK Edge to Data Out Invalid (Data Out Hold) | 0 | 10 | 0 | 10 | 0 | 10 | ns |

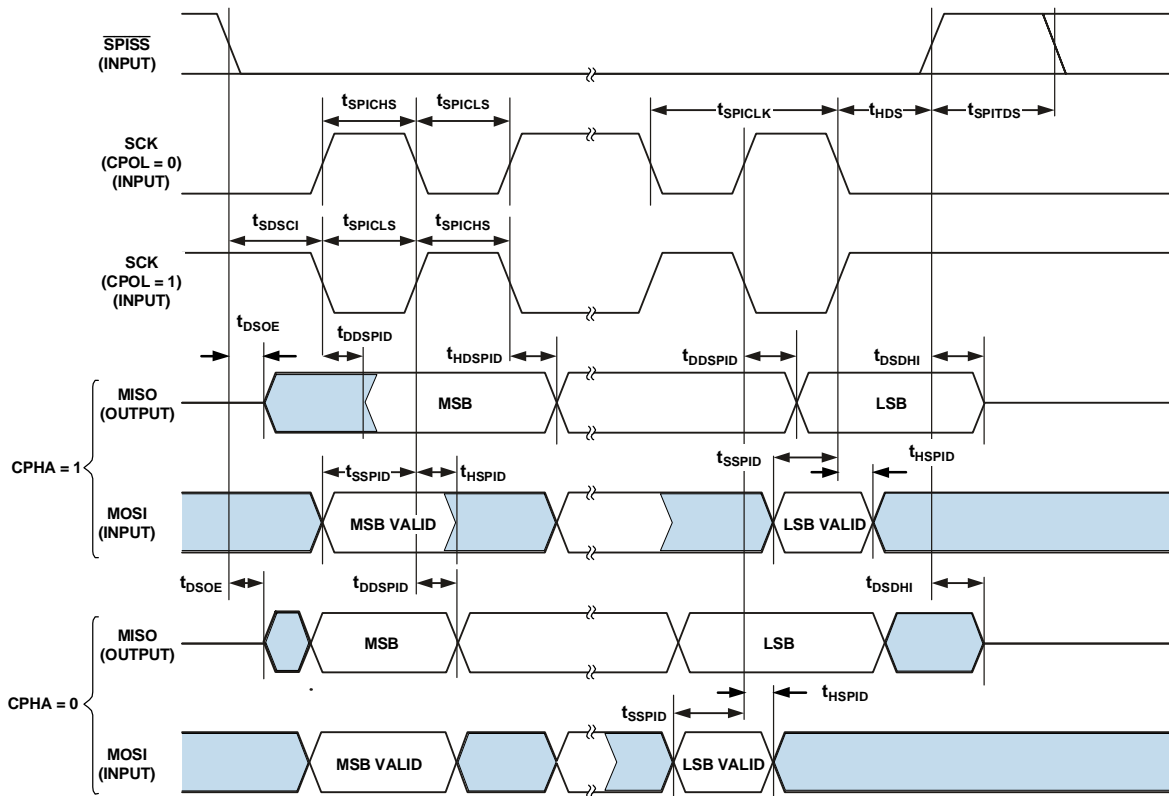


Figure 25. Serial Peripheral Interface (SPI) Port—Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 26 describes UART port receive and transmit operations. The maximum baud rate is SCLK/16. As shown in Figure 26 there is some latency between the generation internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

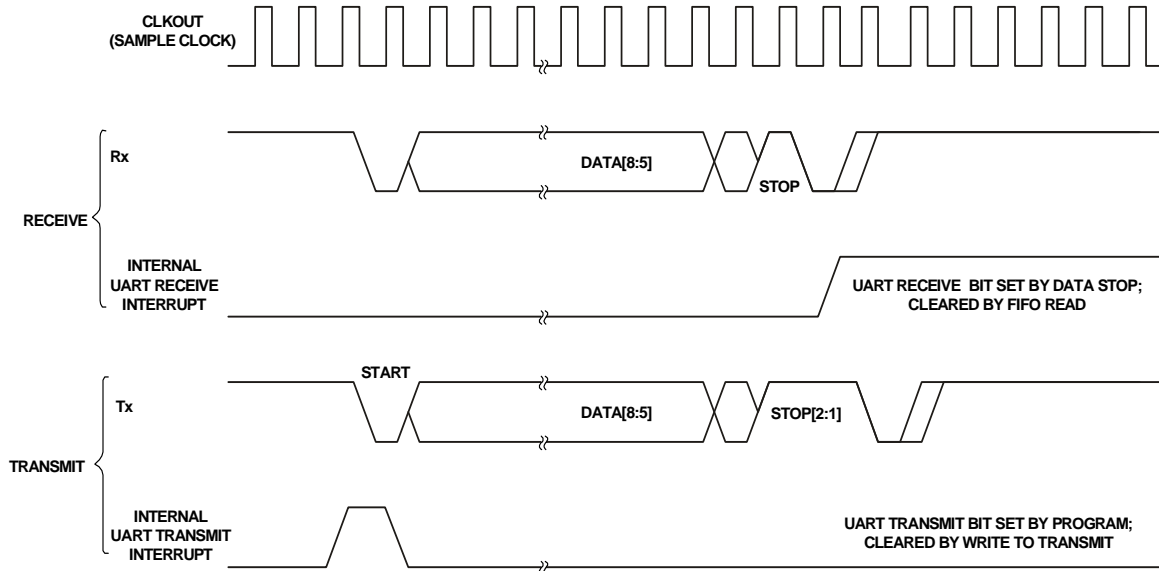


Figure 26. UART Port—Receive and Transmit Timing

ADSP-BF531/ADSP-BF532/ADSP-BF533

[查询"ADSP-BF531SBSTZ400"供应商](#)

General-Purpose I/O Port F Pin Cycle Timing

Table 28 and Figure 27 describe GPIO pin operations.

Table 28. General-Purpose I/O Port F Pin Cycle Timing

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ | | Unit |
|---|----------------------------|-----|---|-----|------|
| | Min | Max | Min | Max | |
| <i>Timing Requirement</i> | | | | | |
| t_{WFI} GPIO Input Pulse Width | $t_{SCLK} + 1$ | | $t_{SCLK} + 1$ | | ns |
| <i>Switching Characteristic</i> | | | | | |
| t_{DFO} GPIO Output Delay from CLKOUT Low | 6 | | 6 | | ns |

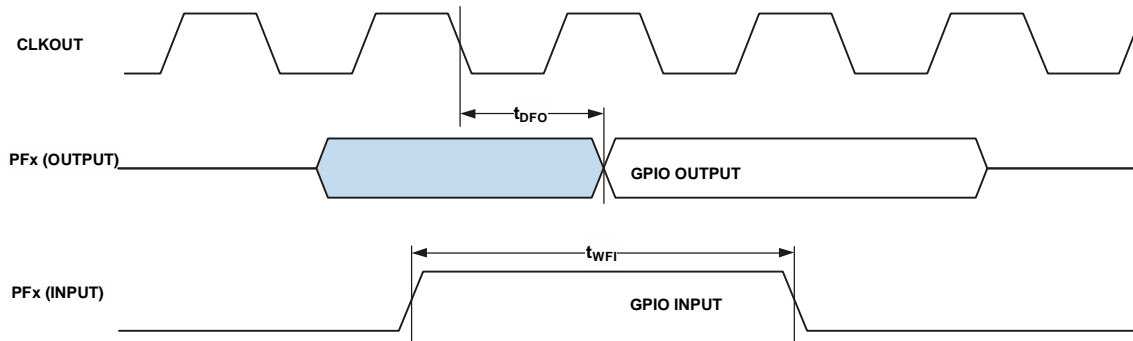


Figure 27. GPIO Cycle Timing

Timer Cycle Timing

Table 29 and Figure 28 describe timer expired operations. The input signal is asynchronous in width capture mode and external clock mode and has an absolute maximum input frequency of $f_{SCLK}/2$ MHz.

Table 29. Timer Cycle Timing

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ | | Unit |
|--|----------------------------|--------------|---|--------------|------|
| | Min | Max | Min | Max | |
| <i>Timing Characteristics</i> | | | | | |
| t_{WL} Timer Pulse Width Input Low ¹ (Measured in SCLK Cycles) | 1 | | 1 | | SCLK |
| t_{WH} Timer Pulse Width Input High ¹ (Measured in SCLK Cycles) | 1 | | 1 | | SCLK |
| <i>Switching Characteristic</i> | | | | | |
| t_{HTO} Timer Pulse Width Output ² (Measured in SCLK Cycles) | 1 | $(2^{32}-1)$ | 1 | $(2^{32}-1)$ | SCLK |

¹ The minimum pulse widths apply for TMRx input pins in width capture and external clock modes. They also apply to the PF1 or PPI_CLK input pins in PWM output mode.

² The minimum time for t_{HTO} is one cycle, and the maximum time for t_{HTO} equals $(2^{32}-1)$ cycles.

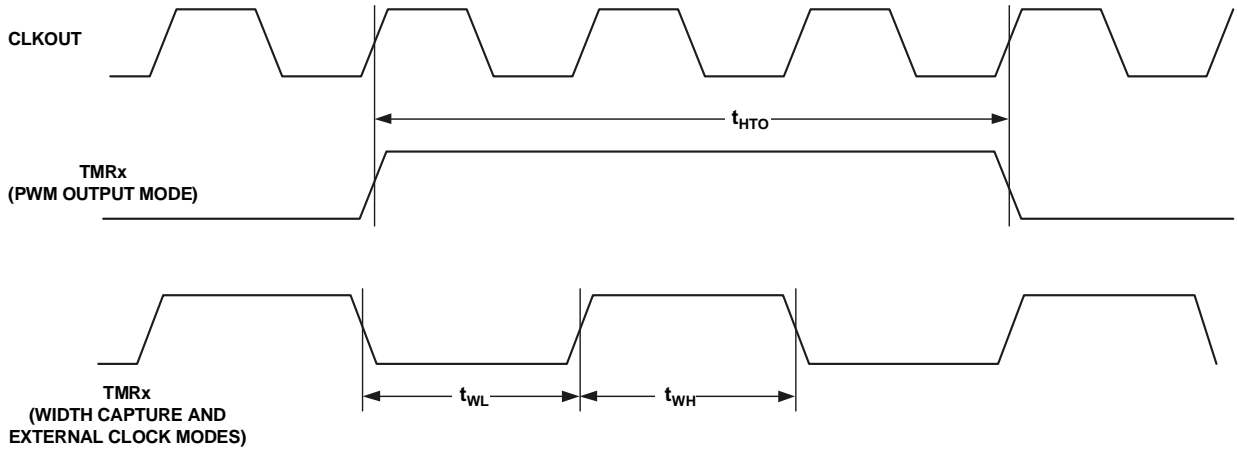


Figure 28. Timer PWM_OUT Cycle Timing

ADSP-BF531/ADSP-BF532/ADSP-BF533

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JTAG Test and Emulation Port Timing

Table 30 and Figure 29 describe JTAG port operations.

Table 30. JTAG Port Timing

| Parameter | $V_{DDEXT} = 1.8\text{ V}$ | | $V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$ | | Unit |
|---|----------------------------|-----|---|-----|------|
| | Min | Max | Min | Max | |
| <i>Timing Requirements</i> | | | | | |
| t_{TCK} TCK Period | 20 | | 20 | | ns |
| t_{STAP} TDI, TMS Setup Before TCK High | 4 | | 4 | | ns |
| t_{HTAP} TDI, TMS Hold After TCK High | 4 | | 4 | | ns |
| t_{SSYS} System Inputs Setup Before TCK High ¹ | 4 | | 4 | | ns |
| t_{HSYS} System Inputs Hold After TCK High ¹ | 5 | | 5 | | ns |
| t_{TRSTW} \overline{TRST} Pulse Width ² (Measured in TCK Cycles) | 4 | | 4 | | TCK |
| <i>Switching Characteristics</i> | | | | | |
| t_{DTDO} TDO Delay from TCK Low | | 10 | | 10 | ns |
| t_{DSYS} System Outputs Delay After TCK Low ³ | 0 | 12 | 0 | 12 | ns |

¹ System Inputs = DATA15–0, ARDY, TMR2–0, PF15–0, PPI_CLK, RSCLK0–1, RFS0–1, DR0PRI, DR0SEC, TSCLK0–1, TFS0–1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, RESET, NMI, BMODE1–0, BR, PP3–0.

² 50 MHz maximum

³ System Outputs = DATA15–0, ADDR19–1, ABE1–0, AOE, ARE, AWE, AMS3–0, SRAS, SCAS, SWE, SCKE, CLKOUT, SA10, SMS, TMR2–0, PF15–0, RSCLK0–1, RFS0–1, TSCLK0–1, TFS0–1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, BG, BGH, PPI3–0.

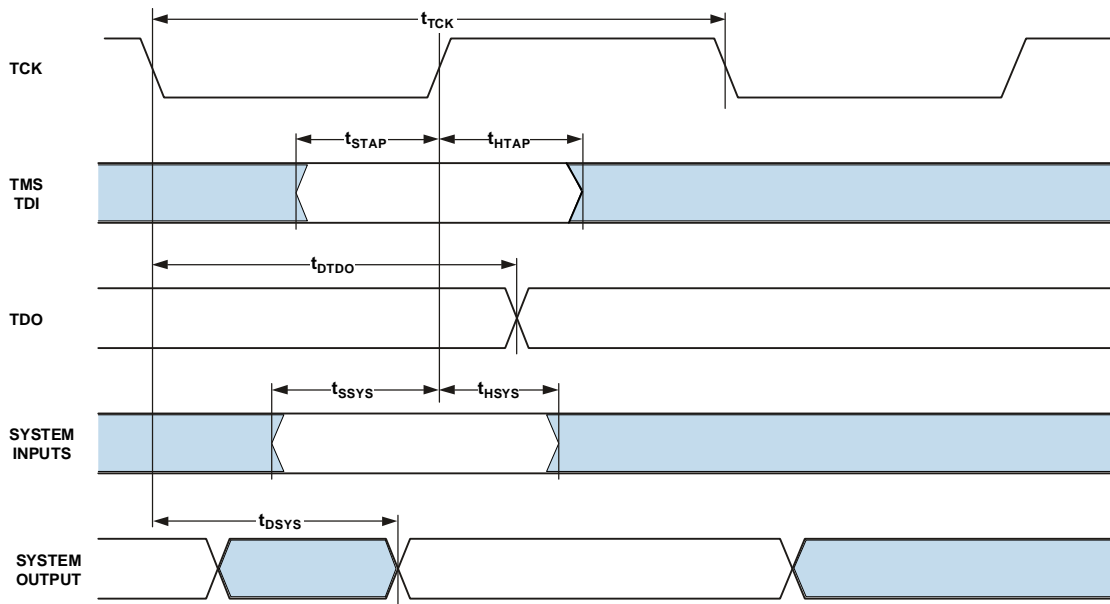


Figure 29. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 30 through Figure 41 show typical current-voltage characteristics for the output drivers of the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor. The curves represent the current drive capability of the output drivers as a function of output voltage.

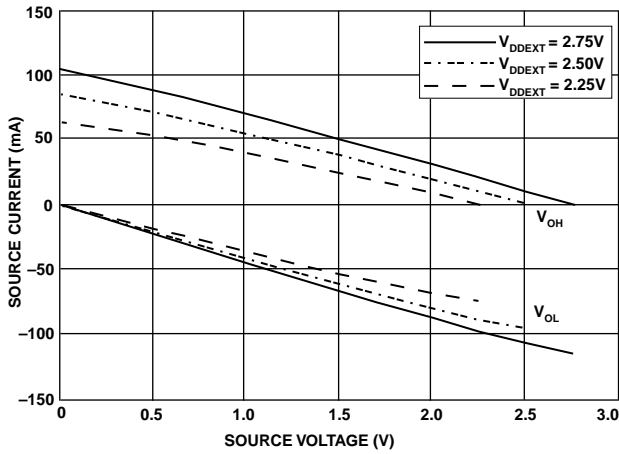


Figure 30. Drive Current A ($V_{DDEXT} = 2.5\text{ V}$)

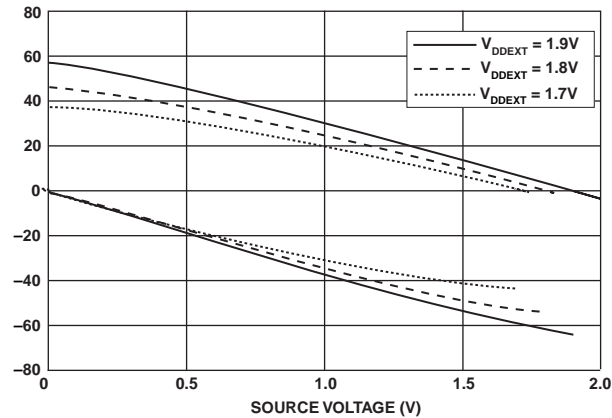


Figure 31. Drive Current A ($V_{DDEXT} = 1.8\text{ V}$)

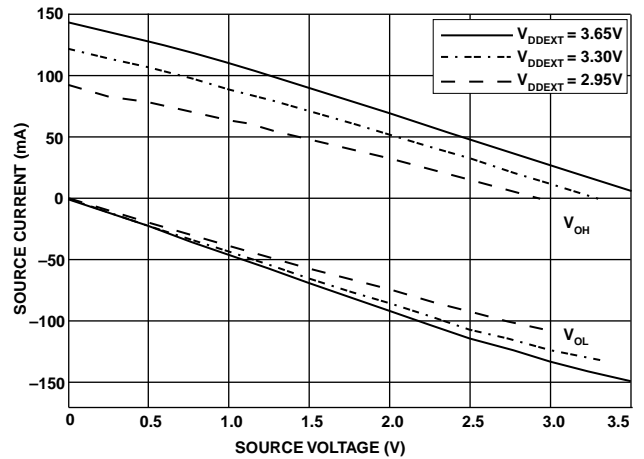


Figure 32. Drive Current A ($V_{DDEXT} = 3.3\text{ V}$)

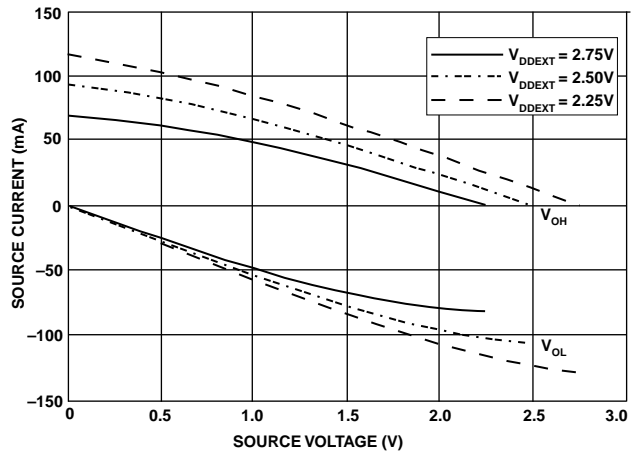


Figure 33. Drive Current B ($V_{DDEXT} = 2.5\text{ V}$)

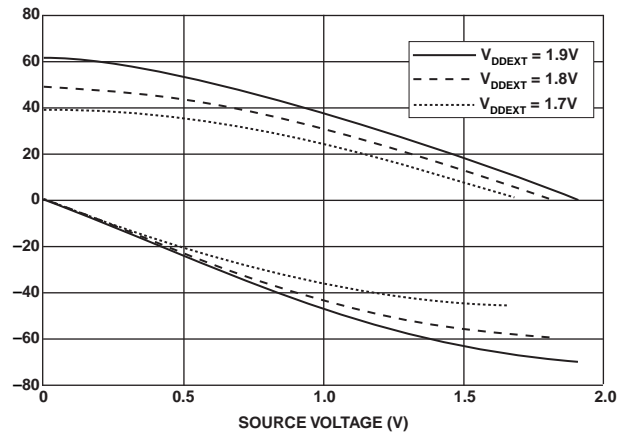


Figure 34. Drive Current B ($V_{DDEXT} = 1.8\text{ V}$)

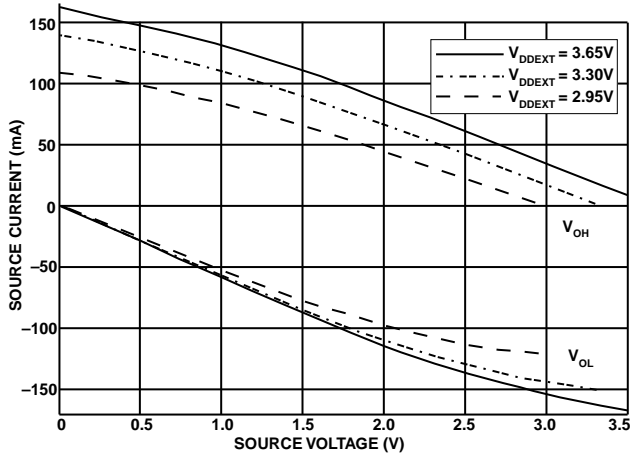


Figure 35. Drive Current B ($V_{DDEXT} = 3.3 V$)

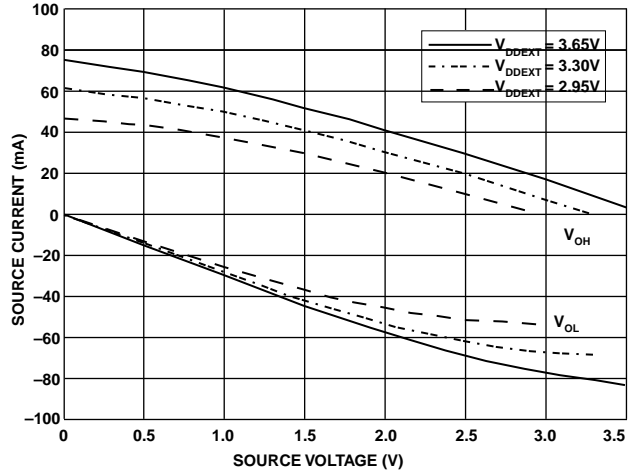


Figure 38. Drive Current C ($V_{DDEXT} = 3.3 V$)

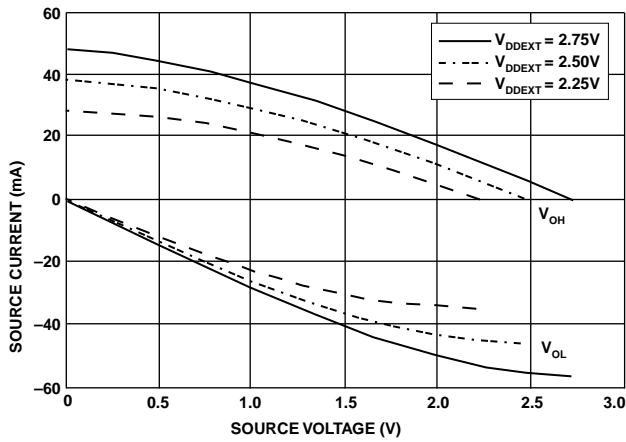


Figure 36. Drive Current C ($V_{DDEXT} = 2.5 V$)

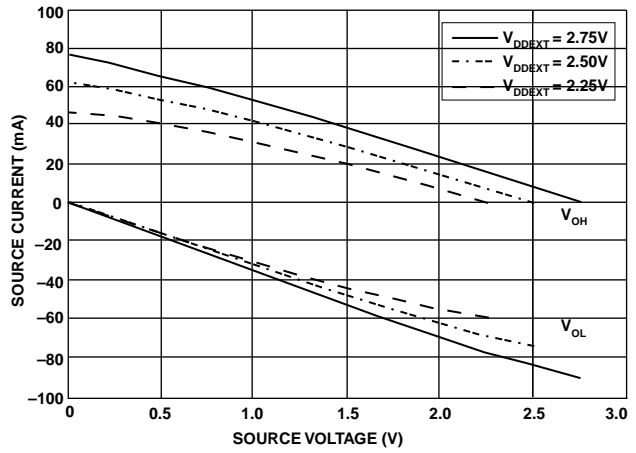


Figure 39. Drive Current D ($V_{DDEXT} = 2.5 V$)

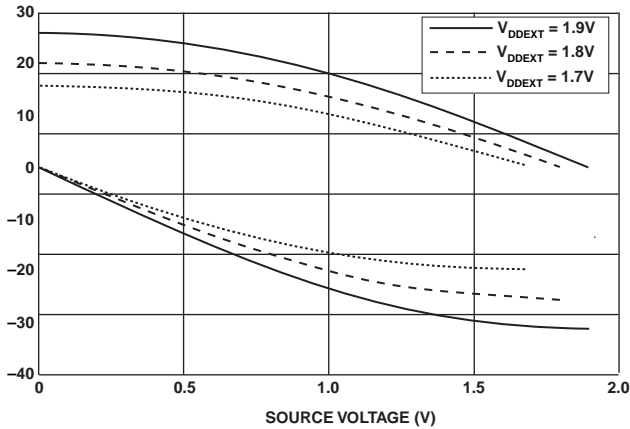


Figure 37. Drive Current C ($V_{DDEXT} = 1.8 V$)

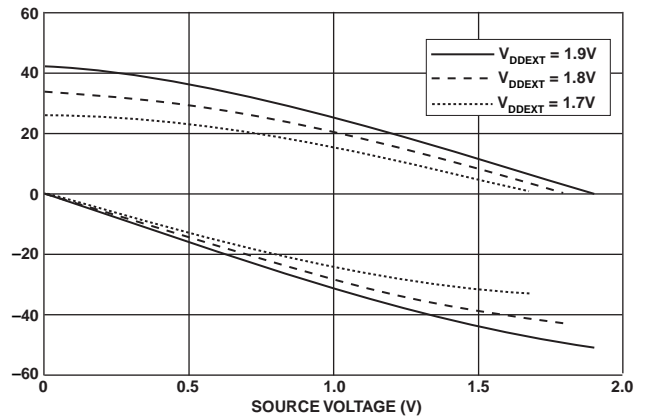


Figure 40. Drive Current D ($V_{DDEXT} = 1.8 V$)

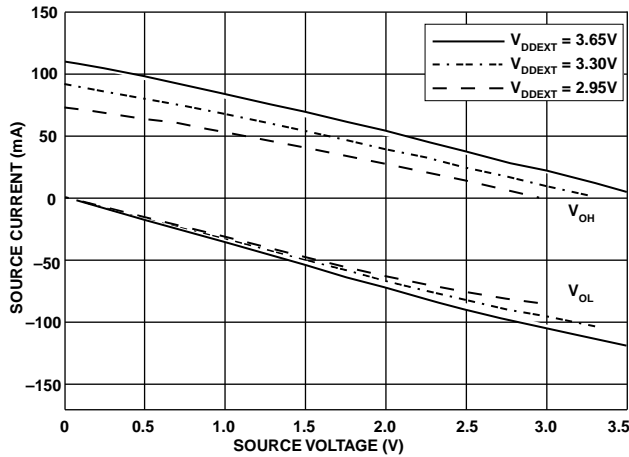


Figure 41. Drive Current D ($V_{DDEXT} = 3.3\text{ V}$)

POWER DISSIPATION

Many operating conditions can affect power dissipation. System designers should refer to *Estimating Power for ADSP-BF531/BF532/BF533 Blackfin Processors (EE-229)* on the Analog Devices website (www.analog.com)—use site search on “EE-229.” This document provides detailed information for optimizing your design for lowest power.

See the *ADSP-BF533 Blackfin Processor Hardware Reference Manual* for definitions of the various operating modes and for instructions on how to minimize system power.

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 42 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.



Figure 42. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 43.

The time $t_{ENA_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches $V_{TRIP(HIGH)}$ or $V_{TRIP(LOW)}$. For V_{DDEXT} (nominal) = 1.8 V— $V_{TRIP(HIGH)}$ is 1.3 V and $V_{TRIP(LOW)}$ is 0.7 V. For V_{DDEXT} (nominal) = 2.5 V/3.3 V—

$V_{TRIP(HIGH)}$ is 2.0 V and $V_{TRIP(LOW)}$ is 1.0 V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the $V_{TRIP(HIGH)}$ or $V_{TRIP(LOW)}$ trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 42.

$$t_{DIS} = t_{DIS_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L . This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V) / I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L , and with ΔV equal to 0.1 V for V_{DDEXT} (nominal) = 1.8 V or 0.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

The time $t_{DIS_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

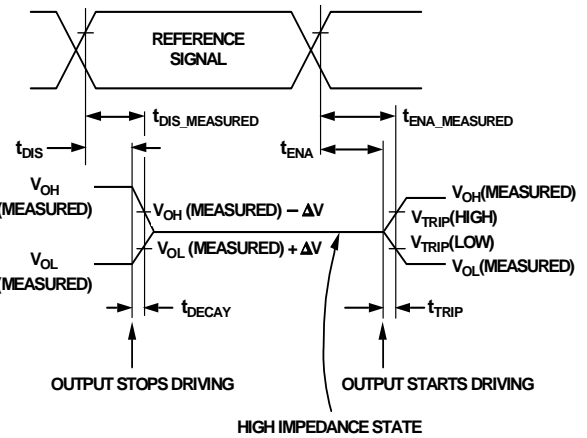


Figure 43. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF531/ADSP-BF532/ADSP-BF533 processor’s output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY}

plus the various output disable times as specified in the [Timing Specifications on Page 24](#) (for example t_{DSDAT} for an SDRAM write cycle as shown in [SDRAM Interface Timing on Page 28](#)).

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see [Figure 44](#)). V_{LOAD} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. [Figure 45](#) through [Figure 56 on Page 48](#) show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

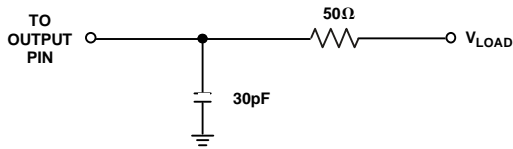


Figure 44. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

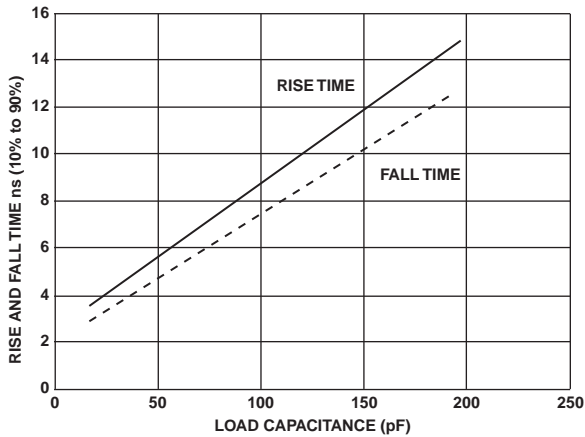


Figure 45. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver A at $V_{\text{DDEXT}} = 1.75 \text{ V}$

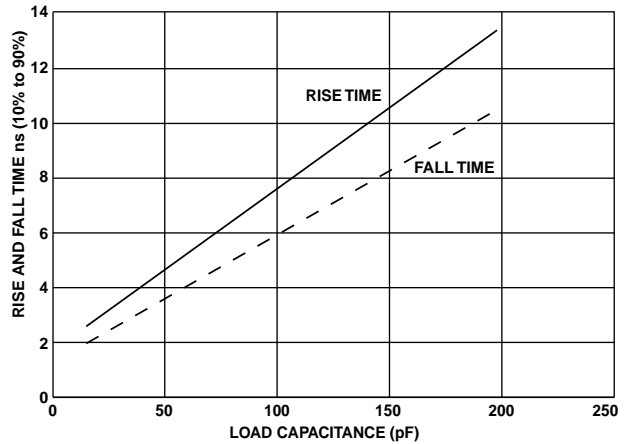


Figure 46. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver A at $V_{\text{DDEXT}} = 2.25 \text{ V}$

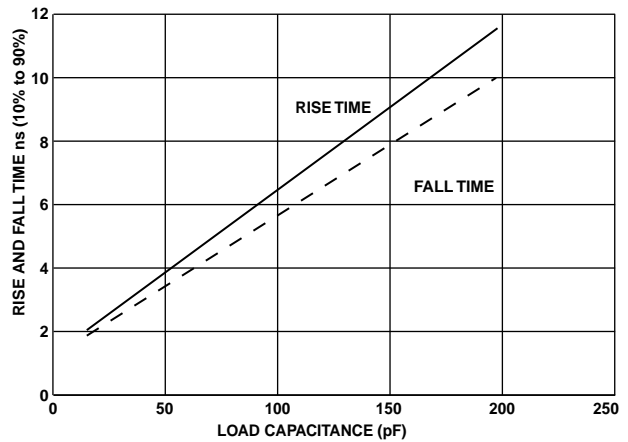


Figure 47. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver A at $V_{\text{DDEXT}} = 3.65 \text{ V}$

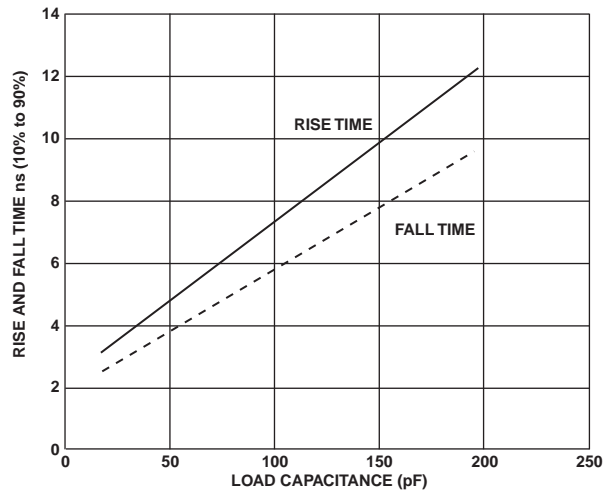


Figure 48. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver B at $V_{\text{DDEXT}} = 1.75 \text{ V}$

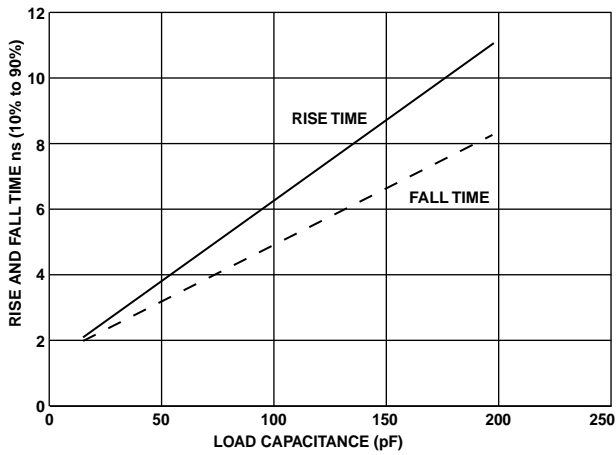


Figure 49. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver B at $V_{DDEXT} = 2.25\text{ V}$

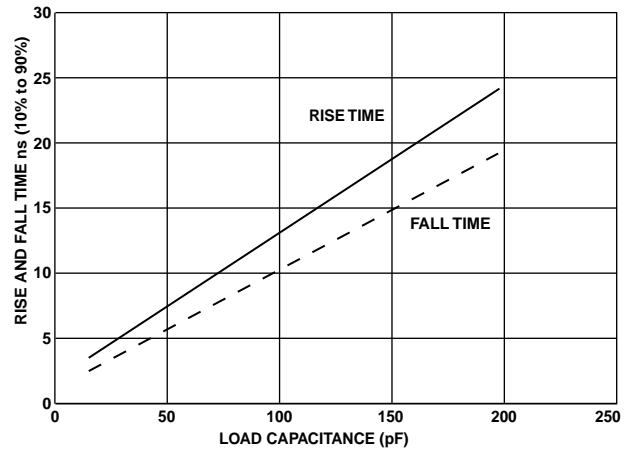


Figure 52. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver C at $V_{DDEXT} = 2.25\text{ V}$

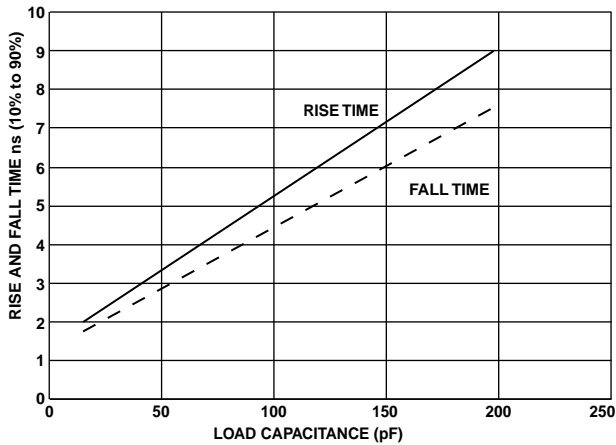


Figure 50. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver B at $V_{DDEXT} = 3.65\text{ V}$

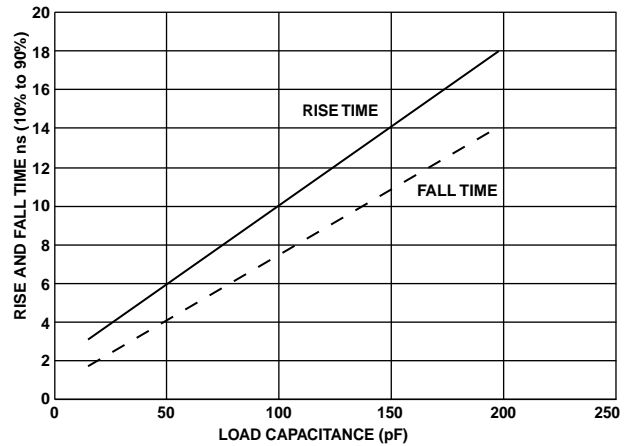


Figure 53. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver C at $V_{DDEXT} = 3.65\text{ V}$

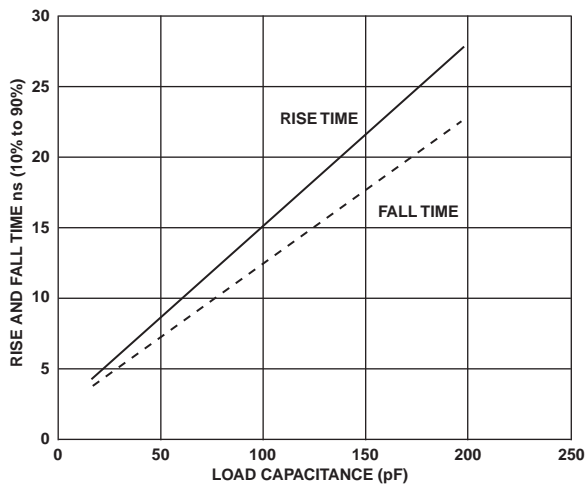


Figure 51. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver C at $V_{DDEXT} = 1.75\text{ V}$

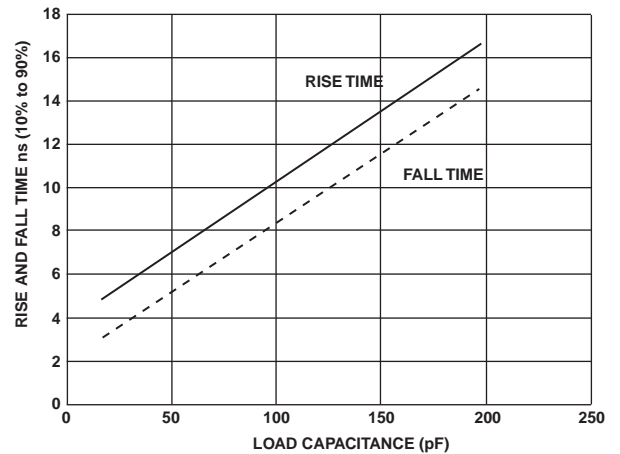


Figure 54. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver D at $V_{DDEXT} = 1.75\text{ V}$

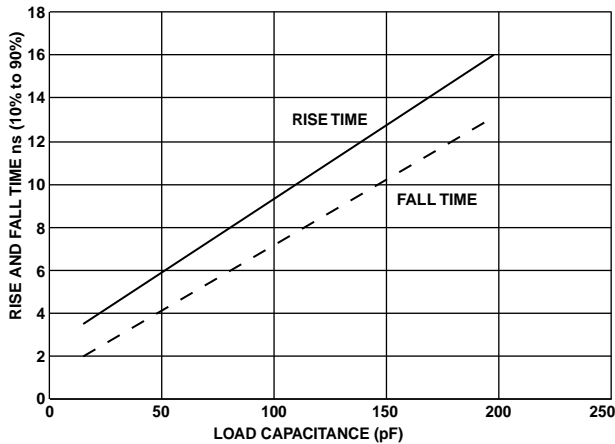


Figure 55. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver D at $V_{DDEXT} = 2.25 V$

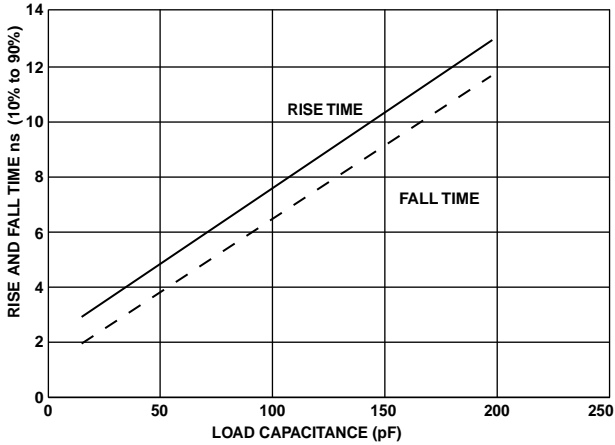


Figure 56. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver D at $V_{DDEXT} = 3.65 V$

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

$$T_j = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_j = junction temperature (°C).

T_{CASE} = case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = from Table 31 through Table 33.

P_D = power dissipation (see Power Dissipation on Page 45 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_j by the equation:

$$T_j = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C).

In Table 31 through Table 33, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance θ_{JA} in Table 31 through Table 33 is the figure of merit relating to performance of the package and board in a convective environment. θ_{JMA} represents the thermal resistance under two conditions of airflow. Ψ_{JT} represents the correlation between T_j and T_{CASE} .

Table 31. Thermal Characteristics for BC-160 Package

| Parameter | Condition | Typical | Unit |
|----------------|----------------------|---------|------|
| θ_{JA} | 0 Linear m/s Airflow | 27.1 | °C/W |
| θ_{JMA} | 1 Linear m/s Airflow | 23.85 | °C/W |
| θ_{JMA} | 2 Linear m/s Airflow | 22.7 | °C/W |
| θ_{JC} | Not Applicable | 7.26 | °C/W |
| Ψ_{JT} | 0 Linear m/s Airflow | 0.14 | °C/W |
| Ψ_{JT} | 1 Linear m/s Airflow | 0.26 | °C/W |
| Ψ_{JT} | 2 Linear m/s Airflow | 0.35 | °C/W |

Table 32. Thermal Characteristics for ST-176-1 Package

| Parameter | Condition | Typical | Unit |
|----------------|----------------------|---------|------|
| θ_{JA} | 0 Linear m/s Airflow | 34.9 | °C/W |
| θ_{JMA} | 1 Linear m/s Airflow | 33.0 | °C/W |
| θ_{JMA} | 2 Linear m/s Airflow | 32.0 | °C/W |
| Ψ_{JT} | 0 Linear m/s Airflow | 0.50 | °C/W |
| Ψ_{JT} | 1 Linear m/s Airflow | 0.75 | °C/W |
| Ψ_{JT} | 2 Linear m/s Airflow | 1.00 | °C/W |

Table 33. Thermal Characteristics for B-169 Package

| Parameter | Condition | Typical | Unit |
|----------------|----------------------|---------|------|
| θ_{JA} | 0 Linear m/s Airflow | 22.8 | °C/W |
| θ_{JMA} | 1 Linear m/s Airflow | 20.3 | °C/W |
| θ_{JMA} | 2 Linear m/s Airflow | 19.3 | °C/W |
| θ_{JC} | Not Applicable | 10.39 | °C/W |
| Ψ_{JT} | 0 Linear m/s Airflow | 0.59 | °C/W |
| Ψ_{JT} | 1 Linear m/s Airflow | 0.88 | °C/W |
| Ψ_{JT} | 2 Linear m/s Airflow | 1.37 | °C/W |

160-BALL BGA BALL ASSIGNMENT

Table 34 lists the BGA ball assignment by signal. Table 35 on Page 50 lists the BGA ball assignment by ball number.

Table 34. 160-Ball CSP_BGA Ball Assignment (Alphabetically by Signal)

| Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. |
|-------------------|----------|------------------|----------|--------------------|----------|-------------------|----------|
| $\overline{ABE0}$ | H13 | DATA4 | N8 | GND | L6 | SCK | D1 |
| $\overline{ABE1}$ | H12 | DATA5 | P8 | GND | L8 | SCKE | B13 |
| ADDR1 | J14 | DATA6 | M7 | GND | L10 | \overline{SMS} | C13 |
| ADDR2 | K14 | DATA7 | N7 | GND | M4 | \overline{SRAS} | D13 |
| ADDR3 | L14 | DATA8 | P7 | GND | M10 | \overline{SWE} | D12 |
| ADDR4 | J13 | DATA9 | M6 | GND | P14 | TCK | P2 |
| ADDR5 | K13 | DATA10 | N6 | MISO | E2 | TDI | M3 |
| ADDR6 | L13 | DATA11 | P6 | MOSI | D3 | TDO | N3 |
| ADDR7 | K12 | DATA12 | M5 | NMI | B10 | TFS0 | H3 |
| ADDR8 | L12 | DATA13 | N5 | PF0 | D2 | TFS1 | E1 |
| ADDR9 | M12 | DATA14 | P5 | PF1 | C1 | TMRO | L2 |
| ADDR10 | M13 | DATA15 | P4 | PF2 | C2 | TMR1 | M1 |
| ADDR11 | M14 | DR0PRI | K1 | PF3 | C3 | TMR2 | K2 |
| ADDR12 | N14 | DROSEC | J2 | PF4 | B1 | TMS | N2 |
| ADDR13 | N13 | DR1PRI | G3 | PF5 | B2 | \overline{TRST} | N1 |
| ADDR14 | N12 | DR1SEC | F3 | PF6 | B3 | TSCLK0 | J1 |
| ADDR15 | M11 | DT0PRI | H1 | PF7 | B4 | TSCLK1 | F1 |
| ADDR16 | N11 | DT0SEC | H2 | PF8 | A2 | TX | K3 |
| ADDR17 | P13 | DT1PRI | F2 | PF9 | A3 | VDDEXT | A1 |
| ADDR18 | P12 | DT1SEC | E3 | PF10 | A4 | VDDEXT | C7 |
| ADDR19 | P11 | \overline{EMU} | M2 | PF11 | A5 | VDDEXT | C12 |
| $\overline{AMS0}$ | E14 | GND | A10 | PF12 | B5 | VDDEXT | D5 |
| $\overline{AMS1}$ | F14 | GND | A14 | PF13 | B6 | VDDEXT | D9 |
| $\overline{AMS2}$ | F13 | GND | B11 | PF14 | A6 | VDDEXT | F12 |
| $\overline{AMS3}$ | G12 | GND | C4 | PF15 | C6 | VDDEXT | G4 |
| \overline{AOE} | G13 | GND | C5 | PPI_CLK | C9 | VDDEXT | J4 |
| ARDY | E13 | GND | C11 | PPI0 | C8 | VDDEXT | J12 |
| \overline{ARE} | G14 | GND | D4 | PPI1 | B8 | VDDEXT | L7 |
| \overline{AWE} | H14 | GND | D7 | PPI2 | A7 | VDDEXT | L11 |
| \overline{BG} | P10 | GND | D8 | PPI3 | B7 | VDDEXT | P1 |
| \overline{BGH} | N10 | GND | D10 | \overline{RESET} | C10 | VDDINT | D6 |
| BMODE0 | N4 | GND | D11 | RFS0 | J3 | VDDINT | E4 |
| BMODE1 | P3 | GND | F4 | RFS1 | G2 | VDDINT | E11 |
| \overline{BR} | D14 | GND | F11 | RSCLK0 | L1 | VDDINT | J11 |
| CLKIN | A12 | GND | G11 | RSCLK1 | G1 | VDDINT | L4 |
| CLKOUT | B14 | GND | H4 | RTXI | A9 | VDDINT | L9 |
| DATA0 | M9 | GND | H11 | RTXO | A8 | VDDRTC | B9 |
| DATA1 | N9 | GND | K4 | RX | L3 | VROUT0 | A13 |
| DATA2 | P9 | GND | K11 | SA10 | E12 | VROUT1 | B12 |
| DATA3 | M8 | GND | L5 | \overline{SCAS} | C14 | XTAL | A11 |

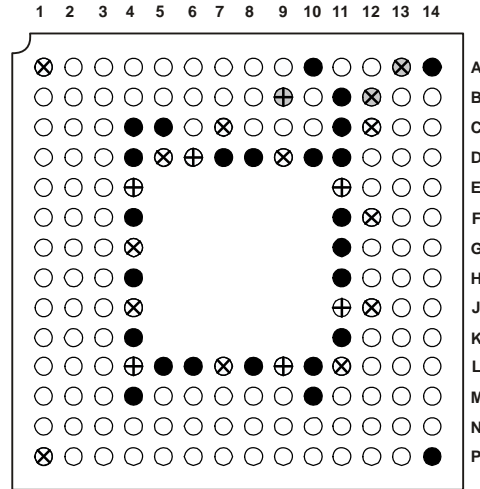
ADSP-BF531/ADSP-BF532/ADSP-BF533

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Table 35. 160-Ball CSP_BGA Ball Assignment (Numerically by Ball Number)

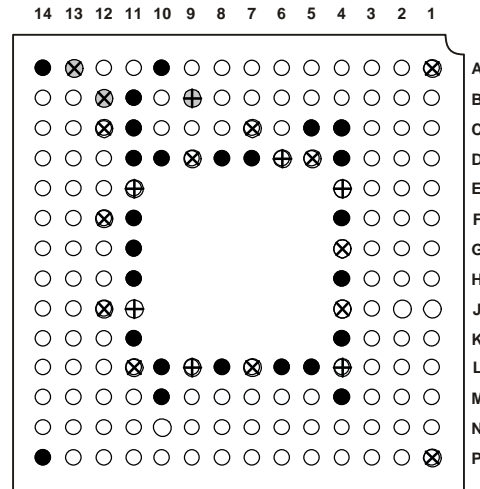
| Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal |
|----------|--------------------|----------|-------------------|----------|-------------------|----------|-------------------|
| A1 | VDDEXT | C13 | \overline{SMS} | H1 | DTOPRI | M3 | TDI |
| A2 | PF8 | C14 | \overline{SCAS} | H2 | DT0SEC | M4 | GND |
| A3 | PF9 | D1 | SCK | H3 | TFS0 | M5 | DATA12 |
| A4 | PF10 | D2 | PF0 | H4 | GND | M6 | DATA9 |
| A5 | PF11 | D3 | MOSI | H11 | GND | M7 | DATA6 |
| A6 | PF14 | D4 | GND | H12 | $\overline{ABE1}$ | M8 | DATA3 |
| A7 | PPI2 | D5 | VDDEXT | H13 | $\overline{ABE0}$ | M9 | DATA0 |
| A8 | RTX0 | D6 | VDDINT | H14 | \overline{AWE} | M10 | GND |
| A9 | RTXI | D7 | GND | J1 | TSCLK0 | M11 | ADDR15 |
| A10 | GND | D8 | GND | J2 | DR0SEC | M12 | ADDR9 |
| A11 | XTAL | D9 | VDDEXT | J3 | RFS0 | M13 | ADDR10 |
| A12 | CLKIN | D10 | GND | J4 | VDDEXT | M14 | ADDR11 |
| A13 | VROUT0 | D11 | GND | J11 | VDDINT | N1 | \overline{TRST} |
| A14 | GND | D12 | \overline{SWE} | J12 | VDDEXT | N2 | TMS |
| B1 | PF4 | D13 | \overline{SRAS} | J13 | ADDR4 | N3 | TDO |
| B2 | PF5 | D14 | \overline{BR} | J14 | ADDR1 | N4 | BMODE0 |
| B3 | PF6 | E1 | TFS1 | K1 | DR0PRI | N5 | DATA13 |
| B4 | PF7 | E2 | MISO | K2 | TMR2 | N6 | DATA10 |
| B5 | PF12 | E3 | DT1SEC | K3 | TX | N7 | DATA7 |
| B6 | PF13 | E4 | VDDINT | K4 | GND | N8 | DATA4 |
| B7 | PPI3 | E11 | VDDINT | K11 | GND | N9 | DATA1 |
| B8 | PPI1 | E12 | SA10 | K12 | ADDR7 | N10 | \overline{BGH} |
| B9 | VDDRTC | E13 | ARDY | K13 | ADDR5 | N11 | ADDR16 |
| B10 | NMI | E14 | $\overline{AMS0}$ | K14 | ADDR2 | N12 | ADDR14 |
| B11 | GND | F1 | TSCLK1 | L1 | RSCLK0 | N13 | ADDR13 |
| B12 | VROUT1 | F2 | DT1PRI | L2 | TMR0 | N14 | ADDR12 |
| B13 | SCKE | F3 | DR1SEC | L3 | RX | P1 | VDDEXT |
| B14 | CLKOUT | F4 | GND | L4 | VDDINT | P2 | TCK |
| C1 | PF1 | F11 | GND | L5 | GND | P3 | BMODE1 |
| C2 | PF2 | F12 | VDDEXT | L6 | GND | P4 | DATA15 |
| C3 | PF3 | F13 | $\overline{AMS2}$ | L7 | VDDEXT | P5 | DATA14 |
| C4 | GND | F14 | $\overline{AMS1}$ | L8 | GND | P6 | DATA11 |
| C5 | GND | G1 | RSCLK1 | L9 | VDDINT | P7 | DATA8 |
| C6 | PF15 | G2 | RFS1 | L10 | GND | P8 | DATA5 |
| C7 | VDDEXT | G3 | DR1PRI | L11 | VDDEXT | P9 | DATA2 |
| C8 | PPI0 | G4 | VDDEXT | L12 | ADDR8 | P10 | \overline{BG} |
| C9 | PPI_CLK | G11 | GND | L13 | ADDR6 | P11 | ADDR19 |
| C10 | \overline{RESET} | G12 | $\overline{AMS3}$ | L14 | ADDR3 | P12 | ADDR18 |
| C11 | GND | G13 | \overline{AOE} | M1 | TMR1 | P13 | ADDR17 |
| C12 | VDDEXT | G14 | \overline{ARE} | M2 | \overline{EMU} | P14 | GND |

Figure 57 lists the top view of the BGA ball configuration.
 Figure 58 lists the bottom view of the BGA ball configuration.



KEY:
 ⊕ V_{DDINT} ● GND ⊕ V_{DDRTC}
 ⊗ V_{DDEXT} ○ I/O ⊗ V_{ROUT}

Figure 57. 160-Ball CSP_BGA Ground Configuration (Top View)



KEY:
 ⊕ V_{DDINT} ● GND ⊕ V_{DDRTC}
 ⊗ V_{DDEXT} ○ I/O ⊗ V_{ROUT}

Figure 58. 160-Ball CSP_BGA Ground Configuration (Bottom View)

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169-BALL PBGA BALL ASSIGNMENT

Table 36 lists the PBGA ball assignment by signal. Table 37 on

Page 53 lists the PBGA ball assignment by ball number.

Table 36. 169-Ball PBGA Ball Assignment (Alphabetically by Signal)

| Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. |
|-------------------|----------|------------------|----------|--------------------|----------|-------------------|----------|--------|----------|
| $\overline{ABE0}$ | H16 | DATA4 | U12 | GND | K9 | RTXI | A10 | VDDEXT | K6 |
| $\overline{ABE1}$ | H17 | DATA5 | U11 | GND | K10 | RTXO | A11 | VDDEXT | L6 |
| ADDR1 | J16 | DATA6 | T10 | GND | K11 | RX | T1 | VDDEXT | M6 |
| ADDR2 | J17 | DATA7 | U10 | GND | L7 | SA10 | B15 | VDDEXT | M7 |
| ADDR3 | K16 | DATA8 | T9 | GND | L8 | \overline{SCAS} | A16 | VDDEXT | M8 |
| ADDR4 | K17 | DATA9 | U9 | GND | L9 | SCK | D1 | VDDEXT | T2 |
| ADDR5 | L16 | DATA10 | T8 | GND | L10 | SCKE | B14 | VROUT0 | B12 |
| ADDR6 | L17 | DATA11 | U8 | GND | L11 | \overline{SMS} | A17 | VROUT1 | B13 |
| ADDR7 | M16 | DATA12 | U7 | GND | M9 | \overline{SRAS} | A15 | XTAL | A13 |
| ADDR8 | M17 | DATA13 | T7 | GND | T16 | \overline{SWE} | B17 | | |
| ADDR9 | N17 | DATA14 | U6 | MISO | E2 | TCK | U4 | | |
| ADDR10 | N16 | DATA15 | T6 | MOSI | E1 | TDI | U3 | | |
| ADDR11 | P17 | DR0PRI | M2 | NMI | B11 | TDO | T4 | | |
| ADDR12 | P16 | DR0SEC | M1 | PF0 | D2 | TFS0 | L1 | | |
| ADDR13 | R17 | DR1PRI | H1 | PF1 | C1 | TFS1 | G2 | | |
| ADDR14 | R16 | DR1SEC | H2 | PF2 | B1 | TMR0 | R1 | | |
| ADDR15 | T17 | DT0PRI | K2 | PF3 | C2 | TMR1 | P2 | | |
| ADDR16 | U15 | DT0SEC | K1 | PF4 | A1 | TMR2 | P1 | | |
| ADDR17 | T15 | DT1PRI | F1 | PF5 | A2 | TMS | T3 | | |
| ADDR18 | U16 | DT1SEC | F2 | PF6 | B3 | \overline{TRST} | U2 | | |
| ADDR19 | T14 | \overline{EMU} | U1 | PF7 | A3 | TSCLK0 | L2 | | |
| $\overline{AMS0}$ | D17 | GND | B16 | PF8 | B4 | TSCLK1 | G1 | | |
| $\overline{AMS1}$ | E16 | GND | F11 | PF9 | A4 | TX | R2 | | |
| $\overline{AMS2}$ | E17 | GND | G7 | PF10 | B5 | VDD | F12 | | |
| $\overline{AMS3}$ | F16 | GND | G8 | PF11 | A5 | VDD | G12 | | |
| \overline{AOE} | F17 | GND | G9 | PF12 | A6 | VDD | H12 | | |
| ARDY | C16 | GND | G10 | PF13 | B6 | VDD | J12 | | |
| \overline{ARE} | G16 | GND | G11 | PF14 | A7 | VDD | K12 | | |
| \overline{AWE} | G17 | GND | H7 | PF15 | B7 | VDD | L12 | | |
| \overline{BG} | T13 | GND | H8 | PPI_CLK | B10 | VDD | M10 | | |
| \overline{BGH} | U17 | GND | H9 | PPI0 | B9 | VDD | M11 | | |
| BMODE0 | U5 | GND | H10 | PPI1 | A9 | VDD | M12 | | |
| BMODE1 | T5 | GND | H11 | PPI2 | B8 | VDDEXT | B2 | | |
| \overline{BR} | C17 | GND | J7 | PPI3 | A8 | VDDEXT | F6 | | |
| CLKIN | A14 | GND | J8 | \overline{RESET} | A12 | VDDEXT | F7 | | |
| CLKOUT | D16 | GND | J9 | RFS0 | N1 | VDDEXT | F8 | | |
| DATA0 | U14 | GND | J10 | RFS1 | J1 | VDDEXT | F9 | | |
| DATA1 | T12 | GND | J11 | RSCLK0 | N2 | VDDEXT | G6 | | |
| DATA2 | U13 | GND | K7 | RSCLK1 | J2 | VDDEXT | H6 | | |
| DATA3 | T11 | GND | K8 | RTCVD | F10 | VDDEXT | J6 | | |

Table 37. 169-Ball PBGA Ball Assignment (Numerically by Ball Number)

| Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal |
|----------|---------|----------|--------|----------|--------|----------|--------|----------|--------|
| A1 | PF4 | D16 | CLKOUT | J2 | RSCLK1 | M12 | VDD | U9 | DATA9 |
| A2 | PF5 | D17 | AMS0 | J6 | VDDEXT | M16 | ADDR7 | U10 | DATA7 |
| A3 | PF7 | E1 | MOSI | J7 | GND | M17 | ADDR8 | U11 | DATA5 |
| A4 | PF9 | E2 | MISO | J8 | GND | N1 | RFS0 | U12 | DATA4 |
| A5 | PF11 | E16 | AMS1 | J9 | GND | N2 | RSCLK0 | U13 | DATA2 |
| A6 | PF12 | E17 | AMS2 | J10 | GND | N16 | ADDR10 | U14 | DATA0 |
| A7 | PF14 | F1 | DT1PRI | J11 | GND | N17 | ADDR9 | U15 | ADDR16 |
| A8 | PPI3 | F2 | DT1SEC | J12 | VDD | P1 | TMR2 | U16 | ADDR18 |
| A9 | PPI1 | F6 | VDDEXT | J16 | ADDR1 | P2 | TMR1 | U17 | BGH |
| A10 | RTXI | F7 | VDDEXT | J17 | ADDR2 | P16 | ADDR12 | | |
| A11 | RTXO | F8 | VDDEXT | K1 | DT0SEC | P17 | ADDR11 | | |
| A12 | RESET | F9 | VDDEXT | K2 | DT0PRI | R1 | TMR0 | | |
| A13 | XTAL | F10 | RTCVDD | K6 | VDDEXT | R2 | TX | | |
| A14 | CLKIN | F11 | GND | K7 | GND | R16 | ADDR14 | | |
| A15 | SRAS | F12 | VDD | K8 | GND | R17 | ADDR13 | | |
| A16 | SCAS | F16 | AMS3 | K9 | GND | T1 | RX | | |
| A17 | SMS | F17 | AOE | K10 | GND | T2 | VDDEXT | | |
| B1 | PF2 | G1 | TSCLK1 | K11 | GND | T3 | TMS | | |
| B2 | VDDEXT | G2 | TFS1 | K12 | VDD | T4 | TDO | | |
| B3 | PF6 | G6 | VDDEXT | K16 | ADDR3 | T5 | BMODE1 | | |
| B4 | PF8 | G7 | GND | K17 | ADDR4 | T6 | DATA15 | | |
| B5 | PF10 | G8 | GND | L1 | TFS0 | T7 | DATA13 | | |
| B6 | PF13 | G9 | GND | L2 | TSCLK0 | T8 | DATA10 | | |
| B7 | PF15 | G10 | GND | L6 | VDDEXT | T9 | DATA8 | | |
| B8 | PPI2 | G11 | GND | L7 | GND | T10 | DATA6 | | |
| B9 | PPI0 | G12 | VDD | L8 | GND | T11 | DATA3 | | |
| B10 | PPI_CLK | G16 | ARE | L9 | GND | T12 | DATA1 | | |
| B11 | NMI | G17 | AWE | L10 | GND | T13 | BG | | |
| B12 | VROUT0 | H1 | DR1PRI | L11 | GND | T14 | ADDR19 | | |
| B13 | VROUT1 | H2 | DR1SEC | L12 | VDD | T15 | ADDR17 | | |
| B14 | SCKE | H6 | VDDEXT | L16 | ADDR5 | T16 | GND | | |
| B15 | SA10 | H7 | GND | L17 | ADDR6 | T17 | ADDR15 | | |
| B16 | GND | H8 | GND | M1 | DR0SEC | U1 | EMU | | |
| B17 | SWE | H9 | GND | M2 | DR0PRI | U2 | TRST | | |
| C1 | PF1 | H10 | GND | M6 | VDDEXT | U3 | TDI | | |
| C2 | PF3 | H11 | GND | M7 | VDDEXT | U4 | TCK | | |
| C16 | ARDY | H12 | VDD | M8 | VDDEXT | U5 | BMODE0 | | |
| C17 | BR | H16 | ABE0 | M9 | GND | U6 | DATA14 | | |
| D1 | SCK | H17 | ABE1 | M10 | VDD | U7 | DATA12 | | |
| D2 | PF0 | J1 | RFS1 | M11 | VDD | U8 | DATA11 | | |

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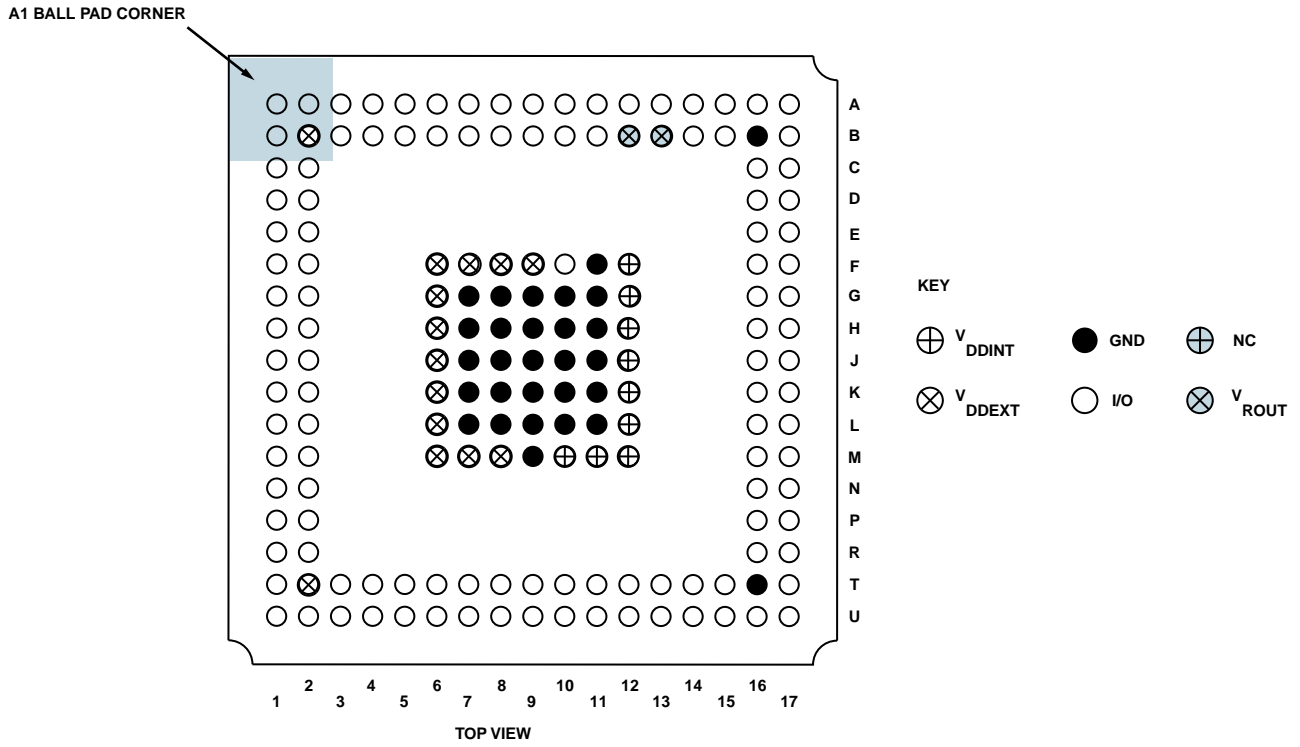


Figure 59. 169-Ball PBGA Ground Configuration (Top View)

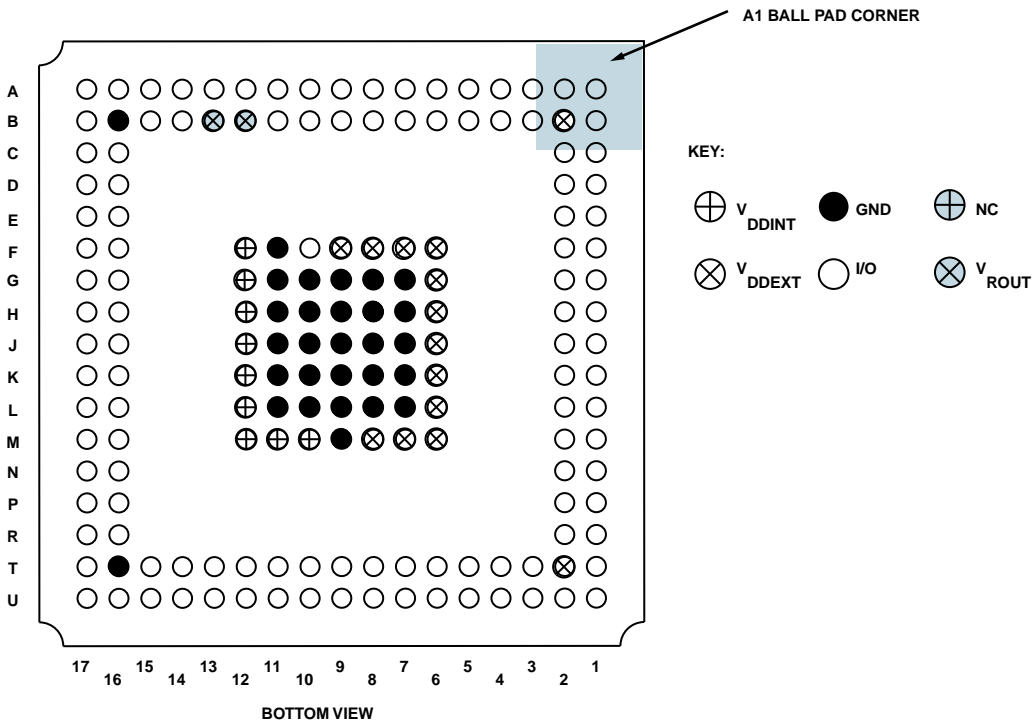


Figure 60. 169-Ball PBGA Ground Configuration (Bottom View)

176-LEAD LQFP PINOUT

Table 38 lists the LQFP pinout by signal. Table 39 on Page 56 lists the LQFP pinout by lead number.

Table 38. 176-Lead LQFP Pin Assignment (Alphabetically by Signal)

| Signal | Lead No. | Signal | Lead No. | Signal | Lead No. | Signal | Lead No. | Signal | Lead No. |
|--------|----------|--------|----------|--------|----------|---------|----------|--------|----------|
| ABE0 | 151 | DATA3 | 113 | GND | 88 | PPI_CLK | 21 | VDDEXT | 71 |
| ABE1 | 150 | DATA4 | 112 | GND | 89 | PPI0 | 22 | VDDEXT | 93 |
| ADDR1 | 149 | DATA5 | 110 | GND | 90 | PPI1 | 23 | VDDEXT | 107 |
| ADDR2 | 148 | DATA6 | 109 | GND | 91 | PPI2 | 24 | VDDEXT | 118 |
| ADDR3 | 147 | DATA7 | 108 | GND | 92 | PPI3 | 26 | VDDEXT | 134 |
| ADDR4 | 146 | DATA8 | 105 | GND | 97 | RESET | 13 | VDDEXT | 145 |
| ADDR5 | 142 | DATA9 | 104 | GND | 106 | RFS0 | 75 | VDDEXT | 156 |
| ADDR6 | 141 | DATA10 | 103 | GND | 117 | RFS1 | 64 | VDDEXT | 171 |
| ADDR7 | 140 | DATA11 | 102 | GND | 128 | RSCLK0 | 76 | VDDINT | 25 |
| ADDR8 | 139 | DATA12 | 101 | GND | 129 | RSCLK1 | 65 | VDDINT | 52 |
| ADDR9 | 138 | DATA13 | 100 | GND | 130 | RTXI | 17 | VDDINT | 66 |
| ADDR10 | 137 | DATA14 | 99 | GND | 131 | RTXO | 16 | VDDINT | 80 |
| ADDR11 | 136 | DATA15 | 98 | GND | 132 | RX | 82 | VDDINT | 111 |
| ADDR12 | 135 | DR0PRI | 74 | GND | 133 | SA10 | 164 | VDDINT | 143 |
| ADDR13 | 127 | DR0SEC | 73 | GND | 144 | SCAS | 166 | VDDINT | 157 |
| ADDR14 | 126 | DR1PRI | 63 | GND | 155 | SCK | 53 | VDDINT | 168 |
| ADDR15 | 125 | DR1SEC | 62 | GND | 170 | SCKE | 173 | VDDRTC | 18 |
| ADDR16 | 124 | DTOPRI | 68 | GND | 174 | SMS | 172 | VROUT0 | 5 |
| ADDR17 | 123 | DT0SEC | 67 | GND | 175 | SRA5 | 167 | VROUT1 | 4 |
| ADDR18 | 122 | DT1PRI | 59 | GND | 176 | SWE | 165 | XTAL | 11 |
| ADDR19 | 121 | DT1SEC | 58 | MISO | 54 | TCK | 94 | | |
| AMS0 | 161 | EMU | 83 | MOSI | 55 | TDI | 86 | | |
| AMS1 | 160 | GND | 1 | NMI | 14 | TDO | 87 | | |
| AMS2 | 159 | GND | 2 | PF0 | 51 | TFS0 | 69 | | |
| AMS3 | 158 | GND | 3 | PF1 | 50 | TFS1 | 60 | | |
| AOE | 154 | GND | 7 | PF2 | 49 | TMR0 | 79 | | |
| ARDY | 162 | GND | 8 | PF3 | 48 | TMR1 | 78 | | |
| ARE | 153 | GND | 9 | PF4 | 47 | TMR2 | 77 | | |
| AWE | 152 | GND | 15 | PF5 | 46 | TMS | 85 | | |
| BG | 119 | GND | 19 | PF6 | 38 | TRST | 84 | | |
| BGH | 120 | GND | 30 | PF7 | 37 | TSCLK0 | 72 | | |
| BMODE0 | 96 | GND | 39 | PF8 | 36 | TSCLK1 | 61 | | |
| BMODE1 | 95 | GND | 40 | PF9 | 35 | TX | 81 | | |
| BR | 163 | GND | 41 | PF10 | 34 | VDDEXT | 6 | | |
| CLKIN | 10 | GND | 42 | PF11 | 33 | VDDEXT | 12 | | |
| CLKOUT | 169 | GND | 43 | PF12 | 32 | VDDEXT | 20 | | |
| DATA0 | 116 | GND | 44 | PF13 | 29 | VDDEXT | 31 | | |
| DATA1 | 115 | GND | 56 | PF14 | 28 | VDDEXT | 45 | | |
| DATA10 | 103 | GND | 70 | PF15 | 27 | VDDEXT | 57 | | |

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Table 39. 176-Lead LQFP Pin Assignment (Numerically by Lead Number)

| Lead No. | Signal | Lead No. | Signal | Lead No. | Signal | Lead No. | Signal | Lead No. | Signal |
|----------|---------|----------|--------|----------|--------|----------|--------|----------|--------|
| 1 | GND | 41 | GND | 81 | TX | 121 | ADDR19 | 161 | AMS0 |
| 2 | GND | 42 | GND | 82 | RX | 122 | ADDR18 | 162 | ARDY |
| 3 | GND | 43 | GND | 83 | EMU | 123 | ADDR17 | 163 | BR |
| 4 | VROUT1 | 44 | GND | 84 | TRST | 124 | ADDR16 | 164 | SA10 |
| 5 | VROUT0 | 45 | VDDEXT | 85 | TMS | 125 | ADDR15 | 165 | SWE |
| 6 | VDDEXT | 46 | PF5 | 86 | TDI | 126 | ADDR14 | 166 | SCAS |
| 7 | GND | 47 | PF4 | 87 | TDO | 127 | ADDR13 | 167 | SRAS |
| 8 | GND | 48 | PF3 | 88 | GND | 128 | GND | 168 | VDDINT |
| 9 | GND | 49 | PF2 | 89 | GND | 129 | GND | 169 | CLKOUT |
| 10 | CLKIN | 50 | PF1 | 90 | GND | 130 | GND | 170 | GND |
| 11 | XTAL | 51 | PF0 | 91 | GND | 131 | GND | 171 | VDDEXT |
| 12 | VDDEXT | 52 | VDDINT | 92 | GND | 132 | GND | 172 | SMS |
| 13 | RESET | 53 | SCK | 93 | VDDEXT | 133 | GND | 173 | SCKE |
| 14 | NMI | 54 | MISO | 94 | TCK | 134 | VDDEXT | 174 | GND |
| 15 | GND | 55 | MOSI | 95 | BMODE1 | 135 | ADDR12 | 175 | GND |
| 16 | RTXO | 56 | GND | 96 | BMODE0 | 136 | ADDR11 | 176 | GND |
| 17 | RTXI | 57 | VDDEXT | 97 | GND | 137 | ADDR10 | | |
| 18 | VDDRTC | 58 | DT1SEC | 98 | DATA15 | 138 | ADDR9 | | |
| 19 | GND | 59 | DT1PRI | 99 | DATA14 | 139 | ADDR8 | | |
| 20 | VDDEXT | 60 | TFS1 | 100 | DATA13 | 140 | ADDR7 | | |
| 21 | PPI_CLK | 61 | TSCLK1 | 101 | DATA12 | 141 | ADDR6 | | |
| 22 | PPI0 | 62 | DR1SEC | 102 | DATA11 | 142 | ADDR5 | | |
| 23 | PPI1 | 63 | DR1PRI | 103 | DATA10 | 143 | VDDINT | | |
| 24 | PPI2 | 64 | RFS1 | 104 | DATA9 | 144 | GND | | |
| 25 | VDDINT | 65 | RSCLK1 | 105 | DATA8 | 145 | VDDEXT | | |
| 26 | PPI3 | 66 | VDDINT | 106 | GND | 146 | ADDR4 | | |
| 27 | PF15 | 67 | DT0SEC | 107 | VDDEXT | 147 | ADDR3 | | |
| 28 | PF14 | 68 | DT0PRI | 108 | DATA7 | 148 | ADDR2 | | |
| 29 | PF13 | 69 | TFS0 | 109 | DATA6 | 149 | ADDR1 | | |
| 30 | GND | 70 | GND | 110 | DATA5 | 150 | ABE1 | | |
| 31 | VDDEXT | 71 | VDDEXT | 111 | VDDINT | 151 | ABE0 | | |
| 32 | PF12 | 72 | TSCLK0 | 112 | DATA4 | 152 | AWE | | |
| 33 | PF11 | 73 | DR0SEC | 113 | DATA3 | 153 | ARE | | |
| 34 | PF10 | 74 | DR0PRI | 114 | DATA2 | 154 | AOE | | |
| 35 | PF9 | 75 | RFS0 | 115 | DATA1 | 155 | GND | | |
| 36 | PF8 | 76 | RSCLK0 | 116 | DATA0 | 156 | VDDEXT | | |
| 37 | PF7 | 77 | TMR2 | 117 | GND | 157 | VDDINT | | |
| 38 | PF6 | 78 | TMR1 | 118 | VDDEXT | 158 | AMS3 | | |
| 39 | GND | 79 | TMRO | 119 | BG | 159 | AMS2 | | |
| 40 | GND | 80 | VDDINT | 120 | BGH | 160 | AMS1 | | |

OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

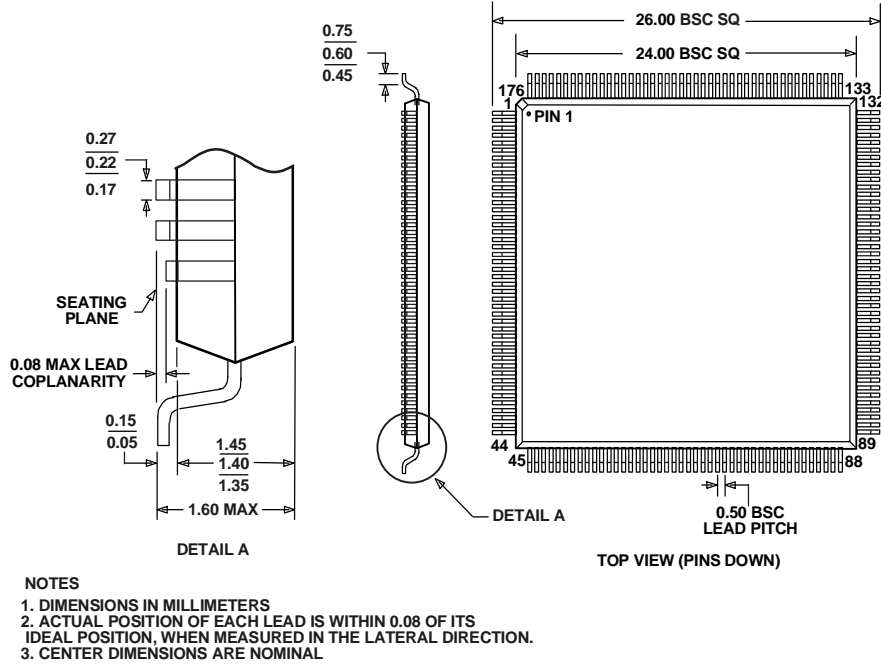


Figure 61. 176-Lead Low Profile Quad Flat Package (LQFP) ST-176-1

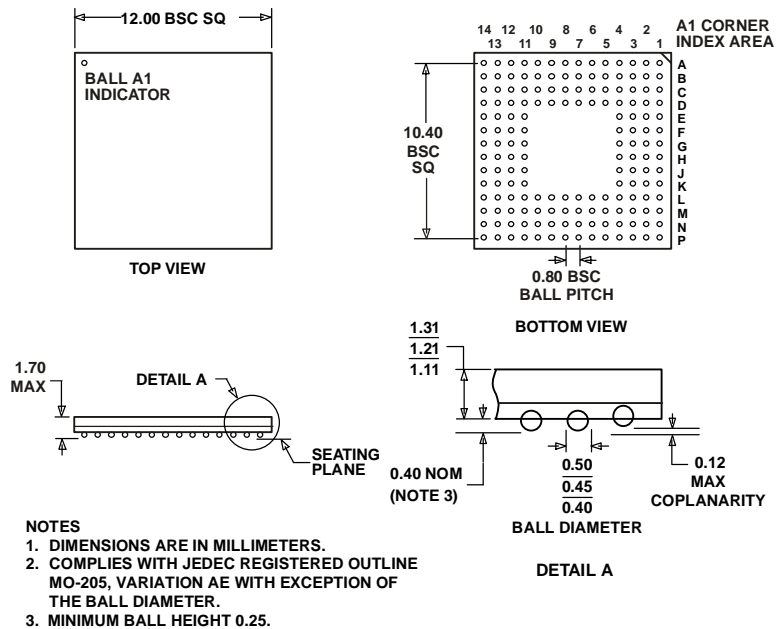


Figure 62. 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) BC-160-2

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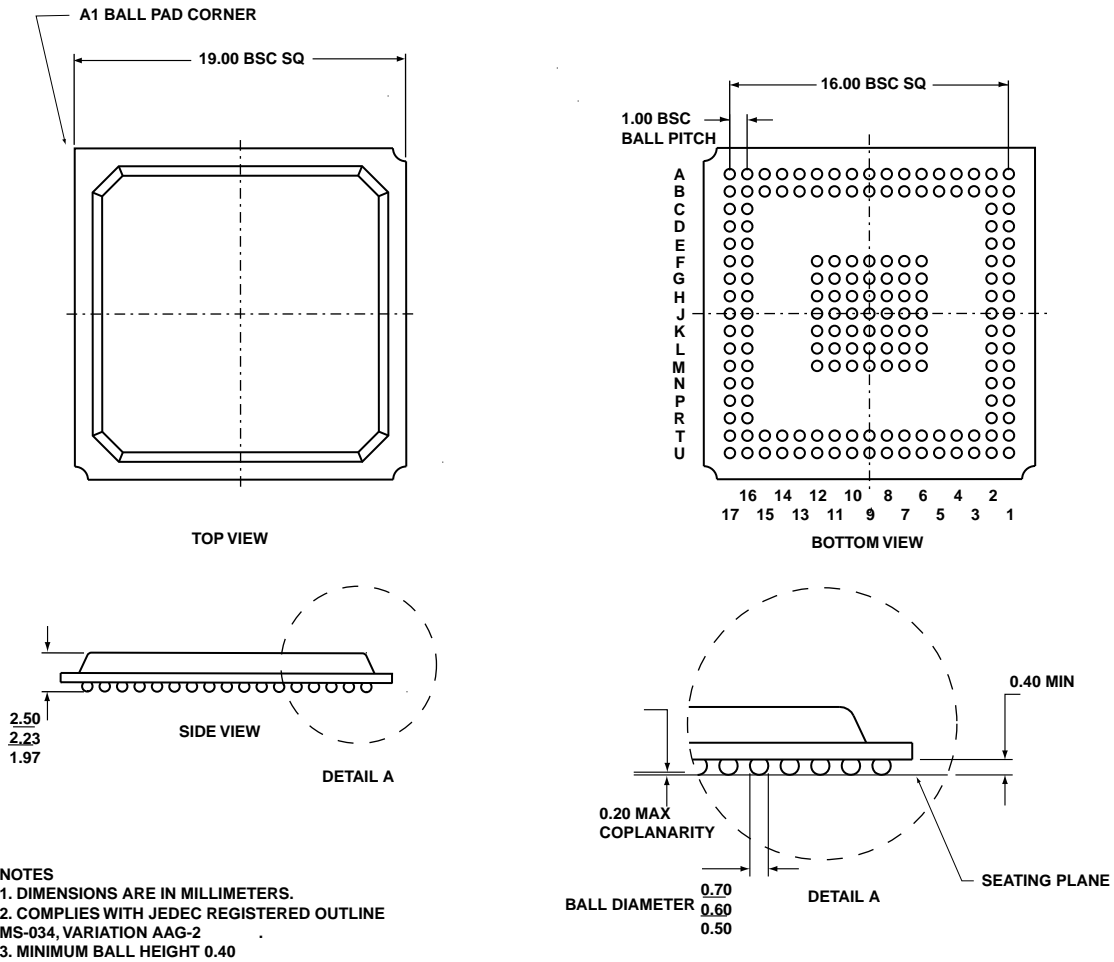


Figure 63. 169-Ball Plastic Ball Grid Array (B-169)

SURFACE MOUNT DESIGN

Table 40 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard*.

Table 40. BGA Data for Use with Surface Mount Design

| Package | Ball Attach Type | Solder Mask Opening | Ball Pad Size |
|---|---------------------|---------------------|------------------|
| Chip Scale Package Ball Grid Array (CSP_BGA) BC-160-2 | Solder Mask Defined | 0.40 mm diameter | 0.55 mm diameter |
| Plastic Ball Grid Array (PBGA) B-169 | Solder Mask Defined | 0.43 mm diameter | 0.56 mm diameter |

ORDERING GUIDE

| Model | Temperature Range ¹ | Speed Grade (Max) | Operating Voltage (Nom) | Package Description | Package Option |
|-----------------------------------|--------------------------------|-------------------|---|---|----------------|
| ADSP-BF531SBB400 | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V or 2.5 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |
| ADSP-BF531SBBZ400 | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V or 2.5 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |
| ADSP-BF531SBBC400 | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF531SBBCZ400 ² | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF531SBST400 | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V or 2.5 V or 3.3 V I/O | 176-Lead Quad Flatpack (LQFP) | ST-176-1 |
| ADSP-BF531SBSTZ400 ² | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V or 2.5 V or 3.3 V I/O | 176-Lead Quad Flatpack (LQFP) | ST-176-1 |
| ADSP-BF531WBBCZ-4A ^{2,3} | -40°C to +85°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF531WBBZ-4A ^{2,3} | -40°C to +85°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |
| ADSP-BF531WBSTZ-4A ^{2,3} | -40°C to +85°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 176-Lead Quad Flatpack (LQFP) | ST-176-1 |
| ADSP-BF531WYBCZ-4A ^{2,3} | -40°C to +105°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF531WYBZ-4A ^{2,3} | -40°C to +105°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |
| ADSP-BF532SBB400 | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V or 2.5 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |
| ADSP-BF532SBBZ400 ² | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V or 2.5 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |
| ADSP-BF532SBBC400 | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF532SBBCZ400 ² | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF532SBST400 | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V or 2.5 V or 3.3 V I/O | 176-Lead Quad Flatpack (LQFP) | ST-176-1 |
| ADSP-BF532SBSTZ400 | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V or 2.5 V or 3.3 V I/O | 176-Lead Quad Flatpack (LQFP) | ST-176-1 |
| ADSP-BF532WBBCZ-4A ² | -40°C to +85°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF532WBBZ-4A ^{2,3} | -40°C to +85°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |
| ADSP-BF532WBSTZ-4A ^{2,3} | -40°C to +85°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 176-Lead Quad Flatpack (LQFP) | ST-176-1 |
| ADSP-BF532WYBCZ-4A ^{2,3} | -40°C to +105°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF532WYBZ-4A ^{2,3} | -40°C to +105°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |

ADSP-BF531/ADSP-BF532/ADSP-BF533

[查询"ADSP-BF531SBSTZ400"供应商](#)

| Model | Temperature Range ¹ | Speed Grade (Max) | Operating Voltage (Nom) | Package Description | Package Option |
|-----------------------------------|--------------------------------|-------------------|---|---|----------------|
| ADSP-BF533SBB500 | -40°C to +85°C | 500 MHz | 1.2 V Internal, 1.8 V or 2.5 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |
| ADSP-BF533SBBZ500 ² | -40°C to +85°C | 500 MHz | 1.2 V Internal, 1.8 V or 2.5 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |
| ADSP-BF533SBBC500 | -40°C to +85°C | 500 MHz | 1.2 V Internal 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF533SBBCZ500 ² | -40°C to +85°C | 500 MHz | 1.2 V Internal 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF533SBBC-5V | -40°C to +85°C | 533 MHz | 1.25 V Internal 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF533SBBCZ-5V ² | -40°C to +85°C | 533 MHz | 1.2 V Internal 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF533SBBCZ400 ² | -40°C to +85°C | 400 MHz | 1.25 V internal, 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF533SBST400 | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V or 2.5 V or 3.3 V I/O | 176-Lead Quad Flatpack (LQFP) | ST-176-1 |
| ADSP-BF533SBSTZ400 ² | -40°C to +85°C | 400 MHz | 1.2 V internal, 1.8 V or 2.5 V or 3.3 V I/O | 176-Lead Quad Flatpack (LQFP) | ST-176-1 |
| ADSP-BF533SKBC-6V | 0°C to +70°C | 600 MHz | 1.3 V Internal 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF533SKBCZ-6V ² | 0°C to +70°C | 600 MHz | 1.3 V Internal 1.8 V, 2.5 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF533WBBCZ-5A ^{2,3} | -40°C to +85°C | 500 MHz | 1.2 V Internal, 3.0 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF533WBBZ-5A ^{2,3} | -40°C to +85°C | 500 MHz | 1.2 V Internal, 3.0 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |
| ADSP-BF533WYBCZ-4A ^{2,3} | -40°C to +105°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 160-Ball Chip Scale Package Ball Grid Array (CSP_BGA) | BC-160-2 |
| ADSP-BF533WYBZ-4A ^{2,3} | -40°C to +105°C | 400 MHz | 1.2 V internal, 3.0 V or 3.3 V I/O | 169-Ball Plastic Ball Grid Array (PBGA) | B-169 |

¹ Referenced temperature is ambient temperature.

² Z = RoHS Compliant Part.

³ Automotive grade part.